ispClock 5620A Development Kit

The ispClock 5620 Development Kit includes everything the designer needs to quickly configure and evaluate the ispClock5620A on a fully assembled printed-circuit board. The four-layer board supports a 100-pin TQFP package, a header for user I/O and a JTAG programming cable connector. SMA connectors are installed to provide high-signal integrity access to selected high-speed I/O signals. JTAG programming signals can be generated by using an ispDOWNLOAD® programming cable connected between the evaluation board and a PC. All user-programmable features of the ispPAC-CLK5620A can be easily configured using Lattice Semiconductor's PAC-Designer® software.

Product Contents

The ispClock5620A Development Kit includes:

- ispClock5620A Evaluation Board
- ispDOWNLOAD Cable
- AC Adapter
- User Documentation

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Device Support

You will need the **PAC-Designer software** to use this board. PAC-Designer can be **downloaded from the Lattice web site**.

Ordering Information

Purchase Now
Part Number: PAC-SYSCLK5620AV

To purchase, visit our **online store**.