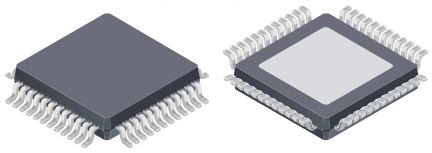
80 V Automotive Three-Phase MOSFET Driver

FEATURES AND BENEFITS

- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Fixed-frequency buck converter
- Operation at any PWM duty cycle up to and including 100%
- Programmable gate drive strength
- 10 to 80 V supply voltage operating range
- Programmable 3.3 or 5 V CMOS compatible logic I/O
- Three programmable current sense amplifiers
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Programmable control input logic sense
- Extensive programmable diagnostics
- Diagnostic verification
- Safety-assist features
- Automotive AEC-Q100 qualified
- A²-SIL™ product—device features for safety-critical systems*

PACKAGE:

48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

*The AMT49100 was developed in accordance with ISO 26262:2011 as a hardware safety element out of context with ASIL D capability (pending assessment) for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety application note and datasheet.

DESCRIPTION

The AMT49100 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a 3-phase bridge arrangement and is specifically designed for 48 V automotive power applications with high-power inductive loads, such as BLDC motors.

A fixed-frequency buck converter provides a regulated gate drive and bootstrap charge voltage over the full supply voltage range from 10 to 80 V. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs. The bootstrap charge is maintained by an additional charge pump providing 0-100% PWM with no duty cycle restriction.

Full control over all six power MOSFETs in the 3-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and optional programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface.

In addition to providing full access to the bridge control, the serial interface is also used to alter programmable settings such as dead time, VDS threshold, and fault blank time. Detailed diagnostic information can be read through the serial interface.

The AMT49100 is supplied in a 48-pin QFP package (suffix JP) with exposed thermal pad. The package is lead (Pb) free with 100% matte-tin leadframe plating.

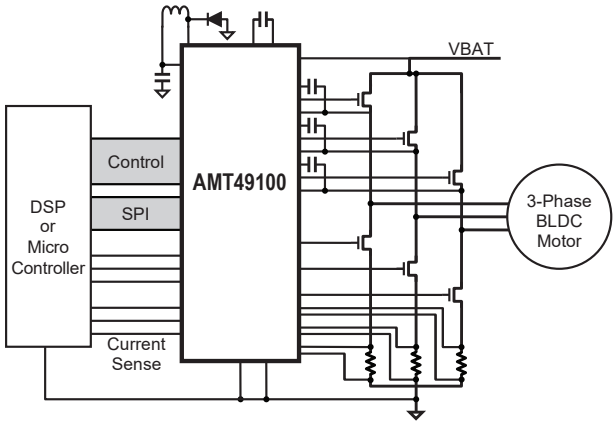


Figure 1: Typical Application

SELECTION GUIDE

Part Number	Buck Regulator	V_{IO} (V)	Packing	Package
AMT49100KJPTR-A-3	Enabled	3.3	1500 pieces per 13-inch reel	7 mm × 7 mm, 1.6 mm nominal height 48-terminal LQFP with exposed thermal pad
AMT49100KJPTR-A-5	Enabled	5		
AMT49100KJPTR-B-3	Disabled	3.3		
AMT49100KJPTR-B-5	Disabled	5		

Table of Contents

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ABSOLUTE MAXIMUM RATINGS [1][2]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		–0.3 to 80	V
Between Ground Terminals		Connect GND terminals together at package	–0.1 to 0.1	V
Drive Regulator Terminal	V_{REG}	VREG	–0.3 to 16	V
Buck Switch Terminal	V_{LX}	LX	–1 to 80	V
Bootstrap Pump Capacitor Terminal	V_{CP1}	CP1	–0.3 to V_{BRG} + 0.3	V
Bootstrap Pump Capacitor Terminal	V_{CP2}	CP2	V_{CP1} – 0.3 to V_{BRG} + 12	V
Battery-Compliant Logic Input Terminals	V_{IB}	HA, HB, HC, LA, LB, LC, ENABLE, RESETn	–0.3 to 80	V
Logic Input Terminals	V_I	STRn, SCK, SDI	–0.3 to 6	V
Logic Output Terminals	V_O	SDO, SAL, SBL, SCL	–0.3 to 6	V
Diagnostic Output Terminal	V_{DIAG}	DIAG	–0.3 to 80	V
Sense Amplifier Inputs	V_{CSI}	CSxP, CSxM	–4 to 6.5	V
Sense Amplifier Output	V_{CSO}	CSxO	–0.3 to 6	V
Bridge Drain Monitor Terminal	V_{BRG}	VBRG	–5 to 85	V
Bootstrap Supply Terminals	V_{Cx}	CA, CB, CC	–0.3 to V_{REG} + 80	V
High-Side Gate Drive Outputs	V_{GHx}	GHA, GHB, GHC	V_{Cx} – 16 to V_{Cx} + 0.3	V
		GHA, GHB, GHC (transient) [3]	–18 to V_{Cx} + 0.3	V
Motor Phase Terminals	V_{Sx}	SA, SB, SC	V_{Cx} – 16 to V_{Cx} + 0.3	V
		SA, SB, SC (transient) [3]	–18 to V_{Cx} + 0.3	V
Low-Side Gate Drive Outputs	V_{GLx}	GLA, GLB, GLC	V_{REG} – 16 to 18	V
		GLA, GLB, GLC (transient) [3]	–8 to 18	V
Bridge Low-Side Source Terminals	V_{LSS}	LSSA, LSSB, LSSC	V_{REG} – 16 to 18	V
		LSSA, LSSB, LSSC (transient) [3]	–8 to 18	V
NVM Maximum Programming Junction Temperature	T_{NVM}	Guaranteed by design characterization	85	°C
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Over temperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, guaranteed by design characterization.	180	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

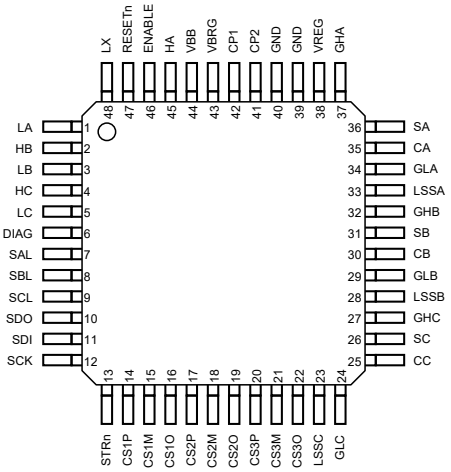
[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.
[2] Lowercase “x” in terminal names and symbols indicates a variable sequence character.
[3] Not tested in production. Confirmed by design and characterization. Duration less than 1 µs.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [4]	Value	Unit
JP Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	23	°C/W
		2-layer PCB with 3.8 in.^{2} of copper area each side	44	°C/W
	$R_{\theta JP}$		2	°C/W

[4] Additional thermal information available on the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



QFP-48 (JP) Package Pinout Diagram

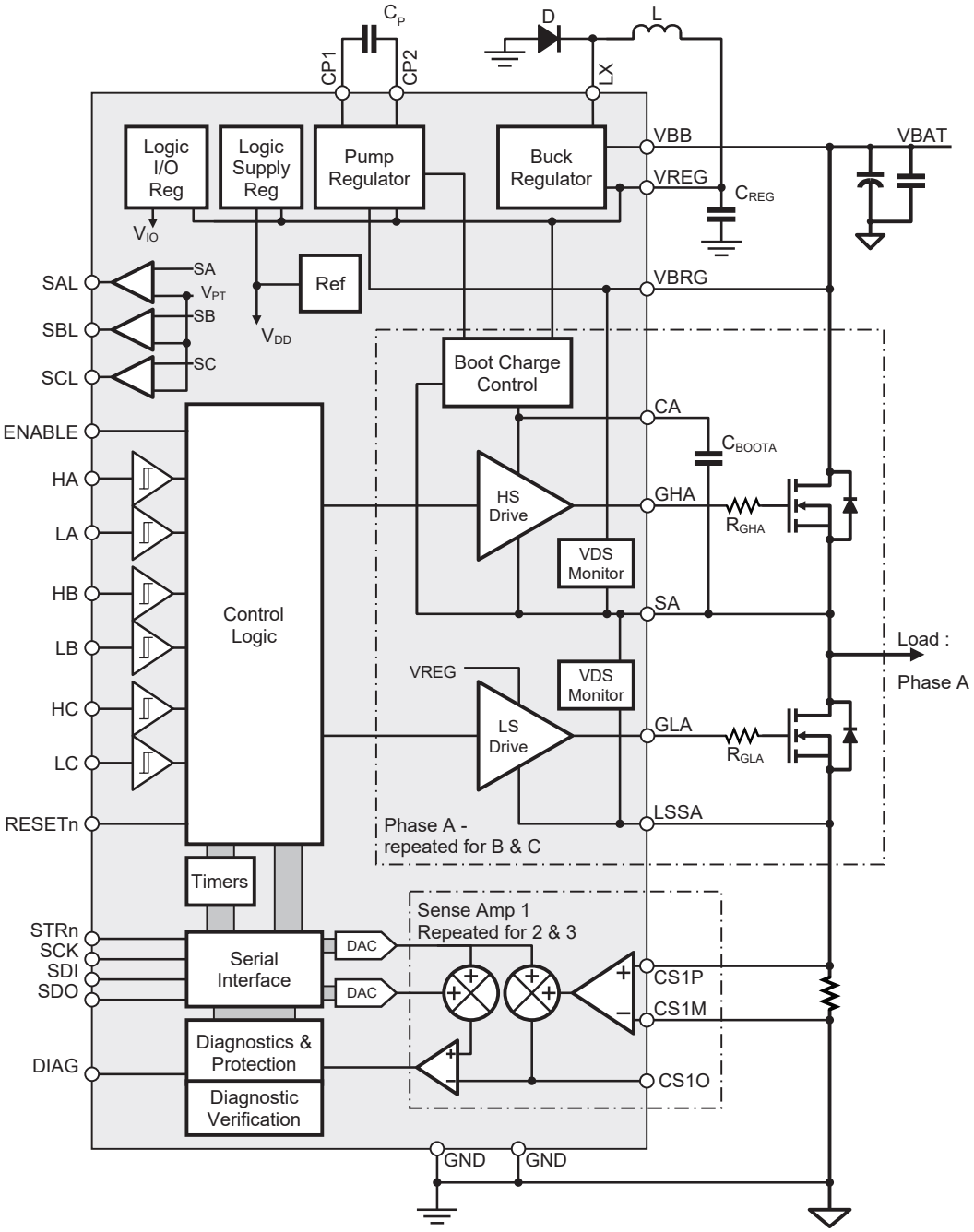
Pinout List

Name	Number	Function
CA	35	Bootstrap Capacitor Phase A
CB	30	Bootstrap Capacitor Phase B
CC	25	Bootstrap Capacitor Phase C
CP1	42	Pump Capacitor Terminal
CP2	41	Pump Capacitor Terminal
CS1M	15	Current Sense Amplifier 1 -Input
CS1O	16	Current Sense Amplifier 1 Output
CS1P	14	Current Sense Amplifier 1 +Input
CS2M	18	Current Sense Amplifier 2 -Input
CS2O	19	Current Sense Amplifier 2 Output
CS2P	17	Current Sense Amplifier 2 +Input
CS3M	21	Current Sense Amplifier 3 -Input
CS3O	22	Current Sense Amplifier 3 Output
CS3P	20	Current Sense Amplifier 3 +Input
DIAG	6	Programmable Diagnostic Output
ENABLE	46	Direct Output Activity Control
GHA	37	High-Side Gate Drive Phase A
GHB	32	High-Side Gate Drive Phase B
GHC	27	High-Side Gate Drive Phase C
GLA	34	Low-Side Gate Drive Phase A
GLB	29	Low-Side Gate Drive Phase B
GLC	24	Low-Side Gate Drive Phase C
GND	39	Ground
GND	40	Ground
PAD	Pad	Connect To Ground

Name	Number	Function
HA	45	Control Input A High Side
HB	2	Control Input B High Side
HC	4	Control Input C High Side
LA	1	Control Input A Low Side
LB	3	Control Input B Low Side
LC	5	Control Input C Low Side
LSSA	33	Low-Side Source Phase A
LSSB	28	Low-Side Source Phase B
LSSC	23	Low-Side Source Phase C
LX	48	Buck Regulator Switch Terminal
RESETn	47	RESET input
SA	36	Load Connection Phase A
SAL	7	Phase A Logic Output
SB	31	Load Connection Phase B
SBL	8	Phase B Logic Output
SC	26	Load Connection Phase C
SCK	12	Serial Clock Input
SCL	9	Phase C Logic Output
SDI	11	Serial Data Input
SDO	10	Serial Data Output
STRn	13	Serial Strobe (Chip Select) Input
VBB	44	Main Power Supply
VBRG	43	High-Side Drain Voltage Sense
VREG	38	Gate Drive Supply Output

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL BLOCK DIAGRAM



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 10 to 80 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range, Regulator Active	V_{BB}	Operating; outputs active	10	–	80	V
		Operating [1]; outputs disabled	5	–	80	V
		No unsafe states	0	–	80	V
V_{BB} Quiescent Current, Regulator Active	I_{BBQ}	V_{BB} = 48 V, all gate drive outputs low	–	6	15	mA
V_{BB} Quiescent Current, Regulator Inactive	I_{BBQ}	V_{BB} = V_{REG} = 12 V, all gate drive outputs low	–	1	2	mA
V_{BB} Sleep Current	I_{BBS}	V_{RESETn} ≤ 300 mV, sleep mode, V_{BB} < 60 V	–	–	10	µA
Bridge Operating Range	V_{BRG}		4.5	48	80	V
VBRG Sleep Current	I_{BRGS}	V_{RESETn} ≤ 300 mV, sleep mode, V_{BRG} < 60 V	–	–	10	µA
VREG Functional Operating Input Range, Regulator Inactive	V_{REG}	Operating; outputs active	11	–	14.5	V
		Operating [1]; outputs disabled	4.5	–	15	V
		No unsafe states	0	–	16	V
VREG Quiescent Current, Regulator Inactive	I_{REGQ}	V_{REG} = 12 V, all gate drive outputs low	–	20	30	mA
Buck Regulator Switching Frequency	f_{BR}		370	410	450	kHz
VREG Output Voltage, Regulator Active	V_{REG}	V_{BB} > 20 V, 0 mA < I_{VREG} < 50 mA	11.5	12.5	13.5	V
Internal Logic Supply Regulator Voltage [4][5]	V_{DD}	V_{REG} > 6.5 V	–	3.3	–	V
Internal Logic I/O Regulator Voltage [4][5]	V_{IO}	VIO = 0, V_{REG} > 6.5 V	3.1	3.3	3.5	V
		VIO = 1, V_{REG} > 8.5 V	4.8	5.0	5.2	V
Logic I/O Regulator Drop-Out Voltage	V_{IODO}	w.r.t. V_{REG}	0.5	1.5	3.0	V
Bootstrap Boost Voltage	V_{CX}	w.r.t. V_{BRG}, Boot capacitor fully charged	7.9	9.1	10.5	V
		w.r.t. V_{BRG}, I_{CA} = I_{CB} = I_{CC} = 5 mA (15 mA total), 11 V ≤ V_{REG} ≤ 14.4 V	7.4	8.2	10	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	1.4	2.2	2.8	V
Bootstrap Diode Resistance	r_D	$r_{D(100\ mA)}$ = ($V_{fBOOT(150\ mA)}$ – $V_{fBOOT(50mA)}$) / 100 mA	5	11	22	Ω
Bootstrap Diode Current Limit	I_{DBOOT}		250	500	750	mA
High-Side Gate Drive Static Load Resistance	R_{GSH}		100	–	–	kΩ
Start-Up Time, Buck Regulator Active [8]	t_{INIT}	V_{BB} > 10 V to gate drives enabled, C_{REG} ≤ 10 µF, V_{RESETn} > V_{IH}, V_{BRG} > V_{BRGUV}	–	–	3	ms
Start-Up Time, Buck Regulator Inactive [8]	t_{INIT}	V_{REG} > 10 V to gate drives enabled, V_{RESETn} > V_{IH}, V_{BRG} > V_{BRGUV}	–	–	3	ms
System Clock Period	t_{OSC}		45	50	55	ns
NVM – PROGRAMMING PARAMETERS						
Programming Voltage Applied To VBRG When Programming	V_{PP}	VPU = 0	24	–	–	V
		VPU = 1	40	–	–	V
Programming Supply Setup Time	t_{PRS}	V_{PP} > V_{PPMIN} to start of NVM write	10	–	–	ms
Number of Write Cycles [8]	N_{WC}	T_J ≤ 85ºC	–	–	400	–

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 10 to 80 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE						
Turn-On Time (High-Side)	$t_{r(HS)}$	C_{LOAD} = 30 nF, 2 V to 8 V, $V_{Cx} – V_{Sx}$ = 11 V	110	–	454	ns
Turn-On Time (Low-Side)	$t_{r(LS)}$	C_{LOAD} = 30 nF, 2 V to 8 V, $V_{VREG} – V_{LSSx}$ = 11 V	110	–	454	ns
Turn-Off Time (High-Side)	$t_{f(HS)}$	C_{LOAD} = 30 nF, 8 V to 2 V, $V_{Cx} – V_{Sx}$ = 11 V	47	–	250	ns
Turn-Off Time (Low-Side)	$t_{f(LS)}$	C_{LOAD} = 30 nF, 8 V to 2 V, $V_{VREG} – V_{LSSx}$ = 11 V	47	–	250	ns
Pull-Up On-Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GH} = –150 mA [2]	2.5	–	7.7	Ω
		T_J = 150°C, I_{GH} = –150 mA [2]	4	–	11.9	Ω
Pull-Up Peak Source Current (High-Side) [2]	$I_{PUPK(HS)}$	$V_{Cx} – V_{Sx}$ = 11 V	–2200	–	–600	mA
Pull-Up Peak Source Current (Low-Side) [2]	$I_{PUPK(LS)}$	$V_{REG} – V_{LSSx}$ = 11 V	–2200	–	–600	mA
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GL} = 150 mA [2]	0.6	–	1.9	Ω
		T_J = 150°C, I_{GL} = 150 mA [2]	0.9	–	2.7	Ω
Pull-Down Peak Sink Current (High-Side) [2]	$I_{PDPK(HS)}$	$V_{Cx} – V_{Sx}$ = 11 V	1100	–	4100	mA
Pull-Down Peak Sink Current (Low-Wide) [2]	$I_{PDPK(LS)}$	$V_{REG} – V_{LSSx}$ = 11 V	1100	–	4100	mA
High-Side Minimum Turn-On Time	t_{HRM}	THR = 0	42	55	65	ns
High-Side Turn-On Time Mean Step Size	t_{HRS}	THR > 0	12	16	20	ns
High-Side Turn-On Current 1	I_{HR1}	V_{GS} = 0 V, IHR1 = 15	–1050	–240	–160	mA
		Programmable range DT[6:0] > 0	–240	–	–16	mA
High-Side Turn-On Current 2	I_{HR2}	V_{GS} = 0 V, IHR2 = 15	–1050	–240	–160	mA
		Programmable range DT[6:0] > 0	–240	–	–16	mA
High-Side Minimum Turn-Off Time	t_{HFM}	THF = 0	42	55	65	ns
High-Side Turn-Off Time Mean Step Size	t_{HFS}	THF > 0	12	16	20	ns
High-Side Turn-Off Current 1	I_{HF1}	V_{GS} = 9 V, IHF1 = 15	160	240	320	mA
		Programmable range DT[6:0] > 0	16	–	240	mA
High-Side Turn-Off Current 2	I_{HF2}	V_{GS} = 9 V, IHF2 = 15	160	240	320	mA
		Programmable range DT[6:0] > 0	16	–	240	mA
Low-Side Minimum Turn-On Time	t_{LRM}	TLR = 0	42	55	65	ns
Low-Side Turn-On Time Mean Step Size	t_{LRS}	TLR > 0	12	16	20	ns
Low-Side Turn-On Current 1	I_{LR1}	V_{GS} = 0 V, ILR1 = 15	–1050	–240	–160	mA
		Programmable range DT[6:0] > 0	–240	–	–16	mA
Low-Side Turn-On Current 2	I_{LR2}	V_{GS} = 0 V, ILR2 = 15	–1050	–240	–160	mA
		Programmable range DT[6:0] > 0	–240	–	–16	mA
Low-Side Minimum Turn-Off Time	t_{LFM}	TLF = 0	42	55	65	ns
Low-Side Turn-Off Time Mean Step Size	t_{LFS}	TLF > 0	12	16	20	ns
Low-Side Turn-Off Current 1	I_{LF1}	V_{GS} = 9 V, ILF1 = 15	160	240	320	mA
		Programmable range DT[6:0] > 0	16	–	240	mA
Low-Side Turn-Off Current 2	I_{LF2}	V_{GS} = 9 V, ILF2 = 15	160	240	320	mA
		Programmable range DT[6:0] > 0	16	–	240	mA

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 10 to 80 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE (continued)						
GHx Output Voltage High	V_{GHH}	Bootstrap capacitor fully charged	V_{Cx} – 0.02	–	–	V
GHx Output Voltage Low	V_{GHL}	–10 µA < I_{GH} < 10 µA	–	–	V_{Sx} + 0.02	V
GLx Output Voltage High	V_{GLH}		V_{REG} – 0.02	–	–	V
GLx Output Voltage Low	V_{GLL}	–10 µA < I_{GL} < 10 µA	–	–	V_{LSSx}+0.02	V
Gate-Source Voltage, MOSFET On	V_{GSon}	No faults present	V_{ROFF}	–	V_{REG}	V
GHx Passive Pull-Down	R_{GHPD}	V_{BB} = 0 V, V_{GHx} – V_{Sx} = 0.1 V	0.25	–	2	MΩ
		V_{BB} = 0 V, I_{GHx} = 500 µA	0.5	–	10	kΩ
GLx Passive Pull-Down	R_{GLPD}	V_{BB} = 0 V, V_{GLx} – V_{LSSx} = 0.1 V	0.25	–	2	MΩ
		V_{BB} = 0 V, I_{GLx} = 500 µA	0.5	–	10	kΩ
GHx Active Pull-Down	R_{GHPA}	V(Cx-Sx) > 4 V	0.3	–	20	Ω
GLx Active Pull-Down	R_{GLPA}	V(VREG-LSSx) > 4 V	0.3	–	20	Ω
Turn-Off Propagation Delay [6]	$t_{P(off)}$	Phase input change to unloaded gate output change (see Figure 4); DT[6:0] = 0	–	–	73	ns
		Phase input change to unloaded gate output change, excluding jitter (see Figure 4); DT[6:0] > 0	–	–	148	ns
Turn-On Propagation Delay [6]	$t_{P(on)}$	Phase input change to unloaded gate output change (see Figure 4); DT[6:0] = 0	–	–	58	ns
		Phase input change to unloaded gate output change, excluding jitter (see Figure 4); DT[6:0] > 0	–	–	133	ns
Propagation Delay Matching (Phase-to-Phase)	Δt_{PP}	Same state change, DT[6:0] = 0	–	–	15	ns
Propagation Delay Matching (On-to-Off)	Δt_{OO}	Single phase, DT[6:0] = 0	–	–	22	ns
Propagation Delay Matching (GHx-to-GLx)	Δt_{HL}	Same state change, DT[6:0] = 0	–	–	17	ns
Dead Time (Turn-Off to Turn-On Delay)	t_{DEAD}	Default power-up state (see Figure 4)	1.35	1.6	1.85	µs
		Programmable range	0.1	–	6.35	µs
Phase Output Leakage Current	I_{Sx}	CPM1 = 1, CPM0 = 1	–500	–	500	µA

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 10 to 80 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS & OUTPUTS						
Input Low Voltage	V_{IL}	Except RESETn	–	–	0.3 × V_{IO}	V
Input High Voltage	V_{IH}	Except RESETn	0.7 × V_{IO}	–	–	V
Input Hysteresis	V_{Ihys}	Except RESETn	200	550	800	mV
Input Low Voltage	V_{IL}	RESETn	–	–	0.8	V
Input High Voltage	V_{IH}	RESETn	2.4	–	–	V
Input Hysteresis	V_{Ihys}	RESETn	200	400	600	mV
Input Pull-Down ENABLE, RESETn	R_{PD}	0 V < V_{IN} < V_{IO}	25	50	85	kΩ
	I_{PD}	V_{IO} <V_{IN} < 80 V	40	100	200	µA
Input Pull-Down HA, HB, HC	R_{PD}	HSI = 0, 0 V ≤ V_{IN} ≤ V_{IO}	30	50	77	kΩ
	I_{PD}	V_{IO} < V_{IN} < 80 V	40	–	800	µA
Input Pull-Down LA, LB, LC	R_{PD}	LSI = 0, 0 V ≤ V_{IN} ≤ V_{IO}	30	50	77	kΩ
	I_{PD}	V_{IO} < V_{IN} < 80 V	40	–	800	µA
Input Pull-Up HA, HB, HC	R_{PU}	HSI = 0, 0 V ≤ V_{IN} ≤ 0.7 × V_{IO}	30	50	77	kΩ
	I_{PD}	0.7 × V_{IO} < V_{IN} < 80 V	–50	–	800	µA
Input Pull-Up LA, LB, LC	R_{PU}	LSI = 0, 0 V ≤ V_{IN} ≤ 0.7 × V_{IO}	30	50	77	kΩ
	I_{PD}	0.7 × V_{IO} < V_{IN} < 80 V	–50	–	800	µA
Input Pull-Down SDI, SCK	R_{PDS}	0 V < V_{IN} < V_{IO}	30	50	77	kΩ
Input Pull-Up STRn (to V_{IO})	R_{PUS}		30	50	77	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	–	0.2	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –1mA [2]	V_{IO} – 0.4	V_{IO} – 0.2	–	V
Output Leakage SDO [2]	I_{OSD}	0 V < V_{SDO} < V_{IO}, STRn = 1	–1	–	1	µA
Output Leakage DIAG [2]	I_{ODI}	0 V < V_{DIAG} < V_{IO}, DG[1:0] = 0	–	–	1	µA
LOGIC I/O – DYNAMIC PARAMETERS						
Reset Pulse Width	t_{RST}		1	–	4.5	µs
Reset Shutdown Time, Buck Regulator Active [8]	t_{RSD}	V_{RESETn} ≤ 300 mV to regulator switching stopped and gate drives disabled	5	–	20	µs
Reset Shutdown Time, Buck Regulator Inactive [8]	t_{RSD}	V_{RESETn} ≤ 300 mV to gate drives disabled	5	–	20	µs
Input Pulse Filter Time	t_{PIN}	HA, LA, HB, LB, HC, LC	–	35	–	ns
Clock High Time	t_{SCKH}	A in Figure 3	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 3	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 3	100	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 3	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 3	350	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 3; C_{LOAD} = 10 pF	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 3	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 3; C_{LOAD} = 10 pF	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	I in Figure 3	5	–	–	ns
Data In Setup Time To Clock Rising	t_{SDIS}	J in Figure 3	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	K in Figure 3	10	–	–	ns

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 10 to 80 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIERS						
Input Offset Voltage	V_{IOS}		–1	–	+1	mV
Input Offset Voltage Drift Over Temperature	ΔV_{IOS}		–2	–	+2	µV/°C
Input Bias Current [2]	I_{BIAS}	V_{ID} = 0 V, V_{CM} in range	–100	–35	–5	µA
Input Offset Current [2]	I_{OS}	V_{ID} = 0 V, V_{CM} in range	–1.5	–	+1.5	µA
Gain	A_V	Default power-up value	–	20	–	V/V
Gain Error	E_A	V_{CM} in range	–1.6	–	1.6	%
Gain Drift Over Temperature	E_{AD}	V_{CM} in range	–50	–	15	ppm/°C
Output Offset	V_{OOS}	Default power-up value	–	2.5	–	V
Output Offset Error	E_{VO}	V_{CM} in range, V_{OOS} > 0 V	–75	±25	75	mV
Output Offset Drift	V_{OOSD}	V_{CM} in range, V_{OOS} > 0 V	–135	–	135	µV /°C
Small Signal –3 dB Bandwidth [8]	BW	Gain = 20 V/V, V_{IN} = 10 mVpp	1	–	–	MHz
Output Settling Time (to within 40 mV)	t_{SET}	V_{CSO} = 1 Vpp square wave, Gain = 20 V/V, C_{OUT} = 50 pF	0.2	–	1	µs
Output Dynamic Range	V_{CSOUT}	VCL = 0, –100 µA < I_{CSO} < 100 µA [2]	0.3	–	3.1	V
		VCL = 1, –100 µA < I_{CSO} < 100 µA [2]	0.3	–	4.8	V
Output Voltage Clamp	V_{CSC}	VCL = 0, I_{CSO} = –2 mA [2]	3.2	3.5	3.9	V
		VCL = 1, I_{CSO} = –2 mA [2]	4.9	5.2	5.6	V
Output Voltage Clamp Current [2]	I_{CSC}	$V_{CSOUT(MAX)}$ < V_{CSOUT} < V_{CSC}	–10	–	–	mA
Output Current Sink [2]	I_{CSsink}	V_{ID} = 0 V, V_{CSO} = 1.5 V, Gain = 20 V/V	230	–	480	µA
Output Current Sink (Boosted) [2][7]	$I_{CSsinkb}$	V_{OOS} = 1.5 V, V_{ID}= –50 mV, Gain = 20 V/V, V_{CSO} = 1.5 V	1.9	–	4.4	mA
Output Current Source [2]	$I_{CSsource}$	VCL = 1, V_{OOS} = 0 V, V_{ID} = 200 mV, Gain = 20 V/V, V_{CSO} = 1.5 V	–5	–	–1.2	mA
VBB Supply Ripple Rejection	PSRR	V_{ID} = 0 V, 100 kHz, Gain = 20 V/V	–	75	–	dB
		V_{CSP} = V_{CSM} = 0 V, DC, Gain = 20 V/V	75	–	–	dB
DC Common-Mode Rejection	CMRR	V_{CM} step from 0 to 200 mV, Gain = 20 V/V	52	100	–	dB
AC Common-Mode Rejection	CMRR	V_{CM} = 200 mVpp, 100 kHz, Gain = 20 V/V	–	62	–	dB
		V_{CM} = 200 mVpp, 1 MHz, Gain = 20 V/V	–	43	–	dB
		V_{CM} = 200 mVpp, 10 MHz, Gain = 20 V/V	–	25	–	dB
Common-Mode Recovery Time (to within 100 mV)	t_{CMrec}	V_{CM} step from –4 V to +1 V, Gain = 20 V/V, C_{OUT} = 50 pF	–	–	2.1	µs
Output Slew Rate 10% to 90%	SR	V_{ID} step from 0 V to 175 mV, Gain = 20 V/V, C_{OUT} = 50 pF	1.8	–	5	V/µs
Input Overload Recovery (to within 40 mV)	t_{IDrec}	V_{ID} step from 250 mV to 0 V, Gain = 20 V/V, C_{OUT} = 50 pF	0.4	–	2.3	µs
Offset Calibration Time	t_{Cal}	From STRn rising edge	–	–	100	µs

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 10 to 80 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION						
VREG Undervoltage	V_{RON}	V_{REG} rising	7.7	8.0	8.3	V
	V_{ROFF}	V_{REG} falling	7.0	7.25	7.5	V
VREG Overvoltage Warning	V_{ROV}	V_{REG} rising	14.8	15.4	16.1	V
VREG Overvoltage Hysteresis	V_{ROVHys}		1100	1400	1620	mV
VBRG Overvoltage Warning	V_{BRGOV}	VPO = 0, V_{BRG} rising	52	54	58	V
		VPO = 1, V_{BRG} rising	57	60	63	V
VBRG Overvoltage Hysteresis	$V_{BRGOVHys}$		2.2	2.8	3.8	V
VBRG Undervoltage	V_{BRGUV}	VPU = 0, V_{BRG} falling	18	19	20	V
		VPU = 1, V_{BRG} falling	32	34	36	V
VBRG Undervoltage Hysteresis	$V_{BRGUVHys}$		1.3	1.6	2.1	V
VBB Undervoltage	V_{BBON}	V_{BB} rising	9.1	9.5	9.9	V
	V_{BBOFF}	V_{BB} falling	8.1	8.5	8.9	V
Bootstrap Undervoltage	V_{BCON}	V_{BOOT} rising, $V_{BOOT} = V_{Cx} – V_{Sx}$	6.3	7.1	7.9	V
	V_{BCOFF}	V_{BOOT} falling, $V_{BOOT} = V_{Cx} – V_{Sx}$	5.6	6.4	7.3	V
Gate Drive Off Overvoltage Threshold	V_{GSOV}	High-side	V_{Sx} + 1.05	V_{Sx} + 1.2	V_{Sx} + 1.4	V
		Low-Side	V_{LSSx} + 1.05	V_{LSSx} + 1.2	V_{LSSx} + 1.4	V
Gate Drive On Undervoltage Threshold	V_{GSUV}	High-side	V_{Cx} – 1.15	V_{Cx} – 1.0	V_{Cx} – 0.85	V
		Low-Side	V_{REG} – 1.15	V_{REG} – 1.0	V_{REG} – 0.85	V
VIO Undervoltage Threshold	V_{IOON}	VIO = 0, V_{IO} rising	2.7	2.9	3.1	V
	V_{IOOFF}	VIO = 0, V_{IO} falling	2.4	2.6	2.8	V
	V_{IOON}	VIO = 1, V_{IO} rising	4.3	4.5	4.7	V
	V_{IOOFF}	VIO = 1, V_{IO} falling	3.7	3.9	4.1	V
Logic Terminal Overvoltage Warning	V_{LOV}	Voltage rising on HA, LA, HB, LB, HC, LC, ENABLE, or DIAG	6.5	–	9.5	V
ENABLE Input Timeout	t_{ETO}		90	100	110	ms
VBRG Input Voltage	V_{BRG}	When VDS monitor is active	4.5	V_{BB}	80	V
VBRG input current	I_{VBRG}		–	3	5	mA
	I_{VBRGQ}	Sleep mode V_{BRG} < 70 V	–	–	2	µA
VDS Threshold – High-Side	V_{DSTH}	Default power-up value	–	1.2	–	V
		Programmable range, 5 V ≤ V_{BRG} ≤ 80 V	0	–	3.15	V
		Programmable range, 4.5 V < V_{BRG} < 5 V	0	–	2.5	V
High-Side VDS Threshold Offset [3]	V_{DSTHO}	High-side on, V_{DSTH} ≥ 1 V, 4.5 V ≤ V_{BRG} ≤ 80 V	–200	±100	+200	mV
		High-side on, V_{DSTH} < 1 V, 4.5 V ≤ V_{BRG} ≤ 80 V	–150	±50	+150	mV
VDS Threshold – Low-Side	V_{DSTL}	Default power-up value	–	1.2	–	V
		Programmable range	0	–	3.15	V
Low-Side VDS Threshold Offset [3]	V_{DSTLO}	Low side on, V_{DSTL} ≥ 1 V, 4.5 V ≤ V_{BRG} ≤ 80 V	–200	±100	+200	mV
		Low side on, V_{DSTL} <1 V, 4.5 V ≤ V_{BRG} ≤ 80 V	–150	±50	+150	mV
VDS and VGS Fault Qualification Time	t_{VDQ}	Default power-up value (Figure 7)	1.46	1.7	1.91	µs
		Programmable range	0	–	6.3	µs

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 10 to 80 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION (continued)						
Phase Comparator Threshold	V_{PT}	Phase voltage rising, 4.5 V < V_{BRG} < 80 V, Default power-up value	48	50	52.5	%V_{BRG}
		Programmable range	0	–	98.4	%V_{BRG}
Overcurrent Threshold Voltage	V_{OCT}	Default power-up value	0.8	0.9	1.08	V
		Programmable range	0.3	–	4.8	V
Overcurrent Qualify Time	t_{OCQ}	Default power-up value	6.7	7.5	8.3	µs
		Programmable range	0	–	15.5	µs
On-State Open-Load Threshold Voltage	V_{OLTH}	Default power-up value	90	200	260	mV
		Programmable range	0	–	375	mV
Off-State Test Sink Current	I_{SD}	V(Sx) = 3 V	1.25	2.5	3.75	mA
Off-State Test Source Current [2]	I_{SU}	YSC = 0, V(Sx) = 1 V	–120	–90	–50	µA
		YSC = 1, V(Sx) = 1 V	–460	–410	–300	µA
Open Load Timeout	t_{OLTO}		85	100	115	ms
LSS Open Threshold (Rising)	V_{LSO}		4.5	5	5.5	V
LSS Open Threshold Hysteresis	V_{LSOHys}		420	500	620	mV
LSS Current	I_{LU}	V(LSSx) = 5 V, V_{TL} = 1.2 V	–165	–130	–95	µA
Current Sense Amplifier Input Open Threshold	V_{SAD}		1.9	2.2	2.5	V
DIAG Output: Fault Pulse Period	t_{FP}	DG[1:0] = 0,1	90	100	110	ms
DIAG Output: Fault Pulse Duty Cycle	D_{FP}	DG[1:0] = 0,1: No Fault present		80		%
		DG[1:0] = 0,1: Fault present		20		%
DIAG Output: Temperature Range	V_{TJD}	DG[1:0] = 1,0, T_J = 0°C	–	1440	–	mV
DIAG Output: Temperature Slope	A_{TJD}	DG[1:0] = 1,0	–	–3.92	–	mV/°C
DIAG Output: Clock Division Ratio	N_D	DG[1:0] = 1,1		256000		–
Temperature Warning Threshold [9]	T_{JW}	Temperature increasing	125	135	145	°C
Temperature Warning Hysteresis [9]	T_{JWhys}		13.8	15	20.6	°C
Overtemperature Threshold [9]	T_{JF}	Temperature increasing	165	175	185	°C
Overtemperature Hysteresis [9]	T_{JFhys}	Recovery = T_{JF} – T_{JFhys}	11.3	15	19.8	°C

[1] No internal reset.
[2] For input and output current specifications, negative current is defined as coming out of (being sourced by) the specified device terminal.
[3] VDS offset is the difference between the programmed threshold, V_{DSTH} or V_{DSTL} and the actual trip voltage.
[4] V_{DD} and V_{IO} derived from V_{BB} for internal use only. Not accessible on any device terminal.
[5] Confirmed by design. Not production tested.
[6] For DT[6:0] > 0, jitter of ±25 ns must be added to the limits shown.
[7] If the amplifier output voltage (V_{CSO}) is more positive than the value demanded by the applied differential input (V_{ID}) and output offset (V_{OOS}) conditions, output current sink capability is boosted to enhance negative going transient response.
[8] Confirmed by characterization and design. Not production tested.
[9] Stated values confirmed by design and characterization (not production tested). Associated function production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

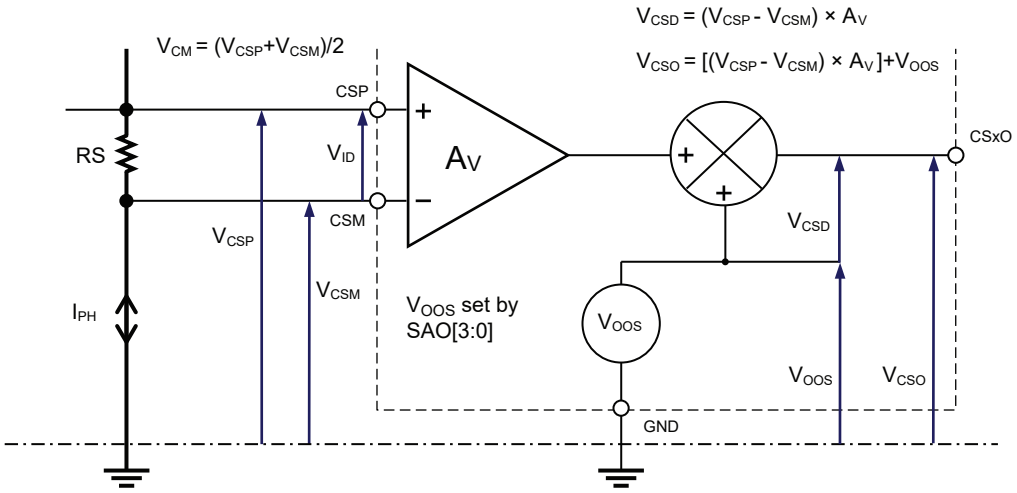
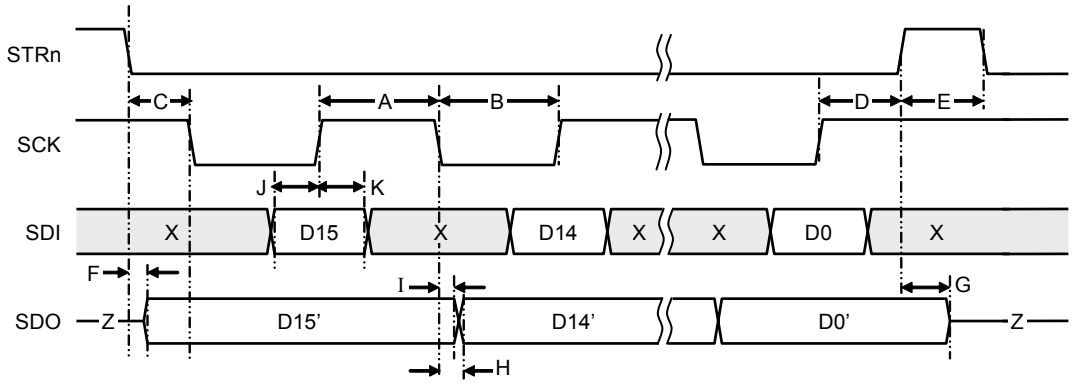


Figure 2: Sense Amplifier Voltage Definitions



X=don't care, Z=high impedance (tri-state)

Figure 3: Serial Interface Timing

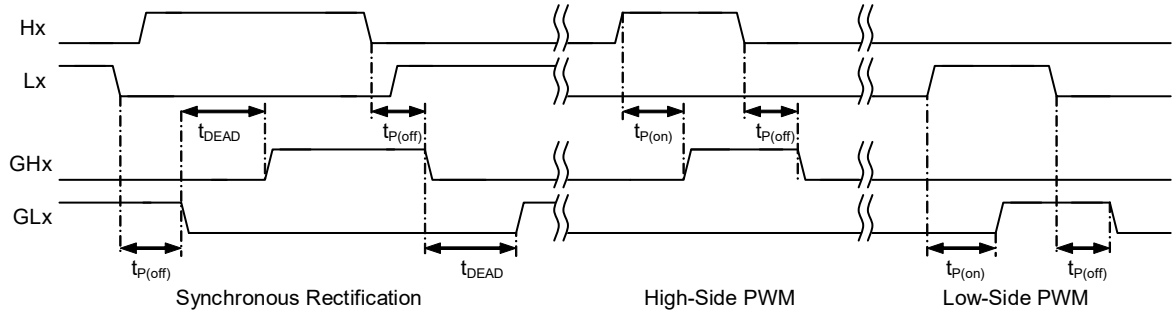


Figure 4: Gate Drive Timing, Phase Logic Control Inputs

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

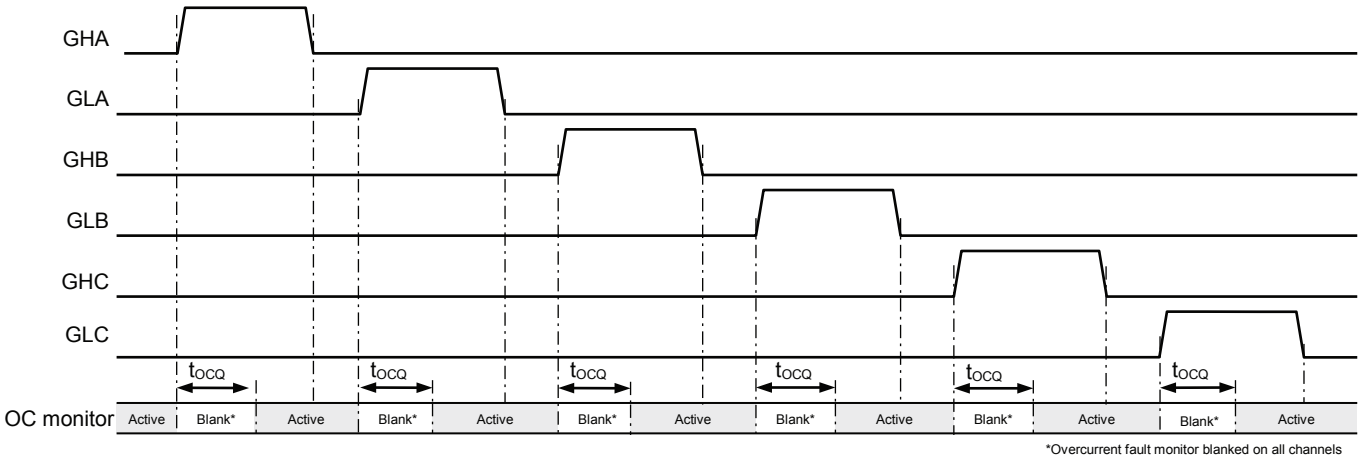


Figure 5: Overcurrent Fault Monitor – Blank Mode Timing (OCQ = 1)

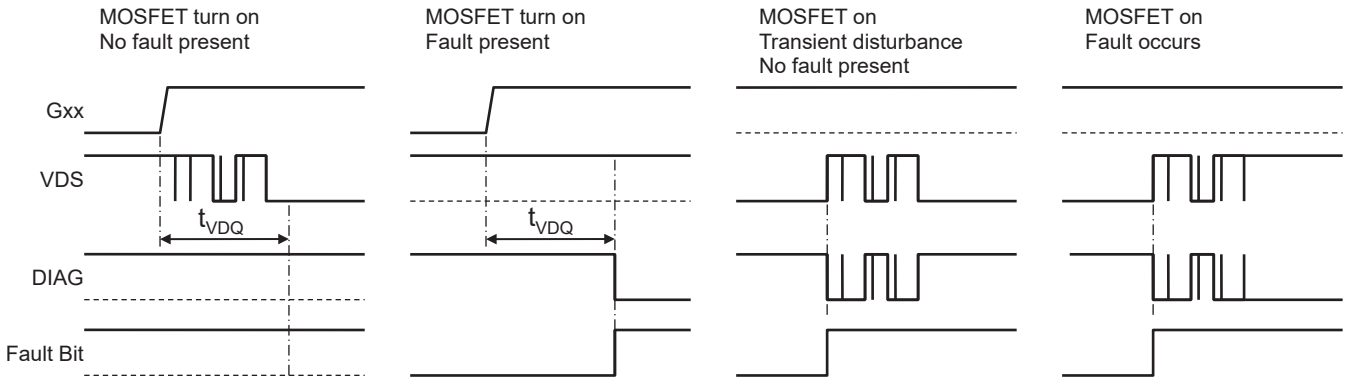


Figure 6: VDS Fault Monitor – Blank Mode Timing (VDQ = 1)

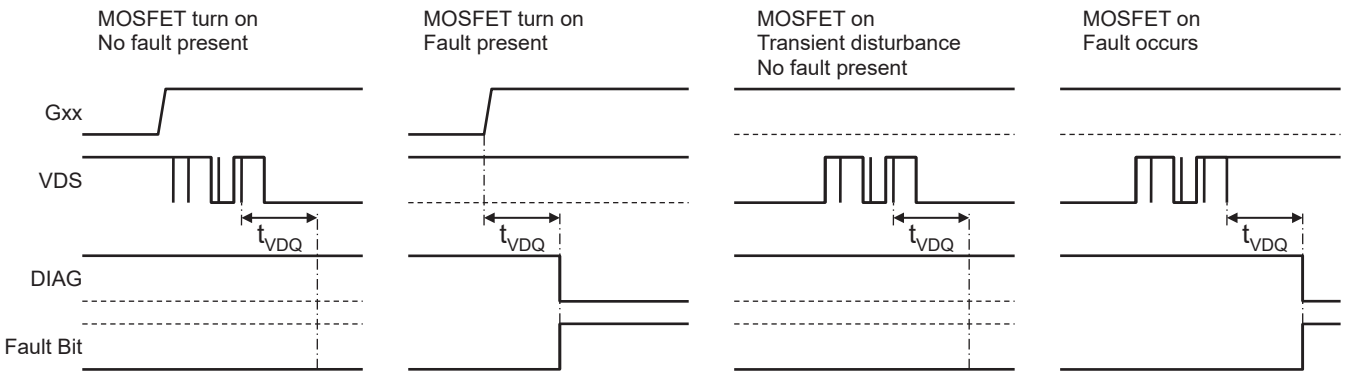


Figure 7: VDS Fault Monitor – Debounce Mode Timing (VDQ = 0)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LOGIC TRUTH TABLES

Table 1: Control Logic – Logic Inputs

Normal: HSI = 0, LSI = 0						
HSI	LSI	Hx	Lx	GHx	GLx	Sx
0	0	0	0	LO	LO	Z
0	0	0	1	LO	HI	LO
0	0	1	0	HI	LO	HI
0	0	1	1	LO	LO	Z

High-Side Inverted: HSI = 1, LSI = 0						
HSI	LSI	Hx	Lx	GHx	GLx	Sx
1	0	0	0	HI	LO	HI
1	0	0	1	LO	LO	Z
1	0	1	0	LO	LO	Z
1	0	1	1	LO	HI	LO

Both Inverted: HSI = 1, LSI = 1						
HSI	LSI	Hx	Lx	GHx	GLx	Sx
1	1	0	0	LO	LO	Z
1	1	0	1	HI	LO	HI
1	1	1	0	LO	HI	LO
1	1	1	1	LO	LO	Z

Low-Side Inverted: HSI = 0, LSI = 1						
HSI	LSI	Hx	Lx	GHx	GLx	Sx
0	1	0	0	LO	HI	LO
0	1	0	1	LO	LO	Z
0	1	1	0	LO	LO	Z
0	1	1	1	HI	LO	HI

HI = high-side FET active, LO = low-side FET active
Z = high impedance, both FETs off
All control register bits set to 0; ENABLE = 1, RESETn = 1

Table 2: Control Logic – Serial Register

Phase A					Phase B					Phase C				
AH	AL	GHA	GLA	SA	BH	BL	GHB	GLB	SB	CH	CL	GHC	GLC	SC
0	0	LO	LO	Z	0	0	LO	LO	Z	0	0	LO	LO	Z
0	1	LO	HI	LO	0	1	LO	HI	LO	0	1	LO	HI	LO
1	0	HI	LO	HI	1	0	HI	LO	HI	1	0	HI	LO	HI
1	1	LO	LO	Z	1	1	LO	LO	Z	1	1	LO	LO	Z

HI = high-side FET active, LO = low-side FET active
Z = high impedance, both FETs off
Logic 0 input on HA, LA, HB, LB, HC, and LC. ENABLE = 1, RESETn = 1, HSI = LSI = 0

Table 3: Control Combination Logic – Logic Inputs and Serial Register

Terminal	Register	Internal
Hx	xH	HIx
0	0	0
0	1	1
1	0	1
1	1	1

Terminal	Register	Internal
Lx	xL	LOx
0	0	0
0	1	1
1	0	1
1	1	1

The three phases are controlled independently.

Internal control signals (HIx, LOx) are derived by combining the logic states applied to the control input terminals (Hx, Lx) with the bit patterns held in the Control register (xH, xL).

Table 3 assumes HSI and LSI = 0.

Normally the input terminals or the Control register method is used for control with the other being held inactive (all terminals or bits at logic 0).

ENABLE	HIx	LOx	GHx	GLx	Sx	Comment
1	0	0	L	L	Z	Phase disabled
1	0	1	L	H	LO	Phase sinking
1	1	0	H	L	HI	Phase sourcing
1	1	1	L	L	Z	Phase disabled
0	X	X	L	L	Z	Phase disabled

X = don't care

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 4: Open-Load Detect Mode

						OL detect	
HIA	LOA	HIB	LOB	HIC	LOC	Off-State	On-State
0	0	0	0	0	0	Yes	
0	0	0	0	0	1		
0	0	0	0	1	0		
0	0	0	0	1	1	Yes	
0	0	0	1	0	0		
0	0	0	1	0	1		
0	0	0	1	1	0		Yes
0	0	0	1	1	1		
0	0	1	0	0	0		
0	0	1	0	0	1		Yes
0	0	1	0	1	0		
0	0	1	0	1	1		
0	0	1	1	0	0	Yes	
0	0	1	1	0	1		
0	0	1	1	1	0		
0	0	1	1	1	1	Yes	
0	1	0	0	0	0		
0	1	0	0	0	1		
0	1	0	0	1	0		Yes
0	1	0	0	1	1		
0	1	0	1	0	0		
0	1	0	1	0	1		
0	1	0	1	1	0		Yes
0	1	0	1	1	1		
0	1	1	0	0	0		Yes
0	1	1	0	0	1		Yes
0	1	1	0	1	0		Yes
0	1	1	0	1	1		Yes
0	1	1	1	0	0		
0	1	1	1	0	1		
0	1	1	1	1	0		
0	1	1	1	1	1		
1	0	0	0	0	0		
1	0	0	0	0	1		Yes
1	0	0	0	1	0		
1	0	0	0	1	1		
1	0	0	1	0	0		Yes
1	0	0	1	0	1		Yes
1	0	0	1	1	0		Yes
1	0	0	1	1	1		Yes
1	0	1	0	0	0		
1	0	1	0	0	1		Yes
1	0	1	0	1	0		
1	0	1	0	1	1		
1	0	1	1	0	0		
1	0	1	1	0	1		Yes
1	0	1	1	1	0		
1	0	1	1	1	1		
1	1	0	0	0	0	Yes	
1	1	0	0	0	1		
1	1	0	0	1	0		
1	1	0	0	1	1	Yes	
1	1	0	1	0	0		
1	1	0	1	0	1		
1	1	0	1	1	0		Yes
1	1	0	1	1	1		
1	1	1	0	0	0		
1	1	1	0	0	1		Yes
1	1	1	0	1	0		
1	1	1	0	1	1		
1	1	1	1	0	0	Yes	
1	1	1	1	0	1		
1	1	1	1	1	0		
1	1	1	1	1	1	Yes	

HIx, LOx derived from Table 3.
RESETn = 1, ENABLE = 1, HSI = 0, LSI = 0, AOL = 1.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

The AMT49100 provides six high current gate drives capable of driving a wide range of n-channel power MOSFETs. The gate drives are configured as three half bridges, each with a high-side drive and a low-side drive. The three half bridges can be operated independently or together as a three-phase bridge driver for BLDC or PMSM motors.

Gate drives have programmable drive strength and can be controlled individually with logic inputs or through the SPI-compatible serial interface. The high-side and low-side gate drive control logic inputs can be inverted as groups and provide a very flexible solution for many motor control applications. Independent control over each MOSFET allows each driver to be driven with an independent PWM signal for full sinusoidal excitation. All logic inputs have standard CMOS threshold levels and can be programmed to be compatible with 3.3 or 5 V logic outputs. The gate drive control logic inputs are battery voltage compliant, meaning they can be shorted to ground or supply without damage, up to the maximum battery voltage of 80 V.

The AMT49100 can operate with the fixed-frequency buck regulator, producing the main regulated voltage (V_{REG}) at the VREG terminal, or with an externally generated regulated supply driving the VREG terminal. In the buck regulator mode, a single unregulated supply of 10 to 80 V is applied to the VBB terminal. In the externally regulated supply mode, a voltage of nominally 12 V is applied to both the VBB and VREG terminals. In this mode, the external inductor and Schottky diode are not required.

A charge pump regulator generates a positive voltage referenced to the applied bridge voltage (V_{BRG}) to allow operation at high PWM duty cycles. This voltage is not available on any device terminal. The supply current required by the charge pump regulator is drawn from VREG.

Two internal linear regulators are integrated: one provides the internal logic supply voltage, V_{DD}, and a second independent programmable regulator provides the supply, V_{IO}, for the digital I/O.

Circuit functions are provided within the AMT49100 to ensure that, under normal operating conditions, all external power MOSFETs are fully enhanced at supply voltages down to 10 V. For extreme battery voltage drop conditions, the AMT49100 is guaranteed not to reset any internal states at supply voltages down to 5 V. A low-power sleep mode allows the AMT49100, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

The AMT49100 includes a number of diagnostic features to provide indication of and/or protection against undervoltage, overvoltage, overtemperature, and power bridge faults. A single diagnostic output terminal can be programmed to provide optional diagnostic outputs, and detailed diagnostic information is available through the serial interface.

For systems requiring a higher level of safety integrity, the AMT49100 includes additional overvoltage monitors on the supplies and the control inputs. In addition, the integrated diagnostics include self-test and verification circuits to ensure verifiable diagnostic operation. When used in conjunction with appropriate system level control, these features can assist power drive systems using the AMT49100 to meet stringent ASIL D safety requirements.

The serial interface also provides access to programmable dead time, fault blanking time, programmable V_{DS} threshold for short detection, and programmable thresholds and currents for open-load detection.

The AMT49100 includes three low-side self-calibrating current sense amplifiers with common programmable output offset and independently programmable gain. These amplifiers are specifically designed for current sensing in the presence of high voltage and current transients. These amplifiers can be used independently to provide low-side current sensing in three phases or can be used together to provide redundant current sensing. The AMT49100 can also check the connections from the current sense amplifiers to the sensing links using integrated verification circuits. The programmed output offset voltage can be made available at the output of each amplifier, measured, stored, and used as the zero output reference potential for each sense amplifier.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Input and Output Terminal Functions

VBB: Main power supply for the buck regulator. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

VBRG: Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drain of the high-side MOSFETs in the bridge. Also used as the reference voltage for the bootstrap charge pump and the non-volatile memory (NVM) programming supply. A 100 nF capacitor should be connected from VBRG to GND close to the device terminals.

VREG: regulated voltage, V_{REG}, nominally 12V , used to supply the low-side gate drivers and to charge the bootstrap capacitors. VREG may be provided by the buck regulator or by an external regulated supply. A sufficiently large storage capacitor must be connected to this terminal to provide the transient charging current.

LX: Buck converter inductor switching node.

CP1, CP2: Pump capacitor connection for bootstrap charge pump. Connect a capacitor with a recommended minimum value of 1 µF between CP1 and CP2.

GND: Ground. Connect both GND terminals together at the AMT49100—see layout recommendations for further information.

CA, CB, CC: High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

GHA, GHB, GHC: High-side gate drive outputs for external N-channel MOSFETs.

SA, SB, SC: Load phase connections. These terminals sense the voltages switched across the load. They are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers.

GLA, GLB, GLC: Low-side gate drive outputs for external N-channel MOSFETs.

LSSA, LSSB, LSSC: Low-side return path for discharge of the capacitance on the MOSFET gates, connected to the sources of the low-side external MOSFETs independently through a low-impedance track.

HA, HB, HC: Logic inputs to control the high-side gate drive outputs. The sense of these inputs can be selected as active high or active low. A pull-down or pull-up is connected to each input depending on the selected sense of the input. Battery voltage compliant terminal.

LA, LB, LC: Logic inputs to control the low-side gate drive outputs. The sense of these inputs can be selected as active high or active low. A pull-down or pull-up is connected to each input depending on the selected sense of the input. Battery voltage compliant terminal.

SDI: Serial data logic input with pull-down. 16-bit serial word input MSB first.

SDO: Serial data output. High impedance when STRn is high. Outputs bit 15 of the status register, the fault flag, as soon as STRn goes low.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCK. There must be 16-rising edges per write, and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

CS1P, CS1M, CS2P, CS2M, CS3P, CS3M: Current sense amplifier inputs.

CS1O, CS2O, CS3O: Current sense amplifier outputs.

DIAG: Diagnostic output. Programmable output to provide one of four functions: fault flag, pulsed fault flag, temperature, and internal timer. Default is fault flag.

ENABLE: Disables all gate drive outputs when pulled low in direct mode or after a timeout in watchdog mode. Provides an independent output disable, directly to the gate drive outputs, to allow a fast disconnect on the power bridge. Can be pulled to VBB.

RESETn: Resets faults when pulsed low. Forces low-power shutdown (sleep) when held low for more than the RESET shutdown time, t_{RSD}. Can be pulled to VBB.

SAL, SBL, SCL: Logic-level outputs representing the state of each phase determined by the output of a programmable threshold comparator.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Power Supplies

The AMT49100 can operate with an integrated fixed-frequency buck regulator producing the main regulated voltage, V_{REG}, at the VREG terminal or with a regulated supply driving the VREG terminal. All internal operating supplies, except for the start-up and sleep state supply and the NVM programming voltage, are derived exclusively from V_{REG}. The start-up and sleep state supply is taken directly from the VBB terminal. The NVM programming voltage is taken from the VBRG terminal.

Buck Regulator Mode

In buck regulator mode, the BRE bit is set to 1 and a single unregulated supply, V_{BB}, of 10 to 80 V is applied to the VBB terminal. If negative supply voltage is expected, then VBB should be connected through a reverse voltage protection circuit. The buck regulator requires a single inductor (L = 100 µH ±20%, I_{SAT} ≥ 420 mA) mounted between the LX and the VREG terminals and a Schottky diode (V_R ≥ 100 V, I_F ≥ 1 A) between the LX and GND terminals. A ceramic decoupling capacitor of at least 4.7 µF should be connected between VBB and GND close to the terminals. The switching frequency of the buck regulator is fixed at 410 kHz.

External Regulated Supply Mode

In external regulated supply (buck regulator disabled) mode, the buck regulator components are not required and the BRE bit is set to 0. In this mode, an external regulated 12 V supply is applied to the VREG terminal and the VBB terminal together for operation. The bridge voltage, V_{BRG}, at the VBRG terminal, can vary over its full operating range from 4.5 to 80 V.

In sleep mode (RESETn = low), the external means of disconnecting the regulated supply voltage from the VREG terminal on the device must be provided as shown in Figure 8.

A ceramic decoupling capacitor of at least 100 nF should be connected between VBB and GND close to the terminals.

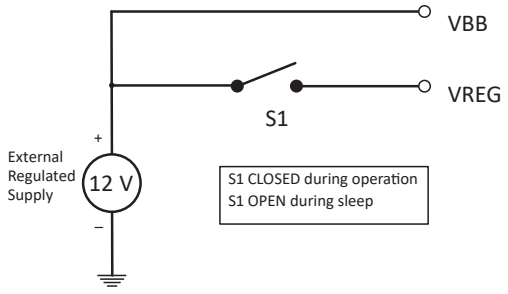


Figure 8: External Regulated Supply Mode

VREG Supply

In both cases, the voltage at the VREG terminal, V_{REG}, is the main operating supply for most of the circuits in the AMT49100. It provides the supply for the internal low-voltage linear regulators, the reference voltage generator, the sense amplifiers, the above VBRG charge pump and the gate drivers. For the gate drivers, this includes the charge current and bias current for the low-side gate drive and the initial charge current for the bootstrap capacitors. A sufficiently large ceramic capacitor must be connected to the VREG terminal to provide the switching currents for the internal logic and logic I/O, the charge pump, and the transient currents for the low-side gate drive and bootstrap charging. This capacitor should have a minimum value of 10 µF, but may need to be larger depending on the total gate charge of the MOSFETs being driven.

VCP Charge Pump Regulator

This regulator generates a voltage above the bridge supply voltage, V_{BRG}. It provides some of the switching current for the high-side drives, the charge current for the bootstrap capacitors at high PWM duty cycles, and the bias current and the gate drive current to hold the high-side MOSFET in the on state.

This regulator uses a charge pump scheme with a switching frequency of 62.5 kHz. The pump capacitor connected between the CP1 and CP2 terminals is charged to V_{REG}, then switches this voltage to be referenced to V_{BRG}. This produces a voltage approximately V_{REG} above V_{BRG}, and provides the required charge current for the high-side gate drive circuits.

The pump capacitor, C_P, between CP1 and CP2, should have a nominal value of 1 µF and should have a rated working voltage of at least 25 V and a tolerance of ±20% or better.

One of four modes of operation may be selected according the value of the CPM[1:0] bits in the System register (Register 7). If CPM[1:0] is set to 00b, the regulator runs in auto mode. Average regulator current is greater than 5 mA per phase until internal device logic detects that no high-side gate drive has been commanded on for more than 200 µs, and then it drops back to a value of just over 200 µA per phase to reduce device dissipation. Alternatively, if CPM[1:0] is set to 01b or 10b, the regulator will drive a fixed current of 200 µA or 5 mA respectively. If CPM[1:0] is set to 11b, the regulator is turned off.

Internal Regulators

Two internal linear regulators are integrated: one provides the internal logic supply voltage, V_{DD}, and a second independent

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

programmable regulator provides the supply, V_{IO}, for all logic inputs and push-pull outputs.

The internal logic regulator is only used for the internal logic and is not available or accessible outside the AMT49100.

The logic I/O regulator can be selected as 3.3 or 5 V by the value in the VIO bit. VIO = 0 sets the I/O voltage to 3.3 V and VIO = 1 sets the I/O voltage to 5 V. This supply is only used to provide the supply for logic inputs and push-pull outputs and is not available or accessible outside the AMT49100.

The sense amplifier outputs are not referenced to the I/O voltage but driven directly from V_{REG}. All three sense amplifier outputs are clamped with a common clamp voltage, V_{CSC}. The sense amplifier clamps are independent from V_{IO}. Care must be taken to select the correct sense amplifier output limit.

Power-Up Sequence

The initial supply is taken from VBB. This energizes the internal logic supply regulator and the internal bias circuits, sets the POR bit to 1, and makes the general fault flag active. Following this, the contents of the NVM are read into the device serial registers. Once the NVM read has completed, the buck regulator is activated if the BRE bit is set to 1. The POR bit in the Status register remains set to 1 until a valid Status register read is completed. During startup, the general fault flag remains in the active state until all gate drive and bridge operating voltages are above their respective undervoltage thresholds. This includes V_{REG}, V_{BRG}, and all three bootstrap voltages. The bridge operating voltage bits in the Diagnostic and Status registers may be set and should be cleared by reading the relevant registers. The AMT49100 will then be fully operational and will respond as specified.

Low Supply Voltage Operation

The AMT49100 will operate within specified parameters with V_{BB} from 10 to 80 V. In all cases, the AMT49100 will operate safely between 0 and 80 V under all supply switching conditions. This provides a very rugged solution for use in the harsh automotive environment.

Low Power Sleep State

RESETn is an active-low input that allows the AMT49100 to enter a sleep state where the current consumption from the main supply and the internal logic regulator is reduced to its minimum level. When RESETn is held low for longer than the reset shutdown time, t_{RSD}, the regulator and all internal circuitry is disabled and the AMT49100 enters the sleep state. In the sleep state, the buck regulator is disabled and the latched faults and corresponding fault flags are cleared, as are any fault bits in the Diagnostic and Status registers. When in the sleep state, all power is taken directly from the VBB terminal. When coming out of the sleep state, the protection logic ensures that the gate drive outputs are off until all gate drive and bridge operating voltages are above their respective undervoltage thresholds (this takes approximately 2 ms under nominal conditions) and any latched fault states are cleared.

To allow the AMT49100 to start up without the need for an external logic input, the RESETn terminal can be pulled to VBB with an external pull-up resistor.

RESETn can also be used to clear any fault conditions without entering the sleep state by taking it low for the reset pulse width, t_{RST}. Any latched fault conditions such as short detection or bootstrap capacitor undervoltage, which disable the outputs, will be cleared, but any fault bits set in the Diagnostic and/or Status registers will not be cleared.

Gate Drives

The AMT49100 is designed to drive external, low on-resistance, power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drives and the main recharge current for the bootstrap capacitors are provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitors connected between the Cx and Sx terminals, one for each phase. MOSFET gate charge and discharge rates may be controlled by setting a group of parameters via the serial interface.

Bootstrap Supply

When the high-side drivers are active, the reference voltage for the gate drive output will rise close to the bridge supply voltage. The supply to the gate drive then must be above the bridge supply voltage to ensure that it remains active. This temporary high-side supply is provided by bootstrap capacitors, one for each high-side driver. These three bootstrap capacitors are connected between the bootstrap supply terminals, CA, CB, and CC, and the corresponding high-side reference terminal, SA, SB, and SC.

The bootstrap capacitors are independently charged to approximately V_{REG} when the associated reference Sx terminal is low. When the output swings high, the voltage on the bootstrap supply terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

When the Sx terminal remains high for extended periods of time,

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

the gate drive voltage is maintained by an additional charge pump that provides a regulated voltage to charge the bootstrap capacitor. This charge pump also provides the charging current when the output PWM duty cycle is too high to permit the bootstrap capacitor to be recharged between high-side turn-on events. This combination of bootstrap drive and charge pump provides the most efficient gate drive system for a PWM system able to operate between 0 and 100% without restriction.

High-Side Gate Drive

High-side, gate-drive outputs for external N-channel MOSFETs are provided on terminals GHA, GHB, and GHC. GHx = 1 (or "high") means that the upper half of the driver is turned on and its drain will source current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. GHx = 0 (or "low") means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET's gate circuit to the respective Sx terminal, turning it off.

The reference points for the high-side drives are the load phase connections, SA, SB, and SC. These terminals sense the voltages at the load connections. They also connect to the negative side of the bootstrap capacitors and are the negative supply reference connections for the floating high-side drivers. The discharge current from the high-side MOSFET gate capacitance flows through these connections, which should have low impedance traces, to the MOSFET bridge.

MOSFET gate charge and discharge rates may be controlled via the serial interface as detailed in the Gate Drive Control section below.

To limit phase node voltage slew and ringing, a series gate resistor with a minimum value of 22 Ω is required. The PCB should be designed to minimize stray inductance and incorporate ceramic capacitors to bypass the bridge supply local to each half bridge. Snubber circuits across each MOSFET can be used where additional noise suppression is needed. For additional information, refer to the AMT49100/1 application note.

Low-Side Gate Drive

The low-side gate-drive outputs on GLA, GLB, and GLC are referenced to the corresponding LSSx terminal. These outputs are designed to drive external N-channel power MOSFETs. GLx = 1 (or "high") means that the upper half of the driver is turned on and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. GLx = 0 (or "low") means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET's gate circuit to the LSSx terminal, turning it off.

The LSSx terminals provide the return paths for discharge of the capacitance on the low-side MOSFET gates. These terminals should be connected independently to the common sources of the low-side external MOSFETs through a low-impedance tracks.

MOSFET gate charge and discharge rates may be controlled via the serial interface as detailed in the Gate Drive Control section below.

To limit phase node voltage slew and ringing, a series gate resistor with a minimum value of 22 Ω is required. The PCB should be designed to minimize stray inductance and incorporate ceramic capacitors to bypass the bridge supply local to each half bridge. Snubber circuits across each MOSFET can be used where additional noise suppression is needed. For additional information, refer to the AMT49100/1 application note.

Gate Drive Passive Pull-Down

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as a variable resistance pull-down but is not active when the AMT49100 is in normal operating mode. At low gate source voltage, the resistance is approximately 1 MΩ to ensure that any charge accumulated on the MOSFET gate has a discharge path. This resistance reduces rapidly as the voltage increases such that any MOSFET gate that becomes charged by external means is rapidly discharged to below the turn-on threshold. In some applications, this can eliminate the requirement for a permanent external gate source resistor.

Dead Time

To prevent cross-conduction (shoot-through) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs are switched at the same time, for example, at the PWM switch point. In the AMT49100, the dead time for all phases is set by the contents of the DT[6:0] bits in Bridge Timing register. These seven bits contain a positive integer that determines the dead time by division from the system clock.

The dead time is defined as:

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[6:0] and t_{DEAD} has a minimum active value of 100 ns.

For example, when DT[6:0] contains [011 0000] (= 48 in decimal), then t_{DEAD} = 2.4 µs, typically.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the Electrical Characteristics table. The range of t_{DEAD} is 100 ns to 6.35 µs. A value of 1 or 2 in DT[6:0] sets the minimum active dead time of 100 ns.

If DT[6:0] is set to zero, the dead timer is disabled and no minimum dead time is generated by the AMT49100. The logic that prevents permanent cross-conduction is, however, still active. Adequate dead time must be generated externally by, for example, the microcontroller producing the drive signals applied to the AMT49100 logic inputs or control register.

If using gate drive control, the extended MOSFET switching times that result must be accounted for when setting dead time, as described in the Gate Drive Control section below.

The internally generated dead time is only present if the on command for one MOSFET occurs within one dead time after the off command for its complementary partner. In the case where one side of a phase drive is permanently off, for example when using diode rectification with slow decay, then the dead time does not occur. In this case, the gate drive turns on within the specified propagation delay after the corresponding phase input goes high. (See Figure 4).

Gate Drive Control

MOSFET gate drives are controlled according to the values set in registers 8 through 13.

High-side off-to-on transitions are controlled as detailed in Figure 9a. When a gate drive is commanded to turn on a current, I_1 (as defined by IHR1[3:0]), is sourced on the relevant GHx terminal for a duration, t_1 (defined by THR[3:0]). These parameters should typically be set to quickly charge the MOSFET input capacitance to the start of the Miller region, as drain-source voltage does not change during this period. Thereafter, the current sourced on GHx is set to a value of I_2 (as defined by IHR2[3:0]) and remains at this value while the MOSFET transitions through the Miller region and reaches the fully on-state. For high-side gate drives, the MOSFET fully on-state is defined as the voltage on the GHx gate drive output rising to a value within 1 V(typ) of the Cx terminal. I_2 should be set to achieve the required rising time on the motor phase connection. Once in the fully on-state, the GHx output switches from current to voltage drive to hold the MOSFET in the on-state.

If the values of IHR1 and IHR2 are set to 0, GHx produces maximum drive to turn on the MOSFET as quickly as possible without attempting to control the input capacitance charge time (Figure 9b). The value of THR has no effect on switching speed.

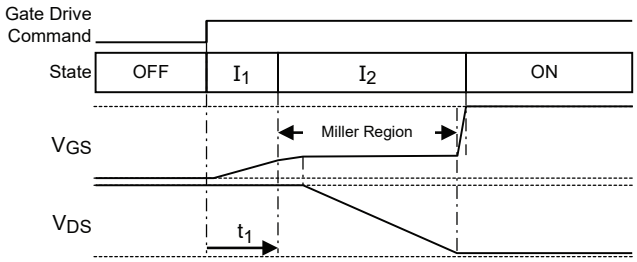


Figure 9a: Off-to-On Transition (Gate Drive Control)

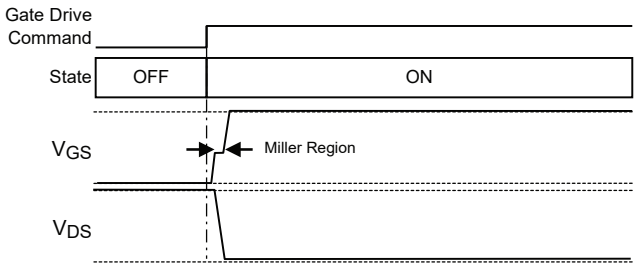


Figure 9b: Off-to-On Transition (Switched)

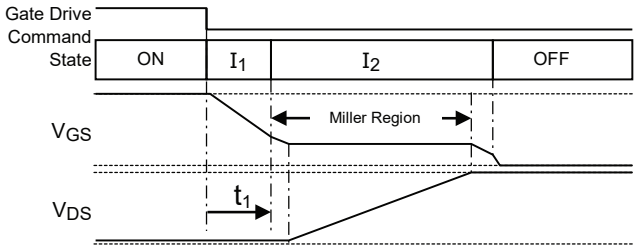


Figure 9c: On-to-Off Transition (Gate Drive Control)

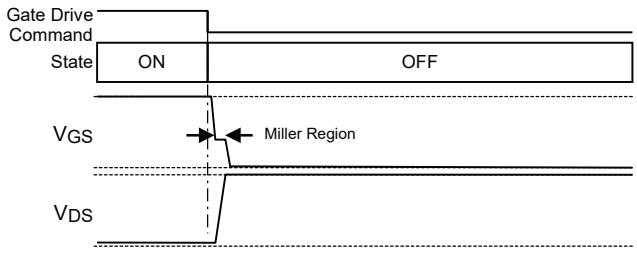


Figure 9d: On-to-Off Transition (Switched)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Low-side off-to-on transitions are controlled in a similar manner by setting TLR[3:0], ILR1[3:0], and ILR2[3:0] to control GLx. For low-side gate drives, the MOSFET fully on-state is defined as the voltage on the GLx gate drive output rising to a value within 1 V(typ) of VREG. I_2 should be set to achieve the required falling slew time on the motor phase connection.High-side on-to-off transitions are controlled as detailed in Figure 9c. When a gate drive is commanded to turn off, a current, I_1 (as defined by IHF1[3:0]), is sunk by the relevant GHx terminal for a duration, t_1 (defined by THF[3:0]). These parameters should typically be set to quickly discharge the MOSFET input capacitance to the start of the Miller region as drain-source voltage does not change during this period. Thereafter, the current sunk by GHx is set to a value of I_2 (as defined by IHF2[3:0]) and remains at this value while the MOSFET transitions through the Miller region and reaches the fully off-state. For high-side gate drives, the MOSFET fully off-state is defined as the voltage on the GHx gate drive output falling to a value within 1 V(typ) of the Sx terminal. I_2 should be set to achieve the required falling slew time on the motor phase connection. Once in the fully off condition, the GHx output switches from current to voltage drive to hold the MOSFET in the off-state.

If the values of IHF1 and IHF2 are set to 0, GHx produces maximum drive to turn off the MOSFET as quickly as possible without attempting to control the input capacitance discharge time (Figure 9d). The value of THF has no effect on switching speed.

Low-side on-to-off transitions are controlled in a similar manner by setting TLF[3:0], ILF1[3:0] and ILF2[3:0] to control GLx. For low-side gate drives the MOSFET fully off-state is defined as the voltage on the GLx gate drive output falling to a value within 1 V(typ) of LSSx. I_2 should be set to achieve the required rising slew time on the motor phase connection.

If non-zero values of I_1 and I_2 are selected, a long enough value of dead time must be set to ensure that any MOSFET turning off fully transitions to the off-state before the complementary MOSFET in the same phase is allowed to start turning on. Gate drive control is active regardless of the set value of dead time.

Logic Control Inputs

Six logic level digital inputs, HA, LA, HB, LB, HC, LC, provide direct control for the gate drives, one for each drive. The Hx inputs correspond to the high-side drives and the Lx inputs correspond to the low-side drives. All logic inputs have standard CMOS levels referenced to the voltage of the logic I/O regulator, V_{IO}, providing compatibility with 3.3 or 5 V control inputs. Logic inputs have a typical hysteresis of 550 mV to improve noise performance. Each input can be shorted to the VBB supply, up to the absolute maximum supply voltage, without damage to the input.

The sense of the gate drive control inputs can be inverted using the HSI and LSI bits. If HSI = 1, the sense of all three high-side inputs HA, HB, and HC are inverted. If LSI = 1, the sense of all three low-side inputs LA, LB, and LC are inverted. The operation of HSI and LSI are shown in the Control Logic Table of Table 1. A pull-down or pull-up is connected to each input depending on the selected sense of the input to ensure a safe state if the control becomes disconnected.

By inverting either the high-side control inputs or the low-side control inputs, the two inputs for each phase can be connected together and driven by a single PWM signal. Inverting the low-side inputs means that the PWM signal should be active high. Conversely, inverting the high-side inputs means that the PWM signal should be active low. If this mode of operation is selected, then an appropriate dead time must be set using the DT variable to ensure that there is no shoot-through at the PWM switching points.

The gate drive outputs can also be controlled through the serial interface by setting the appropriate bit in the control register. In the control register all bits are active high. The logical relationship between the register bit setting and the gate drive outputs is defined in Table 2.

The logic inputs are combined, using logical OR, with the corresponding bits in the serial interface control register to determine the state of the gate drive. The logical relationship between the combination of logic input and register bit setting and the gate drive outputs is defined in Table 3 (assuming HSI = LSI = 0).

In most applications, either the logic inputs or the serial control will be used. When using only the logic inputs to control the bridge, the serial register should be left in the reset condition with all control bits set to 0. When using only the serial interface to control the bridge, the inputs should be connected to GND and HSI and LSI should be set to 0. The internal pull-down resistors on these inputs ensure that they go to the inactive state should they become disconnected from the control signal level.

Internal lockout logic ensures that the high-side output drive and low-side output drive on any one phase cannot be commanded to be active simultaneously When the control inputs request both the high-side MOSFET and the low-side MOSFET to be active at the same time for a single phase, then both high-side and low side gate drives will be forced low.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Output Enable / Disable

The ENABLE input is connected directly to the gate drive output command signal, bypassing the main synchronous logic block on the chip (including all phase control logic). This input can be used to provide a fast output disable (emergency cut-off) or to provide non-synchronous fast decay PWM.

ENABLE can also monitored by a watchdog timer by setting the EWD bit to 1. In this mode, the signal is routed through the synchronous logic block on the chip before connecting to the gate drive output command signal. The first change of state on the ENABLE input will activate the gate drive outputs under command from the corresponding phase control signals and a watchdog timer is started. The ENABLE input must then change state before the end of the ENABLE timeout period, t_{ETO}. If the ENABLE input does not change before the end of the timeout period and FEWD = 1, then all gate drive outputs will be driven low, the ETO bit will be set in the Status register, and the general fault flag will be active. Any following change of state on the ENABLE input will re-activate the gate drive outputs and reset the fault. If FEWD = 0, then the outputs are not affected. The ETO bit remains in the Status register until reset.

Logic Outputs

Any one of the SxL and SDO outputs can be shorted to ground without interfering with signal integrity on the others.

Current Sense Amplifiers

Three programmable-gain/programmable-offset differential sense amplifiers are provided to allow the use of a low-value sense resistor or current shunt as a current sensing element in the low-side connection of each phase. The input common mode range of the CSxP and CSxM inputs allows below ground current sensing typically required for low-side current sense in PWM control of motors, or other inductive loads, during switching transients. The output of the sense amplifier is available at the CSxO outputs and can be used in peak or average current control systems. The output can drive up to 4.8 V to permit maximum dynamic range with higher input voltage A-to-D converters. The maximum output voltage is clamped to V_{CSC} as defined in the Electrical Characteristics table and selected to be compatible with 3.3 or 5 V inputs using the VCL bit.

The gain, A_V, of each sense amplifier is independently programmable and defined by the contents of the S1G[2:0], S2G[2:0], and S3G[2:0] variables as:

SxG	Gain
0	10
1	15
2	20
3	25

SxG	Gain
4	30
5	35
6	40
7	50

A single output offset, V_{OOS}, is common to all sense amplifiers and is defined by the contents of the SAO[3:0] variable as:

SAO	V_{OOS}
0	0
1	0
2	100 mV
3	100 mV
4	200 mV
5	300 mV
6	400 mV
7	500 mV

SAO	V_{OOS}
8	750 mV
9	1 V
10	1.25 V
11	1.5 V
12	1.65 V
13	2 V
14	2.25 V
15	2.5 V

Equations describing the relationship between sense amplifier gain and output offset are shown in Figure 1. Current sense amplifier calibration minimizes Input Offset Voltage, V_{IOS}, and is initiated via the serial interface. Unless calibrated, input offset voltage may exceed the limits detailed in the Electrical Characteristics table. Calibration is not required to achieve the specified Input Offset Voltage Drift Over Temperature, ΔV_{IOS}, and leaves this parameter unaltered.

Amplifiers are calibrated by writing a 1 to the appropriate SxC bit. If an SxC bit is already set to 1, it must first be cleared to 0 before writing 1, otherwise a calibration cycle will not take place. Before initiating a calibration, the relevant positive and negative amplifier input terminals (CSxP and CSxM) must be held at the same potential by ensuring that no current is flowing in the associated sense resistor, and this condition must be maintained until the calibration operation is complete. Calibration starts on the STRn rising edge associated with writing 1 to the SxC bit and is completed within an Offset Calibration Time, t_{Cal}, from this point. After a calibration, the amplifier automatically reverts to normal operating mode. More than one amplifier may be calibrated simultaneously by setting multiple SxC bits on a given serial interface write cycle. The calibration of one amplifier should not be initiated if the calibration of any other is in progress as the accuracy of both operations may be reduced. During calibration, transient voltage variations may be observed on the CSxO terminals.

After completion of automatic calibration, all three SxC bits

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

are set to a default state of 1 requiring that they are cleared to 0 before initiating another calibration.

To eliminate output offset error and drift, the sense amplifier output offset can be output on each sense amplifier output by setting the YOL bit (on-state open-load verification function) to 1. This internally shorts the sense amplifier input to the offset adder to zero, resulting in only the output offset at each sense amplifier. If the offset is then sampled, it can be used to mathematically remove the offset from the current sense signal.

The sense amplifier, including the sense amplifier output, is powered from the VREG regulated voltage to achieve the required performance. To avoid excessive stress on any input protection circuits of external monitoring or measurement circuits, the sense amplifier output voltage is limited by an active clamp circuit with a selectable clamp voltage. The clamp voltage may be selected as 5.2 V, suitable for 5 V compatible inputs by setting VCL to 1, or 3.5 V, suitable for 3.3 V compatible inputs by setting VCL to 0.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Diagnostic Monitors

Multiple diagnostic features provide three levels of fault monitoring. These include critical protection for the AMT49100, monitors for operational voltages and states, and detection of power bridge and load fault conditions. All diagnostics, except for POR, serial transfer error, EEPROM error and overtemperature can be masked by setting the appropriate bit in the mask registers.

Table 5: Diagnostic Functions

Name	Diagnostic	Level
POR	Internal logic supply undervoltage causing power-on reset	Chip
SE	Serial transmission error	Chip
EE	EEPROM error	Chip
OT	Chip junction overtemperature	Chip
TW	High chip junction temperature warning	Monitor
VSO	VBRG supply overvoltage (Load dump detection)	Monitor
VSU	VBRG supply undervoltage	Monitor
VLO	Logic terminal overvoltage	Monitor
ETO	ENABLE input watchdog timeout	Monitor
VRO	VREG output overvoltage	Monitor
VRU	VREG output undervoltage	Monitor
VBR	Buck regulator fault	Monitor
VLU	VIO undervoltage	Monitor
AHU	A high-side VGS undervoltage	Monitor
ALU	A low-side VGS undervoltage	Monitor
BHU	B high-side VGS undervoltage	Monitor
BLU	B low-side VGS undervoltage	Monitor
CHU	C high-side VGS undervoltage	Monitor
CLU	C low-side VGS undervoltage	Monitor
LAD	LSSA Disconnect	Monitor
LBD	LSSB Disconnect	Monitor
LCD	LSSC Disconnect	Monitor
OC1	Overcurrent on sense amplifier 1	Bridge
OC2	Overcurrent on sense amplifier 2	Bridge
OC3	Overcurrent on sense amplifier 3	Bridge
OL	Open Load	Bridge
VA	Bootstrap undervoltage phase A	Bridge
VB	Bootstrap undervoltage phase B	Bridge
VC	Bootstrap undervoltage phase C	Bridge
AHO	Phase A high-side V_{DS} overvoltage	Bridge
ALO	Phase A low-side V_{DS} overvoltage	Bridge
BHO	Phase B high-side V_{DS} overvoltage	Bridge
BLO	Phase B low-side V_{DS} overvoltage	Bridge
CHO	Phase C high-side V_{DS} overvoltage	Bridge
CLO	Phase C low-side V_{DS} overvoltage	Bridge

Except for the three phase state outputs, the fault status is available from two sources: the DIAG output terminal, and the diagnostic and status registers accessed through the serial interface.

DIAG Diagnostic Output

The DIAG terminal is a single diagnostic output signal that can be programmed by setting the contents of the DG[1:0] variable through the serial interface to provide one of four dedicated diagnostic signals:

DG = 0 – a general fault flag

DG = 1 – a pulsed fault flag

DG = 2 – a voltage representing the temperature of the internal silicon

DG = 3 – a clock signal derived from the internal chip clock

At power-up, or after a power-on-reset, the DIAG terminal outputs a general logic-level fault flag which will be active-low if a fault is present. This fault flag remains low while the fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset, the DIAG output will be high.

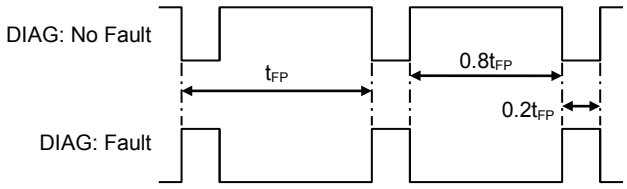


Figure 10: DIAG – Pulsed Output Mode

The pulsed fault output option provides a continuous, low frequency, low-duty cycle pulsed output when a fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset and no fault is present, the signal output on the DIAG terminal is a continuous low frequency, high-duty cycle pulse train. The period of the DIAG signal in pulsed mode is defined by t_{FP} and is typically 100 ms. The two duty cycles are defined by D_{FP} and are typically 20% when a fault is present and 80% when no fault is present.

The temperature output option provides access to the internal voltage representing the surface temperature of the silicon. Temperature may be approximated from this voltage as:

$$T_J \approx (V_{DIAG} - V_{TJD}) / A_{TJD}$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

where T_J is the approximate silicon temperature in ºC, V_{DIAG} is the analog voltage on the DIAG terminal in mV, and V_{TJD} and A_{TJD} are the typical range and slope values presented in the Electrical Characteristics table.

The clock output option provides a logic-level square wave output at a ratio of the internal clock frequency to allow more precise calibration of the timing settings if required.

All digital outputs available on DIAG (DG set to 0, 1, or 3) are open drain. On-state drive capability and off-state leakage current limits are defined in the Electrical Characteristics table by the V_{OL} and I_{ODI} parameters respectively and may be used to calculate a suitable pull-up resistance. In most applications, a resistor in the range 10 to 20 kΩ is suitable.

Diagnostic Registers

The serial interface allows detailed diagnostic information to be read from the diagnostic registers on the SDO output terminal at any time.

A system status register provides a summary of all faults in a single read transaction. The status register is always output on SDO when any register is written.

The first bit (bit 15) of the status register contains a fault flag, FF, which will be high if any of the fault bits in the Status register have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low, the first bit in the status register can be read on SDO to determine if a fault has been detected at any time since the last fault register reset. In all cases, the fault bits in the diagnostic registers are latched and only cleared after a diagnostic register reset when DSR = 0.

Note that FF (bit 15) does not provide the same function as the general fault flag output on the DIAG terminal when STRn is high and the DIAG output is in its default mode. The fault output on the DIAG terminal provides an indication that either a fault is present or the outputs have been disabled due to a latched fault state. FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Chip-Level Protection

Chip-wide parameters critical for correct operation of the AMT49100 are monitored. These include maximum chip temperature, minimum internal logic supply voltage, and serial interface transmission. These three monitors are necessary to ensure that the AMT49100 can respond as specified.

Chip Fault State: Internal Logic Undervoltage

The AMT49100 has an independent integrated logic regulator to supply the internal logic. This is to ensure that external events, other than loss of supply, do not prevent the AMT49100 from operating correctly. The internal logic supply regulator will continue to operate with a low supply voltage, for example, if the main supply voltage drops to a very low value during transient load event. In extreme low supply voltage circumstances, or during power-up or power-down, an undervoltage detector ensures that the AMT49100 operates correctly. The logic supply undervoltage lockout cannot be masked as it is essential to guarantee correct operation over the full supply range.

When power is first applied to the AMT49100, the internal logic is prevented from operating, and all gate drive outputs held in the off state until the internal regulator voltage, V_{DD}, exceeds the logic supply undervoltage lockout rising (turn-on) threshold. At this point, all serial control registers will be reset to their power-on state and all fault states and the general fault flag will be reset. The FF bit and the POR bit in the Status register will be set to one to indicate that a power-on-reset has taken place. The AMT49100 then goes into its fully operational state and begins operating as specified.

Once the AMT49100 is operational, the internal logic supply continues to be monitored. During the operational state, if V_{DD} drops below logic supply undervoltage lockout falling (turn-off) threshold, then the logical function of the AMT49100 cannot be guaranteed and the outputs will be immediately disabled. The AMT49100 will enter a power-down state and all internal activity, other than the logic regulator voltage monitor, will be suspended. If the logic supply undervoltage is a transient event, then the AMT49100 will follow the power-up sequence above as the voltage rises.

Chip Fault State: Overtemperature

If the chip temperature rises above the overtemperature threshold, T_{JF}, the general fault flag will be active and the overtemperature bit, OT, will be set in the Status register. If FOT = 1 when an overtemperature is detected, all gate drive outputs will be disabled automatically. If FOT = 0, then no circuitry will be disabled and action must be taken by the user to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFHys}, the general fault flag will be reset, but the overtemperature bit remains in the Status register until reset.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Chip Fault State: Serial Error

The data transfer into the AMT49100 through the serial interface is monitored for two fault conditions: transfer length and parity. A transfer length fault is detected if there are more than 16 rising edges on SCK or if STRn goes high and there have been fewer than 16 rising edges on SCK. A parity fault is detected if the total number of logic 1 states in the 16-bit transfer is an even number. In both cases, the write will be cancelled without writing data to the registers. In addition, the status register will not be reset, and the FF bit and SE bit will be set to indicate a data transfer error. If the transfer is a diagnostic or verification result read, then the addressed register will not be reset.

If a serial error is detected and FSE = 1, then all gate drive outputs will be driven low (disabled). If FSE = 0, no further action will be taken.

Chip Fault State: EEPROM

Configuration and calibration information is stored within internal EEPROM and loaded into working registers to configure the device at power up. As part of this process, a data integrity check is carried out. If the check returns a single bit error, automatic error correction is applied, and the part starts up. If the check returns a multiple bit error, all gate drives are disabled, the general fault flag is set low, and the EEPROM error bit, EE, is set in the Status register. EEPROM faults can only be cleared by a power-on-reset (POR).

Chip Fault State: Buck Regulator Fault

If the buck regulator is enabled (BRE = 1) and switching, and an open or short circuit is detected between the Lx terminal and ground, the buck regulator will be held in the off state, the general fault flag will be active, the VBR fault bit will be set in the Diagnostic 1 register, and the VR bit will be set in the Status register. Additionally, V_{REG} will not be generated, a VREG undervoltage fault will be indicated, and it will not be possible to turn on any gate drive outputs. To clear the fault, the underlying short or open circuit must be removed and the VBB supply to the AMT49100 must be cycled off and back on. If the buck regulator is not enabled (BRE = 0) or not switching, the VBR bit will never be set.

Operational Monitors

Parameters related to the safe operation of the AMT49100 in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers.

Voltages relating to driving the external power MOSFETs are monitored, specifically V_{REG}, each bootstrap capacitor voltage and the V_{GS} of each gate drive output. The main bridge voltage, V_{BRG}, is monitored for overvoltage and undervoltage events.

The battery-compliant logic inputs and outputs are capable of being shorted to the main supply voltage without damage, but any high voltage on these terminals will be detected. In addition, a watchdog timer can be applied to the ENABLE input to verify continued operation of the external controller.

Monitor: VBB Undervoltage

The voltage at the VBB terminal, V_{BB}, is monitored in order to indicate when the supply is rising or falling. This is to ensure a safe startup and shutdown as V_{BB} is applied or removed. As V_{BB} rises, the buck converter is disabled until V_{BB} rises above the VBB undervoltage rising threshold, V_{BBON}. Once above the rising threshold, the buck converter (if enabled) is allowed to start and run. As V_{BB} falls below the VBB falling undervoltage threshold, V_{BBOFF}, the buck converter is disabled. There are no fault bits set nor any fault output when V_{BB} is undervoltage.

Monitor: VREG Undervoltage and Overvoltage

It is critical to ensure that the regulated voltage, V_{REG}, at the VREG terminal is sufficiently high before enabling any of the outputs.

If V_{REG} goes below the VREG undervoltage threshold, V_{ROFF}, the general fault flag is active and the VREG undervoltage bit, VRU, is set in the Diagnostic 1 register.

If a VREG undervoltage state is present and FVRU = 1, all gate drive outputs go low. When V_{REG} rises above the rising threshold, V_{RON}, the fault is cleared and, if FVRU = 1, the gate drive outputs are re-enabled. The fault bit remains in the Diagnostic register until cleared. If FVRU = 0, fault reporting will be the same, but the gate drive outputs are not disabled and appropriate action to avoid potential misoperation or damage to the AMT49100 and/or bridge MOSFETs must be taken by the external controller.

The VREG undervoltage monitor circuit is active during power up. If FVRU = 1, all gate drives will be low until V_{REG} is greater than V_{RON}. If FVRU = 0, the gate drive outputs will be active as soon as there is sufficient voltage on VREG to activate the gate drive outputs.

The VREG undervoltage monitor can be disabled by setting the VRU bit in the Mask 1 register. Although not recommended, setting VRU to 1 or setting FVRU to 0 can allow the AMT49100 to operate below its minimum specified supply voltage level with a

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

severely impaired gate drive. The specified electrical parameters will not be valid in this condition.

The output of the VREG regulator is also monitored to detect any overvoltage applied to the VREG terminal.

If V_{REG} goes above the VREG overvoltage threshold, V_{ROV}, the general fault flag is active and the VREG overvoltage bit, VRO, is set in the Diagnostic 1 register. If FVRO = 1, all gate drive outputs go low, the motor drive is disabled and the motor coasts. If FVRO = 0, no action is taken and the gate drive outputs are protected from overvoltage by independent Zener clamps. When V_{REG} falls below V_{ROV} by more than the hysteresis voltage, V_{ROVHys}, the general fault flag is cleared, but the VRO bit remains in the Diagnostic 1 register until reset. If the outputs have been disabled because FVRO = 1, they are re-enabled.

Monitor: Temperature Warning

If the chip temperature rises above the temperature warning threshold, T_{JW}, the hot warning bit, TW, will be set in the Status register, and if FTW = 1, all gate drives will be low. If FTW = 0, gate drives will remain active. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHys}, the fault is reset and if FTW = 1, the outputs are re-enabled. The TW bit remains in the Status register until reset.

Monitor: VBRG Supply Overvoltage and Undervoltage

The main battery supply to the bridge, V_{BRG}, is monitored by the AMT49100 on the VBRG terminal to indicate if the supply voltage has exceeded its normal operating range (for example, during a load dump transient). If V_{BRG} rises above the VBRG overvoltage warning threshold, V_{BRGOV}, then the general fault flag will be set, the VSO bit will be set in the Diagnostic 2 register, the VS bit (which indicates the logical OR of the VSO and VSU bits) will be set in the Status register, and if FVSO = 1, all gate drive outputs will be driven low (disabled). When V_{BRG} drops below the falling VBRG overvoltage warning threshold, $V_{BRGOV} - V_{BRGOVHys}$, the general fault flag will be cleared and the gate drive outputs will be re-enabled, but the VSO and VS bits will remain set until the Diagnostic 2 register is read with DSR = 0. If FVSO = 0, fault reporting will be the same, but the gate drive outputs will not be disabled. The VBRG overvoltage warning threshold can be set to one of two levels using the VPO bit.

If V_{BRG} falls below the VBRG undervoltage warning threshold, V_{BRGUV}, then the VSU bit will be set in the Diagnostic 2 register and the VS bit (which indicates the logical OR of the VSO and VSU bits) will be set in the Status register. If FVSU = 1, the general fault flag will be set and all gate drive outputs will be driven low (disabled), causing the motor to coast. When V_{BRG} moves above the rising VBRG undervoltage threshold, $V_{BRGUV} + V_{BRGUVHys}$, the general fault flag will be cleared and the gate drive outputs will be re-enabled, but the VSU and VS bits will remain set until the Diagnostic 2 register is read with DSR = 0. If FVSU = 0, fault reporting will be the same, but the gate drive outputs will be not be disabled. The VBRG undervoltage warning threshold can be set to one of two levels using the VPU bit.

Monitor: VGS Undervoltage

To ensure that the gate drive output is operating correctly, each gate drive output voltage is independently monitored, when active, to ensure the drive voltage, V_{GS}, is sufficient to fully enhance the power MOSFET in the external bridge.

If V_{GS} on any active gate drive output is lower than the gate drive undervoltage warning threshold, V_{GSUV}, the general fault flag will be active, the corresponding gate drive undervoltage bit, AHU, ALU, BHU, BLU, CHU, or CLU will be set in the Diagnostic 0 register, and if FGSU = 1, all gate drive outputs will be inactive (low). The gate drive outputs will remain inactive (low) until the fault state and the general fault flag are reset by a low pulse on the RESETn input, a serial read of the Diagnostic 0 register when DSR = 0, or by a power-on reset. The gate drive undervoltage bits, AHU, ALU, BHU, BLU, CHU, or CLU will only be reset by a serial read of the Diagnostic 0 register when DSR = 0 or by a power-on reset. If FGSU = 0, fault reporting will be the same but the gate drive outputs will be not be disabled.

The output from each VGS undervoltage comparator is filtered by a VGS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VGS fault. The duration of the VGS fault qualifying timer, t_{VDQ}, is determined by the contents of the TVD[5:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100\ ns$$

where n is a positive integer defined by TVD[5:0].

The qualifier can operate in one of two ways, debounce mode or blanking mode, selected by the VDQ bit.

In debounce mode (the default setting), a timer is started each time the comparator output indicates a VGS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate VGS is within 1 V of the voltage on the Cx terminal (high-side gate drives) or VREG (low-side gate drives). If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the VGS fault is considered valid, and the AMT49100 follows the fault action described above.

In blanking mode (optional), a timer is started when any gate drive

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

is turned on or turned off. The outputs from the VGS undervoltage comparators for all MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ}. If any gate drive changes state while a blanking period is in progress, then the timer is re-triggered, resulting in an extended overall blanking time. If any comparator output indicates a VGS fault and the blanking timer is not active, then the VGS fault is considered valid and the AMT49100 follows the fault action described above.

The VDQ and TVD[5:0] qualifier parameters apply to both the VGS undervoltage and VDS overvoltage monitors.

Monitor: Gate Drive Output State

Each gate drive output includes a comparator that detects if the gate drive output is greater or less than 1 V. This is used to provide the output state of each gate drive output. The output of the six comparators are available by reading the xHM and xLM bits in Verify Result 0 register. These bits are continuously updated with the unqualified output of each of the six VGS state comparators. The state of the comparator is captured at the start of each serial transmission.

Monitor: LSS Disconnect

Each LSS terminal includes a continuous current source, I_{LU}, to VREG, that will pull each LSSx terminal up if there is no low-impedance path from the LSSx terminal to ground. If the voltage at an LSSx terminal with respect to ground rises above the rising LSS open threshold, V_{LSO}, then the appropriate LxD bit is set in the Diagnostic 0 register and the general fault flag on DIAG becomes active.

If FLSS = 0, no further action is taken. If the voltage on the LSS pin drops below the falling LSS open threshold, $V_{LSO} - V_{LSOHys}$, the general fault flag becomes inactive. The LxD bit in the Diagnostic register may then be cleared by reading the Diagnostic 1 register.

If FLSS = 1 and FDSO = 0, the low-side VDS overvoltage fault on the same phase as the detected LSS disconnect is also indicated. The relevant xLO bit is set in the Diagnostic 1 register along with the DSO and FF bits in the Status register, and all gate drives are disabled. If the voltage on the LSS pin drops below the falling LSS open threshold, $V_{LSO} - V_{LSOHys}$, the gate drive outputs are re-enabled. The Diagnostic 0 register may then be read to clear the LxD bit. After this, the Diagnostic 1 register may be read to clear the xLO, DSO, and FF bits and the general fault flag.

If FLSS = 1 and FDSO = 1, the low-side VDS overvoltage fault on the same phase as the detected LSS disconnect is also indicated. The relevant xLO bit is set in the Diagnostic 1 register along with the DSO and FF bits in the Status register, and all gate drives are disabled. After the voltage on the LSS pin drops below the falling LSS open threshold, $V_{LSO} - V_{LSOHys}$, the Diagnostic 0 register may be read to clear the LxD bit. Then, the Diagnostic 1 register may be read to clear the xLO, DSO, and FF bits and to set the general fault flag to inactive.

Monitor: Logic Terminal Overvoltage

Eight of the logic inputs are capable of being shorted to the main supply voltage, up to 50 V, without damage. These terminals are HA, LA, HB, LB, HC, LC, ENABLE, and RESETn. The DIAG output can also survive connection to the main supply. Except for RESETn, the voltage on these terminals, V_L, is monitored to provide an indication of an input short-to-battery fault. RESETn is intended to be able to be connected to the supply and is not monitored for overvoltage. If V_L on any of the remaining terminals rises above the logic terminal overvoltage warning threshold, V_{LOV}, then the VLO bit is set in the Status register. Additionally, the general fault flag is set to active (low) except in the case of a DIAG terminal overvoltage where the open-drain output maintains a high-impedance (off) state. The DIAG terminal is protected and the overvoltage detect function is active regardless of the signal output selected via the DG variable in the System register. If the fault is on one of the inputs and FVLO = 1, then all gate drive outputs will be disabled. If FVLO = 0, the outputs are not affected. When V_L on all terminals falls below the logic input overvoltage warning threshold, V_{LOV}, the fault flag will be reset and the outputs will be re-activated. The VLO bit remains in the Status register until reset.

Monitor: VIO Undervoltage

The AMT49100 has an independent integrated logic regulator to provide the reference for all logic inputs and outputs. If the combined external load current drawn from the device's push-pull logic outputs (SxL and SDO) is sufficient to pull this regulator voltage down to a level where the specified logic high output voltage, V_{OH}, cannot be maintained, the general fault flag is activated, the VLU bit is set in the Status register, and if FVLU = 1, the gate drive outputs are disabled. If FVLU = 0, the faults are indicated and recorded but the gate drive outputs remain unaffected. The regulator voltage rises to a sufficiently high value. The fault state is cleared. The VLU bit remains in the register until reset.

Monitor: ENABLE Watchdog Timeout

The ENABLE input provides a direct connection to all gate drive outputs and can be used as a safety override to immediately disable the outputs. The ENABLE input is programmed to

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

operate as a direct logic control by default but can be monitored by a watchdog timer by setting the EWD bit to 1. In the direct mode, the input is not monitored other than for input overvoltage as described in the Logic Input Overvoltage section above. In watchdog mode, the first change of state on the ENABLE input will activate the gate drive outputs under command from the corresponding phase control signals, and a watchdog timer is started. The ENABLE input must then change state before the end of the ENABLE timeout period, t_{ETO}. If the ENABLE input does not change before the end of the timeout period, then the general fault flag will be active, the ETO bit will be set in the Status register, and if FEWD = 1, all gate drive outputs will be driven low (disabled). Any following change of state on the ENABLE input will reset the general fault flag and re-activate the gate drive outputs. If FEWD = 0, the faults will be indicated and stored but the gate drive outputs will not be affected. The ETO bit will remain set in the Status register until reset.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Power Bridge and Load Faults

Bridge: Overcurrent Detect

Current sense amplifiers 1, 2, and 3 are fully independent and may be allocated to any phase (A, B, or C).

The output from each of the three sense amplifiers is fed into a comparator referenced to the overcurrent threshold voltage, V_{OCT}, to provide indication of overcurrent events. V_{OCT} is generated by a 4-bit DAC with a resolution of 300 mV and defined by the contents of the OCT[3:0] variable. V_{OCT} is approximately defined as:

$$V_{OCT} = (n + 1) \times 300\ mV$$

where n is a positive integer defined by OCT[3:0].

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier output and the VOCT threshold and has no effect on the overcurrent threshold, I_{OCT}. In effect, V_{CSD} is compared with V_{OCT} and the relationship between the threshold voltage and threshold current is given by:

$$I_{OCT} = V_{OCT} / (R_S \times A_V)$$

where V_{OCT} is the overcurrent threshold voltage programmed by OCT[3:0], I_{OCT} is the corresponding current value, R_S is the sense resistor value in Ω, and A_V is the sense amplifier gain defined by S1G[2:0], S2G[2:0], or S3G[2:0].

The output from each overcurrent comparator is filtered by an overcurrent qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid overcurrent event. The qualifier can operate in one of two ways: debounce or blanking, selected by the OCQ bit.

In the default debounce mode, a timer is started each time a comparator output indicates an overcurrent detection. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{OCQ}, then the overcurrent event is considered valid and the corresponding overcurrent bit (OC1, OC2, or OC3) will be set in the Diagnostic 2 register.

In the optional blanking mode, a timer is started when any gate drive is turned on. The output from all comparators is ignored (blanked) for the duration of the timeout period, set by t_{OCQ}. If a comparator output indicates an overcurrent event when the blanking timer is not active, then the overcurrent event is considered valid and the corresponding overcurrent bit (OC1, OC2, or OC3) will be set in the Diagnostic 2 register. If a gate drive is turned on while a timeout period is in progress, the timeout is extended to run for a period of t_{OCQ} from the new turn on event. If all gate drives are turned off during a timeout period, the timeout period is terminated.

The duration of the overcurrent qualifying timer, t_{OCQ}, is determined by the contents of the TOC[4:0] variable. t_{OCQ} is approximately defined as:

$$t_{OCQ} = n \times 500\ ns$$

where n is a positive integer defined by TOC[4:0].

When a valid overcurrent is detected with FOC = 1, the general fault flag is set, all gate drive outputs are driven inactive (low), and the corresponding OC1, OC2, and OC3 bits are set. The gate drive outputs will remain inactive (low) until the fault state and the general fault flag are reset by a low pulse on the RESETn input, a serial read of the Diagnostic 2 register when DSR = 0, or by a power-on reset. The OC1, OC2, and OC3 bits will only be reset by a serial read of the Diagnostic 2 register when DSR = 0 or by a power-on reset.

If FOC = 0 and an overcurrent is detected, the general fault flag is set and the corresponding OC1, OC2, and OC3 bits are set, but the outputs remain active.

Bridge: Open-Load Detect

Two open-load fault detection methods are provided: an on-state current monitor and an off-state open-load detector. An on-state is defined by the state of the gate drive outputs as one or two high-side MOSFETs switched on and one or two low-side MOSFETs switched on. The resulting combinations are the only ones where current can be passed through the low-side sense resistor. An off-state is defined by the state of the gate drive outputs as all MOSFETs switched off. In this state, the load connections are high impedance and can be used to detect the presence or otherwise of a load.

On-State Open-Load Detection

On-state open-load detection is only active when AOL = 1, one or two high-side MOSFETs are switched on and one or two low-side MOSFETs are switched on. This excludes the cases where a high-side MOSFET and a low side MOSFET in the same phase are commanded to be on at the same time. Table 4 shows the open-load detection mode for each combination of output demand.

During the on-state, the AMT49100 compares the output from each sense amplifier against the open-load threshold voltage, V_{OLTH}. V_{OLTH} is generated by an internal DAC and is defined by the value in the OLT[3:0] variable. These bits provide the input to a 4-bit DAC with a least significant bit value of typically 25 mV.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The output of the DAC produces V_{OLTH} approximately defined as:

$$V_{OLTH} = n \times 25\ mV$$

where n is a positive integer defined by OLT[3:0].

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier output and the V_{OLTH} threshold and has no effect on the open-load detect threshold current, I_{OLT}. In effect, V_{CSD} is compared with V_{OLTH}, and the relationship between the threshold voltage and threshold current is given by:

$$I_{OLT} = V_{OLTH} / (R_S \times A_V)$$

where V_{OLTH} is the open-load threshold voltage programmed by OLT[3:0], I_{OLT} is the corresponding current value, R_S is the sense resistor value in Ω, and A_V is the sense amplifier gain defined by S1G[2:0], S2G[2:0], or S3G[2:0].

If the output of all sense amplifiers is less than V_{OLTH} during the on-state, then a timer is allowed to increment. If the output of any amplifier is higher than V_{OLTH} during the on-state, then the timer is reset. If the timer reaches the open load timeout value t_{OLTO}, typically 100 ms, then the general fault flag will be active and the open-load fault bit, OL, will be set in the Diagnostic 2 register, indicating a valid open-load condition.

As soon as the output of any amplifier is higher than V_{OLTH} during the on-state, then the general fault flag will be reset, but the open-load fault bit remains in the Diagnostic 2 register until reset.

If the sense amplifier is not used in the application, then the on-state open-load detection can be completely disabled by setting AOL to 0.

Off-State Open-Load Detection

Prior to initiating an off-state open-load test, the bootstrap charge pump must be turned off by setting the charge pump mode variable, CPM[1:0], to 3 and all gate drive outputs must be commanded off. Open-load detection is then initiated by setting YPS = 3. While YPS = 3, a current sink, I_{SD}, is applied to the SB terminal and a current source, I_{SU}, is applied to the SA and SC terminals.

I_{SD} is typically 2.5 mA, which is low enough to allow the AMT49100 to survive a short to VBB on the SB terminal during the off-state without damage, and high enough to discharge any output capacitance in an acceptable time.

The value of I_{SU} is selected by the YSC bit. When YSC = 0, I_{SU} = –90 µA; when YSC = 1, I_{SU} = –410 µA.

Off-state open-load detection relies on there being no residual current in the load or the bridge and no large capacitors connected to the load or the bridge phase connections. If these requirements are not satisfied, then sufficient time must elapse before the state of the load connection is correctly indicated. This timeout is not provided by the AMT49100 and must be managed by the external controller.

Once any residual energy has dissipated, the sink current, I_{SD}, pulls the SB terminal to ground. The source current, I_{SU}, applies a test current to the load. As the sink current is much larger than the source current, the current through the load will be the source current. The voltage at the SB terminal, V_{SB}, should be close to zero and the voltages at the SA and SC terminals, V_{SA} and V_{SC}, will allow the load resistance to be measured. V_{SA} and V_{SC} are compared to the low-side VDS threshold, V_{DSTL}. If V_{SA} or V_{SC} is greater than V_{DSTL}, then the open load fault bit, OL, will be set in the Diagnostic 2 register. The LDF and FF bits will not be set in the Status register. If there are external capacitors connected to the bridge phase nodes or there is residual current in the load, then it may take some time for these nodes to discharge to the final value and OL may indicate a fault during this time. On reaching the final steady-state value, if V_{SA} and V_{SC} are both less than V_{DSTL}, then OL will be 0 and a load is assumed to be present.

To allow the external controller to read the present state of the open-load test result, OL is not latched. The point at which the open-load result is read is therefore controlled by the external controller and should be determined by characterization of the system settling time during the open-load test.

The threshold for load resistance is determined by the current source, I_{SU}, and the low-side VDS threshold, V_{DSTL}.

For example, if V_{DSTL} is 1.2 V and I_{SU} = –410 µA, the equivalent threshold resistance is approximately 3 kΩ, so any load resistance greater than this value is detected as an open-load.

On completion of the open-load test, the variables YSC, YPS, and CPM should all be set to 0 to resume normal operation.

Motor Winding Considerations

If driving a star-connected motor, the on-state and off-state methods described above allow the detection of open-load faults in the bridge-to-motor interconnects and within the motor itself. If driving a delta-connected motor, only faults in the bridge-to-motor interconnects may be detected as motor inter-terminal impedance will remain relatively low in the event of a single-point failure internal to the motor (this type of motor having two internal current paths between each terminal).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Bridge: Bootstrap Capacitor Undervoltage Fault

The AMT49100 attempts to ensure that the bootstrap capacitor always remains charged when it is in the operating state. The bootstrap capacitor voltage is monitored by an undervoltage comparator, which is active when the corresponding high-side gate drive is active (on). If the bootstrap voltage is below the undervoltage threshold, V_{BCUV}, when the high-side is commanded on, or at any time while the high-side is on, then a bootstrap undervoltage fault will be detected.

The action taken when a valid bootstrap undervoltage fault is detected, and the fault reset conditions, depends on the state of the FVBU bit.

If FVBU = 0, the fault state will be latched, the general fault flag will be active, the associated bootstrap undervoltage fault bit (VA, VB, VC) will be set in the Diagnostic 2 register, and the associated gate drive output will be inactive (low). The fault state and the general fault flag, but not the bootstrap undervoltage fault bit, will be reset the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. The general fault flag will only be reset for the duration of the validation timer. The bootstrap undervoltage fault bit will only be reset by a serial read of the Diagnostic 2 register when DSR = 0 or by a power-on reset.

If FVBU = 1, the fault will be latched, the general fault flag will be active, the associated bootstrap undervoltage fault bit (VA, VB, VC) will be set in the Diagnostic 2 register, and all gate drive outputs will be inactive (low).

The gate drive outputs will remain inactive (low) until the fault state and the general fault flag are reset by a low pulse on the RESETn input, a serial read of the Diagnostic 2 register when DSR = 0, or by a power-on reset. The bootstrap undervoltage fault bit will only be reset by a serial read of the Diagnostic 2 register when DSR = 0 or by a power-on reset.

Each bootstrap undervoltage monitor is always active, regardless of whether the associated high-side gate drive is commanded on or off.

The bootstrap undervoltage monitor can be disabled for all three phases by setting the BSU bit in the Mask 2 register. Although not recommended, this can allow the AMT49100 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters may not be valid in this condition.

Bridge: MOSFET VDS Overvoltage Fault

Faults on any external MOSFETs are determined by monitoring the drain-source voltage of the MOSFET and comparing it to a drain-source overvoltage threshold. There are two thresholds, V_{DSTH}, for the high-side MOSFETs, and V_{DSTL} for the low-side. V_{DSTH} and V_{DSTL} are generated by internal DACs and are defined by the values in the VTH[5:0] and VTL[5:0] variables respectively. These variables provide the input to two 6-bit DACs with a least significant bit value of typically 50 mV. The output of the DAC produces the threshold voltage approximately defined as:

$$V_{DSTH} = n \times 50\,mV$$

where n is a positive integer defined by VTH[5:0],

or

$$V_{DSTL} = n \times 50\,mV$$

where n is a positive integer defined by VTL[5:0].

The low-side drain-source voltage for any MOSFET is measured between the adjacent Sx terminal and the adjacent LSSx terminal. Using the LSSx terminal rather than the ground connection avoids adding any low-side current sense voltage to the real low-side drain-source voltage and avoids false VDS fault detection.

The high-side drain-source voltage for any MOSFET is measured between the adjacent Sx terminal and the VBRG terminal. Using the VBRG terminal rather than the VBB avoids adding any reverse diode voltage or high-side current sense voltage to the real high-side drain-source voltage and avoids false VDS fault detection.

The VBRG terminal is an independent low-current sense input to the top of the MOSFET bridge. It should be connected independently and directly to the common connection point for the drains of the power bridge MOSFETs at the positive supply connection point in the bridge. The input current drawn by the VBRG terminal is approximately 1 mA.

Note that the VBRG terminal can withstand a negative voltage up to –5 V. This allows the terminal to remain connected directly to the top of the power bridge during negative transients where the body diodes of the power MOSFETs are used to clamp the negative transient. The same applies to the more extreme case where the MOSFET body diodes are used to clamp a reverse battery connection.

The output from each VDS overvoltage comparator is filtered by a VDS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VDS fault. The duration of the VDS fault qualifying timer, t_{VDQ}, is determined by the contents of the TVD[5:0] variable. t_{VDQ} is

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

approximately defined as:

$$t_{VDQ} = n \times 100\ ns$$

where n is a positive integer defined by TVD[5:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In debounce mode (the default setting), a timer is started each time the comparator output indicates a VDS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the VDS fault is considered valid and the corresponding VDS fault bit, ALO, AHO, BLO, BHO, CLO, or CHO will be set in the Diagnostic 1 register.

In blanking mode (optional), a timer is started when any gate drive is turned on or turned off. The outputs from the VDS overvoltage comparators for all MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ}. If any gate drive changes state while a blanking period is in progress, the timer will be retriggered, resulting in an extended overall blanking time. If any comparator output indicates a VDS fault and the blanking timer is not active, then the VDS fault is considered valid and the corresponding VDS fault bit, ALO, AHO, BLO, BHO, CLO, or CHO is set in the Diagnostic 1 register.

The VDQ and TVD[5:0] qualifier parameters set in the VDS Qualifier register apply to both the VGS undervoltage and VDS overvoltage monitors.

The action taken when a valid VDS fault is detected and the action then required to clear the fault state depend upon the FDSO bit value. If FDSO = 0, the fault state will be latched, the general fault flag will be active, the associated VDS fault bit will be set, and the gate drive for the associated MOSFET will be inactive (low). The gate drive output will remain inactive (low) until the fault state and the general fault flag are reset the next time the MOSFET, on which the fault was detected, is commanded to switch on. The associated VDS fault bit remains set in the Diagnostic 1 register until reset. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. The general fault flag will only be reset for the duration of the validation timer. The VDS fault bits will only be reset by a serial read of the Diagnostic 1 register with DSR = 0 or by a power-on reset.

If FDSO = 1, the fault will be latched, the general fault flag will be active, the associated VDS fault bit will be set, and all gate drive outputs will be inactive (low). The gate drive outputs will remain inactive (low) until the fault state and the general fault flag are reset by a low pulse on the RESETn input, a serial read of the Diagnostic 1 register with DSR = 0, or by a power-on reset. The VDS fault bit will only be reset by a serial read of the Diagnostic 1 register with DSR = 0 or by a power-on reset.

If FDSO = 0, care must be taken to avoid damage to the MOSFET where the VDS fault is detected. Although the MOSFET will be switched off as soon as the fault is detected at the end of the fault validation timeout, it is possible that it could still be damaged by excessive power dissipation and heating. To limit any damage to the external MOSFETs or the motor, the gate drive outputs should be fully disabled by logic inputs from the external controller.

Fault Action

The action taken when one of the diagnostic functions indicates a fault is listed in Table 6.

When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (held in the fault state) until reset. The faults that are latched are indicated in Table 6. Latched fault states are always reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface with DSR = 0. Any fault bits that have been set in the diagnostic registers are only reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface with DSR = 0.

For most of the diagnostic functions, the action taken when a fault state is detected can be programmed to force the gate drive output into the inactive (low) state or to leave them active. The action is selected by setting a 1 or 0 in the specific stop on fault (SoF) bit associated with the diagnostic. The specific SoF bits for each diagnostic and the actions taken for each setting are listed in Table 6.

If a power-on-reset state is detected, all gate drive outputs are driven low and all MOSFETs in the bridge are held in the off state. This persists until the power-on-reset state is cleared.

Setting any of the FVRU, FVSU, FOT, FLSS, or FGSU bits in the Stop-on-Fault registers to 0 such that the gate drive outputs are not disabled in the event of the corresponding fault being detected means that the AMT49100 will not take any action to protect itself or the external bridge MOSFETs and damage may

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

occur. Setting either FVBU or FDSO bits in the Stop-on-Fault registers to 0 results in only the MOSFET on which the fault is detected being turned off for a single PWM cycle. This means that the AMT49100 only takes limited action to protect itself and the external bridge MOSFET and damage may still occur in some circumstances. In all cases appropriate action must be taken by the external controller.

Table 6: Fault Actions

Fault Description	SoF Bit Name	Disable Outputs		Fault State Latched
		SoF Bit = 0	SoF Bit = 1	
No Fault	–	No		–
Power-On-Reset	–	Yes [1]		No
Buck Regulator Fault	–	–	–	–
VREG Undervoltage	FVRU	No [3]	Yes [1]	No
VIO Undervoltage	FVLU	No	Yes [1]	No
Bootstrap Undervoltage	FVBU	Yes [2][3]	Yes [1]	Yes
Logic Terminal Overvoltage	FVLO	No	Yes [1][4]	No
ENABLE WD Timeout	FEWD	No	Yes [1]	No
Overtemperature	FOT	No [3]	Yes [1]	No
LSS Disconnect	FLSS	No [3]	Yes [5]	No [5]
VDS Fault	FDSO	Yes [2][3]	Yes [1]	Yes
Serial Transmission Error	FSE	No	Yes [1]	No
VREG Overvoltage	FVRO	No	Yes [1]	No
VBRG Undervoltage	FVSU	No [3]	Yes [1]	No
VBRG Overvoltage	FVSO	No	Yes [1]	No
VGS Undervoltage	FGSU	No [3]	Yes [1]	Yes
Temperature Warning	FTW	No	Yes [1]	No
Overcurrent	FOC	No	Yes [1]	Yes
Open Load	–	No	No	No
EEPROM	–	Yes [1]	Yes [1]	Yes

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Stated fault condition may damage the AMT49100 and/or bridge MOSFETs unless appropriate action taken by the external controller.
[4] Outputs disabled on Hx, Lx, ENABLE overvoltage, but not on RESETn, DIAG overvoltage.
[5] Creates VDS fault. VDS fault will be latched but LSS disconnect fault will not.

Fault Masks

Individual diagnostics except power-on reset, EEPROM error, serial transmission error, overtemperature, open-load, and overcurrent can be disabled by setting the corresponding bit in the mask registers. Power-on-reset cannot be disabled because the diagnostics and the output control depend on the logic regulator for the internal logic to operate correctly. If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, and no fault flags or diagnostic bits will be set. See Mask Register definition for bit allocation.

Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

Diagnostic and System Verification

To comply with various aspects of safe system design, it is necessary for higher-level safety systems to verify that any diagnostics or functions used to guarantee safe operation are operating within specified tolerances.

There are four basic aspects to verification of diagnostic functions:

- Verify connections
- Verify comparators
- Verify thresholds
- Verify fault propagation

These must be completed for each diagnostic. In addition, the operation of system functions not directly covered by diagnostics should also be verified.

The AMT49100 includes additional verification functions to help the system design comply with any safety requirements. Many of these functions can only be completed when the diagnostics are not required and must be commanded to run by the main system controller. These functions are referred to “off-line” verification.

A few of the functions can be continuously active but the results must be checked by the main system controller on a regular basis. These functions are referred to “on-line” verification.

The frequency with which these off-line verification functions are run, or on-line verifications results are checked, will depend on the safety requirements of the system using the AMT49100.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 7: Verification Functions

Verification Type	Function Verified	Operation	
		Offline	Online
Connection	Phase Connection	Y	
Connection	Sense Amp Connection		Y
Monitor	ENABLE Watchdog	Y	
Monitor	Over Current Detectors	Y	
Monitor	Phase State Monitor		Y
Diagnostic	LSS Connection	Y	
Diagnostic	Overtemperature	Y	
Diagnostic	Temperature Warning	Y	
Diagnostic	VBRG Undervoltage	Y	
Diagnostic	VBRG Overvoltage	Y	
Diagnostic	VREG Diagnostics	Y	
Diagnostic	Bootstrap Capacitor	Y	
Diagnostic	VIO Undervoltage	Y	
Diagnostic	VGS Undervoltage	Y	
Diagnostic	Logic Terminal Diagnostic	Y	
Diagnostic	Open Load Detectors	Y	
Diagnostic	VDS Overvoltage Diagnostic	Y	
Diagnostic	All Gate Drives Off	Y	

On-Line Verification

The following functions are permanently active and will set the appropriate bit in the verification result registers to indicate that the verification has failed. No other action will be taken by the AMT49100. These verification functions verify that certain of the AMT49100 terminals are correctly connected to the power bridge circuit.

Bridge: Phase State Monitor

The bridge phase connections at the SA, SB, and SC terminals are connected to a variable threshold comparator. The output of the comparator is stored in the SAS, SBS, and SCS phase state bits in the Verify Result 1 register, to provide a logic level monitor of the state of the power bridge outputs to the load (logic 1 indicating the voltage on SA, SB, and SC respectively is more positive than the threshold). Additionally, the comparator outputs are made available as discrete logic signals on the SAL, SBL, and SCL terminals (logic high indicating the voltage on SA, SB, and SC respectively, is more positive than the threshold). The threshold for the three comparators, V_{PT}, is generated, as a ratio of the voltage between the VBRG terminal and the GND terminal, by a 6-bit DAC and determined by the contents of the VPT[5:0] variable. VPT is approximately defined as:

$$V_{PT} = (n / 64) \times V_{BRG}$$

where n is a positive integer defined by VPT[5:0].

V_{PT} can be programmed between 0 and 98.4%V_{BRG}.

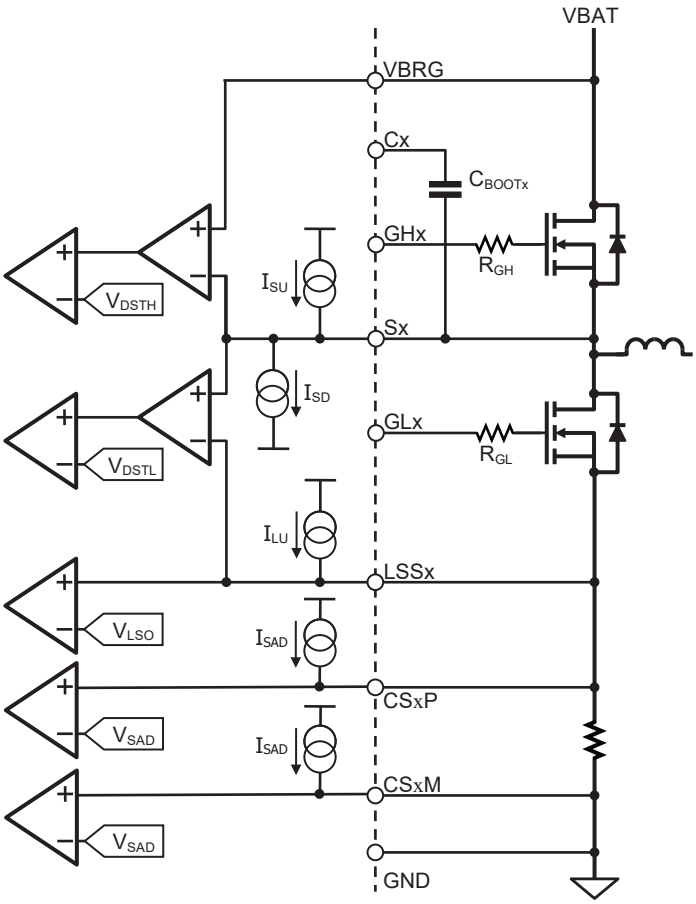


Figure 11: Bridge Terminal Connection Verification

Sense Amplifier Disconnect

Each sense amplifier includes continuous current sources, I_{SAD}, that will allow detection of an input open circuit condition. If an input open circuit occurs, the voltage rises above the sense amplifier open-load detect threshold, V_{SAD}, and the S1D, S2D, or S3D bit is set in the Verify Result 1 register depending upon the sense amplifier affected.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Off-Line Verification

The following functions are only active when commanded by setting the appropriate bit in the verification command registers in addition to any required gate drive commands. If the function only verifies a connection, then a fail will set the appropriate bit in the verification result register. No other action will be taken by the AMT49100. If the function is to verify one of the diagnostic circuits in the AMT49100, then the verification is completed by checking that the associated fault bit is set in the diagnostic registers.

Bridge: Phase Disconnected

The connections from each Sx terminal to the corresponding common node of the high-side MOSFET source and low-side MOSFET drain are verified individually by a combination of MOSFET commands and test currents. The connection to all MOSFETs must be checked to fully verify the connection for each phase.

Connection to each high-side MOSFET is tested by first turning it on using the logic inputs or the serial interface. Other high-side MOSFETs and all low-side MOSFETs must be turned off to avoid corrupting the test result.

The phase to be tested is selected by the value in the verify phase select variable, YPS: 0 for phase B, 1 for phase A, and 2 for phase C. The value of 3 is reserved for open-load testing.

In addition, the bootstrap charge pump must be switched to low current source by setting the charge pump mode variable, CPM, to 1. This is to avoid any unnecessary dissipation in the pump regulator during testing. A pull-down current, I_{SD}, is then switched on by setting YSK to 1 in order to pull the phase low if the high-side MOSFET is either disconnected or not switched on. I_{SD} is typically 2.5 mA, which is low enough to allow the AMT49100 to survive a short to VBB on the SB terminal without damage, and high enough to discharge any output capacitance in an acceptable time.

The high-side VDS monitors are used to determine the state of the phase connection by comparing the VDS voltage of the high-side MOSFET, measured between VBRG and Sx with the programmed high-side VDS threshold, V_{DSTH}.

Test timing is not controlled by the AMT49100 and must be managed by the external controller using the phase disconnect verify command bit, YPH.

Phase disconnect detect relies upon there being no residual current in the load or the bridge and time must be allowed for Sx terminal voltages to stabilize prior to completion of the test.

YPH is taken high to initiate the test and should be held in this state until it is known that any residual energy has dissipated, giving the sink current, I_{SD}, time to pull the Sx terminal to ground in the case of a phase disconnect. At the end of this period, YPH should be set to 0. The PxD bit will then be 1 if the phase is connected and the MOSFET is on and 0 if the phase is disconnected or the MOSFET is off. The PxD bit is reset when the state of the PxD bit is determined by reading the Verify Result 0 register. The value of the PxD bit is not valid when YPH is high.

The low-side disconnect test is complementary to the high-side test. Connection to each low-side MOSFET is tested by first turning it on using the logic inputs or the serial interface. Other low-side MOSFETs and all high-side MOSFETs must be turned off to avoid corrupting the test result.

The phase to be tested is selected by the value in the verify phase select variable, YPS: 0 for phase B, 1 for phase A, and 2 for phase C. The value of 3 is reserved for open-load testing.

In addition, the bootstrap charge pump must be set to normal operation by setting the charge pump mode variable, CPM, to 0.

A pull-up current, I_{SU}, is provided in order to pull the phase high if the low-side MOSFET is either disconnected or not switched on. It is recommended that the value of I_{SU} is switched to –410 µA by setting the YSC bit to 1 when performing phase disconnect tests. This allows I_{SU} to charge any output capacitances in an acceptable time. YSK must be set to 0 during low-side disconnect tests.

The low-side VDS monitors are used to determine the state of the phase connection by comparing the VDS voltage of the low-side MOSFET, measured between Sx and LSSx with the programmed low-side VDS threshold, V_{DSTL}.

Test timing is not controlled by the AMT49100 and must be managed by the external controller using the phase disconnect verify command bit, YPL.

Phase disconnect detect relies upon there being no residual current in the load or the bridge and time must be allowed for Sx terminal voltages to stabilize prior to completion of the test.

YPL is taken high to initiate the test and should be held in this state until it is known that any residual energy has dissipated, giving the source current, I_{SU}, time to pull the Sx terminal to VBRG in the case of a phase disconnect. At the end of this period, YPL should be set to 0. The PxD bit will then be 1 if the phase is connected and the MOSFET is on and 0 if the A phase is disconnected or the MOSFET is off. The PxD bit is reset when the state of the PxD bit is determined by reading the Verify Result 0 register. The value of the PxD bit is not valid when YPL is high.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Verify: VREG Undervoltage

The VREG undervoltage detector is verified by setting the YRU bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the undervoltage threshold and should cause the general fault flag to be active and a VREG undervoltage fault bit, VRU, to be latched in the Diagnostic 1 register. When YRU is reset to 0, the general fault flag will be cleared and the VRU bit will remain set in the Diagnostic 1 register until reset. If the VRU bit is not set, then the verification has failed.

Verify: VREG Overvoltage

The VREG overvoltage detector is verified by setting the YRO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the overvoltage threshold and should cause the general fault flag to be active and a VREG overvoltage fault bit, VRO, to be latched in the Diagnostic 1 register. When YRO is reset to 0, the general fault flag will be cleared and the VRO bit will remain set in the Diagnostic 1 register until reset. If the VRO bit is not set, then the verification has failed.

Verify: VIO Undervoltage

The VIO undervoltage detector is verified by setting the YLU bit in the Verify Command 1 register to 1. This applies a voltage to the comparator that is lower than the undervoltage threshold and should cause the VIO undervoltage fault bit, VLU, to be latched in the Status register. When YLU is reset to 0, the VLU bit will remain set in the Status register until reset. If the VLU bit is not set, then the verification has failed.

Verify: Temperature Warning

The temperature warning detector is verified by setting the YTW bit in the Verify Command 2 register to 1. This applies a voltage to the comparator that is lower than the temperature warning threshold and should cause the general fault flag to be active and a temperature warning fault bit, TW, to be latched in the Status register. When YTW is reset to 0, the general fault flag will be cleared and the TW bit will remain set in the Status register until reset. If the TW bit is not set, then the verification has failed.

Verify: Overtemperature

The overtemperature detector is verified by setting the YOT bit in the Verify Command 2 register to 1. This applies a voltage to the comparator that is lower than the overtemperature threshold and should cause the general fault flag to be active and an overtemperature fault bit, OT, to be latched in the Status register. When YOT is reset to 0, the general fault flag will be cleared and the overtemperature fault will remain in the Status register until reset. If the OT bit is not set, then the verification has failed.

Verify: VBRG Supply Overvoltage

The VBRG overvoltage detector is verified by setting the YSO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the VBRG overvoltage threshold and should cause the general fault flag to be active and a VBRG overvoltage fault bit, VSO, to be latched in the Diagnostic 2 register. When YSO is reset to 0, the general fault flag will be cleared and the VSO bit will remain set in the Diagnostic 2 register until reset. If the VSO bit is not set, then the verification has failed.

Verify: VBRG Supply Undervoltage

The VBRG undervoltage detector is verified by setting the YSU bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the VBRG undervoltage threshold and should cause the general fault flag to be active and a VBRG undervoltage fault bit, VSU, to be latched in the Diagnostic 2 register. When YSU is reset to 0, the general fault flag will be reset and the VSU bit will remain set in the Diagnostic 2 register until cleared. If the VSU bit is not set, then the verification has failed.

Verify: VGS Undervoltage

The VGS undervoltage detectors can be verified individually or in two groups, high-side and low-side. The detectors are verified by switching on the required MOSFET using the serial Control register bits or the logic input terminals and then setting the YGU bit in the Verify Command 0 register to 1. This applies a voltage that is lower than the VGS undervoltage threshold to the active comparator and should cause a VGS undervoltage fault to be latched in the corresponding VGS undervoltage fault bit in the Diagnostic 0 register. (For example, the CHU bit should be set after the CH bit is set in the Control register or the HC input is driven high, etc.) After a period exceeding the programmed VGS qualification time plus a dead time, $t_{VDQ} + t_{DEAD}$, YGU must be returned to 0 and all gate drives must be commanded off. The general fault flag will remain active and the VGS undervoltage fault bits will remain in the Diagnostic 0 register until reset. This must be repeated until all MOSFETs have been switched to verify all VGS undervoltage comparators. If any VGS fault bit is not set after all MOSFETs have been switched, then the verification has failed for the corresponding comparator.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Verify: Bootstrap Capacitor Undervoltage Fault

The bootstrap capacitor undervoltage detectors are verified by setting the YBU bit in the Verify Command 0 register to 1. This applies a voltage that is lower than the bootstrap undervoltage threshold to each of the three bootstrap circuit detectors and should cause the general fault flag to be active and a bootstrap undervoltage fault to be latched in the corresponding bootstrap undervoltage fault bits (VA, VB, VC) in the Diagnostic 2 register.

When YBU is reset to 0, the states of the bootstrap fault bits are latched into the Diagnostic 2 register. If any of the bootstrap fault bits is not set, then the verification of the corresponding detector has failed. All bootstrap fault bits and the general fault flag are cleared when the Diagnostic 2 register is read.

Verify: MOSFET VDS Overvoltage Fault

The VDS overvoltage detectors can be verified individually or in two groups: high-side and low-side. The detectors are verified by commanding the intended MOSFETs to turn on using the serial command register bits or the logic input terminals and then setting the YDO bit in the Verify Command 0 register to 1. This applies a voltage that is higher than the VDS overvoltage threshold to any active detector by turning on the complementary MOSFET in the same phase (rather than the commanded MOSFET) to pull the Sx node toward VBB (low-side verification) or LSSx (high-side verification). In response, a VDS overvoltage fault should be latched in the corresponding VDS overvoltage fault bit in the Diagnostic 1 register. (For example, the CHO bit should be set after the CH bit is set in the Control register or the HC input is set to turn on the GHC output, etc.)

After a period exceeding the programmed VDS qualification time plus a dead time, $t_{VDQ} + t_{DEAD}$, the YDO bit must be returned to 0 to exit the verification mode. Diag 1 should then be read to inspect and clear the xLO, xHO bits. This must be repeated until all MOSFETs have been switched to verify all VDS overvoltage comparators. If any VDS overvoltage fault bit has not been set after all MOSFETs have been commanded on, then the verification has failed for the corresponding comparator.

Verify: LSS Disconnect

The LSS disconnect detectors are verified by setting the YLS bit in the Verify Command 2 register to 1. This applies a voltage to each LSS open comparator that is greater than the LSS open threshold and should cause the LSS open fault bits, LAD, LBD, and LCD, to be latched in the Diagnostic 0 register. When YLS is reset to 0, the open fault bits will remain set in the Diagnostic 1 register until reset. If the any LSS open fault bits, LAD, LBD, and LCD is not set, then the verification has failed.

Verify: Logic Terminal Overvoltage

The logic overvoltage detector is verified by setting the YLO bit in the Verify Command 0 register to 1. This applies a voltage to the comparators associated with each relevant logic terminal that is higher than the logic input overvoltage warning, V_{LOV}. Consequently, the input overvoltage fault bit, VLO, in the Status register should be set. To complete the verification, the YLO bit should be set to 0 and the state of the VLO bit should then be read from the Status register. If the VLO bit is set to 1, then the verification has passed, and if set to 0, then it has failed. During the period when YLO is set to 1, the general fault flag may be active and the gate drive outputs may be disabled but neither of these conditions indicates a successful logic input voltage verification.

Verify: Overcurrent Detect and Sense Amplifier

The overcurrent detector is verified by setting the YOC bit in the Verify Command 1 register to 1. This forces the output of each sense amplifier to positive full-scale which can then be measured. The sense amplifier outputs remain connected to the overcurrent comparators and the full-scale output applies a voltage to the comparator that is higher than the overcurrent threshold and should cause the overcurrent fault bits, OC1, OC2, and OC3 to be latched in the Diagnostic 2 register. When YOC is reset to 0, the sense amplifier outputs will return to normal operation and the OC1, OC2, and OC3 bits will remain set in the Diagnostic 2 register until reset. If any of the OC1, OC2, or OC3 bits are not set, then the verification has failed for the corresponding comparator.

During verification of the overcurrent detector, the overcurrent threshold voltage, V_{OCT}, set by OCT[3:0], plus any offset, V_{OOS}, set by SAO[3:0] must not exceed the positive extreme of the sense amplifier output dynamic range of 4.8 V. If it does, then the OC1, OC2, and OC3 bits may not be set and the verification may fail.

Verify: ENABLE Watchdog Timeout

The ENABLE watchdog timeout is verified by setting the EWD bit to 1 to select the watchdog mode and then changing the state of the ENABLE input. This change of state will enable the gate drive outputs under command from the corresponding phase control signals and will start the watchdog timer. The ENABLE input must then be held in this state. At the end of the timeout period, t_{ETO}, the ETO bit should be set in the status register. If the ETO bit is not set then the verification has failed.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Verify: All Gate Drives Off

The successful propagation of control inputs demanding all-gate-drives-off to the gate drive outputs is verified by setting up an appropriate input condition and inspecting the GDO bit in the Verify Result 1 register. If the input condition has successfully turned off all six gate drives the GDO bit is set. The control input conditions (i.e the combinational states of Hx, Lx, xH, xL, HSI, LSI, and ENABLE) that demand all outputs off (GHx = L, GLx = L) and hence set the GDO bit as a result of a successful verification test can be determined by inspection of Tables 1 – 3. If the ENABLE watchdog mode is selected (EWD = 1) and the watchdog timeout is allowed to expire, the GDO bit will similarly be set as the result of a successful test. Verification of propagation from an appropriate combination of phase logic inputs (Hx, Lx) and serial register bits (xH, xL) to the gate drive outputs does not verify propagation from the ENABLE input to the gate drive outputs and vice versa. Gate drive off events are not latched in the Verify Result 1 register and the GDO bit returns to 0 as soon as any gate drive is detected to be in the on state.

Verify: On-State Open-Load Detection and Sense Amplifier

The on-state open-load detector is verified by turning on a low-side gate drive (to select a phase for test) and at least one high-side (on a different phase), setting the activate open load detection bit, AOL, to 1 and then setting the open-load verify bit, YOL to 1. For this verification operation, sense amplifier 1 is verified by turning on phase A low-side, sense amplifier 2 by turning on phase B low-side and sense amplifier 3 by turning on phase C low-side. Turning on the low-side forces the output of the sense amplifier associated with the selected phase to its zero current output condition (equivalent to zero differential input), which then drives the open-load comparator with a voltage that is lower than the comparator's threshold and produces an on-state open-load fault after the open-load timeout.

When YOL is first set to 1, any open load faults are cleared and the open-load timer is reset. At the end of a 100 ms timeout period, if an open-load state has successfully been detected, the YOL bit is reset to indicate that the timeout is complete and the OL and LDF bits should be inspected. If both bits are set the verification has been successful. The OL bit and the LDF bit remain latched until reset. After a period of 102 ms from YOL being set to 1, if an open-load state has not been successfully detected, the YOL bit is reset by the AMT49100. If YOL is reset to 0 before the timeout has completed, then the verification is terminated without setting any fault bits. All three phases must be tested separately to complete the verification.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SERIAL INTERFACE

Table 8: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Bridge Timing	0	0	0	0	0	WR		OCQ	DT6	DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	0	0	0	0	0	
1: Bridge Monitor	0	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	TOC4	TOC3	TOC2	TOC1	TOC0	P
							0	0	1	0	0	1	1	1	1	
2: VDS Qualifier	0	0	0	1	0	WR	VDQ			TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
							0	0	0	0	1	0	0	0	0	
3: Bridge Diagnostics	0	0	0	1	1	WR	VPO			VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
							1	0	0	0	1	1	0	0	0	
4: Bridge Diagnostics	0	0	1	0	0	WR				VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
							0	0	0	0	1	1	0	0	0	
5: Bridge Monitor	0	0	1	0	1	WR	AOL			VPU		OLT3	OLT2	OLT1	OLT0	P
							0	0	0	0	0	1	0	0	0	
6: Bridge Monitor	0	0	1	1	0	WR	EWD			VPT5	VPT4	VPT3	VPT2	VPT1	VPT0	P
							0	0	0	1	0	0	0	0	0	
7: System	0	0	1	1	1	WR	VIO	VCL	BRE	CPM1	CPM0	DSR		DG1	DG0	P
							0/1‡	0/1‡	0/1†	0	0	0	0	0	0	
8: HS Drive Timing	0	1	0	0	0	WR		THR3	THR2	THR1	THR0	THF3	THF2	THF1	THF0	P
							0	0	0	0	0	0	0	0	0	
9: HS Drive Current	0	1	0	0	1	WR		IHR13	IHR12	IHR11	IHR10	IHF13	IHF12	IHF11	IHF10	P
							0	0	0	0	0	0	0	0	0	
10: HS Drive Current	0	1	0	1	0	WR		IHR23	IHR22	IHR21	IHR20	IHF23	IHF22	IHF21	IHF20	P
							0	0	0	0	0	0	0	0	0	
11: LS Drive Timing	0	1	0	1	1	WR		TLR3	TLR2	TLR1	TLR0	TLF3	TLF2	TLF1	TLF0	P
							0	0	0	0	0	0	0	0	0	
12: LS Drive Current	0	1	1	0	0	WR		ILR13	ILR12	ILR11	ILR10	ILF13	ILF12	ILF11	ILF10	P
							0	0	0	0	0	0	0	0	0	
13: LS Drive Current	0	1	1	0	1	WR		ILR23	ILR22	ILR21	ILR20	ILF23	ILF22	ILF21	ILF20	P
							0	0	0	0	0	0	0	0	0	

* Power-on reset value shown below each input register bit.
† Factory set power-on reset value is 1 on AMT49100KJPTR-A-3, AMT49100KJPTR-A-5, and 0 on AMT49100KJPTR-B-3, AMT49100KJPTR-B-5.
‡ Factory set power-on reset value is 1 on AMT49100KJPTR-A-5, AMT49100KJPTR-B-5, and 0 on AMT49100KJPTR-A-3, AMT49100KJPTR-B-3.

Continued on the next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 8: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
14: Sense Amp Offset	0	1	1	1	0	WR	S3C	S2C	S1C			SAO3	SAO2	SAO1	SAO0	P
							0	0	0	0	0	1	1	1	1	
15: Sense Amp Gain	0	1	1	1	1	WR	S3G2	S3G1	S3G0	S2G2	S2G1	S2G0	S1G2	S1G1	S1G0	P
							0	1	0	0	1	0	0	1	0	
16:NVM Write	1	0	0	0	0	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	
18: Stop on Fault 0	1	0	0	1	0	WR	FOT	FTW		FLSS		FSE	FVLU	FVLO	FEWD	P
							1	1	0	0	0	1	1	1	1	
19: Stop on Fault 1	1	0	0	1	1	WR	FOC		FDSO	FGSU	FVBU	FVRO	FVRU	FVSO	FVSU	P
							1	0	1	1	1	1	1	1	1	
20: Verify Command 0	1	0	1	0	0	WR		YDO	YRO	YRU	YBU	YLO	YSO	YSU	YGU	P
							0	0	0	0	0	0	0	0	0	
21: Verify Command 1	1	0	1	0	1	WR	YPH	YPL	YOC	YLU	YOL	YPS1	YPS0	YSK	YSC	P
							0	0	0	0	0	0	0	0	0	
22: Verify Command 2	1	0	1	1	0	WR	YTW	YOT		YLS						P
							0	0	0	0	0	0	0	0	0	
23: Verify Result 0	1	0	1	1	1	0	PCD	PBD	PAD	CHM	CLM	BHM	BLM	AHM	ALM	P
							0	0	0	0	0	0	0	0	0	
24: Verify Result 1	1	1	0	0	0	0			GDO	SCS	SBS	SAS	S3D	S2D	S1D	P
							0	0	1	0	0	0	0	0	0	
25: Mask 0	1	1	0	0	1	WR	LCD	LBD	LAD	CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
26: Mask 1	1	1	0	1	0	WR	VRO	VRU	VBR	CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
27: Mask 2	1	1	0	1	1	WR	VS	VLO	BSU	TW	VLU					P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Continued on the next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 8: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
28: Diagnostic 0	1	1	1	0	0	0	LCD	LBD	LAD	CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
29: Diagnostic 1	1	1	1	0	1	0	VRO	VRU	VBR	CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
30: Diagnostic 2	1	1	1	1	0	0	VC	VB	VA	VSO	VSU	OC3	OC2	OC1	OL	P
							0	0	0	0	0	0	0	0	0	
31: Control	1	1	1	1	1	WR	HSI	LSI		CH	CL	BH	BL	AH	AL	P
							0	0	0	0	0	0	0	0	0	
Status	FF	POR	SE	EE	OT	TW	VS	VLO	ETO	VR	VLU	LDF	BSU	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the AMT49100. The SDO terminal can be used, during a serial transfer, to provide diagnostic feedback and readback of the register contents.

The AMT49100 can be operated without the serial interface using the default settings and the logic control inputs; however, application-specific configurations and several verification functions are only possible by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the bridge MOSFETs directly.

The serial interface timing requirements are specified in the electrical characteristics table and illustrated in Figure 3. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high, allowing a common data readback connection.

After 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the registers are reset depending on the type of transfer and the state of the DSR bit.

If there are more than 16 rising edges on SCK or if STRn goes high, and there are fewer than 16 rising edges on SCK (either being described as a framing error), the write will be cancelled without latching data to the register. The read-only registers, Status, Diagnostic, or Verification Result will not be reset.

The first five bits, D[15:11], in a serial word are the register address bits giving the possibility of 32 register addresses. The sixth bit, WR (D[10]), is the write/read bit. Except for the read-only registers, when WR is 1 the following 9 bits, D[9:1], clocked in from the SDI terminal are written to the addressed register. When WR is 0 the following 9 bits, D[9:1], clocked in from the SDI terminal are ignored, no data is written to the serial registers and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer, D[0], is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

In addition to the addressable registers, a read-only status register is output on SDO for all register addresses when WR is set to 1. For all serial transfers, the first six bits output on SDO will always be the first six bits from the status register. Register data is output on the SDO terminal msb first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the status register, is output as soon as STRn goes low.

Registers 20-24 and 28-30 contain verification results and diagnostic fault indicators and are read only. If the WR bit for these registers is set to 1 then the data input through SDI is ignored and the contents of the status register is clocked out on the SDO terminal then reset as for a normal write. No other action is taken. If the WR bit for these registers is set to 0 then the data input through SDI is ignored and the contents of the addressed register is clocked out on the SDO terminal and the addressed register is reset when DSR = 0.

If a framing error is detected and/or the parity of any received transfer is even rather than odd the SE bit is set in the Status register to indicate a data transfer error. Any data write will be cancelled without latching data to the register and read-only registers will not be reset. This fault condition can be cleared by a subsequent valid serial write or by a power-on-reset.

In some systems, it is preferable to be able to read the status or diagnostic registers without causing a reset and allowing the AMT49100 to re-enable the outputs. The DSR (Disable Serial Reset) bit provides this functionality. When DSR is set to one any valid read of any of the read only registers will not result in that register being reset. When DSR = 0, any valid read of any of the read only registers will reset the content of that register. This provides a way for the external controller to access the diagnostic information without automatically re-enabling any outputs but retains a way to reset the faults under control of the controller.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Configuration Registers

Seventeen registers are used to configure the operating parameters of the AMT49100.

Register 0: Bridge timing settings:

- OCQ, selects the overcurrent time qualifier mode, blank or debounce.
- DT[6:0], a 7-bit integer to set the dead time, t_{DEAD}, in 50 ns increments.

Register 1: Bridge monitor setting:

- OCT[3:0], a 4-bit integer to set the overcurrent threshold voltage, V_{OCT}, in 300 mV increments.
- TOC[4:0], a 5-bit integer to set the overcurrent verification time, t_{OCQ}, in 500 ns increments.

Register 2: VDS Qualifier:

- VDQ, selects the VDS and VGS qualifier mode, blank or debounce.
- TVD[5:0], a 6-bit integer to set the VDS and VGS fault qualification time, t_{VDQ}, in 100 ns increments.

Register 3: Bridge diagnostic thresholds:

- VPO, selects the VBRG overvoltage threshold.
- VTL[5:0], a 6-bit integer to set the low-side drain-source threshold voltage, V_{DSTL}, in 50 mV increments.

Register 4: Bridge diagnostic thresholds:

- VTH[5:0], a 6-bit integer to set the high-side drain-source threshold voltage, V_{DSTH}, in 50 mV increments.

Register 5: Bridge monitor setting:

- AOL, Activate on-state open-load detection.
- VPU, selects VBRG undervoltage threshold.
- OLT[3:0], a 4-bit integer to set the open-load threshold voltage, V_{OLTH}, in 25 mV increments.

Register 6: Bridge monitor setting:

- EWD, Activate ENABLE watchdog monitor.
- VPT[5:0], a 6-bit integer to set the phase comparator threshold voltage, V_{PT}, as a ratio of the bridge voltage, V_{BRG}, in 1.56% increments from 0 to 98.4%.

Register 7: System:

- VIO, Selects Logic I/O voltage as 3.3 or 5 V.
- VCL, Selects Sense Amplifier Clamp voltage as 3.5 or 5.2 V.
- BRE, Buck regulator enabled/disabled bit.
- CPM[1:0], two bits to select the charge pump mode.
- DSR, disables reset on serial transfer.
- DG[1:0], a two-bit integer to select the signal output on the DIAG terminal.

Register 8: High-side gate drive timing:

- THR[3:0], a 4-bit integer to set the high-side rising (GHx low-to-high) I1 Time in 16 ns increments.
- THF[3:0], a 4-bit integer to set the high-side falling (GHx high-to-low) I1 Time in 16 ns increments.

Register 9: High-side gate drive current:

- IHR1[3:0], a 4-bit integer to set the high-side rising (GHx low-to-high) I1 Current in 16 mA increments.
- IHF1[3:0], a 4-bit integer to set the high-side falling (GHx high-to-low) I1 Current in 16 mA increments.

Register 10: High-side gate drive current:

- IHR2[3:0], a 4-bit integer to set the high-side rising (GHx low-to-high) I2 Current in 16 mA increments.
- IHF2[3:0], a 4-bit integer to set the high-side falling (GHx high-to-low) I2 Current in 16 mA increments.

Register 11: Low-side gate drive timing:

- TLR[3:0], a 4-bit integer to set the low-side rising (GLx low-to-high) I1 Time in 16 ns increments.
- TLF[3:0], a 4-bit integer to set the low-side falling (GLx high-to-low) I1 Time in 16 ns increments.

Register 12: Low-side gate drive current:

- ILR1[3:0], a 4-bit integer to set the low-side rising (GLx low-to-high) I1 Current in 16 mA increments.
- ILF1[3:0], a 4-bit integer to set the low-side falling (GLx high-to-low) I1 Current in 16 mA increments.

Register 13: Low-side gate drive current:

- ILR2[3:0], a 4-bit integer to set the low-side rising (GLx low-to-high) I2 Current in 16 mA increments.
- ILF2[3:0], a 4-bit integer to set the low-side falling (GLx high-to-low) I2 Current in 16 mA increments.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Register 14: Sense amplifier offset:

- S3C, S2C, S1C, initiates current sense amplifier input offset calibration.
- SAO[3:0], a 4-bit integer to set the sense amplifier offset of between 0 and 2.5 V.

Register 15: Sense amplifier gain:

- S1G[2:0], a 3-bit integer to set the sense amplifier 1 gain between 10 and 50 V/V.
- S2G[2:0], a 3-bit integer to set the sense amplifier 2 gain between 10 and 50 V/V.
- S3G[2:0], a 3-bit integer to set the sense amplifier 3 gain between 10 and 50 V/V.

Register 16: NVM Write control:

- SAV[1:0], Controls and reports saving the register contents to the NVM.

Stop-On Fault Registers

Two registers to control whether gate drive outputs are to remain enabled or be disabled in response to faults. See Diagnostics section for further detail of fault actions.

Register 18: Stop on Fault 0:

On bit per fault type to define stop on fault behavior for OT, TW, LCD, LBD, LAD, SE, VLU, VLO and EWD diagnostics.

Register 19: Stop on Fault 1:

On bit per fault type to define stop on fault behavior for OC, DSO, GSU, VBU, VRO, VRU, VSO and VSU diagnostics.

Verification Registers

Four registers are used to manage the system and diagnostic verification features.

Register 20: Verify Command 0:

Individual bits to initiate off-line verification tests for VDS, VREG, Bootstrap undervoltage, logic overvoltage, VBRG, and VGS diagnostics.

Register 21: Verify Command 1:

Individual bits to initiate off-line verification tests for phase disconnect, overcurrent, logic I/O undervoltage, and open-load diagnostics.

Register 22: Verify Command 2:

Individual bits to initiate off-line verification tests for TW, OT, and LSS disconnect diagnostics.

Register 23: Verify Result 0 (read only):

Individual bits holding the results of the phase disconnect, verification tests. When DSR = 0, these bits are reset on completion of a successful read of the register. This register also contains the gate drive output state for each MOSFET. These bits are captured at the start of each serial transmission.

Register 24: Verify Result 1 (read only):

Individual bits holding the results of phase state, sense amp and gate drive off verification tests. When DSR = 0, these bits are reset on completion of a successful read of the register.

Diagnostic Registers

In addition to the read-only status register, three read-only diagnostic registers provide detailed diagnostic management and reporting. When DSR = 0, any bits set in a diagnostic register are reset on completion of a successful read of that register. When DSR = 1, the register will not be reset. Reading one diagnostic register will not affect the fault bits in any other register. Reading the status register will not affect fault bits in any diagnostic register.

Register 28: Diagnostic 0 (read only):

Individual bits indicating faults detected in LSS disconnect for each phase and VGS undervoltage diagnostic monitors for each gate drive output.

Register 29: Diagnostic 1 (read only):

Individual bits indicating faults detected in VDS diagnostic monitors for each gate drive output, the VREG diagnostic monitors, and the buck regulator monitor.

Register 30: Diagnostic 2 (read only):

Individual bits indicating faults detected in bootstrap undervoltage, VBRG, overcurrent, and open-load diagnostic monitors.

Mask Registers

Three mask registers allow individual diagnostics to be disabled. If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, no fault flags or diagnostic bits will be set, and no action will be taken if the corresponding fault conditions are present.

Register 25: Mask 0:

Individual bits for each gate drive output to disable VGS diagnostic monitors and the LSS disconnect monitor for each phase.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Register 26: Mask 1:

Individual bits to disable VDS diagnostic monitors for each gate drive output, the VREG monitor, and the buck regulator monitor.

Register 27: Mask 2:

Individual bits to disable VBRG, logic, bootstrap, temperature, and logic I/O regulator diagnostic monitors.

Control Register

The Control register (register 31) contains one control bit for each MOSFET and the high-side and low-side input invert control:

- HSI: sets the sense of the high-side logic inputs.
- LSI: sets the sense of the low-side logic inputs.
- CH, CL: MOSFET Control bits for Phase C.
- BH, BL: MOSFET Control bits for Phase B.
- AH, AL: MOSFET Control bits for Phase A.

Status Register

There is one status register in addition to the addressable registers. When any register transfer takes place, the first six bits output on SDO are always the most significant six bits of the status register irrespective of whether the addressed register is being read or written (see serial timing diagram). The content of the remaining ten bits will depend on the state of the WR bit input on SDI. Except for the read-only registers, when WR is 1, the addressed register will be written and the remaining ten bits output on SDO will be the least significant nine bits of the status register followed by a parity bit. For the read-only registers, that is the two verification result registers and the three diagnostic registers. When WR is 1, the data bits will be ignored, no data will be written to the register, and the remaining ten bits output on SDO will be the least significant nine bits of the status register followed by a parity bit.

For both read-only and read/write registers, when WR is 0, the addressed register will be read and the remaining ten bits will be the contents of the addressed register followed by a parity bit.

The read-only status register provides a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant three bits of the status register indicate critical system faults. Bits 11 through 1 provide indicators for specific individual monitors and the contents of the three diagnostic registers. The contents and mapping to the diagnostic registers is listed in Table 9.

The first most significant bit in the register is the diagnostic status flag, FF. This is high if any bits in the status register are set. If there are no fault bits in the status register, then FF will be zero. When STRn goes low to start a serial write, SDO outputs the diagnostic status flag. This allows the main controller to poll the AMT49100 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state.

The second most significant bit is the POR bit. At power-up or after a power-on-reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on reset has taken place. All other diagnostic bits are reset and all other registers are returned to their default state. Note that a power-on reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on reset is not affected by the state of the VBRG supply or VREG regulator output. In general, the VR, VRU, and VLU bits may also be set following a power-on reset as the regulators will not have reached their respective rising undervoltage thresholds until after the register reset is completed.

Table 9: Status Register Mapping

Status Register Bit	Diagnostic	Related Diagnostic Register Bits
FF	Status Flag	None
POR	Power-on-reset	None
SE	Serial Error	None
EE	EEPROM Error	None
OT	Overtemperature	None
TW	Temperature warning	None
VS	VBRG out of range	VSU, VSO
VLO	Logic OV	None
ETO	ENABLE timeout	None
VR	VREG monitor	VRU, VRO, VBR
VLU	VIO UV	None
VLO	Logic Overvoltage	None
LDF	Load monitor	OC1, OC2, OC3, OL
BSU	Bootstrap UV	VA, VB, VC
GSU	VGS UV	AHU, BHU, CHU, ALU, BLU, CLU
DSO	VDS OV	AHO, BHO, CHO ALO, BLO, CLO

UV = Undervoltage, OV = Overvoltage

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The third bit in the status register is the SE bit, which indicates that the previous serial transfer was not completed successfully.

The fourth bit in the status register is the EE bit, which indicates that an EEPROM error was detected at device power up.

Of the remaining bits, the contents of OT, TW, VLO, ETO, VLU, and VCU are determined by individual diagnostics. These bits along with the POR and SE bits will be reset on the completion of a successful serial write transaction if DSR = 0. If DSR = 1, the fault bits will not be affected. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the reset.

The contents of the remaining bits in the status register, VS, VR, LDF, BSU, GSU, and DSO are all derived from the contents of the diagnostic registers. These bits are only cleared when the corresponding contents of the diagnostic registers are read and reset; they cannot be reset by reading the status register. A fault indicated on any of the related diagnostic register bits will set the corresponding status bit to 1. The related diagnostic register must then be read to determine the exact fault and clear the fault state if the fault condition has cleared.

Non-Volatile Memory

The values in the configuration and control registers are held in non-volatile EEPROM (NVM), allowing the AMT49100 to be pre-programmed with different default values for each application, thus avoiding the need to program the register contents at each power on.

The AMT49100 provides a simple method to write the contents of the registers into the NVM using the serial interface. When the SAV[1:0] bits in register 16 are changed from [01] to [10], in a single serial write, the present contents of registers 0 to 15, 18, 19, 25 to 27, and 31 are saved (written to NVM) as a single operation. The contents of registers 16, 17, 20 to 24, 28 to 30, and the status register is not written to NVM. The save sequence takes typically 400 ms to complete. It is not possible to save single register values. Although the gate drive may be active during the save sequence, it is recommended that the gate drive outputs are inactive (low) before starting a save sequence to avoid any corruption caused by the electrical noise or any faults from the load.

The register save sequence requires a programming voltage V_{PP} to be applied to the VBRG terminal. V_{PP} must be present on the VBRG terminal for a period, t_{PRS}, before the save sequence is started. V_{PP} must remain on VBRG until the save sequence is completed.

During the save sequence, the SPI remains active for read only. Any attempt to write to the registers during the save sequence will cause the FF and SE bits to be set in the Status register.

During the save sequence, the AMT49100 will automatically complete all the necessary steps to ensure that the NVM is correctly programmed and will complete the sequence by verifying that the contents of the NVM have been securely programmed. On successful completion of a save sequence, the SAV[1:0] bits will be set to [01]. Register 16 should be read to determine if the save has completed successfully. If SAV[1:0] is reset to [00], then the save sequence has been terminated and has not completed successfully.

If V_{PP} drops to an unacceptably low level during a save sequence, the sequence will be terminated and SAV[1:0] will be reset to 00.

To externally verify the data saved in the NVM, the VBB supply must be cycled off then on to cause a power-on reset. Following a power-on reset, the contents of the NVM are copied to the serial registers and can then be read through the serial interface and verified.

Refer to the NVM - Programming Parameters section of the Electrical Characteristics table for the permissible number of EEPROM write cycles and the maximum junction temperature limit that applies during programming.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Bridge Timing	0	0	0	0	0	WR		OCQ	DT6	DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	0	0	0	0	0	
1: Bridge Monitor	0	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	TOC4	TOC3	TOC2	TOC1	TOC0	P
							0	0	1	0	0	1	1	1	1	

*Power-on reset value shown below each input register bit.

Register 0: Bridge Timing

OCQ Overcurrent time qualifier mode

OCQ	Qualifier	Default
0	Debounce	D
1	Blanking	

DT[6:0] Dead time.

$t_{DEAD} = n \times 50$ ns

where n is a positive integer defined by DT[6:0]. For example,
for the power-on reset condition,
DT[6:0] = [010 0000], t_{DEAD} = 1.6 µs.

The range of t_{DEAD} is 100 ns to 6.35 µs. Selecting a value of 1 or 2 will set the dead time to 100 ns. The default value of DT[6:0] = 32 sets the dead time to 1.6 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 1: Bridge Monitor

OCT[3:0] Overcurrent threshold.

$V_{OCT} = (n + 1) \times 300$ mV

where n is a positive integer defined by OCT[3:0], e.g. for the power-on-reset condition
OCT[3:0] = [0010] then V_{OCT} = 0.9 V.
The range of V_{OCT} is 0.3 to 4.8 V.

TOC[4:0] Overcurrent qualify time.

$t_{OCQ} = n \times 500$ ns

where n is a positive integer defined by TOC[4:0], e.g. for the power-on-reset condition
TOC[4:0] = [0 1111] then t_{OCQ} = 7.5 µs.
The range of t_{OCQ} is 0 to 15.5 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2: VDS Qualifier	0	0	0	1	0	WR	VDQ			TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
							0	0	0	0	1	0	0	0	0	
3: Bridge Diagnostics	0	0	0	1	1	WR	VPO			VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
							1	0	0	0	1	1	0	0	0	

*Power-on reset value shown below each input register bit.

Register 2: VDS Qualifier

VDQ VDS and VGS Fault qualifier mode.

VDQ	VDS and VGS Fault Qualifier	Default
0	Debounce	D
1	Blank	

TVD[5:0] VDS and VGS qualification time.

$t_{VDQ} = n \times 100$ ns

where n is a positive integer defined by TVD[5:0].
e.g. for the power-on-reset condition
TVD[5:0] = [01 0000] then t_{VDQ} = 1.6 µs.
The usable range of t_{VDQ} is 0.6 to 6.3 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 3: Bridge Diagnostic Thresholds

VPO VBRG Overvoltage threshold.

VPO	VBRGOV Threshold	Default
0	52 V	
1	58 V	D

VTL[5:0] Low-side VDS overvoltage threshold.

$V_{DSTL} = n \times 50$ mV

where n is a positive integer defined by VTL[5:0],
e.g. for the power-on-reset condition
VTL[5:0] = [01 1000] then V_{DSTL} = 1.2 V.
The range of V_{DSTL} is 0 to 3.15 V.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4: Bridge Diagnostics	0	0	1	0	0	WR				VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
							0	0	0	0	1	1	0	0	0	
5: Bridge Monitor	0	0	1	0	1	WR	AOL			VPU		OLT3	OLT2	OLT1	OLT0	P
							0	0	0	0	0	1	0	0	0	

*Power-on reset value shown below each input register bit.

Config 4: Bridge Diagnostics

VTH[5:0] High-side VDS overvoltage threshold.

$V_{DSTH} = n \times 50$ mV

where n is a positive integer defined by VTH[5:0], e.g. for the power-on-reset condition VTH[5:0] = [01 1000] then V_{DSTH} = 1.2 V. The range of V_{DSTH} is 0 to 3.15 V.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 5: Bridge Monitor

AOL On-state open-load detect.

AOL	On-State Open-Load Detect	Default
0	Inactive	D
1	Active	

VPU VBRG Undervoltage threshold.

VPU	VBRGUV Threshold	Default
0	20 V	D
1	36 V	

OLT[3:0] Open-load threshold.

$V_{OLTH} = n \times 25$ mV

where n is a positive integer defined by OLT[3:0], e.g. for the power-on-reset condition OL[3:0] = [1000] then V_{OLT} = 200 mV. The range of V_{OLTH} is 0 to 375 mV.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6: Bridge Monitor	0	0	1	1	0	WR	EWD			VPT5	VPT4	VPT3	VPT2	VPT1	VPT0	P
							0	0	0	1	0	0	0	0	0	
7: System	0	0	1	1	1	WR	VIO	VCL	BRE	CPM1	CPM0	DSR		DG1	DG0	P
							0	0	0/1†	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 6: Bridge Monitor Settings

EWD ENABLE Watchdog.

EWD	ENABLE Watchdog	Default
0	Disabled	D
1	Active	

VPT[5:0] Phase comparator threshold.

$V_{PT} = (n / 64) \times V_{BRG}$

where n is a positive integer defined by VPT[5:0], e.g. for the power-on-reset condition VPT[5:0] = [10 0000] then V_{PT} = 50% V_{BRG}. The range of V_{PT} is 0 to 98.4% V_{BRG}.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

† Factory-set power-on-reset value of BRE is selected by part number:
AMT49100KJPTR-A-3, AMT49100KJPTR-A-5:
BRE = 1, Buck Enabled.
AMT49100KJPTR-B-3, AMT49100KJPTR-B-5:
BRE = 0, Buck Disabled.

‡ Factory-set power-on-reset values of VIO and VCL are selected by part number:
AMT49100KJPTR-A-5, AMT49100KJPTR-B-5:
VIO = 1 (Logic I/O Voltage = 5V),
VCL = 1 (Clamp = 5.2 V).
AMT49100KJPTR-A-3, AMT49100KJPTR-B-3:
VIO = 0 (Logic I/O Voltage = 3V3),
VCL = 1 (Clamp = 3.5 V).

Register 7: System

VIO Select Logic I/O voltage.

VIO	Logic I/O Voltage	Default
0	3.3 V	‡
1	5 V	‡

VCL Select Sense Amp Clamp voltage.

VCL	Sense Amp Clamp Voltage	Default
0	3.5 V	‡
1	5.2 V	‡

BRE Buck regulator enable.

BRE	Buck Regulator Operation	Default
0	Disabled	†
1	Enabled	†

CPM Charge pump mode.

CPM1	CPM0	Charge Pump Mode	Default
0	0	Auto 5 mA / 200 µA	D
0	1	200 µA	
1	0	5 mA	
1	1	Off	

DSR Disable Serial Reset.

DSR	Reset on serial read	Default
0	Enabled	D
1	Disabled	

DG Select signal routed to DIAG.

DG1	DG0	Signal on DIAG output	Default
0	0	Fault – low true	D
0	1	Pulse Fault	
1	0	Temperature	
1	1	Clock	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8: HS Drive Timing	0	1	0	0	0	WR		THR3	THR2	THR1	THR0	THF3	THF2	THF1	THF0	P
							0	0	0	0	0	0	0	0	0	
9: HS Drive Current	0	1	0	0	1	WR		IHR13	IHR12	IHR11	IHR10	IHF13	IHF12	IHF11	IHF10	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 8: High-side gate drive timing

THR[3:0] High-side rising t1 Time.

$t_1 = 60\ \text{ns} + (n \times 16\ \text{ns})$

where n is a positive integer defined by THR[3:0], e.g. if THR[3:0] = [0001] then t_1 = 76 ns. The range of t_1 is 60 to 300 ns.

THF[3:0] High-side falling t1 Time.

$t_1 = 60\ \text{ns} + (n \times 16\ \text{ns})$

where n is a positive integer defined by THF[3:0], e.g. if THF[3:0] = [0001] then t_1 = 76 ns. The range of t_1 is 60 to 300 ns.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 9: High-side gate drive current

IHR1[3:0] High-side rising I1 Current.

$I_1 = n \times -16\ \text{mA}$

where n is a positive integer defined by IHR1[3:0], e.g. if IHR1[3:0] = [1000] then I_1 = –128 mA. The range of I_1 is –16 to –240 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IHF1[3:0] High-side falling I1 Current.

$I_1 = n \times 16\ \text{mA}$

where n is a positive integer defined by IHF1[3:0], e.g. if IHF1[3:0] = [1000] then I_1 = 128 mA. The range of I_1 is 16 to 240 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10: HS Drive Current	0	1	0	1	0	WR		IHR23	IHR22	IHR21	IHR20	IHF23	IHF22	IHF21	IHF20	P
							0	0	0	0	0	0	0	0	0	
11: LS Drive Timing	0	1	0	1	1	WR		TLR3	TLR2	TLR1	TLR0	TLF3	TLF2	TLF1	TLF0	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 10: High-side gate drive current

IHR2[3:0] High-side rising I2 Current.

$I_2 = n \times -16$ mA

where n is a positive integer defined by IHR2[3:0], e.g. if IHR2[3:0] = [1000] then $I_2 = -128$ mA. The range of I_2 is –16 to –240 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IHF2[3:0] High-side falling I2 Current.

$I_2 = n \times 16$ mA

where n is a positive integer defined by IHF2[3:0], e.g. if IHF2[3:0] = [1000] then $I_2 = 128$ mA. The range of I_2 is 16 to 240 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 11: Low-side gate drive timing

TLR[3:0] Low-side rising t1 Time.

$t_1 = 60$ ns + ($n \times 16$ ns)

where n is a positive integer defined by TLR[3:0], e.g. if TLR[3:0] = [0001] then $t_1 = 76$ ns. The range of t_1 is 60 to 300 ns.

TLF[3:0] Low-side falling t1 Time.

$t_1 = 60$ ns + ($n \times 16$ ns)

where n is a positive integer defined by TLF[3:0], e.g. if TLF[3:0] = [0001] then $t_1 = 76$ ns. The range of t_1 is 60 to 300 ns.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12: LS Drive Current	0	1	1	0	0	WR		ILR13	ILR12	ILR11	ILR10	ILF13	ILF12	ILF11	ILF10	P
							0	0	0	0	0	0	0	0	0	
13: LS Drive Current	0	1	1	0	1	WR		ILR23	ILR22	ILR21	ILR20	ILF23	ILF22	ILF21	ILF20	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 12: Low-side gate drive current

ILR1[3:0] Low-side rising I1 Current.

$I_1 = n \times -16$ mA

where n is a positive integer defined by ILR1[3:0], e.g. if ILR1[3:0] = [1000] then $I_1 = -128$ mA. The range of I_1 is –16 to –240 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

ILF1[3:0] Low-side falling I1 Current.

$I_1 = n \times 16$ mA

where n is a positive integer defined by ILF1[3:0], e.g. if ILF1[3:0] = [1000] then $I_1 = 128$ mA. The range of I_1 is 16 to 240 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 13: Low-side gate drive current

ILR2[3:0] Low-side rising I2 Current.

$I_2 = n \times -16$ mA

where n is a positive integer defined by ILR2[3:0], e.g. if ILR2[3:0] = [1000] then $I_2 = -128$ mA. The range of I_1 is –16 to –240 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

ILF2[3:0] Low-side falling I2 Current.

$I_2 = n \times 16$ mA

where n is a positive integer defined by ILF2[3:0], e.g. if ILF2[3:0] = [1000] then $I_2 = 128$ mA. The range of I_2 is 16 to 240 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
14: Sense Amp Offset	0	1	1	1	0	WR	S3C	S2C	S1C			SAO3	SAO2	SAO1	SAO0	P
							0	0	0	0	0	1	1	1	1	
15: Sense Amp Gain	0	1	1	1	1	WR	S3G2	S3G1	S3G0	S2G2	S2G1	S2G0	S1G2	S1G1	S1G0	P
							0	1	0	0	1	0	0	1	0	

*Power-on reset value shown below each input register bit.

Register 14: Sense Amp Offset

S3C Sense amplifier 3 input offset calibrate

S2C Sense amplifier 2 input offset calibrate

S1C Sense amplifier 1 input offset calibrate

A zero to one transition initiates calibration cycle.

SAO[3:0] Sense amp offset

SAO	Offset	Default
0	0	
1	0	
2	100 mV	
3	100 mV	
4	200 mV	
5	300 mV	
6	400 mV	
7	500 mV	
8	750 mV	
9	1 V	
10	1.25 V	
11	1.5 V	
12	1.65 V	
13	2 V	
14	2.25 V	
15	2.5 V	D

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 15: Sense Amp Gain

S3G[2:0] Sense amplifier 3 gain.

S3G	Gain	Default
0	10	
1	15	
2	20	D
3	25	
4	30	
5	35	
6	40	
7	50	

S2G[2:0] Sense amplifier 2 gain.

S2G	Gain	Default
0	10	
1	15	
2	20	D
3	25	
4	30	
5	35	
6	40	
7	50	

S1G[2:0] Sense amplifier 1 gain.

S1G	Gain	Default
0	10	
1	15	
2	20	D
3	25	
4	30	
5	35	
6	40	
7	50	

where SxG is a positive integer defined by SxG[2:0].

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16: NVM Write	1	0	0	0	0	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 16: Write NVM control

SAV[1:0] Save parameters to Non-Volatile Memory (NVM)

When SAV[1:0] is changed from 01 to 10, the present contents of registers 0 to 15, 18, 19, 25 to 27, and register 31 are written to NVM.
When the NVM save has completed successfully, SAV[1:0] will be set to 01 and can be read to verify completion of the write. If SAV[1:0] is reset to 00, the save has not completed successfully.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
18: Stop on Fault 0	1	0	0	1	0	WR	FOT	FTW		FLSS		FSE	FVLU	FVLO	FEWD	P
							1	1	0	0	0	1	1	1	1	
19: Stop on Fault 1	1	0	0	1	1	WR	FOC		FDSO	FGSU	FVBU	FVRO	FVRU	FVSO	FVSU	P
							1	0	1	1	1	1	1	1	1	

*Power-on reset value shown below each input register bit.

Register 18: Stop on Fault 0

- FOT Overtemperature
- FTW Temperature Warning
- FLSS LSS Disconnect
- FSE Serial Error
- FVLU VIO Undervoltage
- FVLO Logic Overvoltage
- FEWD ENABLE WD Timeout

P Parity bit. Ensures an odd number of 1s in any serial transfer.

See Table 6 for details of each diagnostic.

Register 19: Stop on Fault 1

- FOC Overcurrent
- FDSO VDS Overvoltage
- FGSU VGS Undervoltage
- FVBU Bootstrap Undervoltage
- FVRO VREG Overvoltage
- FVRU VREG Undervoltage
- FVSO VBRG Overvoltage
- FVSU VBRG Undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

See Table 6 for details of each diagnostic.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
20: Verify Command 0	1	0	1	0	0	WR		YDO	YRO	YRU	YBU	YLO	YSO	YSU	YGU	P
							0	0	0	0	0	0	0	0	0	
21: Verify Command 1	1	0	1	0	1	WR	YPH	YPL	YOC	YLU	YOL	YPS1	YPS0	YSK	YSC	P
							0	0	0	0	0	0	0	0	0	
22: Verify Command 2	1	0	1	1	0	WR	YTW	YOT		YLS						P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 20: Verify Command 0

YDO VDS Overvoltage
YRO VREG Overvoltage
YRU VREG Undervoltage
YBU Bootstrap Capacitor Undervoltage
YLO Logic Overvoltage
YSO VBRG Supply Overvoltage
YSU VBRG Supply Undervoltage
YGU VGS Undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 21: Verify Command 1

YPH Phase Disconnect High-Side
YPL Phase Disconnect Low-Side
YOC Overcurrent
YLU VIO Undervoltage
YOL On-State Open Load

YPS[1:0] Phase diagnostic select.

YPS1	YPS0	Phase Diagnostic	Default
0	0	Phase B Disconnect	D
0	1	Phase A Disconnect	
1	0	Phase C Disconnect	
1	1	Off-state open load*	

YSK I_{SD} (2.5 mA) sink on phase selected by YPS*
YSC I_{SU} (–410 µA) source on phase selected by YPS*

* When YPS = 3, Phase B has a fixed 2.5 mA sink and the source current on phases A and C are common and set by YSC.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 22: Verify Command 2

YTW Temperature Warning
YOT Overtemperature
YLS LSS Disconnect

P Parity bit. Ensures an odd number of 1s in any serial transfer.

For Verify Command Registers except YPS, YSK, and YSC

Yxx	Verification	Default
0	Inactive	D
1	Active and Initiate	

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23: Verify Result 0	1	0	1	1	1	0	PCD	PBD	PAD	CHM	CLM	BHM	BLM	AHM	ALM	P
							0	0	0	0	0	0	0	0	0	
24: Verify Result 1	1	1	0	0	0	0			GDO	SCS	SBS	SAS	S3D	S2D	S1D	P
							0	0	1	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 23: Verify Result 0 (read only)

PCD Phase C connected

PBD Phase B connected

PAD Phase A connected

CHM Phase C high-side gate drive output state

CLM Phase C low-side gate drive output state

BHM Phase B high-side gate drive output state

BLM Phase B low-side gate drive output state

AHM Phase A high-side gate drive output state

ALM Phase A low-side gate drive output state

xxx	Verification Result	Default
0	Not detected	D
1	Detected	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 24: Verify Result 1 (read only)

GDO All gate drives off

SCS Phase C state

SBS Phase B state

SAS Phase A state

S3D Sense amp 3 disconnect

S2D Sense amp 2 disconnect

S1D Sense amp 1 disconnect

xxx	Verification Result	Default
0	Not detected	D
1	Detected	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
25: Mask 0	1	1	0	0	1	WR	LCD	LBD	LAD	CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
26: Mask 1	1	1	0	1	0	WR	VRO	VRU	VBR	CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
27: Mask 2	1	1	0	1	1	WR	VS	VLO	BSU	TW	VLU					P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 25: Mask 0

- LCD LSSC disconnect
- LBD LSSB disconnect
- LAD LSSA disconnect
- CHU Phase C high-side VGS undervoltage
- CLU Phase C low-side VGS undervoltage
- BHU Phase B high-side VGS undervoltage
- BLU Phase B low-side VGS undervoltage
- AHU Phase A high-side VGS undervoltage
- ALU Phase A low-side VGS undervoltage
- P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 26: Mask 1

- VRO VREG Overvoltage
- VRU VREG Undervoltage
- VBR Buck regulator Fault
- CHO Phase C high-side VDS overvoltage
- CLO Phase C low-side VDS overvoltage
- BHO Phase B high-side VDS overvoltage
- BLO Phase B low-side VDS overvoltage
- AHO Phase A high-side VDS overvoltage
- ALO Phase A low-side VDS overvoltage
- P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 27: Mask 2

- VS VBRG out of range
- VLO Logic Overvoltage
- BSU Bootstrap undervoltage
- TW Temperature Warning
- VLU VIO undervoltage

- P Parity bit. Ensures an odd number of 1s in any serial transfer.

For All Mask Registers

xxx	Fault Mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, no fault flags or diagnostic bits will be set, and no action will be taken if the corresponding fault conditions are present.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
28: Diagnostic 0	1	1	1	0	0	0	LCD	LBD	LAD	CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
29: Diagnostic 1	1	1	1	0	1	0	VRO	VRU	VBR	CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
30: Diagnostic 2	1	1	1	1	0	0	VC	VB	VA	VSO	VSU	OC3	OC2	OC1	OL	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 28: Diagnostic 0 (read only)

- LCD — LSSC disconnect
- LBD — LSSB disconnect
- LAD — LSSA disconnect
- CHU — Phase C high-side VGS undervoltage
- CLU — Phase C low-side VGS undervoltage
- BHU — Phase B high-side VGS undervoltage
- BLU — Phase B low-side VGS undervoltage
- AHU — Phase A high-side VGS undervoltage
- ALU — Phase A low-side VGS undervoltage
- P — Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 29: Diagnostic 1 (read only)

- VRO — VREG Overvoltage
- VRU — VREG Undervoltage
- VBR — Buck regulator fault
- CHO — Phase C high-side VDS overvoltage
- CLO — Phase C low-side VDS overvoltage
- BHO — Phase B high-side VDS overvoltage
- BLO — Phase B low-side VDS overvoltage
- AHO — Phase A high-side VDS overvoltage
- ALO — Phase A low-side VDS overvoltage
- P — Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 30: Diagnostic 2 (read only)

- VC — Phase C bootstrap undervoltage
- VB — Phase B bootstrap undervoltage
- VA — Phase A bootstrap undervoltage
- VSO — VBRG Overvoltage
- VSU — VBRG Undervoltage
- OC3 — Overcurrent on sense amp 3
- OC2 — Overcurrent on sense amp 2
- OC1 — Overcurrent on sense amp 1
- OL — Open load
- P — Parity bit. Ensures an odd number of 1s in any serial transfer.

For All Diagnostic Registers

xxx	Status
0	No fault detected
1	Fault detected

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31: Control	1	1	1	1	1	WR	HSI	LSI		CH	CL	BH	BL	AH	AL	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 31: Control

HSI Invert high-side logic inputs

LSI Invert low-side logic inputs

CH Phase C, High-side gate drive

CL Phase C, Low-side gate drive

BH Phase B, High-side gate drive

BL Phase B, Low-side gate drive

AH Phase A, High-side gate drive

AL Phase A, Low-side gate drive

See Table 2 and Table 3 for control logic operation.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status	FF	POR	SE	EE	OT	TW	VS	VLO	ETO	VR	VLU	LDF	BSU	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Status

FF Status register flag

POR Power-on-reset

SE Serial Error

EE EEPROM Error

OT Overtemperature

TW High temperature warning

VS VBRG out of range

VLO Logic overvoltage

ETO ENABLE watchdog timeout

VR VREG out of range

VLU VIO undervoltage

LDF Load fault

BSU Bootstrap undervoltage

GSU VGS undervoltage

DSO VDS overvoltage

xxx	Status
0	No fault detected
1	Fault detected

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Status Register Bit Mapping

Status Register Bit	Related Diagnostic Register Bits
FF	None
POR	None
SE	None
EE	None
OT	None
TW	None
VS	VSU, VSO
VLO	None
ETO	None
VR	VRU, VRO, VBR
VLU	None
VLO	None
LDF	OC1, OC2, OC3, OL
BSU	VA, VB, VC
GSU	AHU, ALU, BHU, BLU, CHU, CLU
DSO	AHO, ALO, BHO, BLO, CHO, CLO

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

INPUT/OUTPUT STRUCTURES

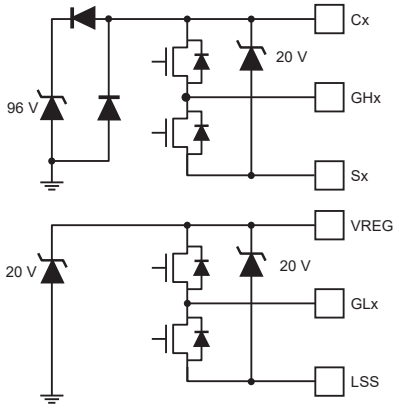


Figure 12a: Gate Drive Outputs

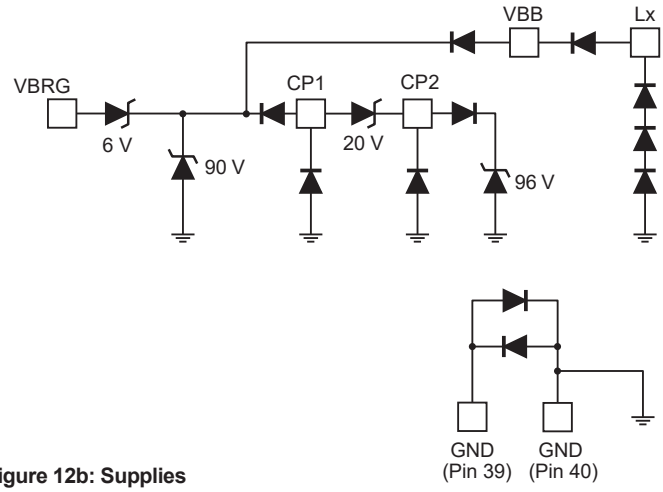


Figure 12b: Supplies

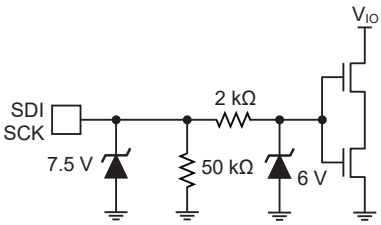


Figure 12c: SDI, SCK Inputs

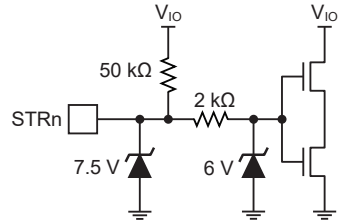


Figure 12d: STRn Input

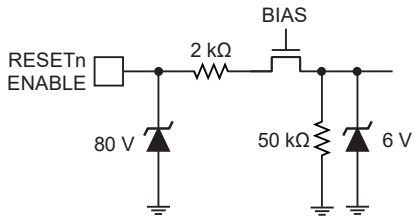


Figure 12e: ENABLE, RESETn Inputs

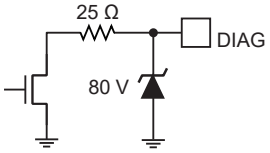


Figure 12f: DIAG Output

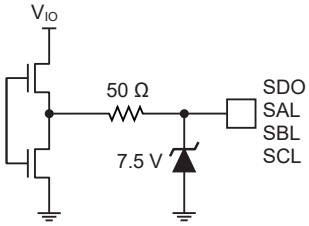


Figure 12g: SDO, SxL Outputs

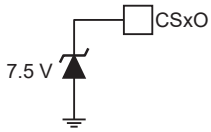


Figure 12h: CSxO Output

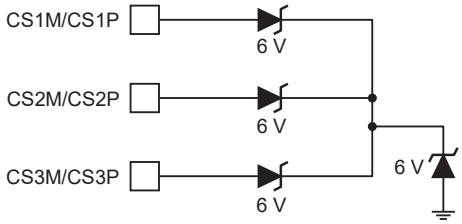


Figure 12i: CSxM, CSxP Inputs

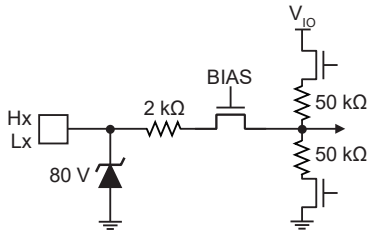
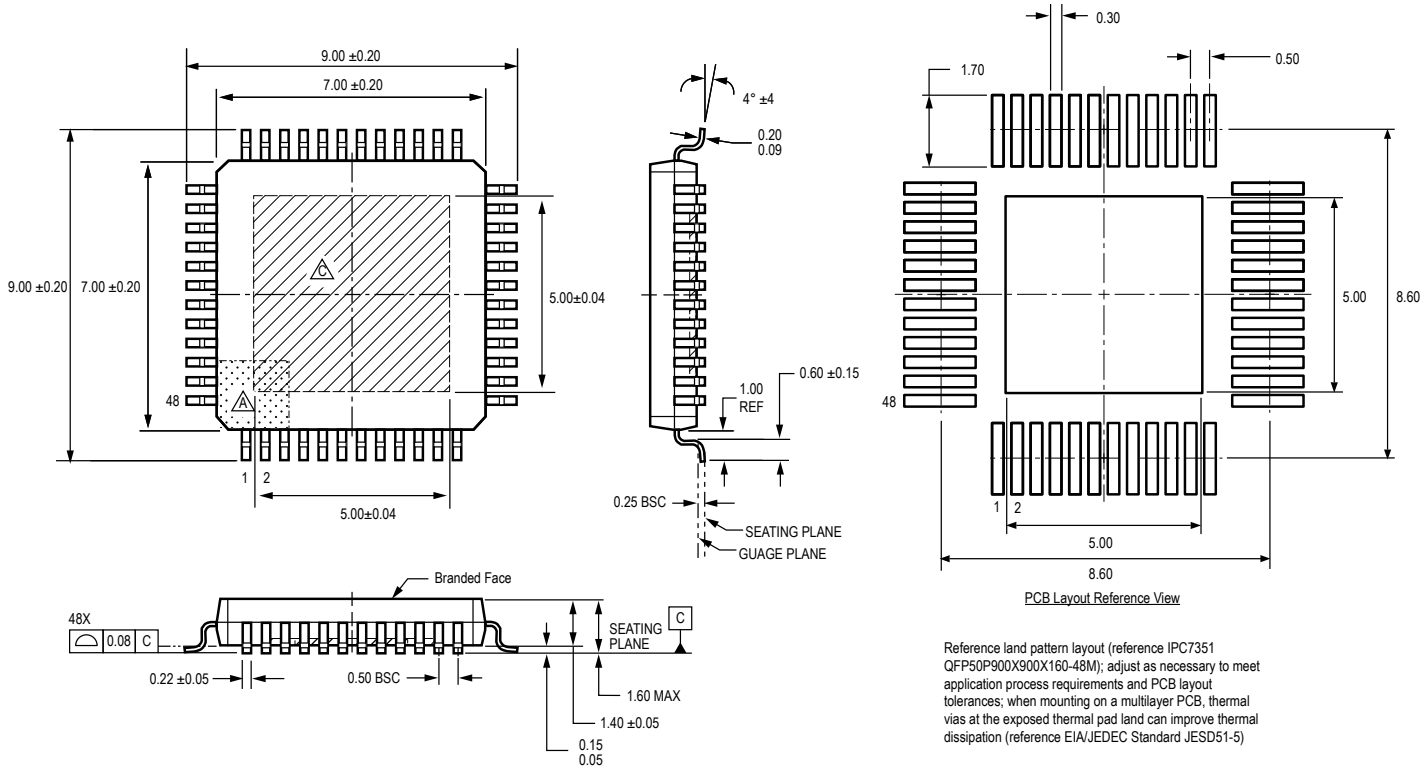


Figure 12j: Hx, Lx Inputs

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

For Reference Only; not for tooling use (reference MS-026 BBCHD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Branding scale and appearance at supplier discretion
C Exposed thermal pad (bottom surface) ; exact dimensions may vary with device

Figure 13: JP Package, 48-Pin LQFP with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	March 24, 2020	Initial release
1	May 8, 2020	Updated GHx and GLx Active Pull-Down test conditions and maximum values (page 8), Off-State Test Sink and Source Current test conditions (page 12), External Regulated Supply Mode section (page 19), Gate Drive Control section (page 23), Register 7 (page 46), and Register 6 (page 53). Removed I_{REGS} characteristic (page 6).
2	July 9, 2020	Updated Bootstrap Boost Voltage values (page 6), Pull-Up On-Resistance max values (page 7); removed Input Common Mode Range (page 10); updated VDS Threshold High-Side and Low-Side values (page 11); added footnote 9 to Temperature Warning Threshold, Temperature Warning Hysteresis, Overtemperature Threshold, and Overtemperature Hysteresis (page 12); updated Logic Outputs section (page 24), Monitor: VCC Undervoltage section (page 28), and Bridge: Phase Disconnected section (page 38).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com