

MOSFET - Power, Single N-Channel, STD Gate, SO8-FL

40 V, 0.42 mΩ, 509 A

NVMFWS0D4N04XM

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5x6 mm) with Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	509
		$T_C = 100^\circ\text{C}$	360
Power Dissipation	P_D	197	W
Pulsed Drain Current	I_{DM}	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	900
Pulsed Source Current (Body Diode)			I_{SM}
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	311	A
Single Pulse Avalanche Energy	$I_{PK} = 38.6 \text{ A}$	E_{AS}	2396 mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

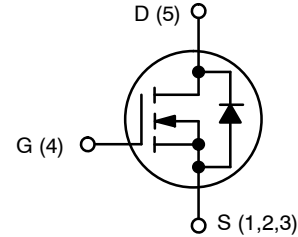
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

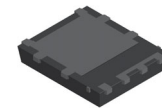
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.76	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	38.2	

1. Surface-mounted on FR4 board using 650 mm², 2 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	0.42 mΩ @ 10 V	509 A

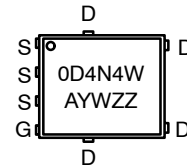


N-CHANNEL MOSFET



DFNW5 (SO-8FL WF)
CASE 507BD

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA, T _J = 25°C	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV _{(BR)DSS} /ΔT _J	I _D = 250 μA, Referenced to 25°C		14.9		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, T _J = 25°C			1	μA
		V _{DS} = 40 V, T _J = 125°C			80	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 50 A, T _J = 25°C		0.33	0.42	mΩ
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 330 μA, T _J = 25°C	2.5	3	3.5	V
Gate Threshold Voltage Temperature Coefficient	ΔV _{GS(TH)} /ΔT _J	V _{GS} = V _{DS} , I _D = 330 μA		-7.21		mV/°C
Forward Trans-conductance	g _{FS}	V _{DS} = 5 V, I _D = 50 A		286		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		8530		pF
Output Capacitance	C _{OSS}			5451		
Reverse Transfer Capacitance	C _{RSS}			72		
Total Gate Charge	Q _{G(TOT)}	V _{DD} = 32 V, I _D = 50 A, V _{GS} = 10 V		132		nC
Threshold Gate Charge	Q _{G(TH)}			24.9		
Gate-to-Source Charge	Q _{GS}			37.2		
Gate-to-Drain Charge	Q _{GD}			23.7		
Gate Resistance	R _G	f = 1 MHz		0.42		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(ON)}	Resistive Load, V _{GS} = 0/10 V, V _{DD} = 32 V, I _D = 50 A, R _G = 0 Ω		9.98		ns
Rise Time	t _r			5.49		
Turn-Off Delay Time	t _{d(OFF)}			15.5		
Fall Time	t _f			8.41		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	I _S = 50 A, V _{GS} = 0 V, T _J = 25°C		0.79	1.2	V
		I _S = 50 A, V _{GS} = 0 V, T _J = 125°C		0.63		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _S = 50 A, di/dt = 100 A/μs, V _{DD} = 32 V		148		ns
Charge Time	t _a			47.3		
Discharge Time	t _b			101		
Reverse Recovery Charge	Q _{RR}			337		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFWS0D4N04XMT1G	0D4N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

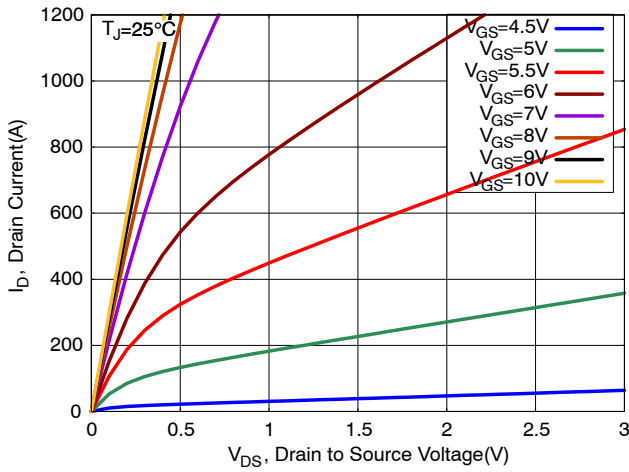


Figure 1. On-Region Characteristics

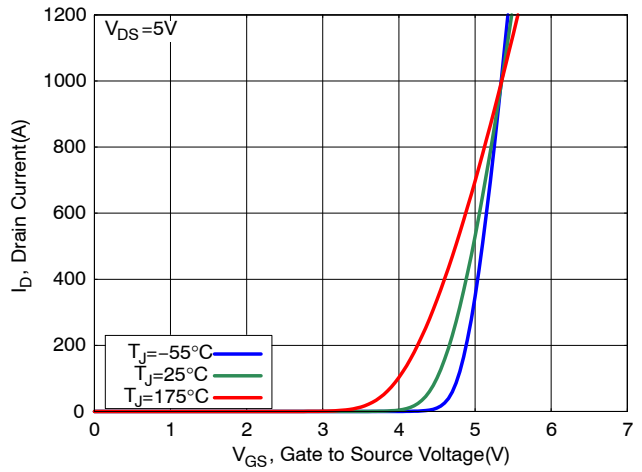


Figure 2. Transfer Characteristics

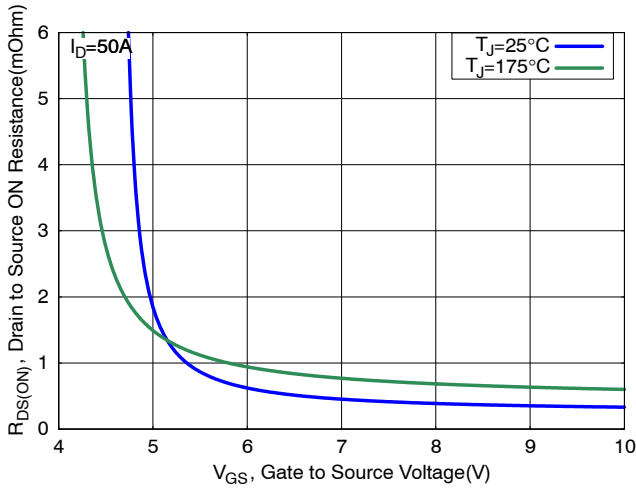


Figure 3. On-Resistance vs. Gate Voltage

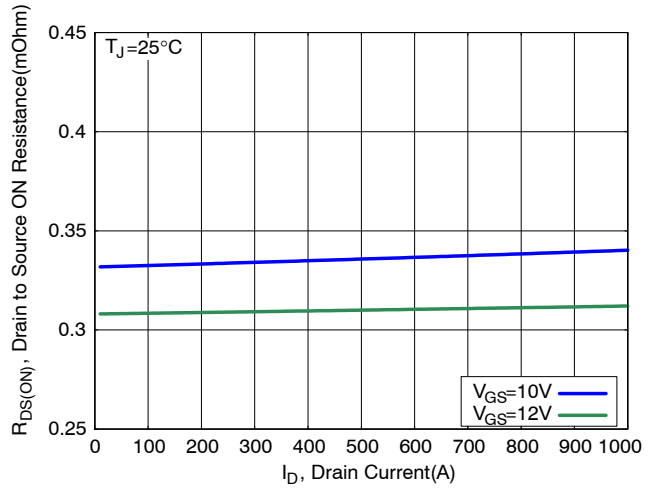


Figure 4. On-Resistance vs. Drain Current

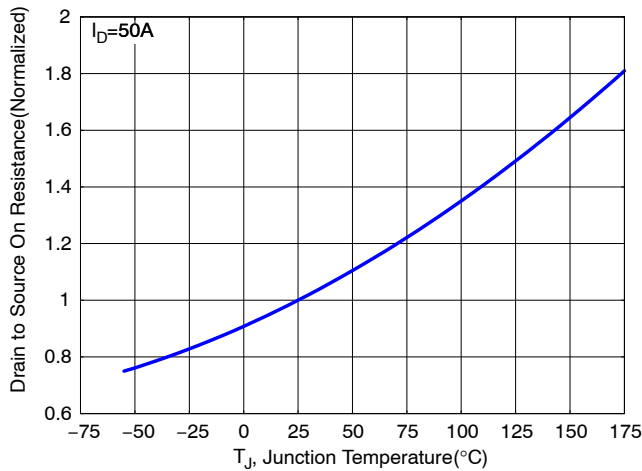


Figure 5. Normalized ON Resistance vs. Junction Temperature

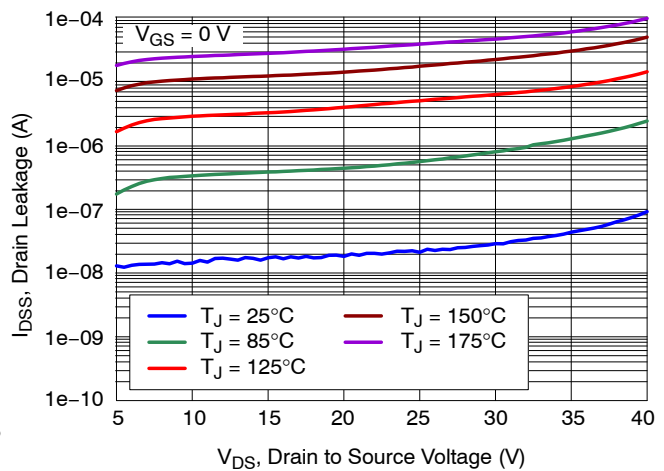


Figure 6. Drain to Source Voltage vs. Drain Leakage

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TYPICAL CHARACTERISTICS (Continued)

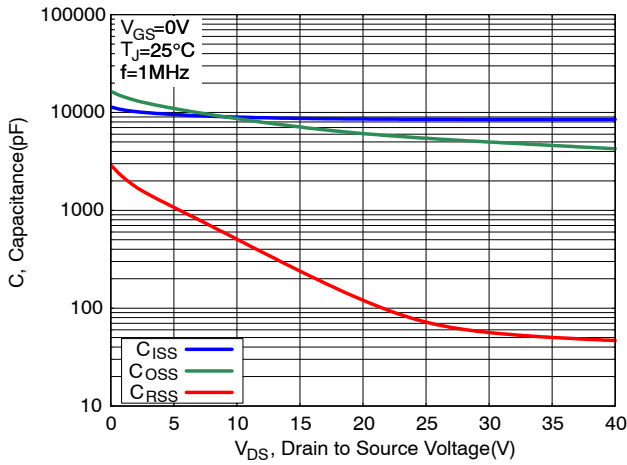


Figure 7. Capacitance Characteristics

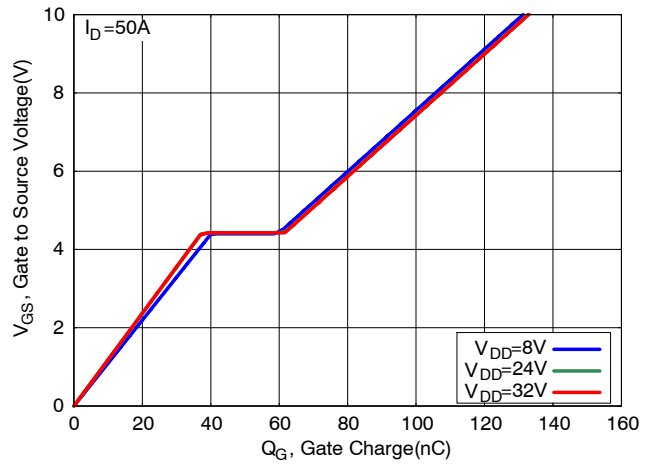


Figure 8. Gate Charge Characteristics

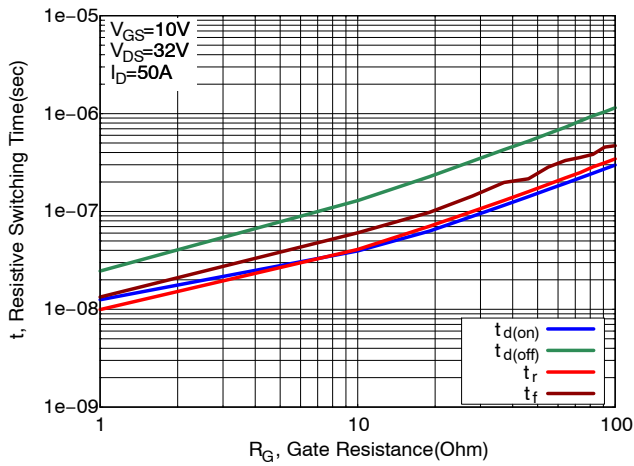


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

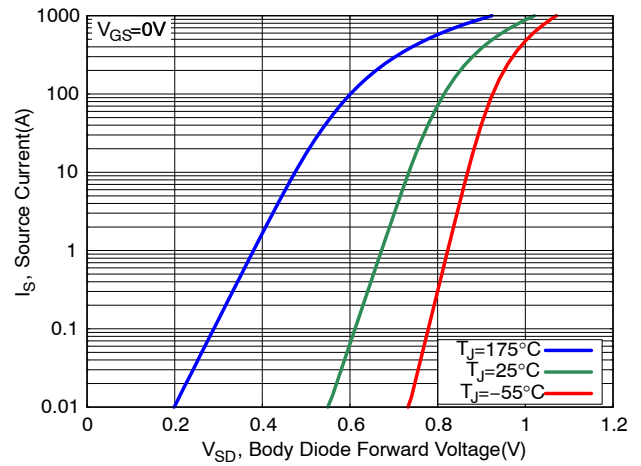


Figure 10. Diode Forward Characteristics

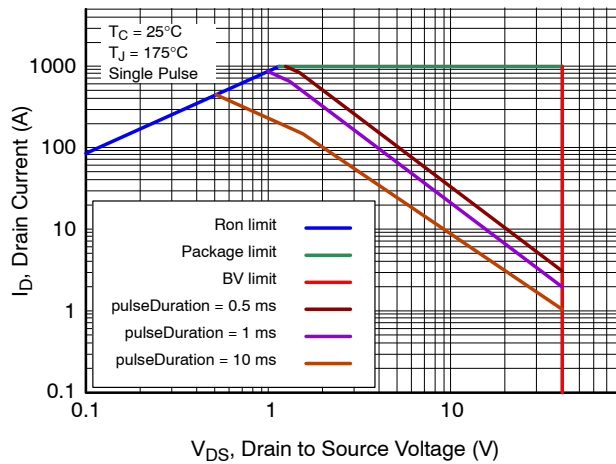


Figure 11. Safe Operating Area (SOA)

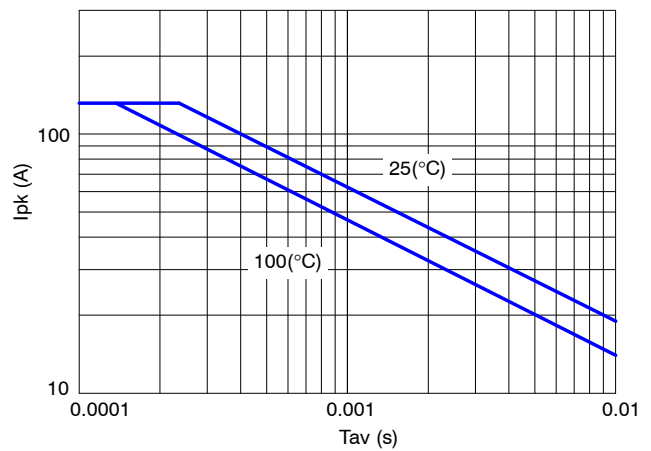


Figure 12. Avalanche Current vs. Pulse Time (UIS)

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TYPICAL CHARACTERISTICS (Continued)

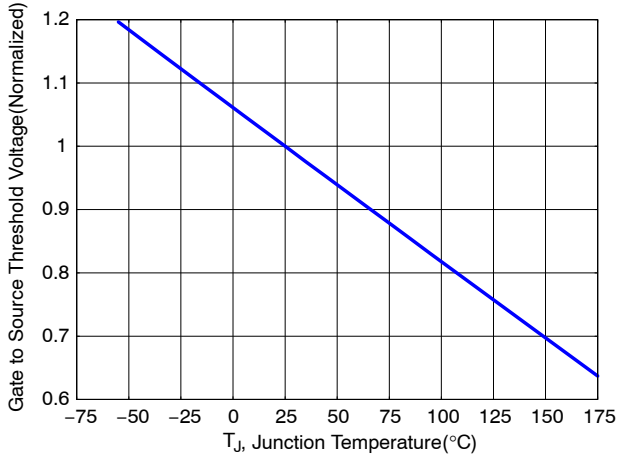


Figure 13. Gate Threshold Voltage vs. Junction Temperature

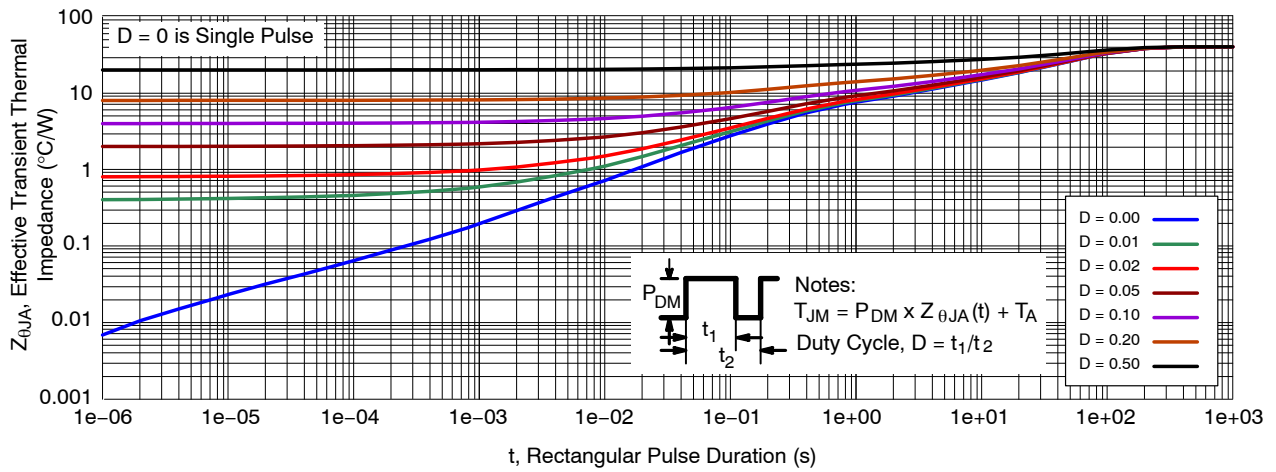
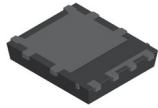


Figure 14. Thermal Response

MECHANICAL CASE OUTLINE

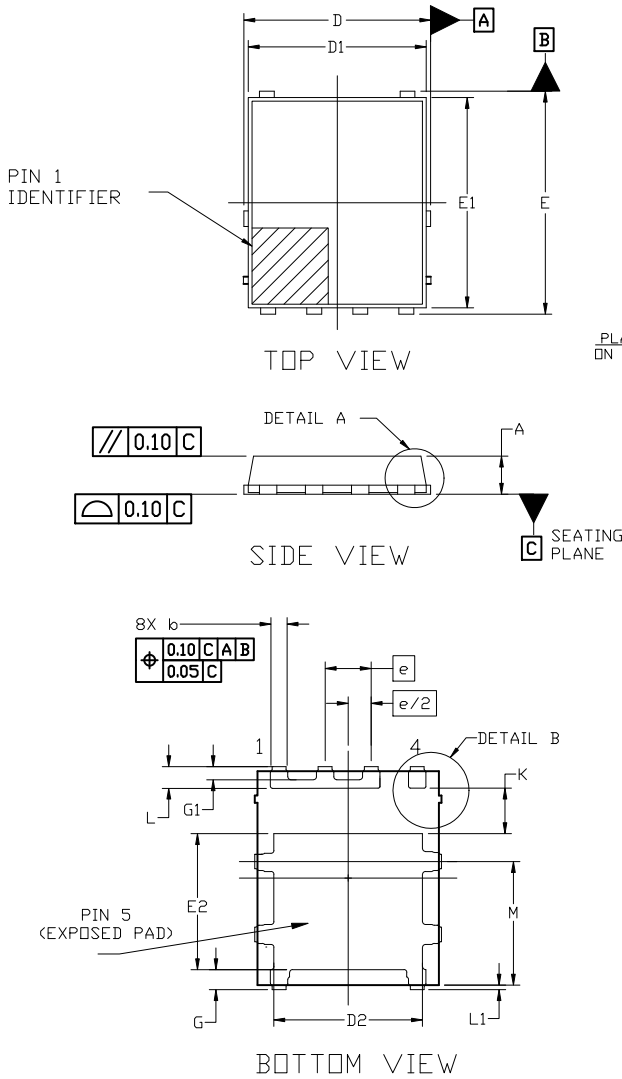
PACKAGE DIMENSIONS

ON Semiconductor®



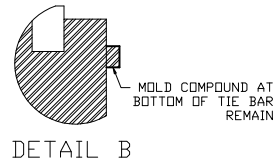
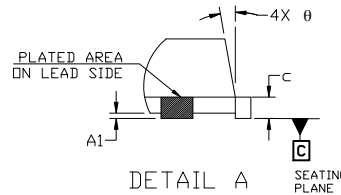
DFNW5 5x6, FULL-CUT SO8FL WF CASE 507BD ISSUE O

DATE 13 APR 2021

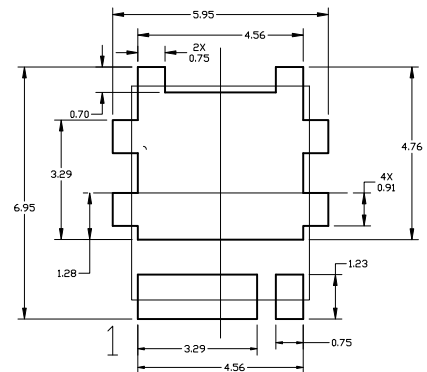


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



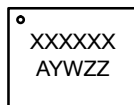
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.80	5.00	5.20
D2	3.90	4.10	4.30
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.55	3.75	3.95
e	1.27 BSC		
G	0.50	0.55	0.70
G1	0.26	0.36	0.46
k	1.10	1.25	1.40
L	0.50	0.60	0.70
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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