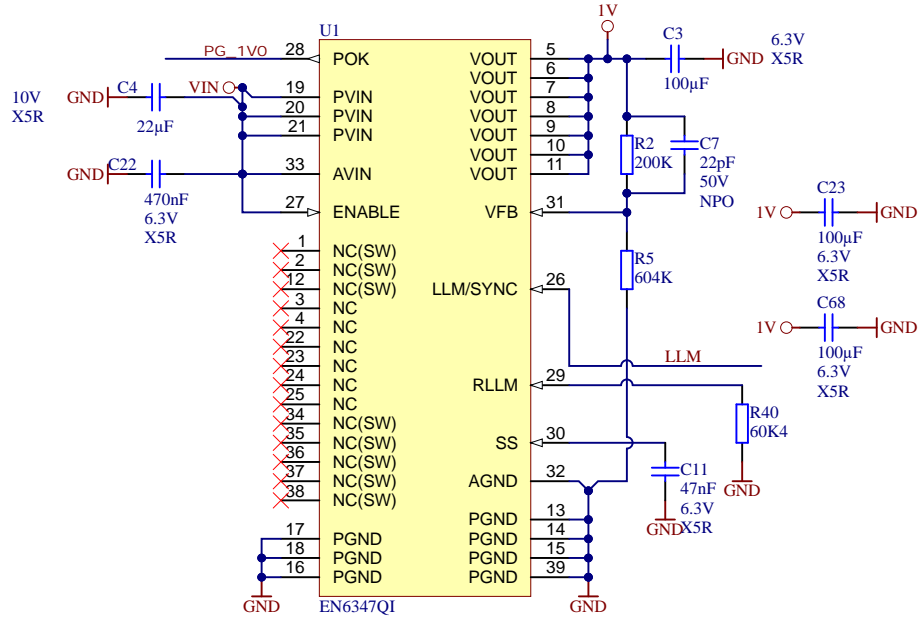
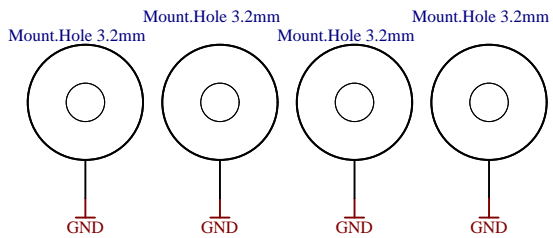
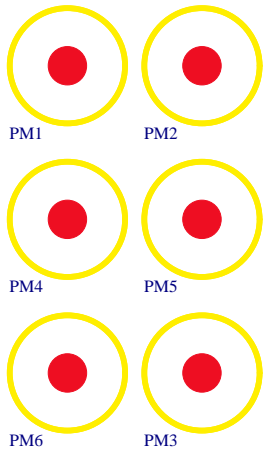
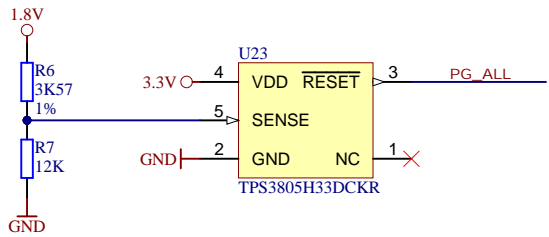
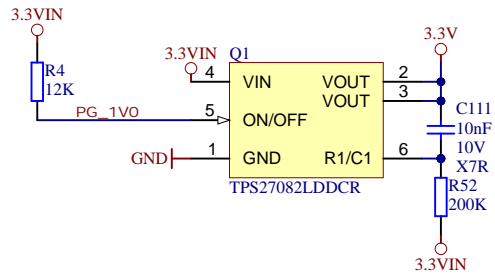
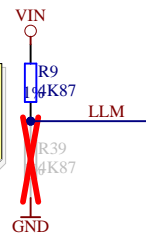


- U_B2B_Connector
B2B_Connector.SchDoc
- U_B14_B16
B14_B16.SchDoc
- U_B15
B15.SchDoc
- U_B34
B34.SchDoc
- U_B35-RAM
B35-RAM.SchDoc
- U_DDR3-MEM
DDR3-MEM.SchDoc
- U_ETHERNET
ETHERNET.SchDoc
- U_FPGA_CFG
FPGA_CFG.SchDoc
- U_FPGA_PWR_MISC
FPGA_PWR_MISC.SchDoc

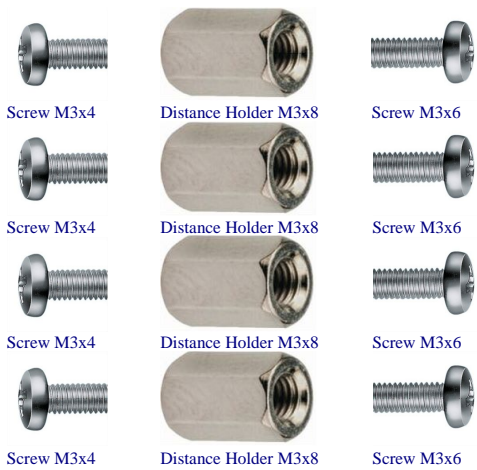
- U_PLL
PLL.SchDoc
- U_POWER
POWER.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT

Select which resistor to mount with assembly variant!
Pullup switch DCDC to light load mode



Top of Board



Assembly variant	100-2IF
Created by	TT
Modified by	VY
Modified at	2019-07-25
SVN Revision	8563

Title: TE0710	
A4	Number: TE0710 100-2IF
Date: 2014-03-07	Copyright: Trenz Electronic GmbH / TT
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Dual 10/100 Ethernet Interface
 4 system controller IO Pins; 3.3V VCCIO
 B14 8 Pins Single ended IO; 3.3V Fixed VCCIO; replacing MIO0 pins on TE0720
 B16 6 Pins; 3 Differential; 3.3V Fixed VCCIO; TE0720 SD Card compatible
 B15: 48 Pins; 24 Differential; variable VCCIO

Total maximum I/O: 112
 JM2 total I/O: 50
 JM1 total I/O: 62

B34: 50 Pins; 24 Differential; variable VCCIO
 JTAG or IO (4 pins); 3.3V Levels

A

B

C

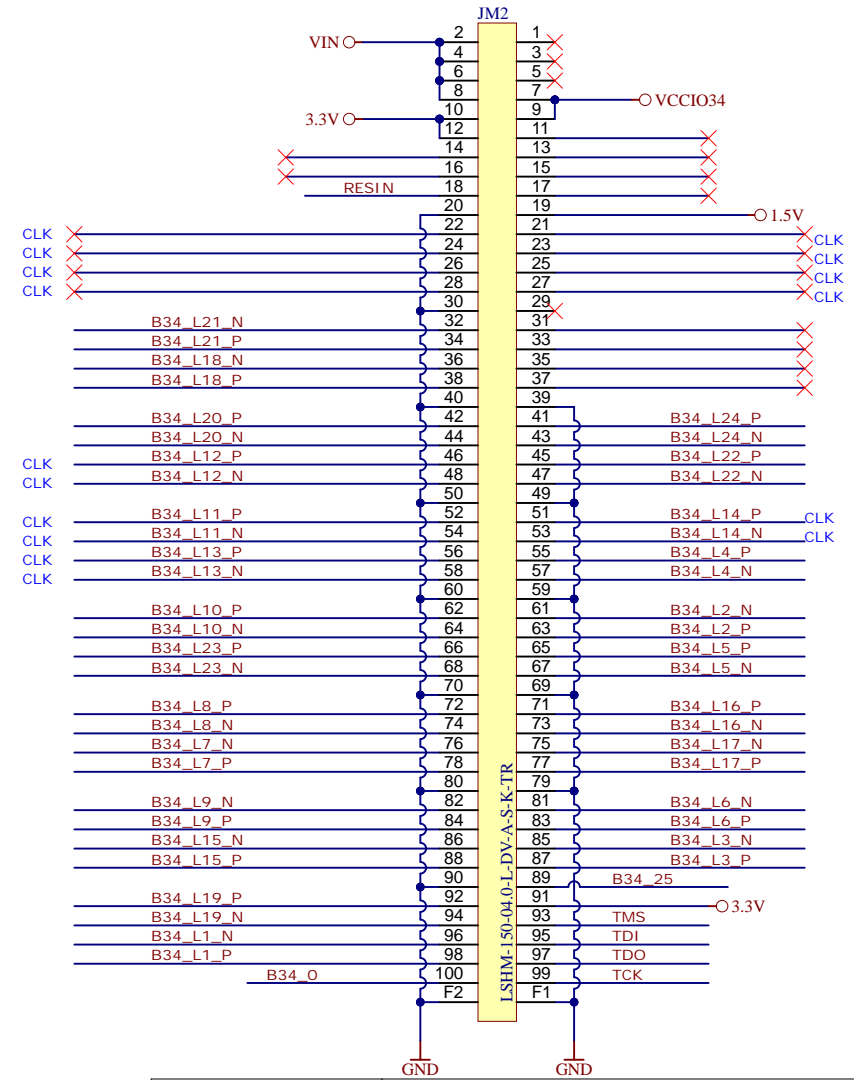
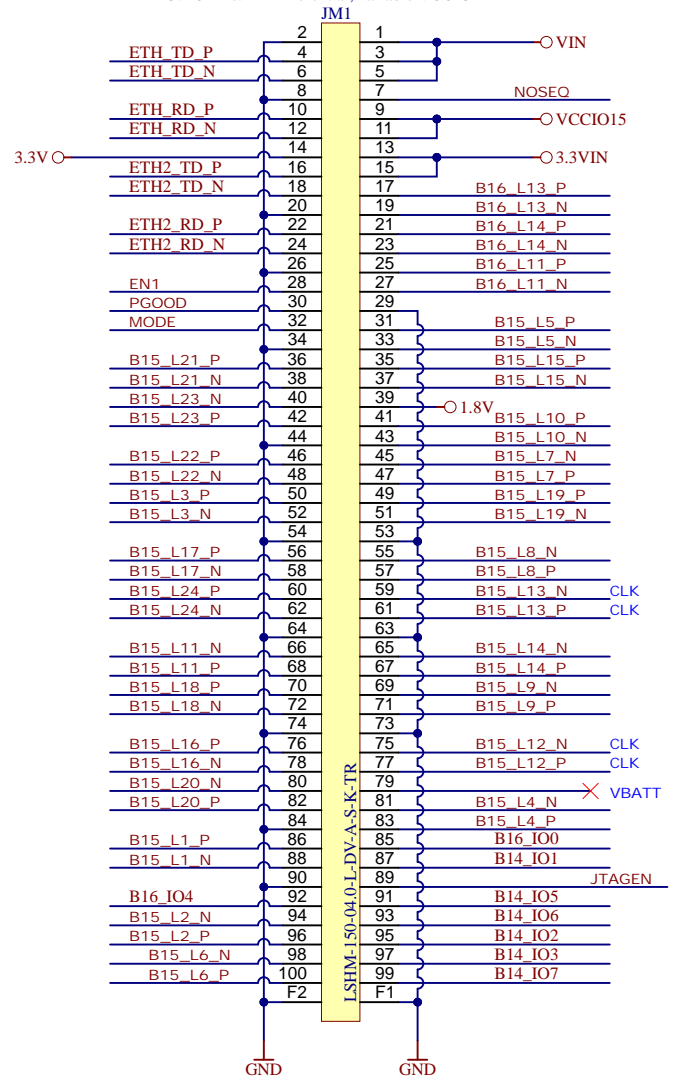
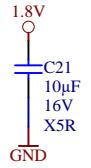
D

A

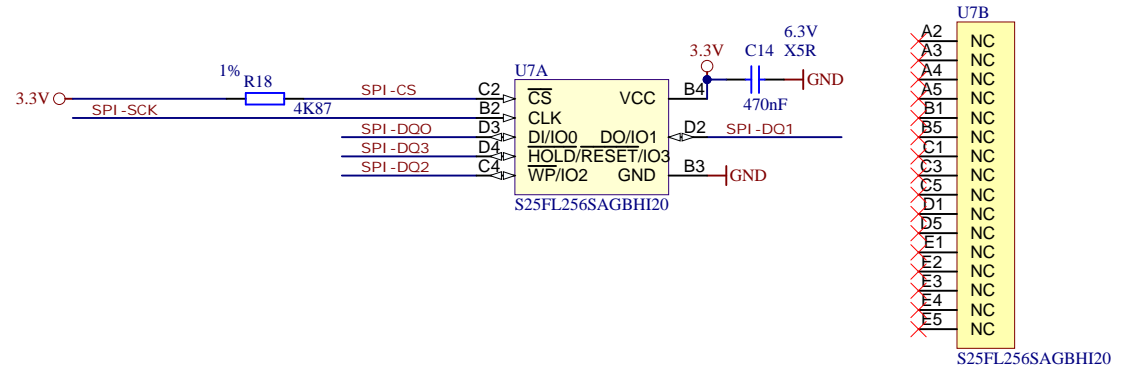
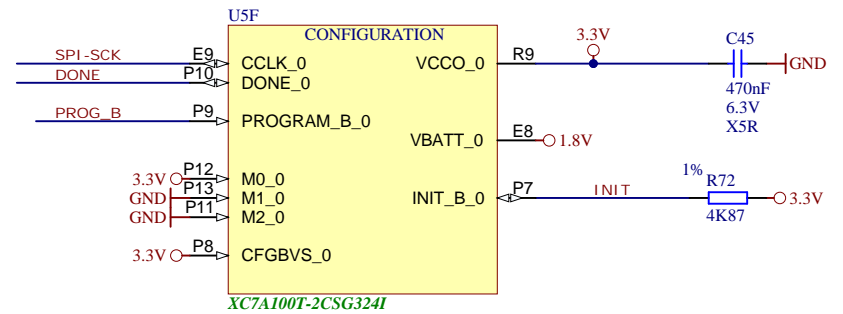
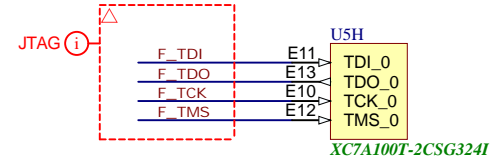
B

C

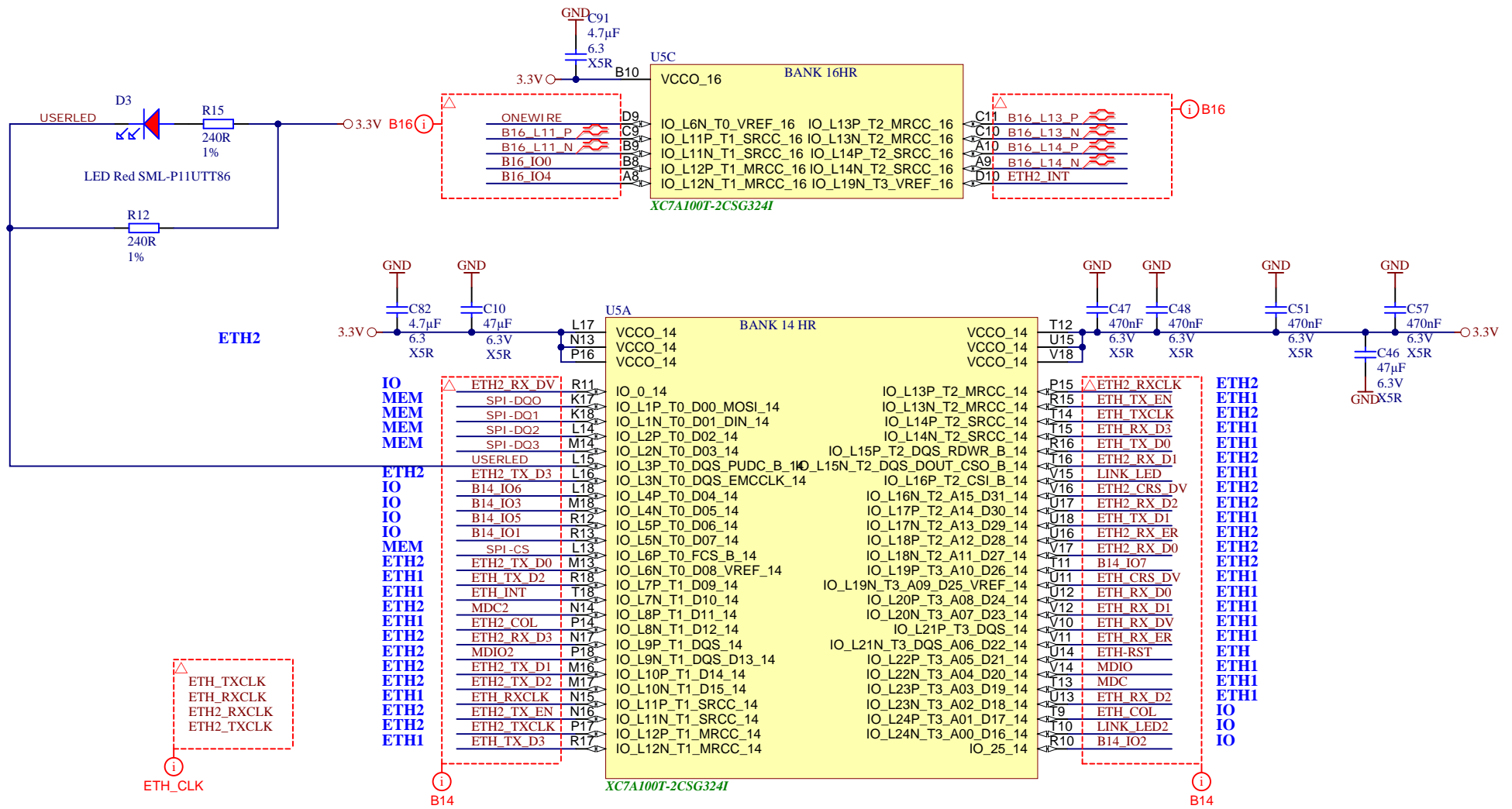
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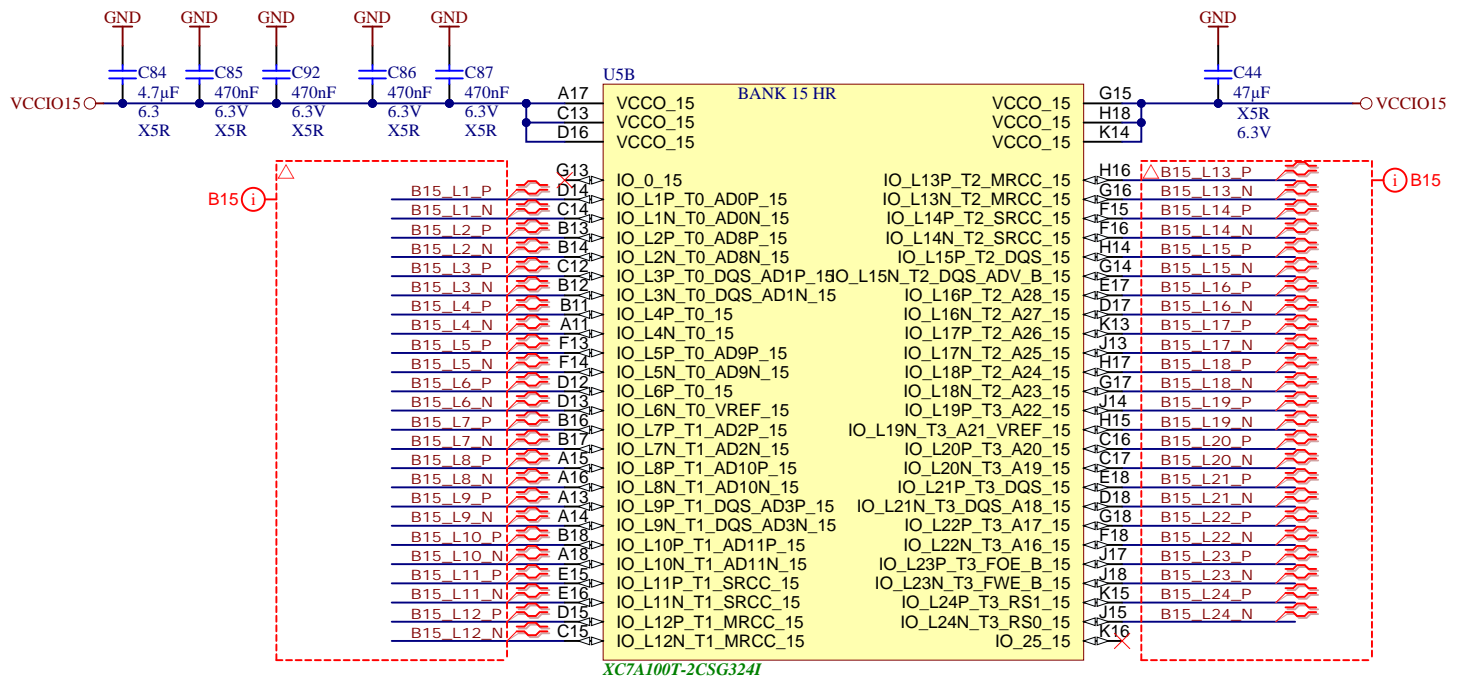
Title: TE0710		
A4	Number: TE0710 100-2IF	Rev. 02
Date: 22.10.2013	Copyright: Trenz Electronic GmbH / TT	Page2 of 13
Filename: B2B_Connector.SchDoc		



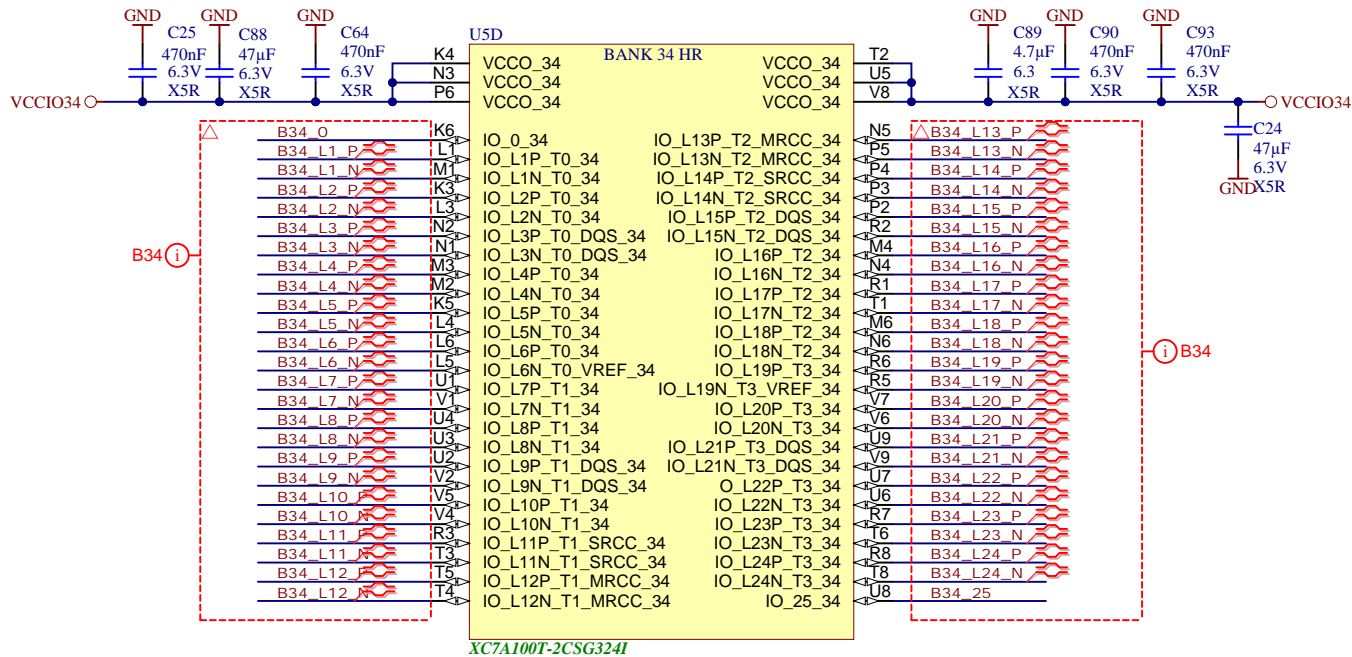
		Title: TE0710	
		A4	Number: TE0710 100-2IF
Date: 2014-03-07		Copyright: Trenz Electronic GmbH / TT	
Date: 2014-03-07		Page 3 of 13	
Filename: FPGA_CFG.SchDoc			



Title: TE0710		
A4	Number: TE0710 100-2IF	Rev. 02
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Filename: B14_B16.SchDoc		



Title: TE0710		
A4	Number: TE0710 100-2IF	Rev. 02
Date: 2014-03-07	Copyright: Trenz Electronic GmbH / TT	Page5 of 13
Filename: B15.SchDoc		



XC7A100T-2CSG324I



Title: TE0710		
A4	Number: TE0710 100-2IF	Rev. 02
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Filename: B34.SchDoc		

A

A

B

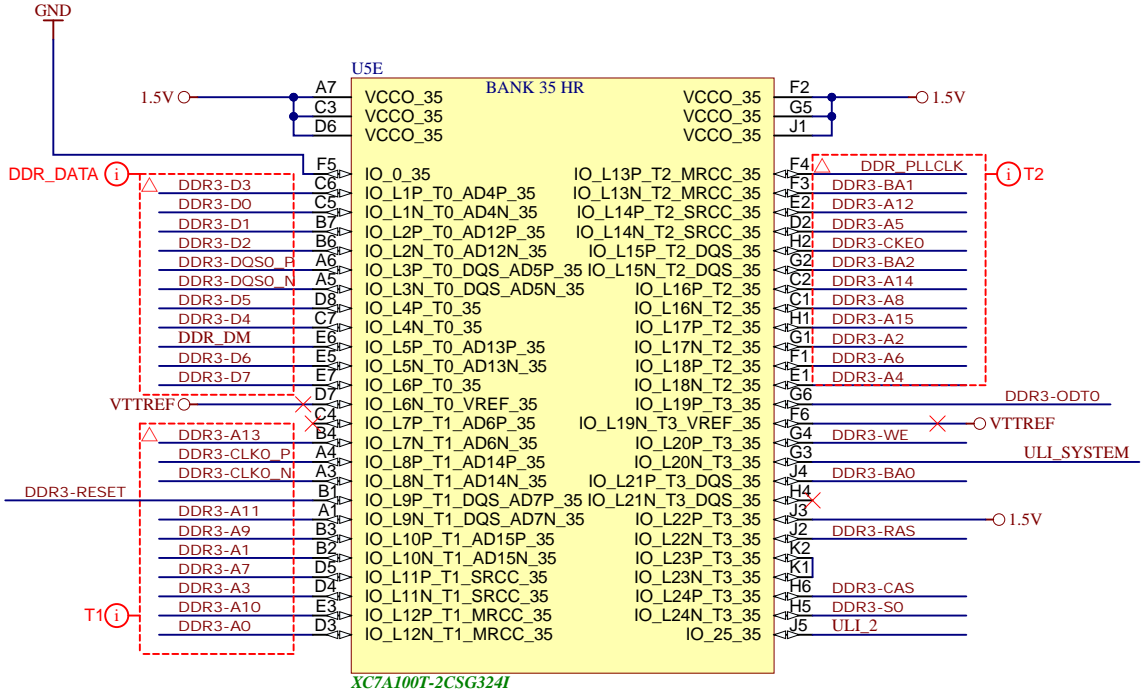
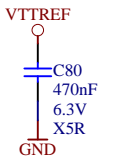
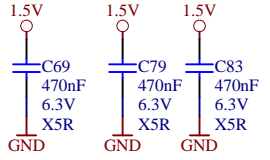
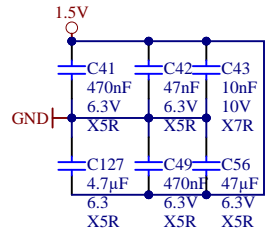
B

C

C

D

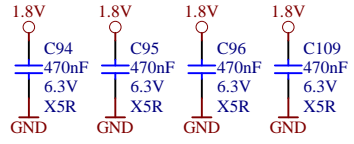
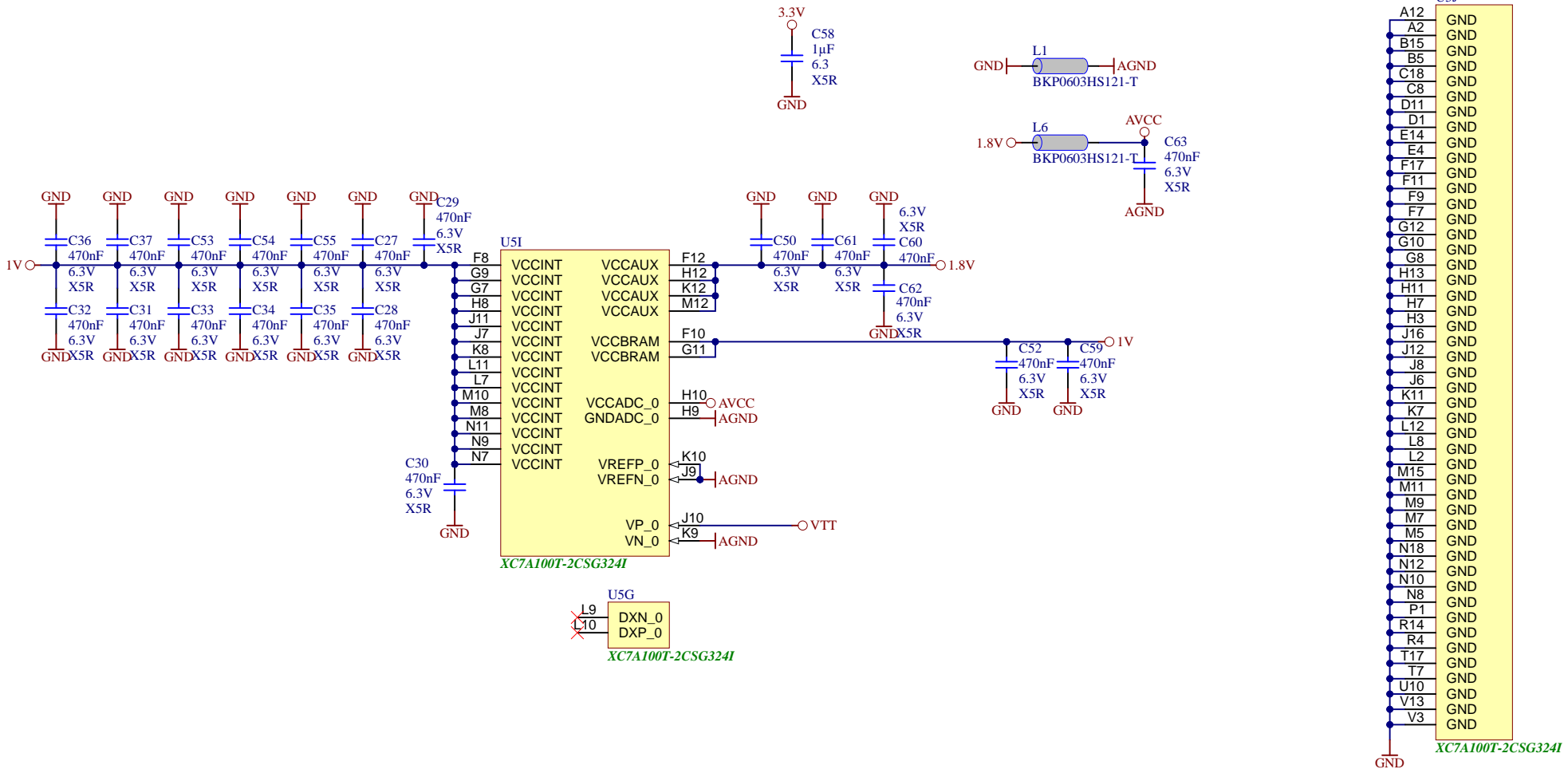
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XC7A100T-2CSG324I



Title: TE0710		
A4	Number: TE0710 100-2IF	Rev. 02
Date: 2014-03-07	Copyright: Trenz Electronic GmbH / TT	Page 7 of 13
Filename: B35-RAM.SchDoc		



Title: TE0710		
A4	Number: TE0710 100-2IF	Rev. 02
Date: 2014-03-07	Copyright: Trenz Electronic GmbH / TT	Page 8 of 13
Filename: FPGA_PWR_MISC.SchDoc		

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3

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1

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A

A

B

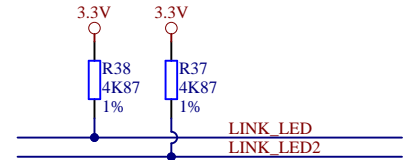
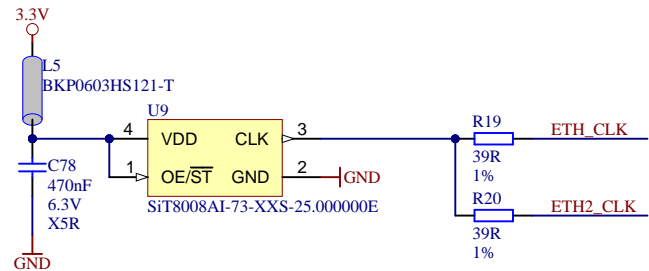
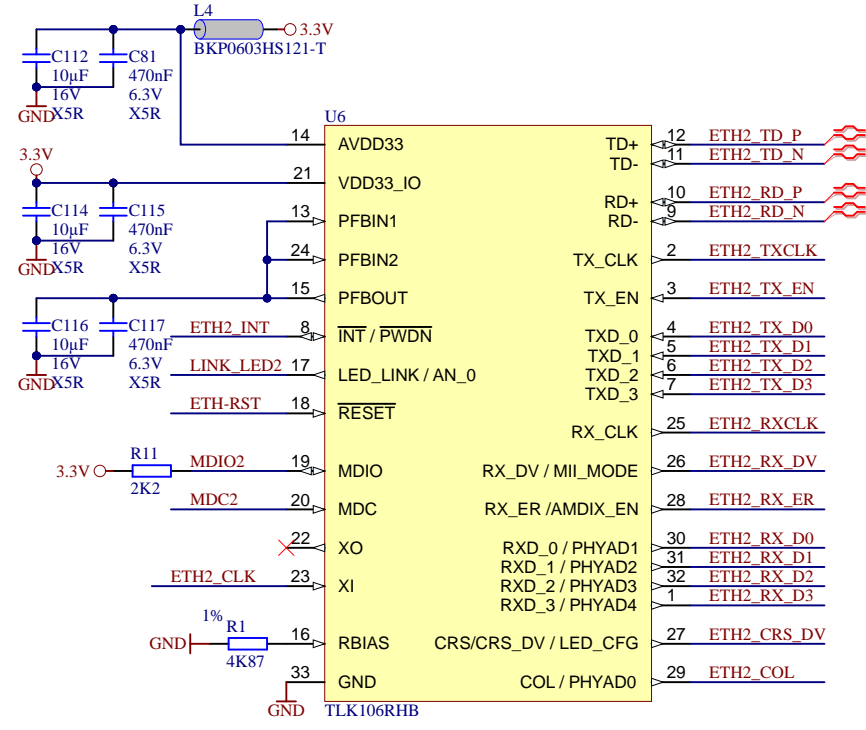
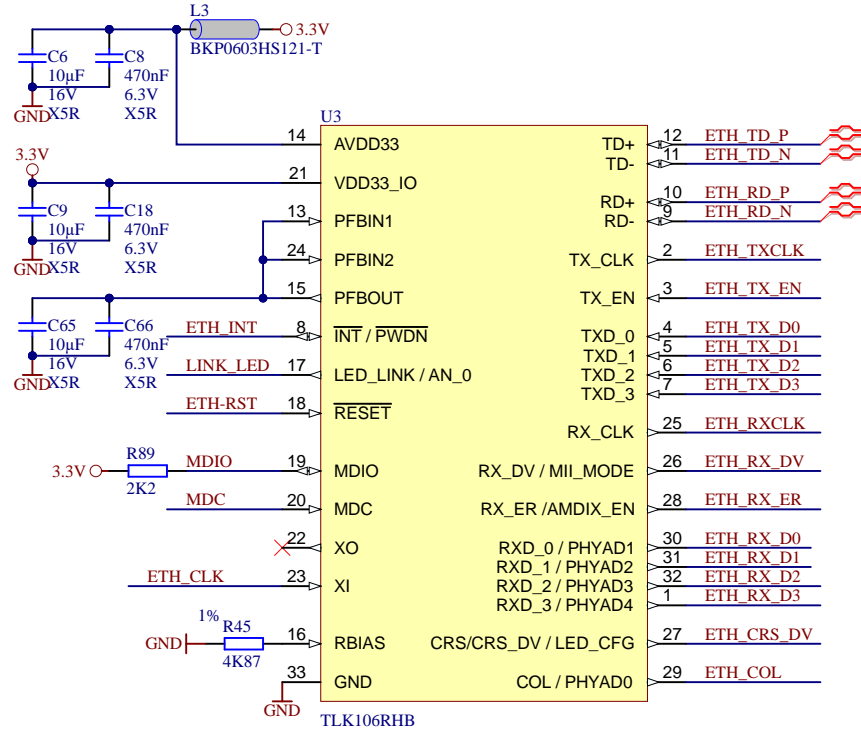
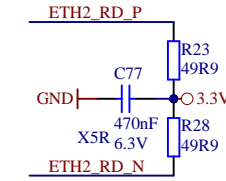
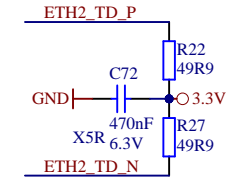
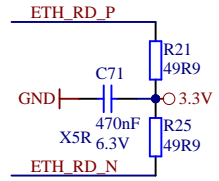
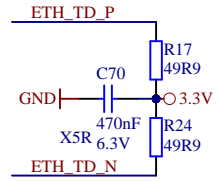
B

C

C

D

D



Title: TE0710		
A4	Number: TE0710 100-21F	Rev. 02
Date: 22.10.2013	Copyright: Trenz Electronic GmbH / TT	Page9 of 13
Filename: ETHERNET.SchDoc		

1

2

3

4

A

A

B

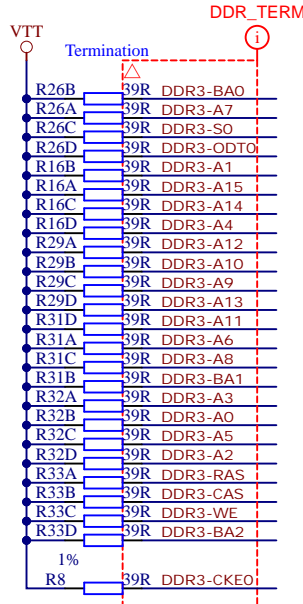
B

C

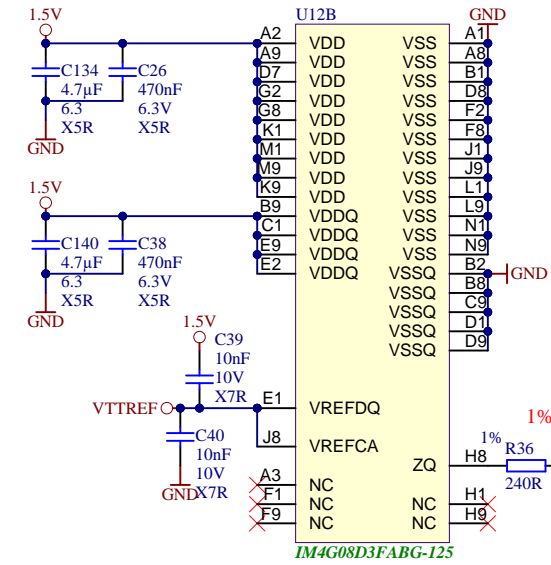
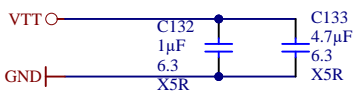
C

D

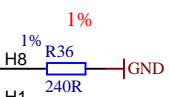
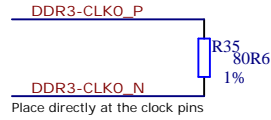
D



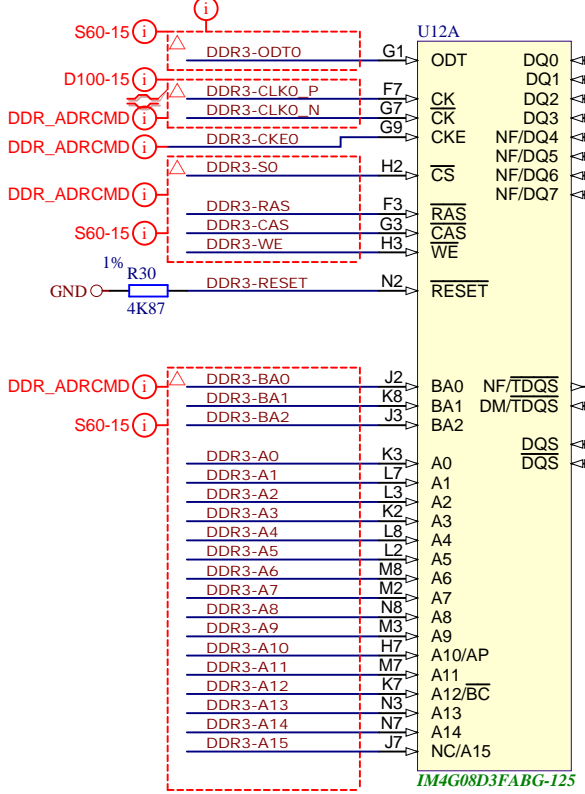
Resistors can be swap to better routing



IM4G08D3FABG-125

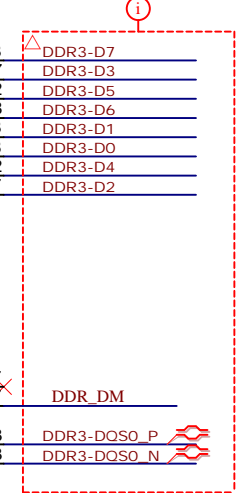


DDR3-ADRCMD

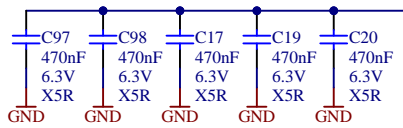
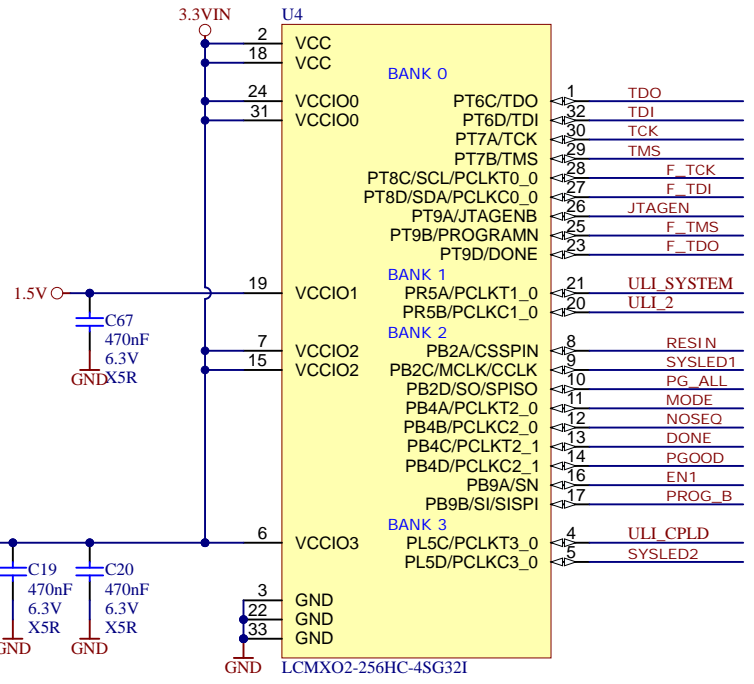
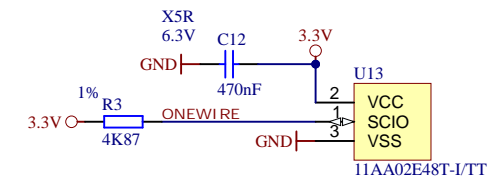
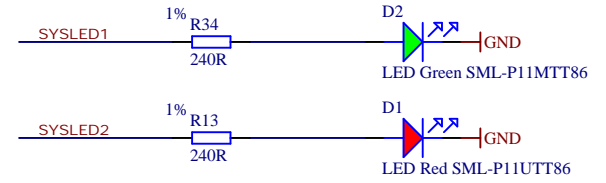
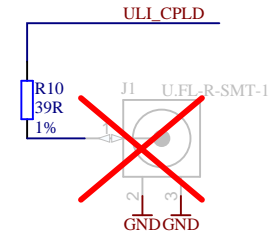
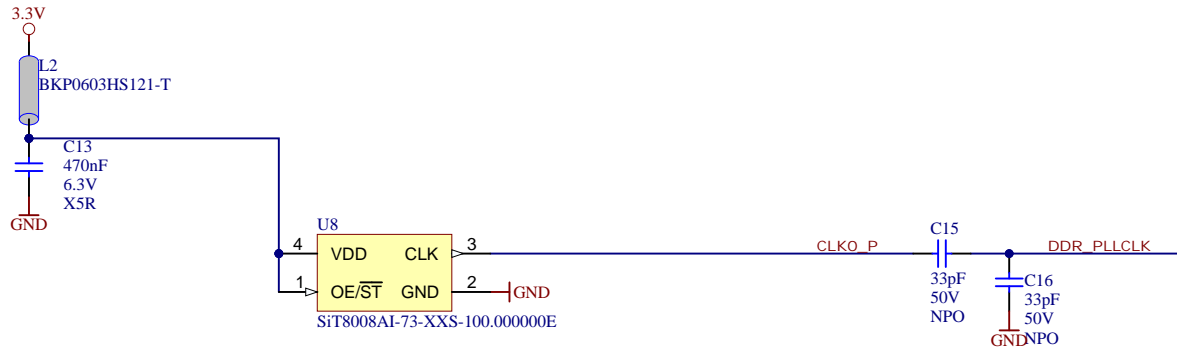


IM4G08D3FABG-125

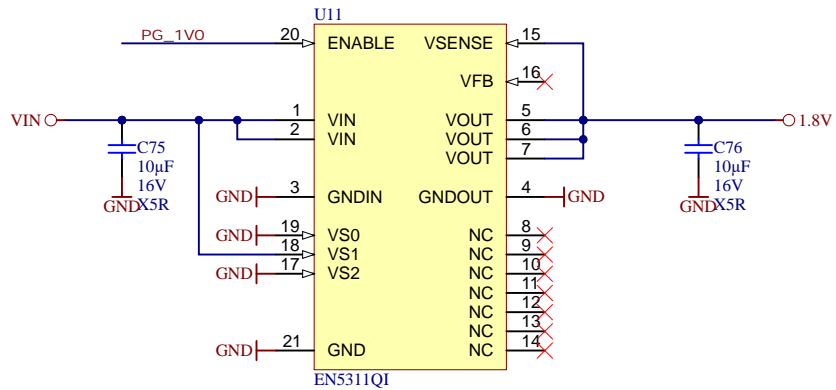
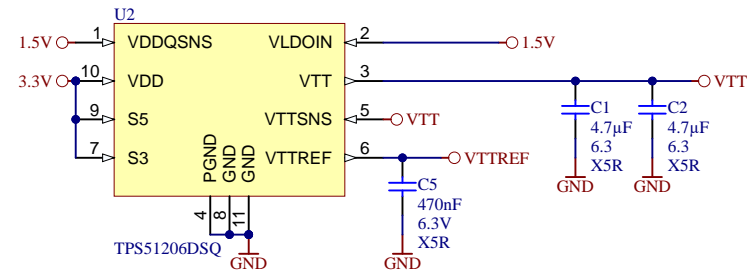
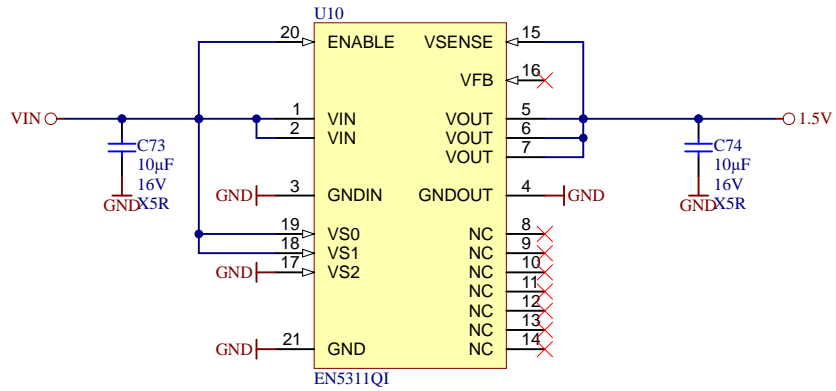
D100-15




Title: TE0710		
A4	Number: TE0710 100-2IF	Rev. 02
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Filename: DDR3-MEM.SchDoc		



	Title: TE0710		
	A4	Number: TE0710 100-2IF	Rev. 02
	Date: 2014-03-07	Copyright: Trenz Electronic GmbH	Page 11 of 13
	Filename: PLL.SchDoc		



	Title: TE0710		
	A4	Number: TE0710 100-2IF	Rev. 02
	Date: 2014-03-07	Copyright: Trenz Electronic GmbH	Page 12 of 13
	Filename: POWER.SchDoc		

Revision changes REV02.a (15.03.19):

- 1) Schematic: nets B14_IO0 and B14_IO4 renamed to B16_IO0 and B16_IO4 accordingly
- 2) Schematic: changed value of R12 and R15 to 240R

Revision changes REV02.b (19.07.19):

- 3) VY: Replaced capacitors C39, C40, C43, C111 from 10nF 6.3V X5R to 10nF 10V X7R

A

A

B


B

C

C

D

D

	Title: TEC0049		
	A4	Number: TE0710 100-2IF	Rev. 02
	Date: 2017-10-09	Copyright: Trenz Electronic GmbH / TT	Page 13 of 13
	Filename: RevisionChanges.SchDoc		