500 V, 1 A to 3 A
High Voltage 3-phase Motor Drivers

SLA68xxMH Series

Data Sheet

Description

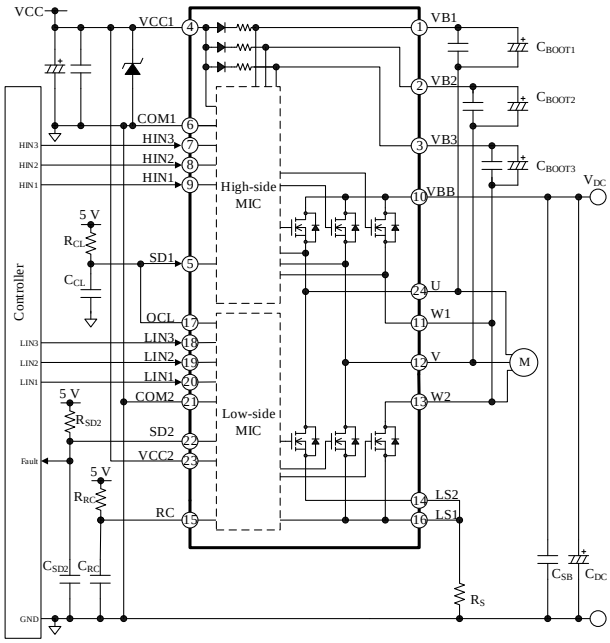
The SLA68xxMH series are high voltage 3-phase motor drivers in which transistors, pre-drive circuits, and bootstrap circuits (diodes and resistors) are highly integrated.

Selectable ZIP24 packages (heatsink type) with various leadforms enable excellent mountability to a wide range of applications. These products can optimally control the inverter systems of low- to medium-capacity motors.

Features

- Built-in Bootstrap Diodes with Current Limiting Resistors (210 Ω)
- CMOS-compatible Input (5 V)
- Shutdown Function
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Protections Include:
  - Undervoltage Lockout for Power Supply
    - VBx Pin (UVLO_VB): Auto-restart
    - VCC1 Pin (UVLO_VCC1): Auto-restart
    - VCC2 Pin (UVLO_VCC2): Auto-restart
  - Overcurrent Limit (OCL)
  - Overcurrent Protection (OCP):
    - Auto-restart with Adjustable OCP Hold Time
  - Thermal Shutdown (TSD): Auto-restart

Typical Application



Packages

ZIP24 (Heatsink type)

Leadform 2175

Leadform 2171

Not to scale

Selection Guide

V_{DSS}	I_O	Part Number
500 V	2.5 A	SLA6868MH
	3.0 A	SLA6870MH

Applications

For motor drives such as:

- Fan Motor and Pump Motor for Washer and Dryer
- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Power MOSFET Breakdown Voltage	V_{DSS}	VBB–LSx, V_{CC} = 15 V, I_D = 100 μA, V_{IN} = 0 V	500	V	
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	20	V	
	V_{BS}	VB1–U, VB2–V, VB3–W1	20		
Output Current (DC)(1)	I_O	T_C = 25 °C, T_J < 150 °C	2.5	A	SLA6868MH
			3.0		SLA6870MH
Output Current (Pulse)	I_{OP}	T_C = 25 °C, T_J < 150 °C, P_W ≤ 100 μs, duty cycle = 1%	3.75	A	SLA6868MH
			4.5		SLA6870MH
Input Voltage	V_{IN}	HIN1–COM, HIN2–COM, HIN3–COM; LIN1–COM, LIN2–COM, LIN3–COM	− 0.5 to 7	V	
SD Pin Voltage	V_{SD}	SD1–COM, SD2–COM	−0.5 to 7	V	
Allowable Power Dissipation	P_D	T_C = 25 °C	32.8	W	SLA6868MH/70MH
Operating Case Temperature (2)	$T_{C(OP)}$		−30 to 100	°C	
Junction Temperature (3)	T_J		150	°C	
Storage Temperature	T_{STG}		−40 to 150	°C	

(1) Should be derated depending on an actual case temperature. See Section 14.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the control MICs and power MOSFETs.

2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBB–LS1, VBB–LS2	—	300	400	V	
Snubber Capacitor for Main Power Supply	C_{SB}		0.01	—	0.1	µF	
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	13.5	15.0	16.5	V	
	V_{BS}	VB1–U, VB2–V, VB3–W1	13.5	—	16.5	V	
Protective Zener Voltage	V_Z	VCC1–COM, VCC2–COM	18	—	20	V	
Input Voltage (HINx, LINx, SDx)	V_{IN}		0	—	5.5	V	
SDx Pin Pull-up Voltage	V_{SD}		3.0	—	5.5	V	
OCL Pin Pull-up Voltage	V_{CL}		3.0	—	5.5	V	
SDx Pin Pull-up Resistor	R_{SD}		3.3	—	10	kΩ	
OCL Pin Pull-up Resistor	R_{CL}		1	—	10	kΩ	
SDx Pin Capacitor	C_{SDx}		1	—	10	nF	
OCL Pin Capacitor	C_{CL}		1	—	10	nF	
RC Pin Capacitor	C_{RC}		1	—	4.7	nF	
RC Pin Pull-up Resistor	R_{RC}		33	—	680	kΩ	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$	T_J = −25 to 150 °C	0.5	—	—	µs	
	$t_{IN(MIN)OFF}$	T_J = −25 to 150 °C	0.5	—	—	µs	
Dead Time of Input Signal	t_{DEAD}		1.5	—	—	µs	
Switching Frequency	f_c		—	—	20	kHz	
Bootstrap Capacitor	C_{BOOT}		1	—	220	µF	
Shunt Resistor	R_S	$I_P \leq$ 3.75A	290	—	—	mΩ	SLA6868MH
		$I_P \leq$ 4.5 A	240	—	—		SLA6870MH
PWM Carrier Frequency	f_C		—	—	20	kHz	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCC1–COM, VCC2–COM	10.5	11.5	12.5	V	
	$V_{BS(ON)}$	VB1–U, VB2–V, VB3–W1	9.5	10.5	11.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC1–COM, VCC2–COM	10.0	11.0	12.0	V	
	$V_{BS(OFF)}$	VB1–U, VB2–V, VB3–W1	9.0	10.0	11.0	V	
Logic Supply Current	I_{CC}	I_{REG} = 0 A	—	2.7	5.0	mA	
	I_{BS}	VBx = 15 V, HINx = 5 V	—	135	380	µA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx, SDx)	V_{IH}		—	2.1	2.6	V	Output transistors ON
Low Level Input Threshold Voltage (HINx, LINx, SDx)	V_{IL}		0.8	1.3	—	V	Output transistors OFF
Input Threshold Voltage Hysteresis	V_{HYS}		—	0.8	—		
Input Voltage	I_{IH}	V_{IN} = 5 V	—	230	500	µA	
Protection							
SDx Pin, OCL Pin Low Level Output Voltage	$V_{SD(ON)}$	V_{SD} = V_{CL} = 5 V, R_{UP} = 3.3 kΩ	—	—	0.6	V	
Current Limit Reference Voltage	V_{LIM}		0.50	0.53	0.56	V	
OCP Threshold Voltage	V_{TRIP}		0.9	1.0	1.1	V	
OCP Hold Time	t_P	V_{RC} = 5 V, R_{RC} = 330 kΩ, C_{RC} = 0.0047 µF	—	1.0	—	ms	
		V_{RC} = 5 V, R_{RC} = 360 kΩ, C_{RC} = 0.0047 µF	—	1.1	—	ms	
OCP Blanking Time	t_{BK}		—	2.0	—	µs	
TSD Operating Temperature	T_{DH}		120	135	150	°C	
TSD Releasing Temperature	T_{DL}		90	105	120	°C	
TSD Operating Temperature Hysteresis	T_{D_HYS}		—	30	—	°C	

3.2 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 500 V, V_{IN} = 0 V	—	—	10	μA	
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.05 A, V_{IN} = 0 V	—	0.8	1.3	V	
Bootstrap Diode Series Resistor	R_{BOOT}		168	210	252	Ω	

3.3 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance [1]	$R_{(J-C)}$ [2]	All power MOSFETs operating	—	—	3.8	°C/W	SLA6868MH/ 70MH

[1] Refers to a case temperature at the measurement point described in Figure 3-1, below.
[2] Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 14.1.

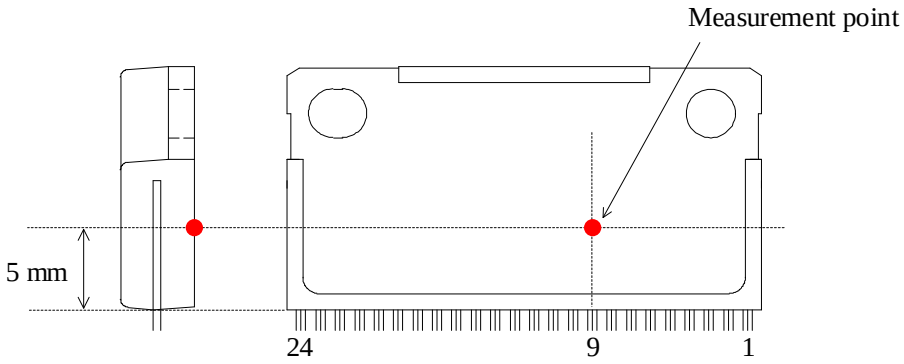


Figure 3-1. Case Temperature Measurement Points

3.4 Power MOSFET Characteristics

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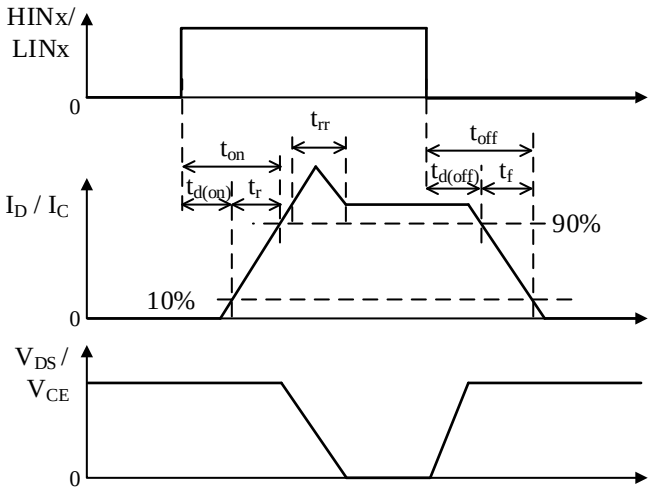


Figure 3-2. Switching Characteristics Definitions

3.4.1 SLA6868MH

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1.25 A, V_{IN} = 5 V	—	2.0	2.4	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 1.25 A, V_{IN} = 0 V	—	1.1	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 2.5 A, V_{IN} = 0 V to 5 V, T_J = 25 °C, inductive load	—	120	—	ns
Turn-on Delay Time	$t_{d(ON)}$		—	820	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(OFF)}$		—	740	—	ns
Fall Time	t_f		—	30	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 2.5 A, V_{IN} = 0 V to 5 V, T_J = 25 °C, inductive load	—	130	—	ns
Turn-on Delay Time	$t_{d(ON)}$		—	790	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(OFF)}$		—	700	—	ns
Fall Time	t_f		—	30	—	ns

3.4.2 SLA6870MH

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1.5 A, V_{IN} = 5 V	—	1.4	1.7	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 1.5 A, V_{IN} = 0 V	—	1.0	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 3 A, V_{IN} = 0 V to 5 V, T_J = 25 °C, inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	755	—	ns
Rise Time	t_r		—	65	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	680	—	ns
Fall Time	t_f		—	15	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 3 A, V_{IN} = 0 V to 5 V, T_J = 25 °C, inductive load	—	105	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	645	—	ns
Rise Time	t_r		—	70	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	560	—	ns
Fall Time	t_f		—	20	—	ns

4. Mechanical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	58.8	—	78.4	N·cm	SLA6868MH/ 70MH

5. Truth Table

Table 5-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx signals in each phase are high at the same time, both the high- and low-side transistors become on (simultaneous on-state). Therefore, HINx and LINx signals, the input signals for the HINx and LINx pins, require dead time setting so that such a simultaneous on-state event can be avoided.

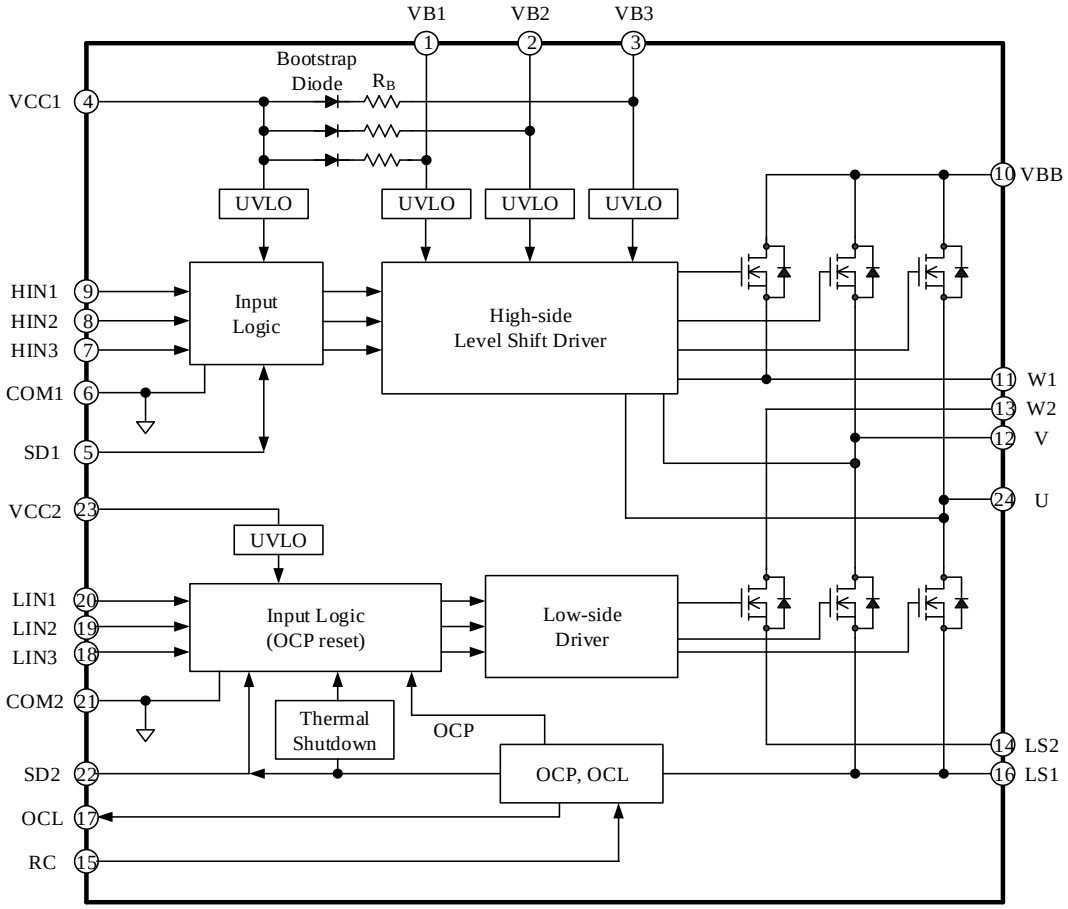
After the IC recovers from a UVLO_VCC2 condition, the low-side transistors resume switching in accordance with the input logic levels of the LINx signals (level-triggered), whereas the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

After the IC recovers from a UVLO_VB or UVLO_VCC1 condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

Table 5-1. Truth Table for Operation Modes

Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON
Shutdown Signal Input (SD2 = “L”)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
VBx Pin Undervoltage Lockout (UVLO_VB) VCC1 Pin Undervoltage Lockout (UVLO_VCC1)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
VCC2 Pin Undervoltage Lockout (UVLO_VCC2)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Overcurrent Limit (OCL) (OCL = SD1)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
Thermal Shutdown (TSD)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF

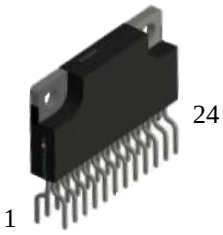
6. Block Diagram



7. Pin Configuration Definitions

Leadform 2175

Leadform 2171



Pin Number	Pin Name	Description
1	VB1	U-phase high-side floating supply voltage input
2	VB2	V-phase high-side floating supply voltage input
3	VB3	W-phase high-side floating supply voltage input
4	VCC1	High-side logic supply voltage input
5	SD1	High-side shutdown signal input; fault signal output at UVLO_VCC1 activation
6	COM1	High-side logic ground
7	HIN3	Logic input for W-phase high-side gate driver
8	HIN2	Logic input for V-phase high-side gate driver
9	HIN1	Logic input for U-phase high-side gate driver
10	VBB	Positive DC bus supply voltage
11	W1	W-phase output (connected to W2 externally)
12	V	V-phase output
13	W2	W-phase output (connected to W1 externally)
14	LS2	W-phase low-side power MOSFET source (connected to LS1 externally)
15	RC	OCP hold time setting
16	LS1	U- and W-phase low-side power MOSFET source (connected to LS2 externally)
17	OCL	Overcurrent limit signal input
18	LIN3	Logic input for W-phase low-side gate driver
19	LIN2	Logic input for V-phase low-side gate driver
20	LIN1	Logic input for U-phase low-side gate driver
21	COM2	Low-side logic ground
22	SD2	Low-side shutdown signal input; fault signal output at UVLO_VCC2, OCP, or TSD activation
23	VCC2	Low-side logic supply voltage input
24	U	U-phase output

8. Typical Application

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

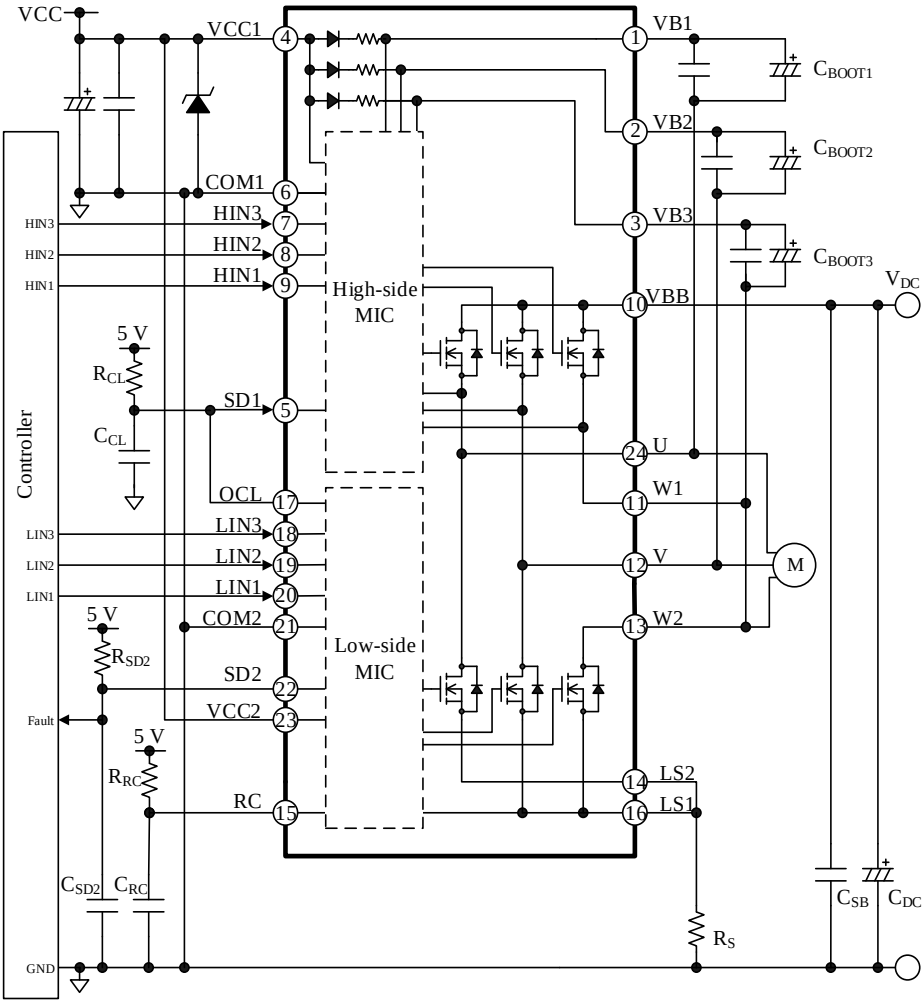
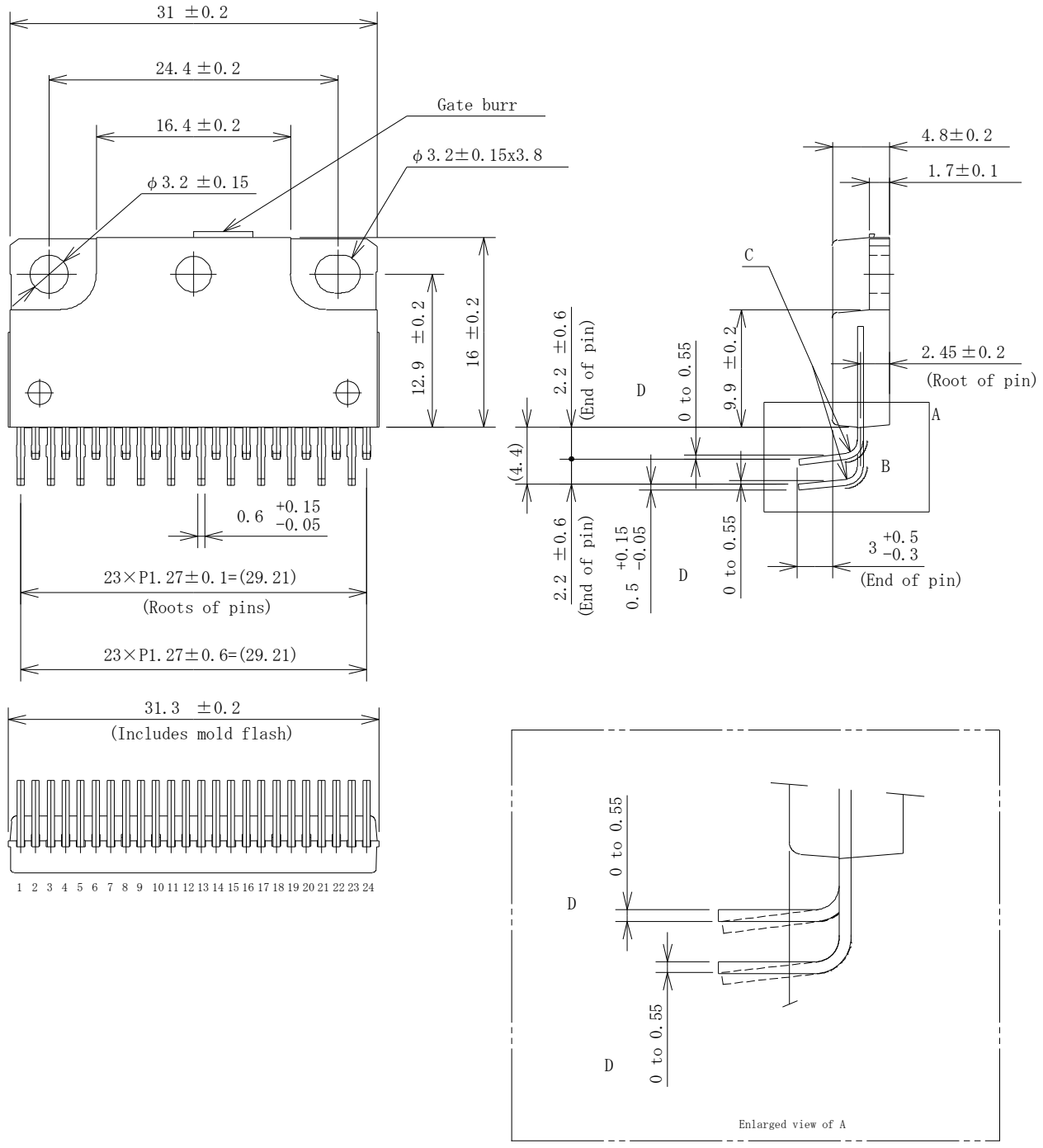


Figure8-1. Typical Application (OCL = SD1)

9. Physical Dimensions

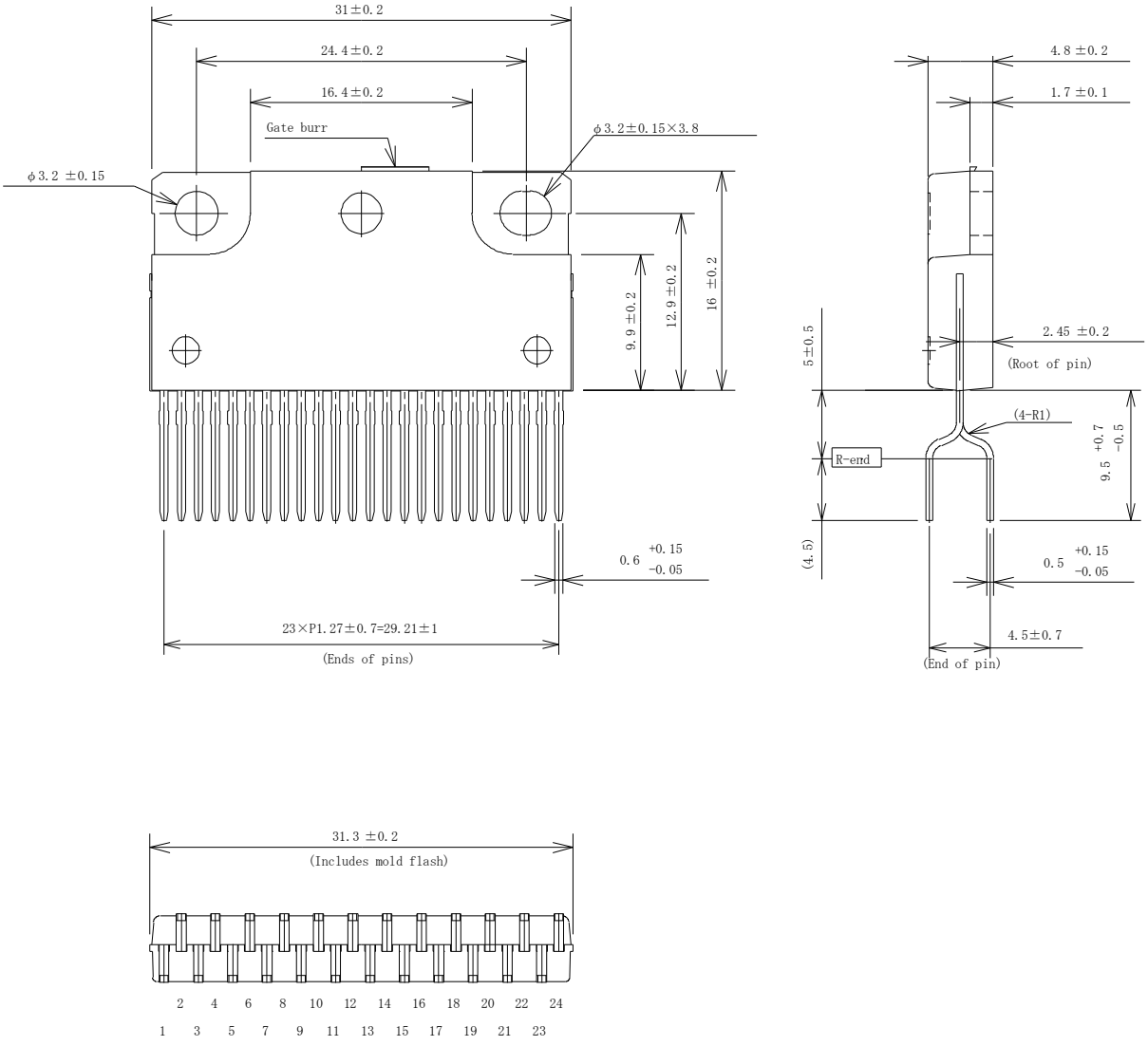
9.1 ZIP24 (Leadform 2175)



NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Maximum gate burr height is 0.3 mm.
- “B” depicts a pin whose plated surface may be cracked.
- “C” shows pins with a minimum inside radius (R) of 0.65 mm.
- “D” represents a pin illustrated for reference only, not the actual state of a bend.

9.2 ZIP24 (Leadform 2171)

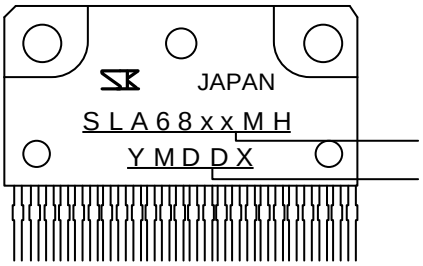


NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Maximum gate burr height is 0.3 mm.

10. Marking Diagram

10.1 ZIP24



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

11. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. Thus, "the VCCx pin" is used when referring to either or both of the VCC1 and VCC2 pins.
- The COM1 pin is always connected to the COM2 pin.

11.1 Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 12.5$ V).

It is required to fully charge bootstrap capacitors, C_{BOOTx}, at startup (see Section 11.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

11.2 Pin Descriptions

11.2.1 U, V, W1, and W2

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The W1 and W2 pins must be connected to each other on a PCB. The U, V, and W1 pins are the grounds for the VB1, VB2, and VB3 pins. The U, V, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{BOOTx}. Since high voltages are applied to these output pins (U, V, W1, and W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

11.2.2 VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the power MOSFET drains of the high-side are connected to this pin. Voltage between the VBB and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

11.2.3 LS1 and LS2

The LS1 pin is connected to the power MOSFET sources of the U- and V-phases; the LS2 pin is connected to the power MOSFET source of the W phase.

The LS1 and LS2 pins must be connected to each other on a PCB. For current detection, these pins should be connected to an external shunt resistor, R_S. When connecting the shunt resistor, place it as near as possible to the IC with a minimum length of traces to the LSx and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

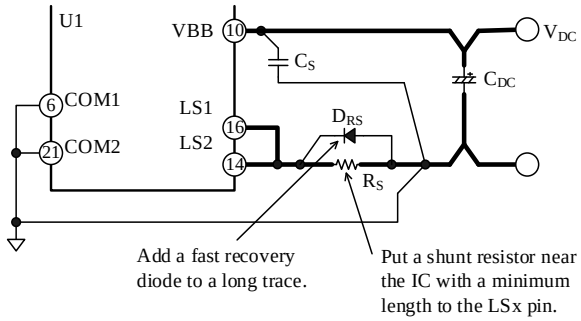


Figure 11-1. Connections to LSx Pin

11.2.4 VB1, VB2, and VB3

These pins are connected to bootstrap capacitors for the high-side floating supply.

Voltages across the VBx and these output pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

A bootstrap capacitor, C_{BOOTx}, should be connected in each of the traces between the VB1 and U pins, the VB2 and V pins, and the VB3 and W1 pins.

For proper startup, turn on the low-side transistors first, then fully charge the bootstrap capacitor, C_{BOOTx}.

For the capacitance of the bootstrap capacitors, C_{BOOTx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{BOOTx}.

$$C_{BOOTx}(\mu F) > 800 \times t_{L(OFF)} \quad (1)$$

$$1\ \mu F \leq C_{BOOTx} \leq 220\ \mu F \quad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{BOOTx}), measured in seconds.

Even while the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 11.3.3.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V (V_{BS} > $V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 11-2 shows, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are internally placed in series between the VCC1 and VBx pins. Time constant for the charging time of C_{BOOTx}, τ, can be computed by Equation (3):

$$\tau = C_{BOOTx} \times R_{BOOTx} \ , \qquad (3)$$

where C_{BOOTx} is the optimized capacitance of the bootstrap capacitor, and R_{BOOTx} is the resistance of the current-limiting resistor (210 Ω ± 20%).

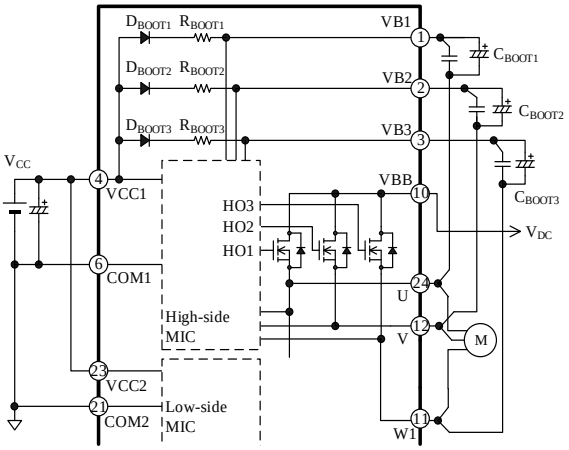


Figure 11-2. Bootstrap Circuit

Figure 11-3 shows an internal level-shifting circuit. A high-side output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a "Set" signal is generated. When the HINx input signal transits from high to low (falling edge), a "Reset" signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 11-4 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and output pins (U, V, or W1; hereafter "VBx–HSx") occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of an HOx signal stays logic high (or "H") because the SR flip-flop does not respond. With the HOx state being held high (i.e., the high-side transistor is in an on-state), the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition, which may result in critical damage to the IC. To protect the VBx pin against such a noise effect, add a bootstrap capacitor, C_{BOOTx}, in each phase. C_{BOOTx} must be placed near the IC and be connected between the VBx and HSx pins with a minimal length of traces. To use an electrolytic capacitor, add a 0.01 μF to 0.1 μF bypass capacitor, C_{Px}, in parallel near these pins used for the same phase.

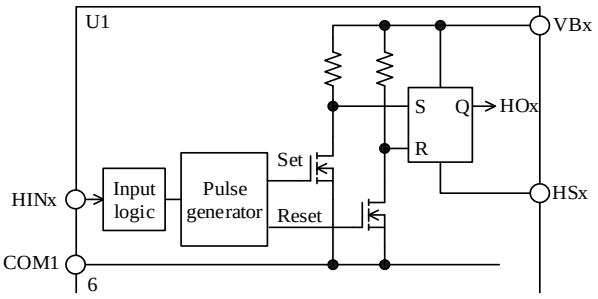


Figure 11-3. Internal Level-shifting Circuit

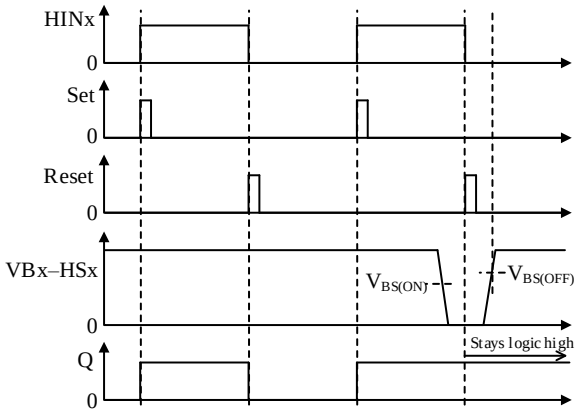


Figure 11-4. Waveforms at VBx–HSx Voltage Drop

11.2.5 VCC1 and VCC2

These are the logic supply pins for the built-in control MIC. The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 μF to 0.1 μF ceramic capacitor, C_{VCC}, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins.

Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

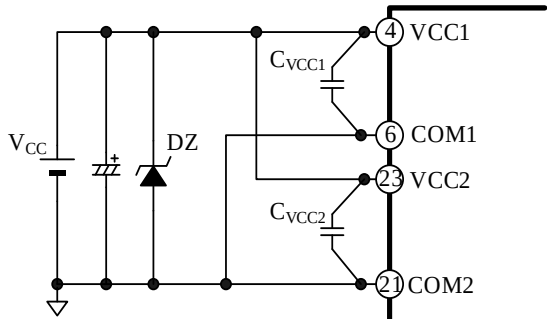


Figure 11-5. VCCx Pin Peripheral Circuit

11.2.6 COM1 and COM2

These are the logic ground pins for the built-in control MICs. The COM1 and COM2 pins should be connected externally on a PCB because they are not internally connected. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 11-6).

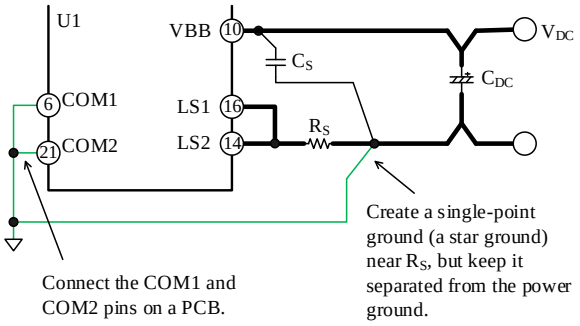


Figure 11-6. Connections to Logic Ground

11.2.7 HIN1, HIN2, and HIN3; LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller. Figure 11-7 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 20 kΩ pull-down resistor, and its input logic is active high.

Input signals applied across the HINx–COMx and the LINx–COMx pins in each phase should be set within the ranges provided in Table 11-1, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 1.

Table 11-1. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 µs	≥0.5 µs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥1.5 µs	

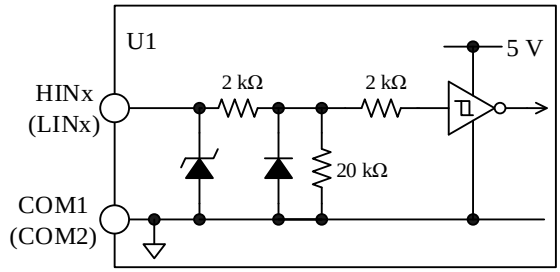


Figure 11-7. Internal Circuit Diagram of HINx or LINx Pin

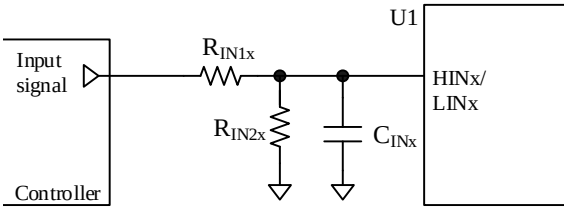


Figure 11-8. Filter Circuit for HINx or LINx Pin

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, the outputs from the microcontroller output line should not be high impedance. Also, if the traces from the microcontroller to the HINx or LINx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 11-8).

Here are filter circuit constants for reference:

- R_{IN1x}: 33 Ω to 100 Ω
- R_{IN2x}: 1 kΩ to 10 kΩ
- C_{INx}: 100 pF to 1000 pF

Care should be taken in adding R_{IN1x} and R_{IN2x} to the traces. When they are connected to each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

11.2.8 OCL

During OCL operation, the OCL pin logic level is low. To turn off the high- or low-side transistors during the OCL operation, connect the OCL pin to the SD1 or SD2 pin according to which side of transistors are to be turned off.

Figure 11-9 illustrates an internal circuit diagram of the OCL pin and its peripheral circuit. Because of its open-collector nature, the OCL pin should be tied by a pull-up resistor, R_{CL}, to the external power supply, which should range from 3.0 V to 5.5 V. When connecting the OCL and SDx pins, it is recommended to use a 1 kΩ to 10 kΩ pull-up resistor. To suppress noise, add a filter capacitor, C_{CL}, near the IC with minimizing a trace length between the OCL and COM2 pins. C_{CL} should have a capacitance of 0.001 µF to 0.01 µF. Leave the OCL pin open if not used.

For more details on the OCL, see Section 11.3.4.

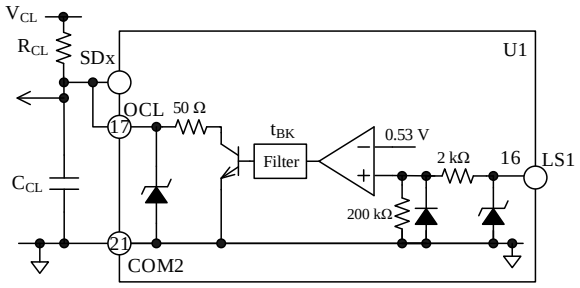


Figure 11-9. Internal Circuit Diagram of OCL Pin and Its Peripheral Circuit

11.2.9 RC

Figure 11-10 is an internal circuit diagram describing the RC pin and its peripheral circuit.

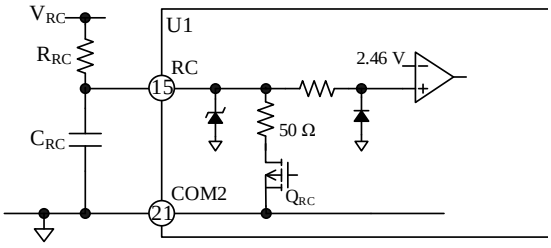


Figure 11-10. Internal Circuit Diagram of RC Pin and Its Peripheral Circuit

The RC pin should be connected to a pull-up resistor, R_{RC}, and a capacitor, C_{RC}, which determine a time from OCP activation until OCP release (i.e., the OCP Hold Time, t_P). Because of its open-drain nature, the RC pin should be tied by the pull-up resistor, R_{RC}, to the external power supply, which should range from 3.0 V to 5.5 V.

R_{RC} should have a resistance of 33 kΩ to 680 kΩ; C_{RC} should have a capacitance of 1000 pF to 0.0047 µF.

If R_{RC} is left open, the IC cannot release the OCP operation. Conversely, if R_{RC} is shorted, the IC cannot activate the OCP circuit. If C_{RC} is left open, t_P becomes shorter and the IC releases the OCP operation in a shorter time correspondingly. Therefore, care should be taken when you set these components.

Figure 11-11 is a timing chart showing the RC pin waveform during the OCP operation. The enabled OCP circuit turns off the low-side transistors and puts the SD2 pin into a low state. (Section 11.3.5 provides more details on the OCP.) At the same time, the internal power MOSFET of the RC pin, Q_{RC}, turns on, then the RC pin becomes logic low. Q_{RC} turns off about 5 µs after the Q_{RC} turn-on. Subsequently, the RC pin voltage increases with the time constant which is determined by R_{RC} and C_{RC}. When the RC pin voltage reaches 2.46 V, the IC releases the OCP operation.

The OCP Hold Time, t_P, depends on the external power supply voltage, V_{RC}. The approximate value of t_P is calculated by the following equations:

- **When External Power Supply Voltage, V_{RC} = 3.3 V:**

$$t_P = 1.35 \times R_{RC} \times C_{RC} . \quad (4)$$

- **When External Power Supply Voltage, V_{RC} = 5 V:**

$$t_{RC} = 0.65 \times R_{RC} \times C_{RC} . \quad (5)$$

Here is an example: when V_{RC} = 5 V, R_{RC} = 330 kΩ, and C_{RC} = 0.0047 µF, we find that t_{RC} = 1 ms.

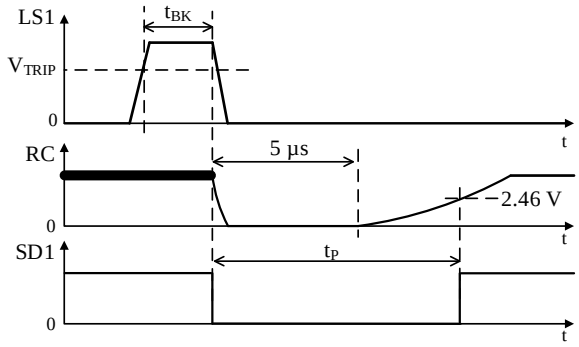


Figure 11-11. RC Pin Waveform during OCP Operation

11.2.10 SD1 and SD2

These pins operate as the fault signal outputs and the shutdown signal inputs. Section 11.3.1 provides detailed functional descriptions on the fault signal output; Section 11.3.2 describes the shutdown function.

Figure 11-12 illustrates an internal circuit diagram of the SDx pin and its peripheral circuit. Note that the SDx pin does not respond to a pulse shorter than an internal filter of 3.3 µs (typ.). Because of its open-collector nature, the SDx pin should be tied by a pull-up resistor, R_{SDx}, to the external power supply, which should range from 3.0 V to 5.5 V. It is recommended to use a 3.3 kΩ to 10 kΩ pull-up resistor. To suppress noise, add a filter capacitor, C_{SDx}, near the IC with minimizing a trace length between the SDx and COMx pins. C_{SDx} should have a capacitance of 0.001 µF to 0.01 µF.

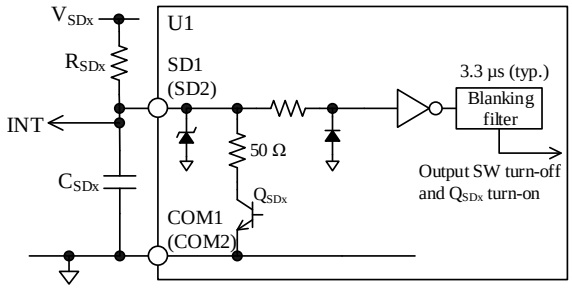


Figure 11-12. Internal Circuit Diagram of SDx Pin and Its Peripheral Circuit

11.3 Protection Functions

This section describes the various protection circuits provided in the IC. The protection circuits are as follows: the undervoltage lockout for power supplies (UVLO) of the VBx, VCC1, and VCC2 pins; the overcurrent protection (OCP); the thermal shutdown (TSD). In case one or more of the following protections are actuated, the SD1 or SD2 pin becomes logic low. By receiving a fault signal from the SDx pin, the external microcontroller can take a protective step such as turning off all the transistors. The external microcontroller can also shut down IC operations by inputting a fault signal to the SDx pin.

In the following functional descriptions, "HOx" denotes a gate input signal on the high-side transistor, whereas "LOx" denotes a gate input signal on the low-side transistor. "VBx–HSx" refers to the voltages between the VBx pin and output pins (U, V, and W1).

11.3.1 Fault Signal Output

The SDx pin is logic high in normal operation and is logic low in fault signal output operation.

- **SD1**

The SD1 pin becomes logic low while the VCC1 pin undervoltage lockout for power supply (UVLO_VCC1) is operating.

- **SD2**

The SD2 pin becomes logic low while one or more of the following protections are operating: the VCC2 pin undervoltage lockout for power supply (UVLO_VCC2), the overcurrent protection (OCP), and the thermal shutdown (TSD). While the SD2 pin is in a low state, all the low-side transistors turn off. The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HINx and LINx pins to logic low within the predetermined OCP hold time, t_P. t_P is determined by the value of the pull-up resistor and capacitor which are externally connected to the RC pin (see Section 11.3.5).

11.3.2 Shutdown Signal Input

The SDx pin also acts as the input pin of shutdown signals. When the SD1 pin becomes logic low, all the high-side transistors turn off. When the SD2 pin becomes logic low, all the low-side transistors turn off.

The voltages and pulse widths of the shutdown signals to be applied are listed in Table 11-2.

Table 11-2. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	—	≥6 µs

Connecting the SD1 or SD2 pin to the OCL pin allows the IC to turn off the high- or low-side transistors at OCL activation (see Section 11.3.4).

11.3.3 Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the IC has the undervoltage lockout (UVLO) circuits for each of the VBx, VCC1, and VCC2 pins.

11.3.3.1. VBx Pin (UVLO_VB)

Figure 11-13 shows operational waveforms of the VBx pin undervoltage lockout for power supply (i.e., UVLO_VB).

When the voltage between the VBx and output pins (VBx–HSx) decreases to the Logic Operation Stop Voltage ($V_{BS(OFF)}$ = 10.0 V) or less, the UVLO_VB circuit in the corresponding phase gets activated and sets an HOx signal to logic low. When the voltage between the VBx and HSx pins increases to the Logic Operation Start Voltage ($V_{BS(ON)}$ = 10.5 V) or more, the IC releases the UVLO_VB operation. Then, the HOx signal becomes logic high at the rising edge of the first

input command after the UVLO_VB release.

Any fault signals are not output from the SDx pin during the UVLO_VB operation. The VBx pin has an internal filter circuit to prevent noise-induced malfunctions.

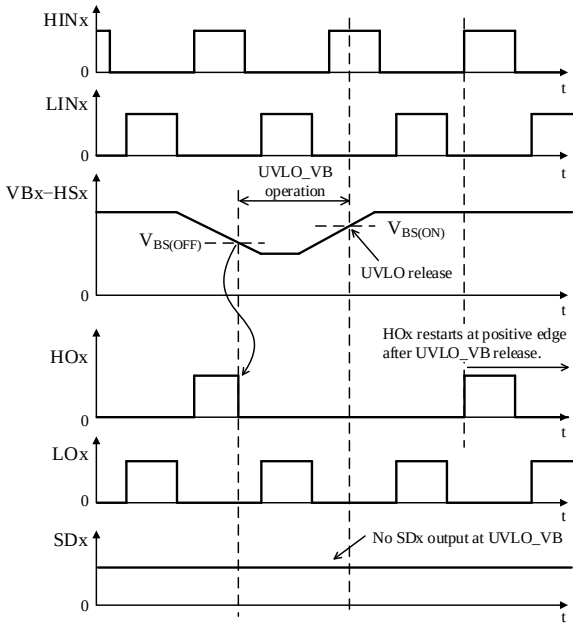


Figure 11-13. UVLO_VB Operational Waveforms

11.3.3.2. VCC1 Pin (UVLO_VCC1)

Figure 11-14 shows operational waveforms of the VCC1 pin undervoltage lockout for power supply (i.e., UVLO_VCC1).

When the VCC1 pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$ = 11.0 V) or less, the UVLO_VCC1 circuit gets activated and sets an HOx signal to logic low. When the VCC1 pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$ = 11.5 V) or more, the IC releases the UVLO_VCC1 operation. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VCC1 release. During the UVLO_VCC1 operation, the SD1 pin becomes logic low and sends fault signals.

The VCC1 pin has an internal filter circuit to prevent noise-induced malfunctions.

11.3.3.3. VCC2 Pin (UVLO_VCC2)

Figure 11-15 shows operational waveforms of the VCC2 pin undervoltage lockout for power supply (i.e., UVLO_VCC2).

When the VCC2 pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$ = 11.0 V) or less, the UVLO_VCC2 circuit gets activated and sets an LOx signal to logic low. When the VCC2 pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$ = 11.5 V) or more, the IC releases the UVLO_VCC2 operation. The IC then resumes transmitting an LOx signal according to an input command on the LINx pin. During the UVLO_VCC2 operation, the SD2 pin becomes logic low and sends fault signals.

The VCC2 pin has an internal filter circuit to prevent noise-induced malfunctions.

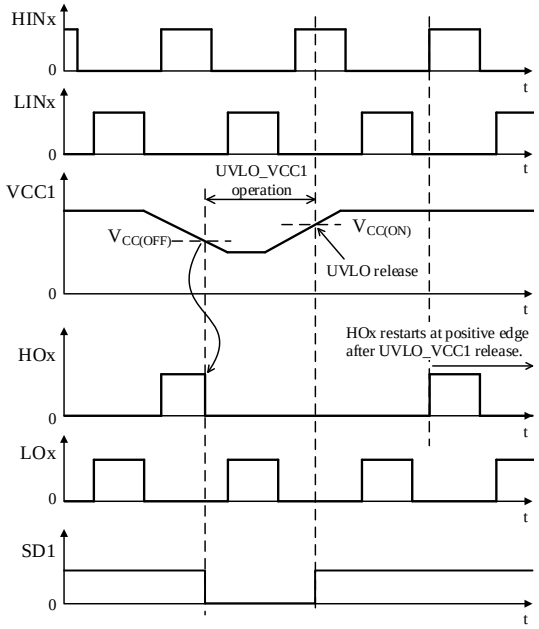


Figure 11-14. UVLO_VCC1 Operational Waveforms

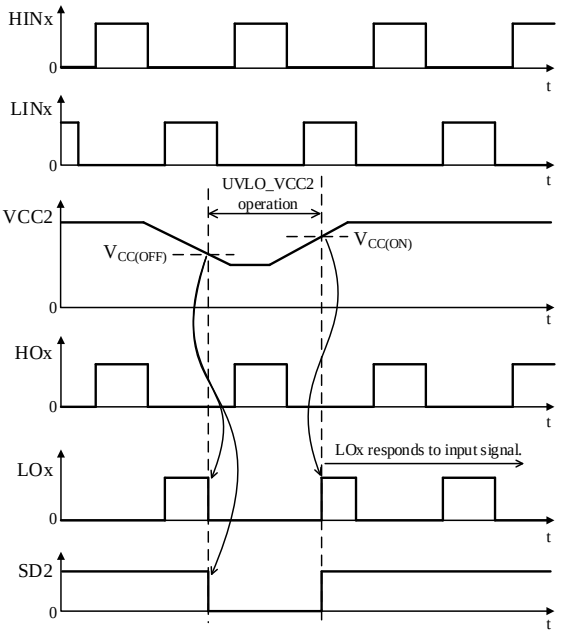


Figure 11-15. UVLO_VCC2 Operational Waveforms

11.3.4 Overcurrent Limit (OCL)

The overcurrent limit (OCL) is a protection against relatively low overcurrent conditions. When the LS1 pin voltage increases to the Current Limit Reference Voltage (V_{LIM} = 0.53 V) or more, and remains in this condition for a period of the Current Limit Blanking Time (t_{BK} = 2.0 µs) or longer, the OCL circuit is activated. Then, the OCL pin goes logic low. When the LS1 pin voltage falls below V_{LIM} (0.53 V), the OCL pin logic level becomes high.

Figure 11-16 is a timing chart that represents operational waveforms during the OCL operation where the OCL and SD1 pins are externally connected on a PCB. The SD1-OCL pin connection allows the IC to turn off the high-side transistors at OCL activation. During the OCL operation, the gate logic levels of the low-side transistors respond to an input command on the LINx pin. The SD1 pin has an internal filter of 3.3 µs (typ.). After the SD1 and OCL pins have become logic high, the high-side transistors remain turned off until the first low-to-high transition on an HINx input signal occurs (i.e., edge-triggered).

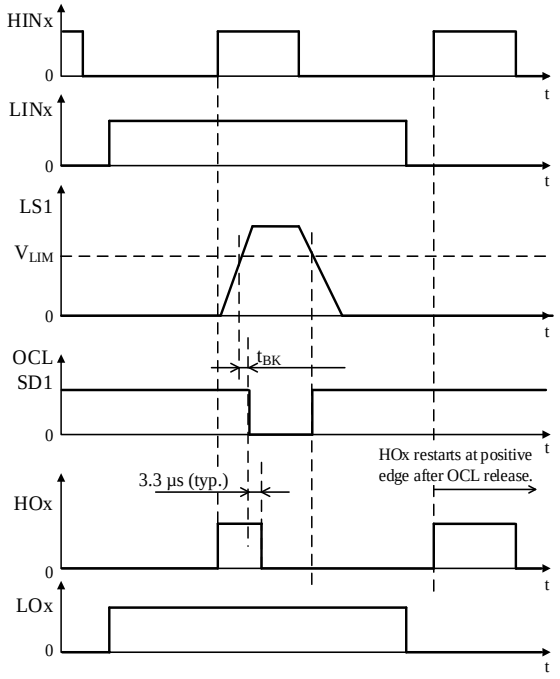


Figure 11-16. OCL Operational Waveforms (OCL = SD)

11.3.5 Overcurrent Protection (OCP)

The overcurrent protection (OCP) is a protection against large inrush currents (i.e., high di/dt).

Figure 11-17 is an internal circuit diagram describing the LS1 pin and its peripheral circuit. The LS1 pin should be connected to an external shunt resistor, R_S, on a PCB. The LS1 pin voltage increases proportionally to a rise in the current flowing through the external shunt resistor, R_S. The built-in dedicated circuit monitors changes in the LS1 pin voltage to detect overcurrents.

Figure 11-18 is a timing chart that represents operational waveforms during OCP operation. When the LS1 pin voltage increases to the OCP Threshold Voltage (V_{TRIP} = 1.0 V) or more, and remains in this condition for a period of the OCP Blanking Time (t_{BK} = 2.0 µs) or longer, the OCP circuit is activated. When the OCP is activated, the IC puts both the LOx and SD2 outputs to a low state.

The current flowing through R_S decreases while the LOx signal is in the low state. Even if the LS1 pin voltage falls below V_{TRIP}, the IC holds the SD2 pin in the low state for a fixed OCP hold time (t_P). Then, the output transistors operate according to input signals. t_P is determined by the RC pin. For details on the RC pin setting, see Section 11.2.9.

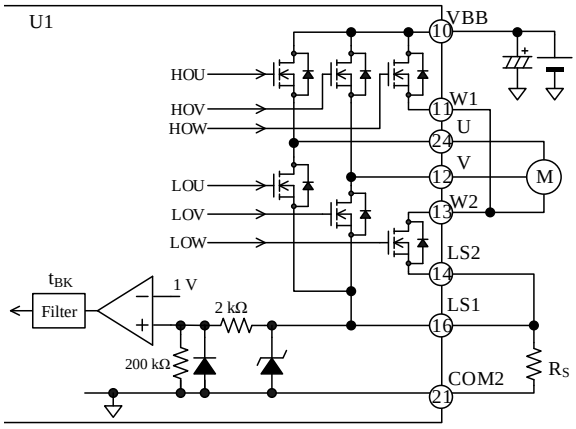


Figure 11-17. Internal Circuit Diagram of LS1 Pin and Its Peripheral Circuit

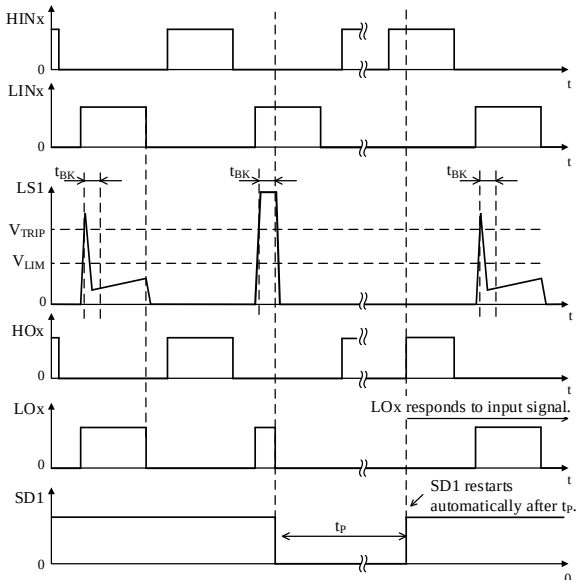


Figure 11-18. OCP Operational Waveforms

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, the external microcontroller, where a fault signal from the SD2 pin is input via its interrupt pin (INT), must be programmed to put the HINx and LINx pins to logic low within a predetermined OCP hold time, t_P.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

Note that overcurrents are undetectable when one or more of the U, V, and W1/W2 pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

11.3.6 Thermal Shutdown (TSD)

The IC incorporates the thermal shutdown (TSD) circuit. Figure 11-19 shows TSD operational waveforms. In case of overheating (e.g., increased power dissipation due to overload, or elevated ambient temperature at the device), the IC puts both the LOx and SD2 outputs to a low state.

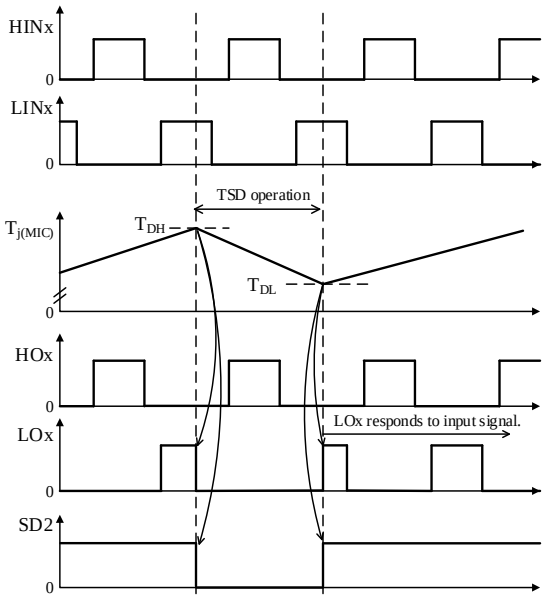


Figure 11-19. TSD Operational Waveforms

The TSD circuit in the MIC monitors temperatures (see Section 6). When the temperature of the MIC exceeds the TSD Operating Temperature (T_{DH} = 135 °C), the corresponding TSD circuit is activated. When the temperature of the MIC decreases to the TSD Releasing Temperature (T_{DL} = 105 °C) or less, the shutdown condition is released. The transistors then resume operating according to input signals.

Note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

12. Design Notes

12.1 PCB Pattern Layout

Figure 12-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

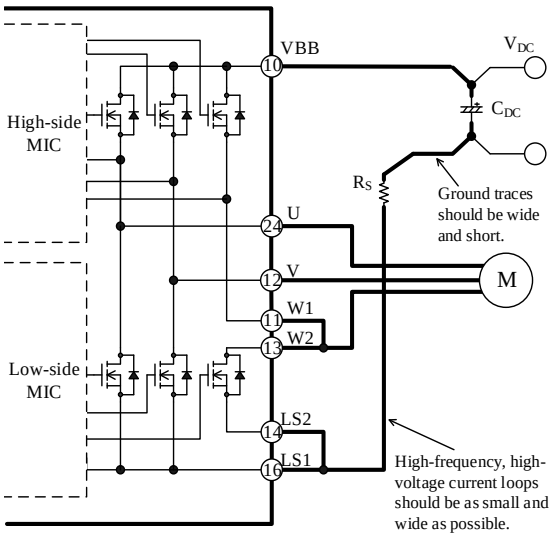


Figure 12-1. High-frequency, High-voltage Current Paths

12.2 Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- It is recommended to use a metric screw of M2.5. To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to about 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 4.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible.

12.3 Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that the gate and source of each transistor should have the same potential. Moreover, care should be taken during the measurement because each transistor is connected as follows:

- All the high-side drains are internally connected to the VBB pin.
- In the U-phase, the high-side source and the low-side drain are internally connected to the U pin.
  (In the W-phase, the high- and low-side transistors are unconnected inside the IC.)

The gates of the high-side transistors are pulled down to the corresponding output (U, V, and W1) pins; similarly, the gates of the low-side transistors are pulled down to the COM2 pin.

When measuring the breakdown voltage or leakage current of the transistors, note that all of the output (U, V, and W1), LSx, and COMx pins must be appropriately connected. Otherwise, the switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 12-2 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 12-3 shows the low-side transistor (Q_{1L}) in the U-phase. And all the pins that are not represented in these figures are open.

When measuring the high-side transistors, leave all the pins not be measured open. When measuring the low-side transistors, connect the LSx pin to be measured to the COM2 pin, then leave other unused pins open.

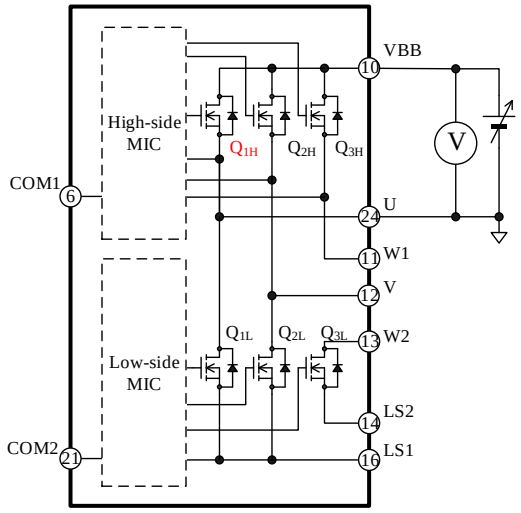


Figure 12-2. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

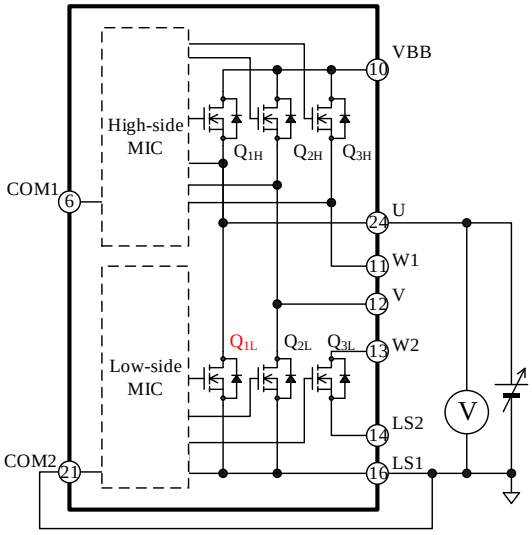


Figure 12-3. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

13. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in output transistors (power MOSFETs), and to estimate a junction temperature. Note that the descriptions listed here are applicable to the IC, which is controlled by a 3-phase sine-wave PWM driving strategy. For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0050: SLA687xMH and SLA686xMH Series Calculation Tool
  http://www.semicon.sanken-ele.co.jp/en/calc-tool/mosfet_caltool_en.html

Total power loss in a power MOSFET can be obtained by taking the sum of the following losses: steady-state loss, P_{RON}; switching loss, P_{SW}; the steady-state loss of a body diode, P_{SD}. In the calculation procedure we offer, the recovery loss of a body diode, P_{RR}, is considered negligibly small compared with the ratios of other losses.

The following subsections contain the mathematical procedures to calculate these losses (P_{RON}, P_{SW}, and P_{SD}) and the junction temperature of all power MOSFETs operating.

13.1 Power MOSFET Steady-state Loss, P_{RON}

Steady-state loss in a power MOSFET can be computed by using the $R_{DS(ON)}$ vs. I_D curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-1, linear approximations at a range the I_D is actually used are obtained by: $R_{DS(ON)} = \alpha \times I_D + \beta$.

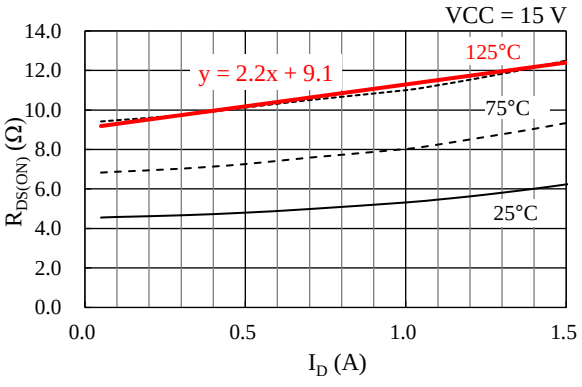


Figure 13-1. Linear Approximate Equation of $R_{DS(ON)}$ vs. I_D Curve

The values gained by the above calculation are then applied as parameters in Equation (6), below. Hence, the equation to obtain the power MOSFET steady-state loss, P_{RON}, is:

$$P_{RON} = \frac{1}{2\pi}\int_0^{\pi} I_D(\varphi)^2 \times R_{DS(ON)}(\varphi) \times DT \times d\varphi$$

$$= 2\sqrt{2}\alpha\left(\frac{1}{3\pi} + \frac{3}{32}M \times \cos\theta\right) {I_M}^3 + 2\beta\left(\frac{1}{8} + \frac{1}{3\pi}M \times \cos\theta\right) {I_M}^2 . \quad (6)$$

Where:

I_D is the drain current of the power MOSFET (A),

$R_{DS(ON)}$ is the drain-to-source on-resistance of the power MOSFET (Ω),

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current (A),

α is the slope of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve, and

β is the intercept of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve.

13.2 Power MOSFET Switching Loss, P_{SW}

Switching loss in a power MOSFET can be calculated by Equation (7), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (7)$$

Where:

f_C is the PWM carrier frequency (Hz),

V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and

α_E is the slope on the switching loss curve (see Section 14.3.2).

13.3 Body Diode Steady-state Loss, P_{SD}

Steady-state loss in the body diode of a power MOSFET can be computed by using the V_{SD} vs. I_{SD} curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-2, linear approximations at a range the I_{SD} is actually used are obtained by: $V_{SD} = \alpha \times I_{SD} + \beta$.

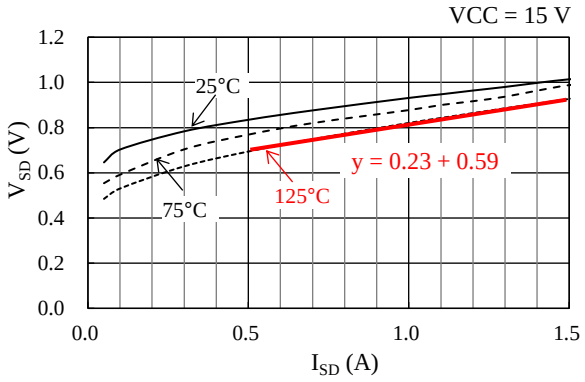


Figure 13-2. Linear Approximate Equation of V_{SD} vs. I_{SD} Curve

The values gained by the above calculation are then applied as parameters in Equation (8), below. Hence, the equation to obtain the body diode steady-state loss, P_{SD}, is:

$$P_{SD} = \frac{1}{2\pi}\int_0^{\pi} V_{SD}(\varphi) \times I_{SD}(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right) I_M . \quad (8)$$

Where:

V_{SD} is the source-to-drain diode forward voltage of the power MOSFET (V),

I_{SD} is the source-to-drain diode forward current of the power MOSFET (A),

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),

$\cos\theta$ is the motor power factor (0 to 1),

I_M is the effective motor current (A),

α is the slope of the linear approximation in the V_{SD} vs. I_{SD} curve, and

$\beta$is the intercept of the linear approximation in the V_{SD} vs. I_{SD} curve.

13.4 Estimating Junction Temperature of Power MOSFET

The junction temperature of all power MOSFETs operating, T_J, can be estimated with Equation (9):

$$T_J = R_{J-C} \times \{(P_{ON} + P_{SW} + P_{SD}) \times 6\} + T_C . \quad (9)$$

Where:

R_{J-C} is the junction-to-case thermal resistance (°C/W) of all the power MOSFETs operating, and

T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

14. Performance Curves

14.1 Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

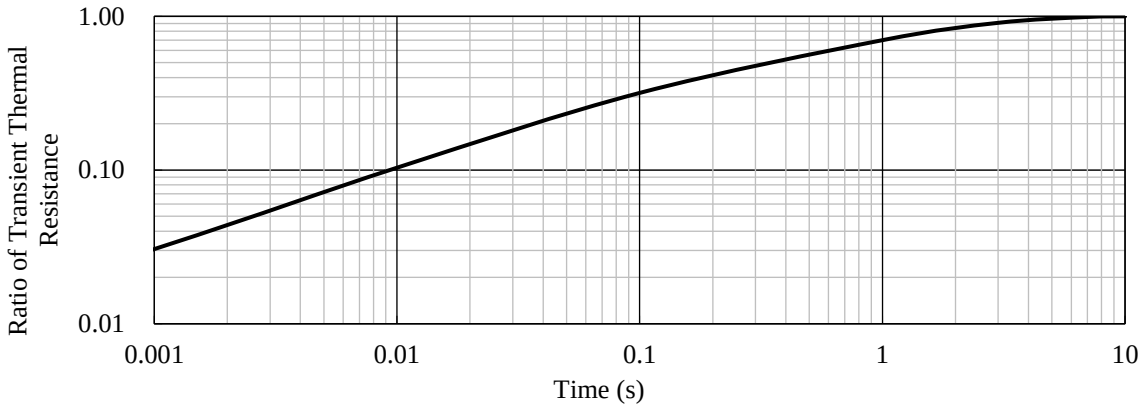


Figure 14-1. Transient Thermal Resistance

14.2 Performance Curves of Control Parts

Figure 14-2 to Figure 14-27 provide performance curves of the control parts integrated in the SLA6870MH and the SLA6860MH series, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 14-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 14-2	Logic Supply Current, I_{CC} vs. T_C (HINx = 0 V, LINx = 0 V)
Figure 14-3	Logic Supply Current, I_{CC} vs. T_C (HINx = 5 V, LINx = 5 V)
Figure 14-4	Logic Supply Current, I_{CC} vs. VCCx Pin Voltage, V_{CC}
Figure 14-5	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C
Figure 14-6	Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C
Figure 14-7	VBx Pin Voltage, V_B vs. Logic Supply Current, I_{BS} (HINx = 0 V)
Figure 14-8	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 14-9	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 14-10	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 14-11	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 14-12	UVLO_VB Filtering Time vs. T_C
Figure 14-13	UVLO_VCC1 Filtering Time vs. T_C
Figure 14-14	UVLO_VCC2 Filtering Time vs. T_C
Figure 14-15	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 14-16	Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C
Figure 14-17	Input Current at High Level (HINx or LINx), I_{IN} vs. T_C
Figure 14-18	High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)
Figure 14-19	Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)
Figure 14-20	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 14-21	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 14-22	SD1 Pin Filtering Time vs. T_C
Figure 14-23	SD2 Pin Filtering Time vs. T_C
Figure 14-24	Current Limit Reference Voltage, V_{LIM} vs. T_C
Figure 14-25	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 14-26	OCP Hold Time, t_P vs. T_C
Figure 14-27	OCP Blanking Time, $t_{BK(OCP)}$ vs. T_C; Current Limit Blanking Time, $t_{BK(OCL)}$ vs. T_C

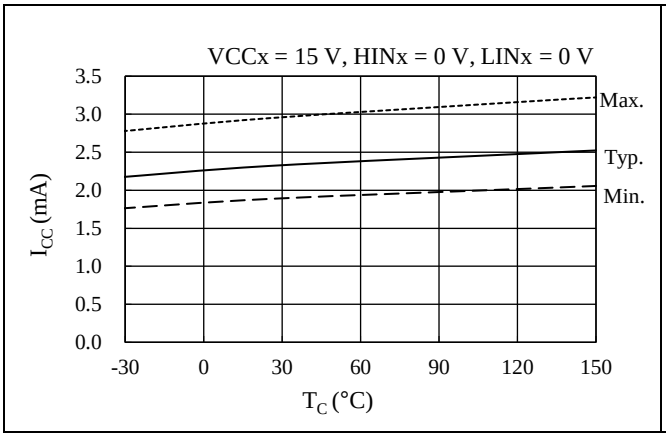


Figure 14-2. Logic Supply Current, I_{CC} vs. T_C (HINx = 0 V, LINx = 0 V)

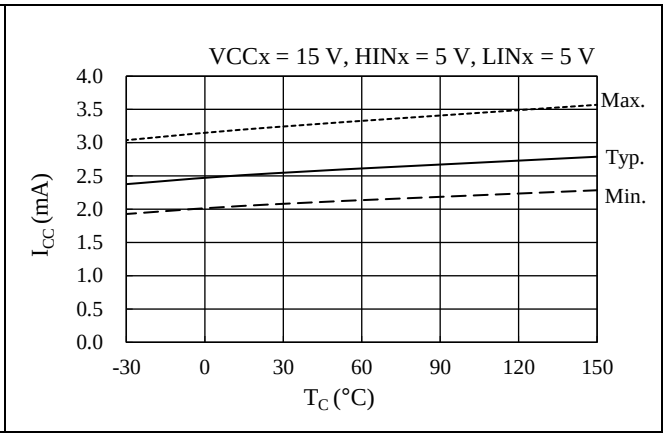


Figure 14-3. Logic Supply Current, I_{CC} vs. T_C (HINx = 5 V, LINx = 5 V)

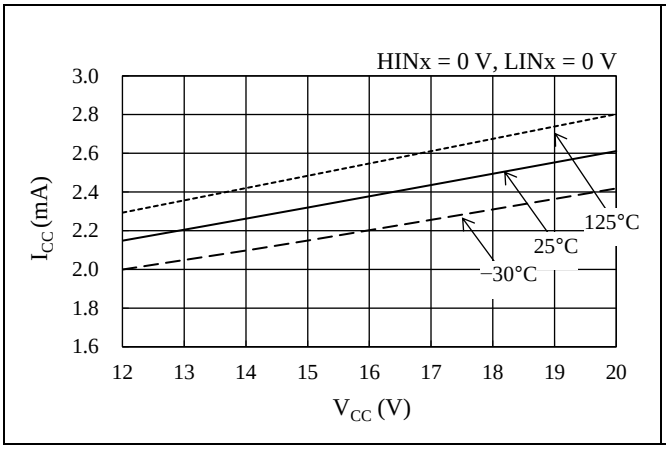


Figure 14-4. Logic Supply Current, I_{CC} vs. VCCx Pin Voltage, V_{CC}

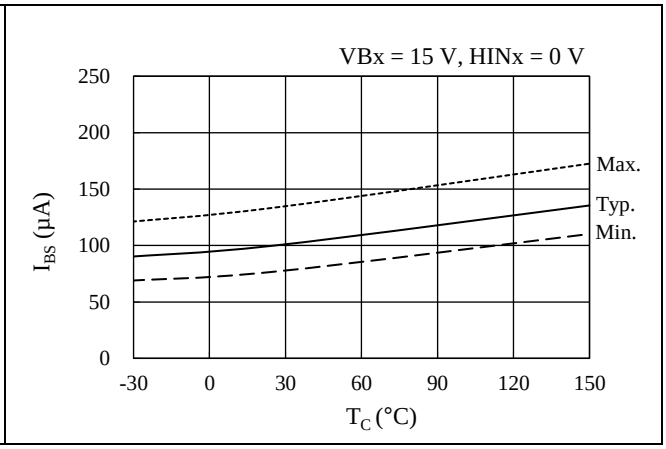


Figure 14-5. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C

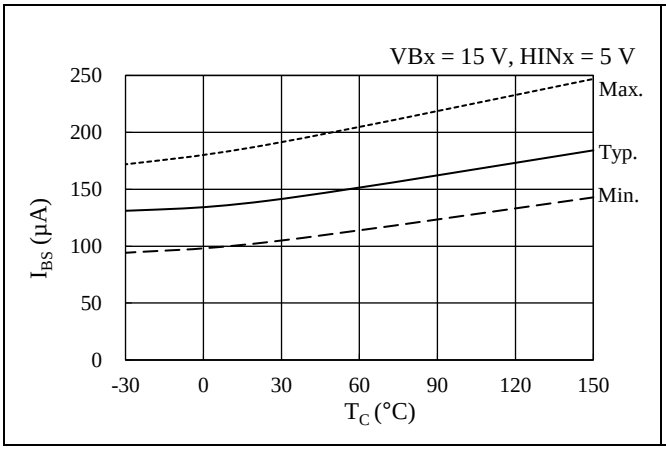


Figure 14-6. Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C

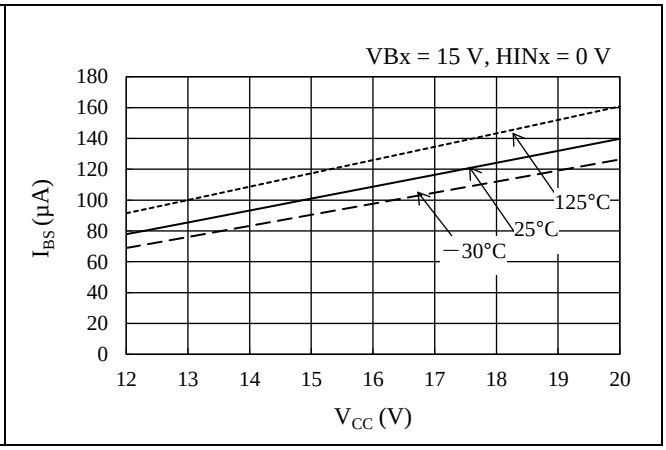


Figure 14-7. VBx Pin Voltage, V_B vs. Logic Supply Current, I_{BS} (HINx = 0 V)

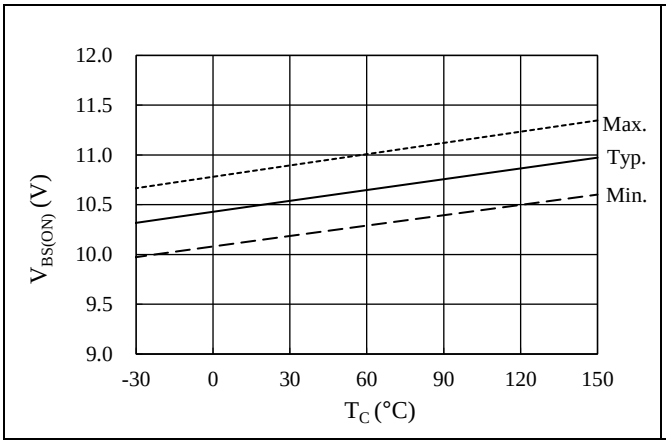


Figure 14-8. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

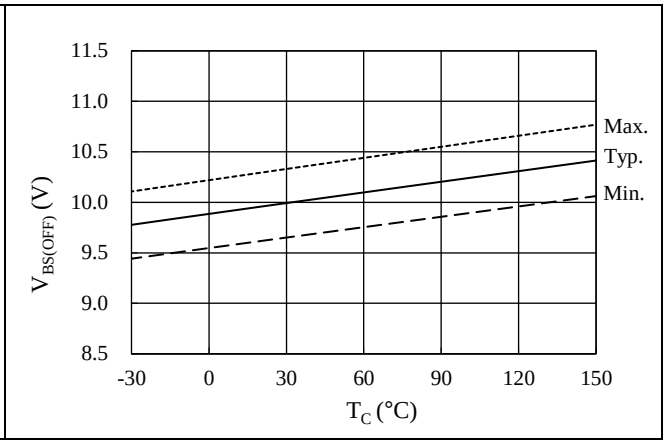


Figure 14-9. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

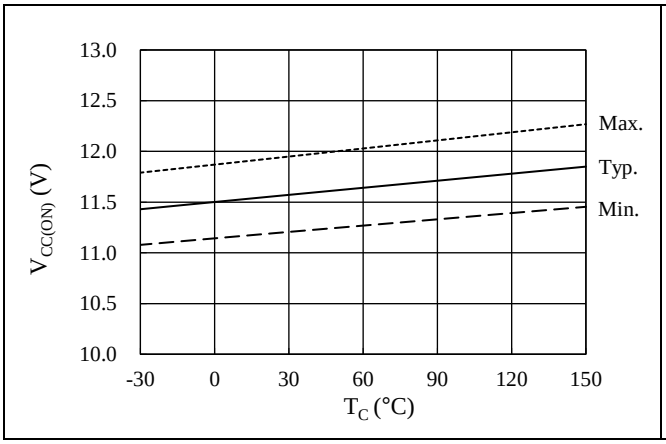


Figure 14-10. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

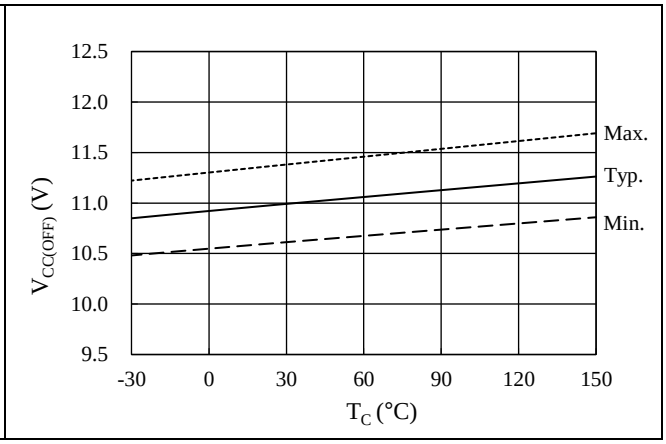


Figure 14-11. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

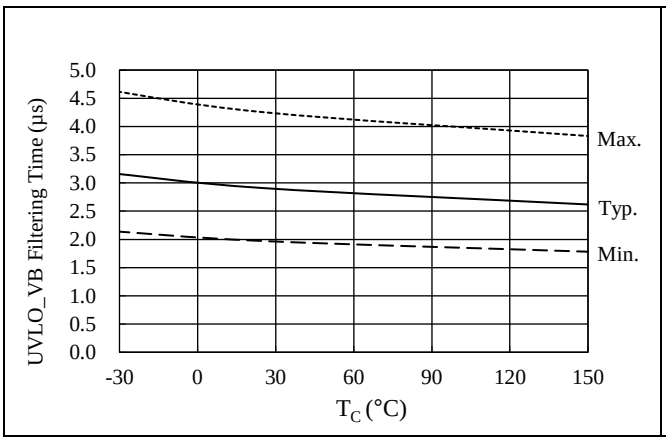


Figure 14-12. UVLO_VB Filtering Time vs. T_C

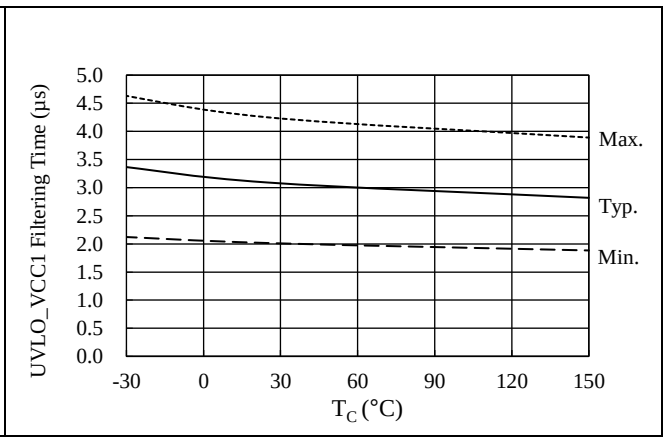


Figure 14-13. UVLO_VCC1 Filtering Time vs. T_C

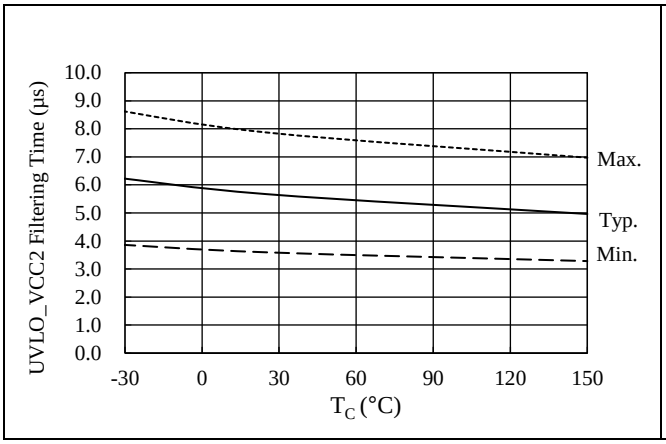


Figure 14-14. UVLO_VCC2 Filtering Time vs. T_C

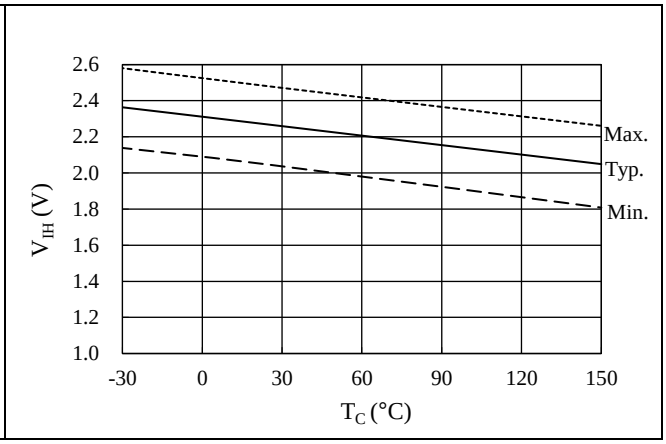


Figure 14-15. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

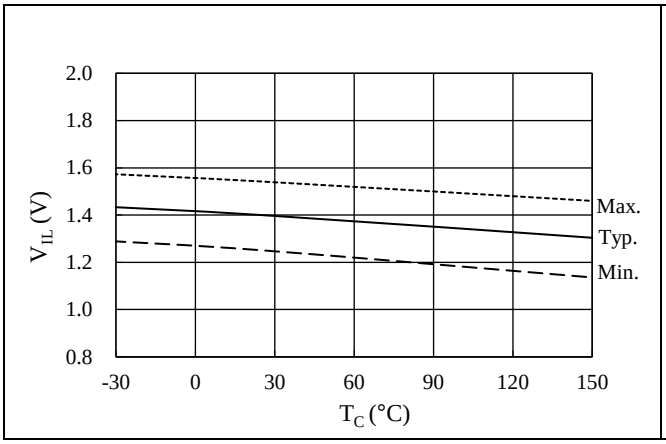


Figure 14-16. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

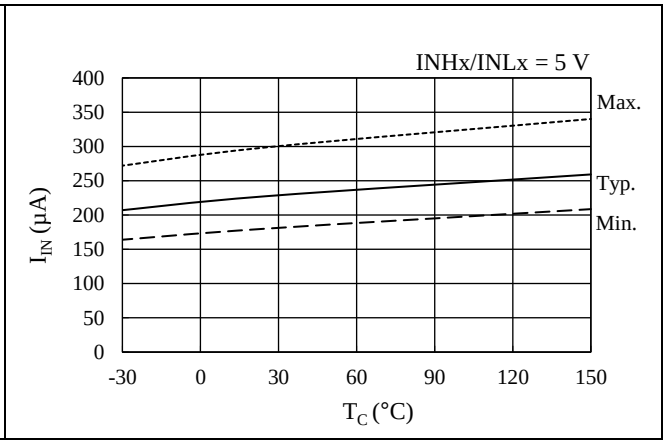


Figure 14-17. Input Current at High Level (HINx or LINx), I_{IN} vs. T_C

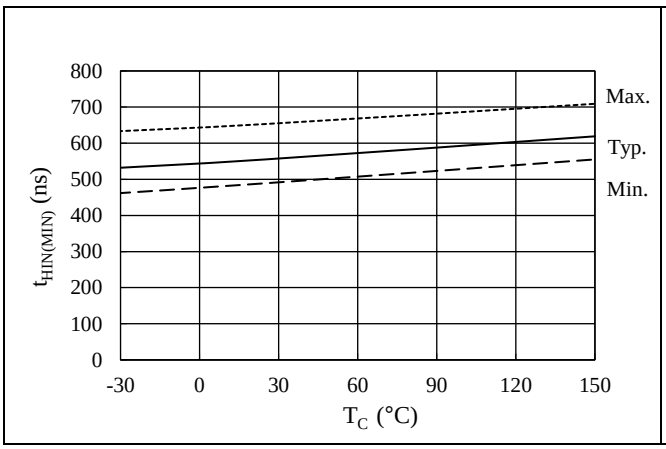


Figure 14-18. High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)

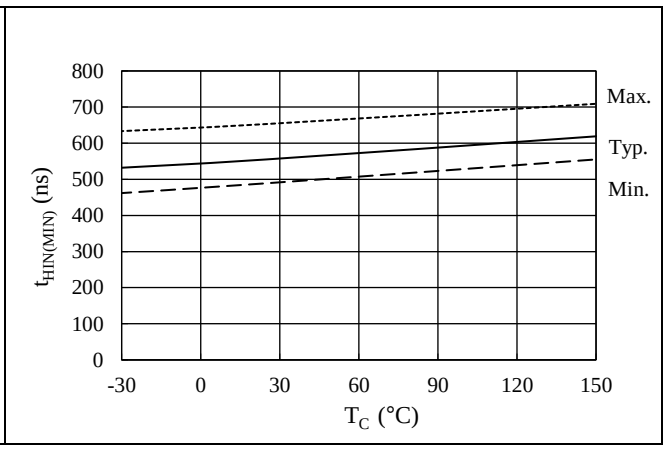


Figure 14-19. Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)

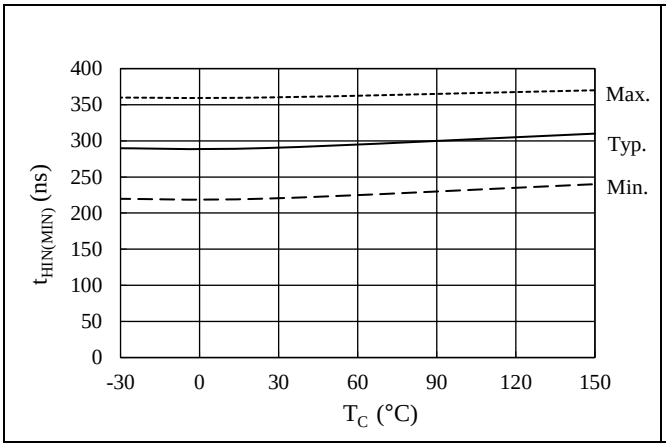


Figure 14-20. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

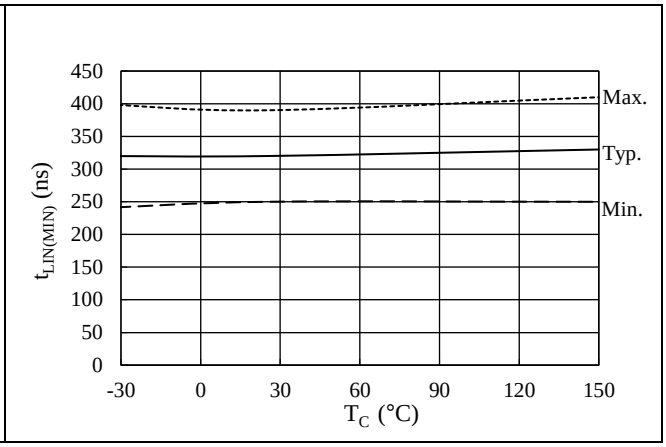


Figure 14-21. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

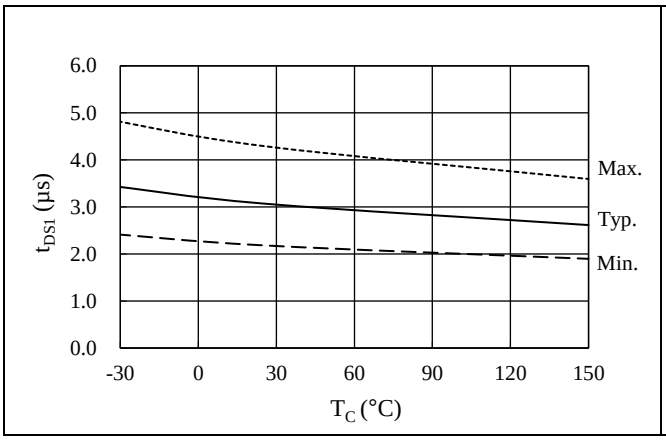


Figure 14-22. SD1 Pin Filtering Time vs. T_C

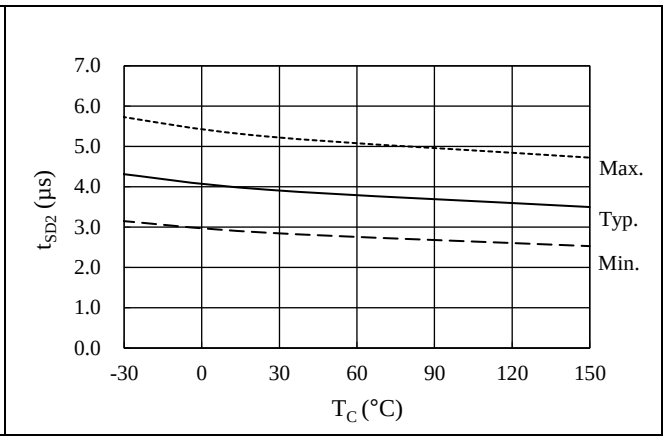


Figure 14-23. SD2 Pin Filtering Time vs. T_C

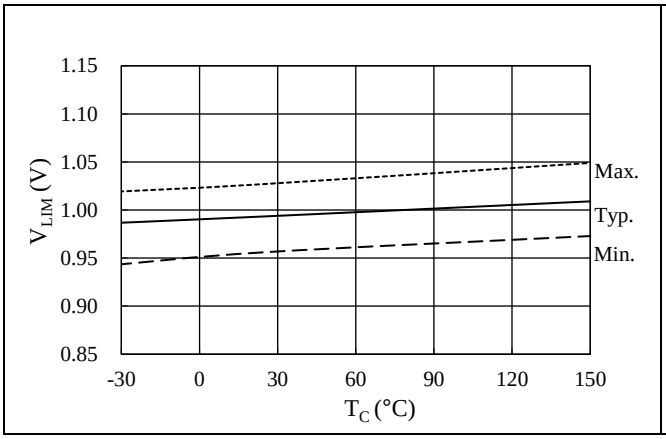


Figure 14-24. Current Limit Reference Voltage, V_{LIM} vs. T_C

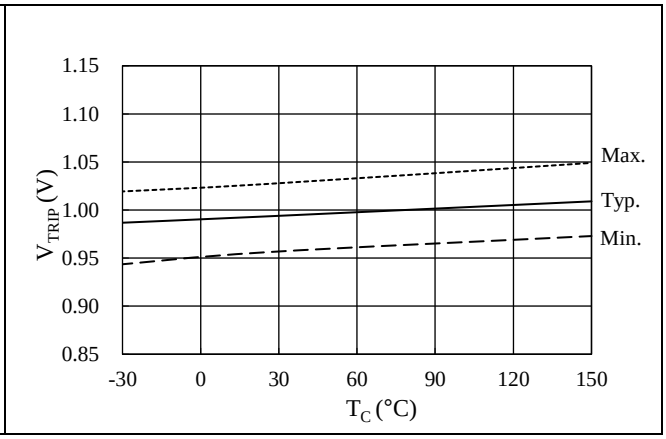


Figure 14-25. OCP Threshold Voltage, V_{TRIP} vs. T_C

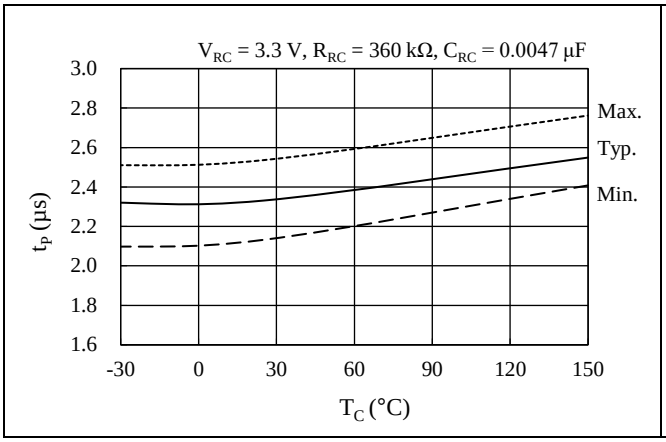


Figure 14-26. OCP Hold Time, t_P vs. T_C

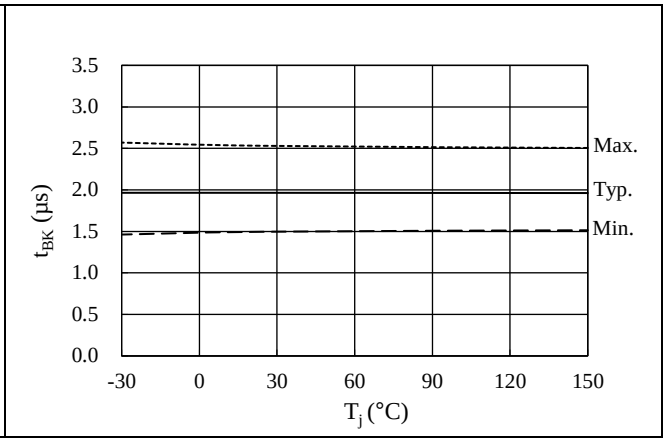


Figure 14-27. OCP Blanking Time, $t_{BK(OCP)}$ vs. T_C;
Current Limit Blanking Time, $t_{BK(OCL)}$ vs. T_C

14.3 Performance Curves of Output Parts

14.3.1 Output Transistor Performance Curves

14.3.1.1. SLA6868MH

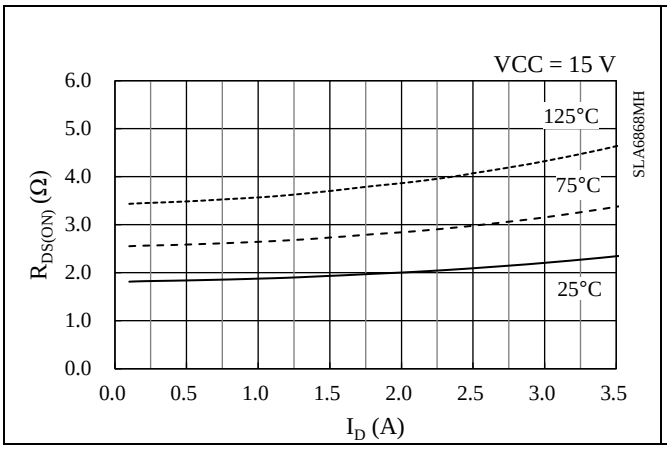


Figure 14-28. Power MOSFET $R_{DS(ON)}$ vs. I_D

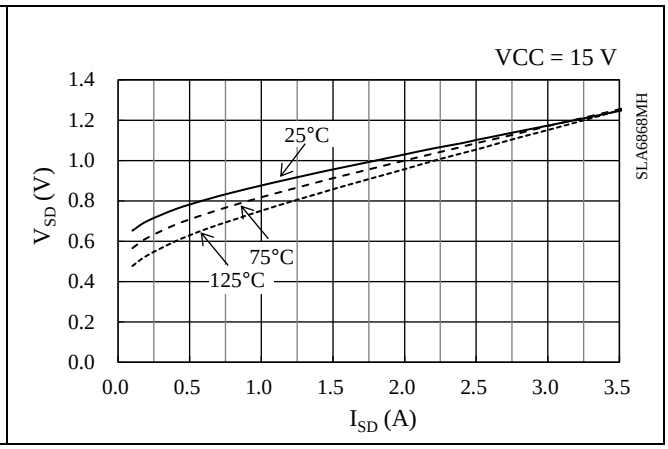


Figure 14-29. Power MOSFET V_{SD} vs. I_{SD}

14.3.1.2. SLA6870MH

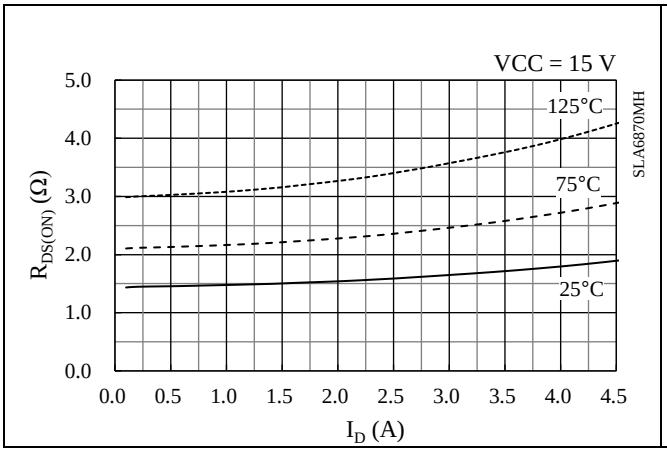


Figure 14-30. Power MOSFET $R_{DS(ON)}$ vs. I_D

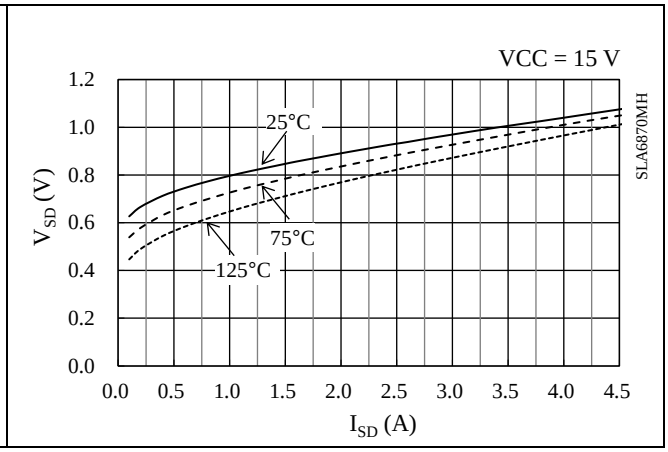


Figure 14-31. Power MOSFET V_{SD} vs. I_{SD}

14.3.2 Switching Losses

Conditions: VBBx pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

14.3.2.1. SLA6868MH

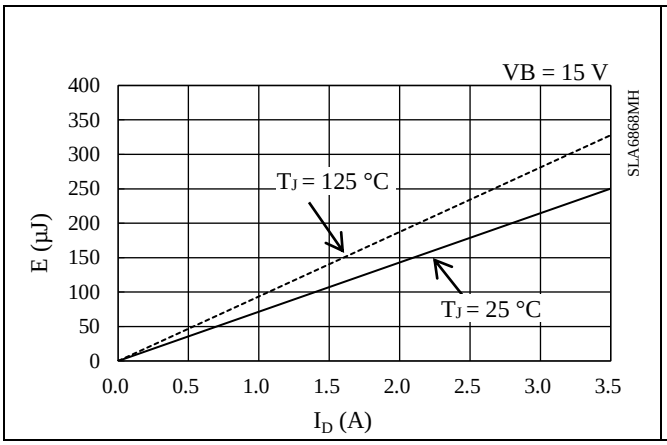


Figure 14-32. High-side Switching Loss

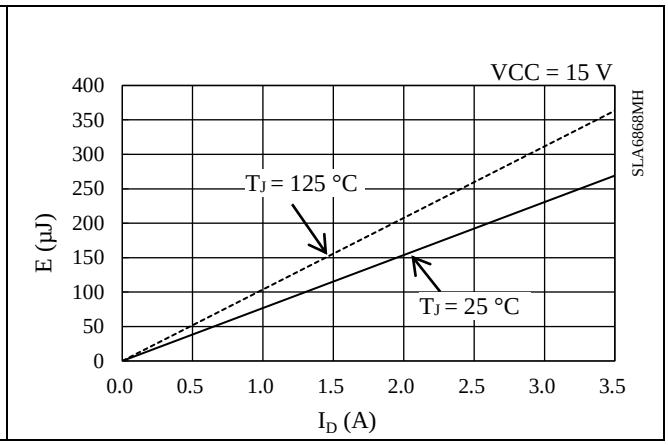


Figure 14-33. Low-side Switching Loss

14.3.2.2. SLA6870MH

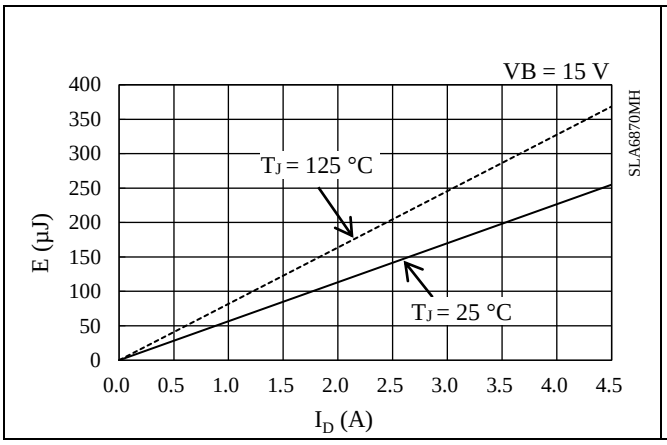


Figure 14-34. High-side Switching Loss

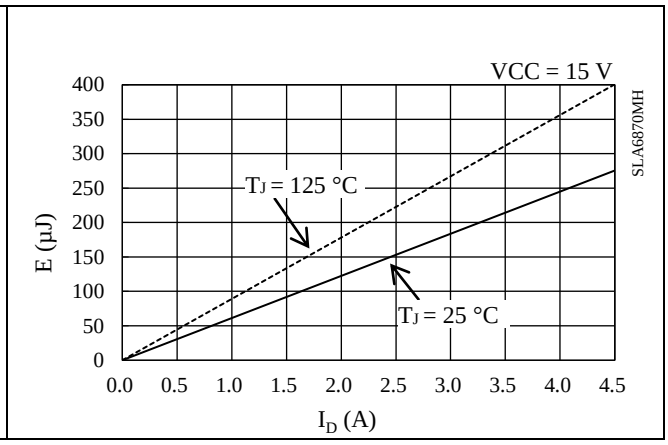


Figure 14-35. Low-side Switching Loss

14.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $R_{DS(ON)}$ or $V_{CE(SAT)}$, and typical switching losses.

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

14.4.1 SLA6868MH

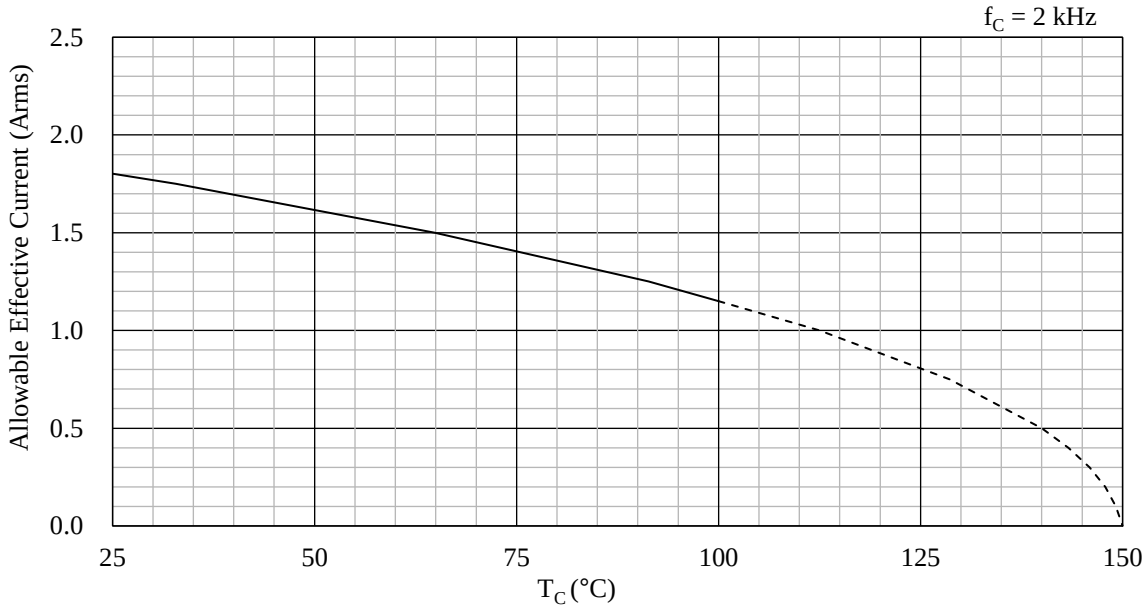


Figure 14-36. Allowable Effective Current (f_C = 2 kHz): SLA6868MH

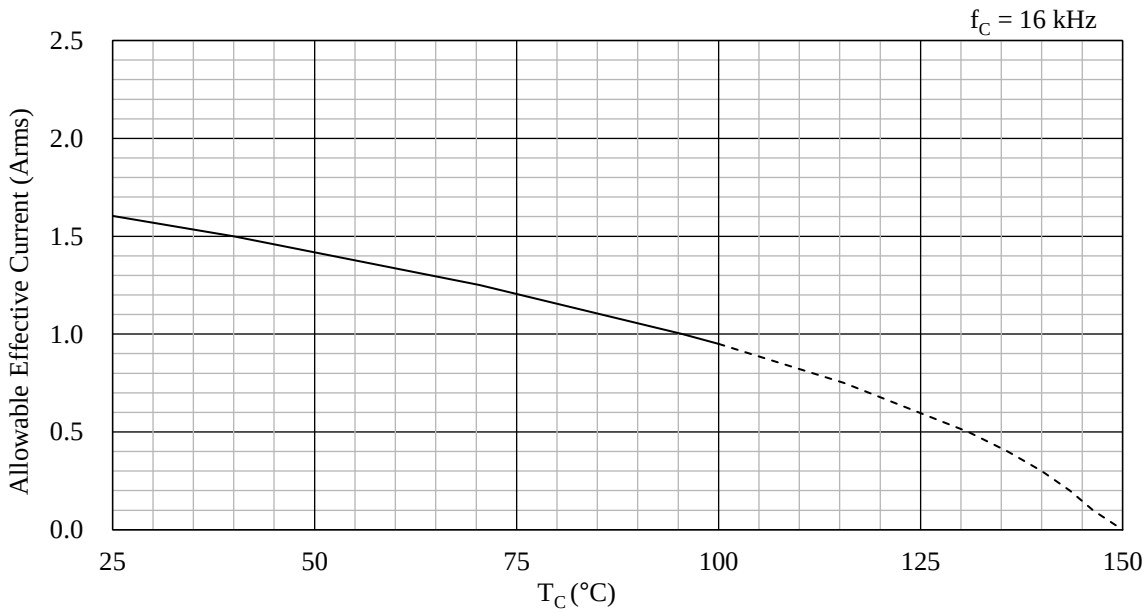


Figure 14-37. Allowable Effective Current (f_C = 16 kHz): SLA6868MH

14.4.2 SLA6870MH

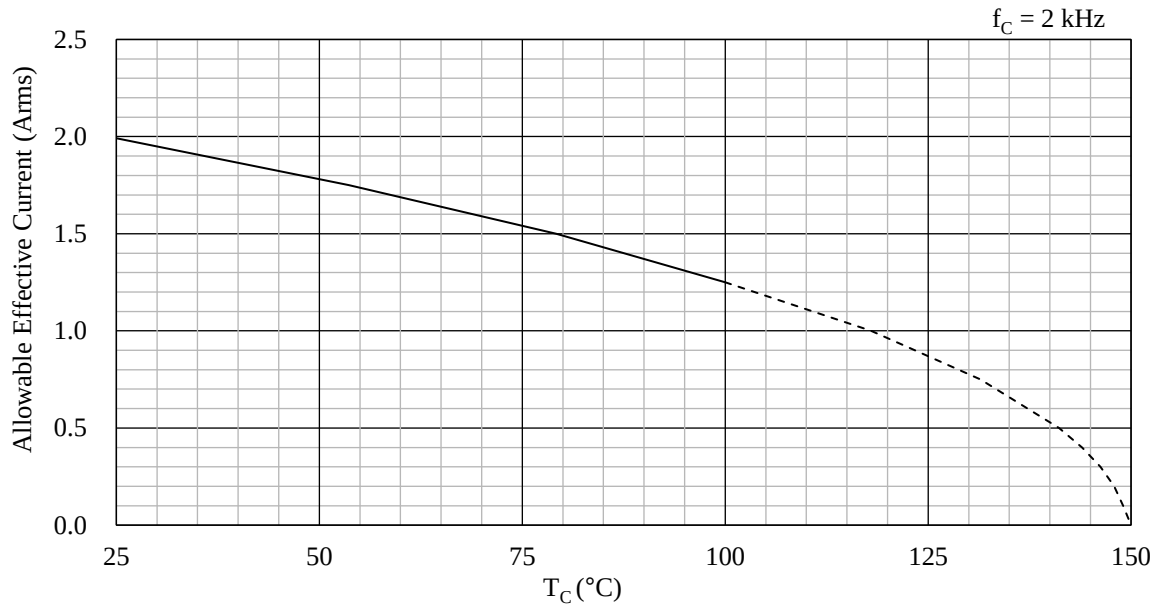


Figure 14-38. Allowable Effective Current (f_C = 2 kHz): SLA6870MH

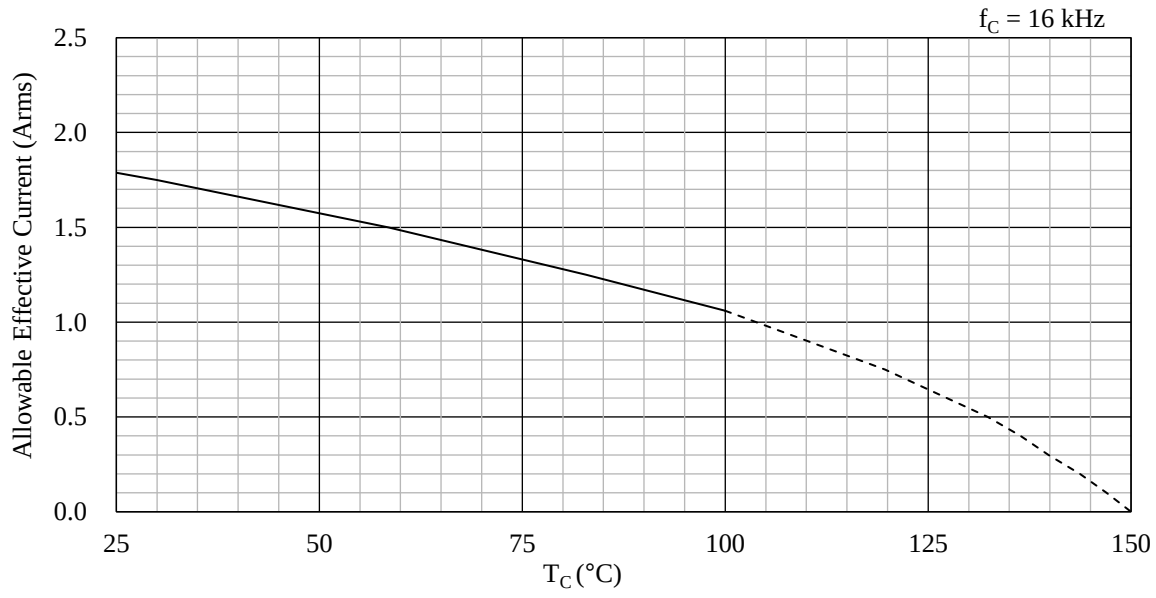


Figure 14-39. Allowable Effective Current (f_C = 16 kHz): SLA6870MH

15. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an IC from the devices listed in this document.

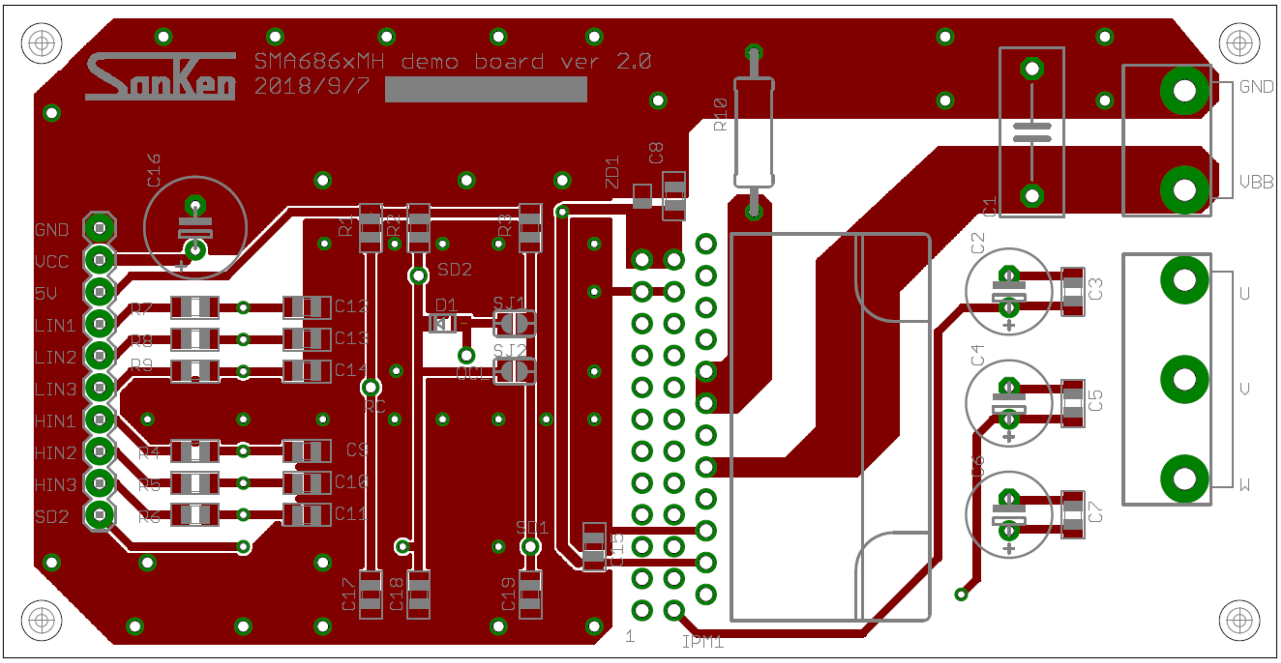


Figure 15-1. Top View

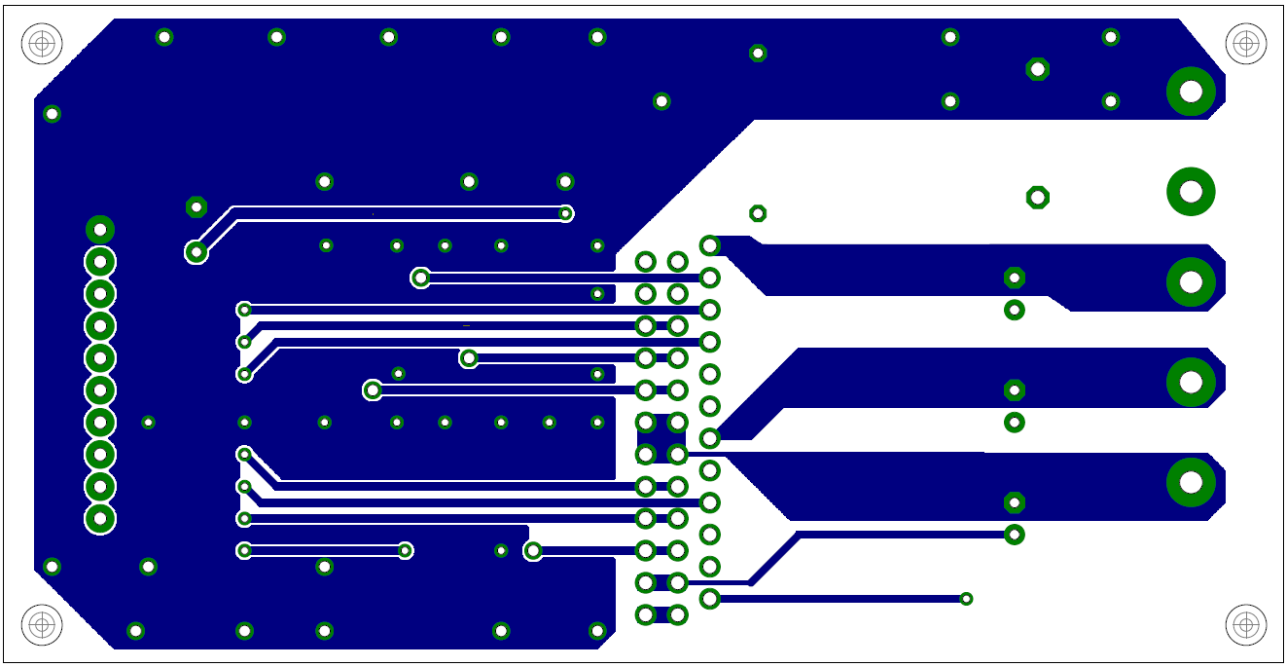


Figure 15-2. Bottom View

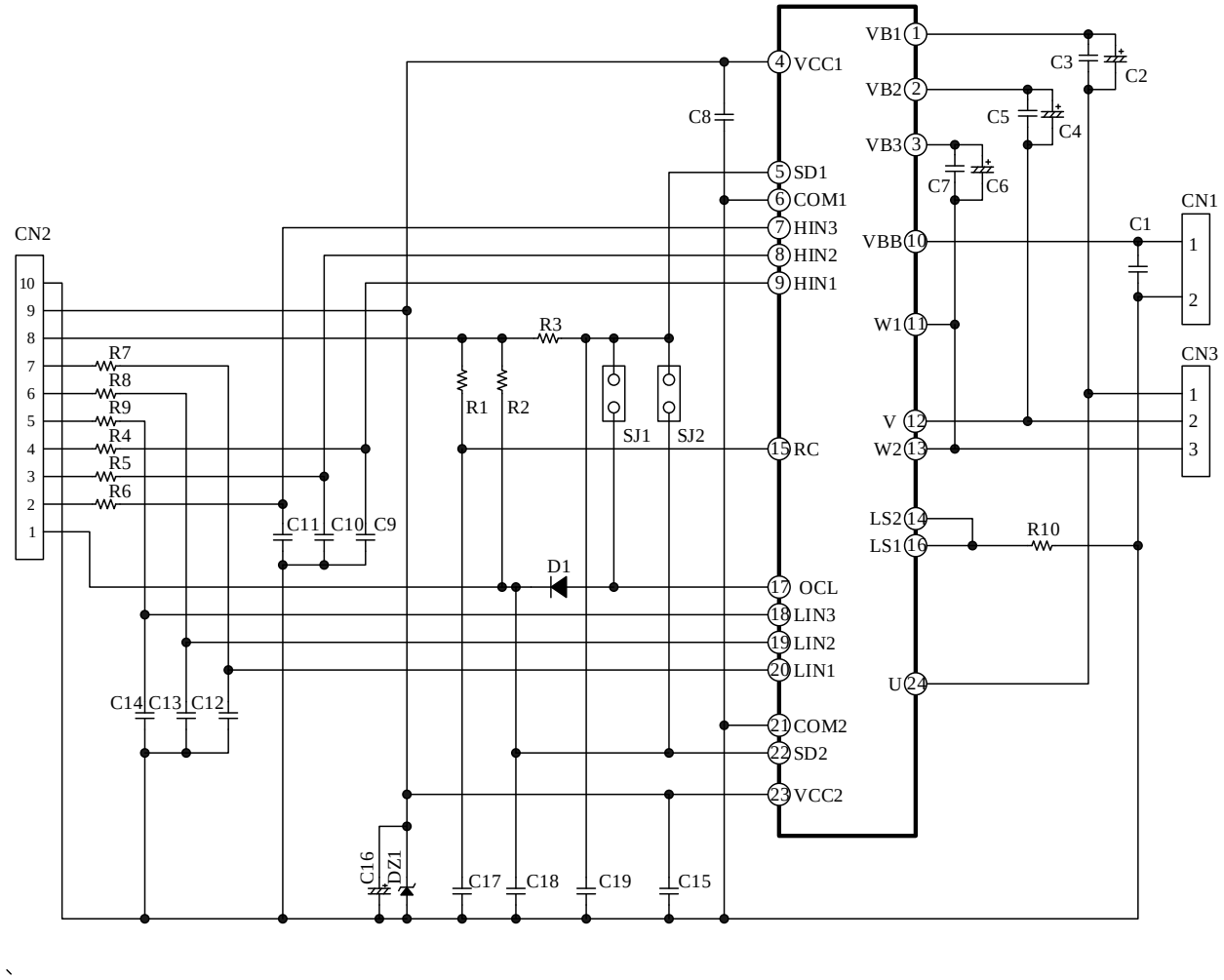


Figure15-3. Circuit Diagram of PCB Pattern Layout Example

16. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used. The SD1-OCL pin connection allows the IC to turn off the high-side transistors at OCL activation (see Section 11.3.4).

- **Motor Driver Specifications**

IC	SLA6870MH
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	300 W

- **Circuit Diagram**

See Figure15-3.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	定格
C1	Film	0.1 µF, 400 V	D1	General-Purpose Rectifier	7 V, 200 mA; $V_F \leq 1.2$ V (I_F = 5 mA, −20 to 125 °C)
C2	Electrolytic	47 µF, 50 V	R1	General	330 kΩ, 1/8 W
C3	Ceramic	0.1 µF, 50 V	R2	General	3.3 kΩ, 1/8 W
C4	Electrolytic	47 µF, 50 V	R3	General	3.3 kΩ, 1/8 W
C5	Ceramic	0.1 µF, 50 V	R4	General	1 kΩ, 1/8 W
C6	Electrolytic	47 µF, 50 V	R5	General	1 kΩ, 1/8 W
C7	Ceramic	0.1 µF, 50 V	R6	General	1 kΩ, 1/8 W
C8	Ceramic	0.1 µF, 50 V	R7	General	1 kΩ, 1/8 W
C9	Ceramic	100 pF, 50 V	R8	General	1 kΩ, 1/8 W
C10	Ceramic	100 pF, 50 V	R9	General	1 kΩ, 1/8 W
C11	Ceramic	100 pF, 50 V	R10(1)	Metal plate	0.24Ω, 2 W
C12	Ceramic	100 pF, 50 V	ZD1	Zener diode	V_Z = 21 V (max.)
C13	Ceramic	100 pF, 50 V	IPM1	IC	SLA6870MH
C14	Ceramic	100 pF, 50 V	SJ1(2)	Jumper	
C15	Ceramic	0.1 µF, 50 V	SJ2(3)	Jumper	
C16	Electrolytic	47 µF, 50 V	CN1	Pin header	Equiv. to B2P3-VH
C17	Ceramic	4700 pF, 50 V	CN2	Connector	Equiv. to MA10-1
C18	Ceramic	0.01 µF, 50 V	CN3	Pin header	Equiv. to B2P5-VH
C19	Ceramic	0.01 µF, 50 V			

(1) Refers to a part that requires adjustment based on operation performance in an actual application.
(2) When connecting the OCL pin to the SD1 pin, set SJ1 = short, SJ2 = open, and insert D1.
When not connecting the OCL pin to the SD1 pin, set SJ1 = open, SJ2 = short, and D1 = open.

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