
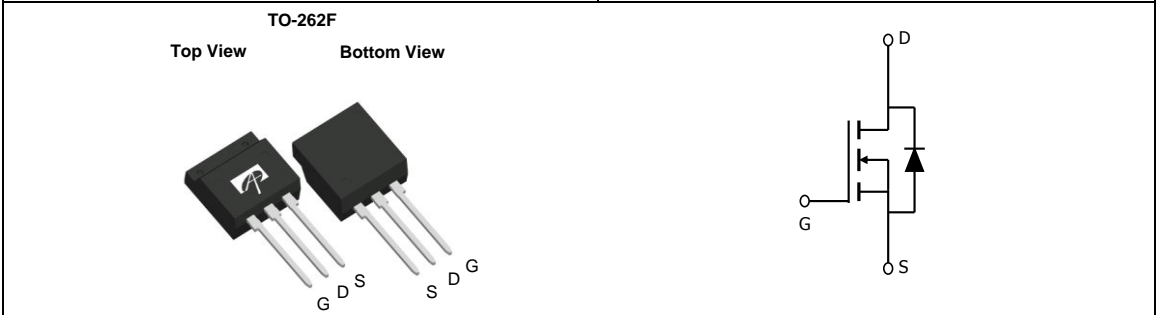


<p>General Description</p> <ul style="list-style-type: none"> Proprietary αMOS5™ technology Low $R_{DS(ON)}$ Optimized switching parameters for better EMI performance Enhanced body diode for robustness and fast reverse recovery <p>Applications</p> <ul style="list-style-type: none"> PFC and PWM stages (Flyback, LLC) of Adapter, PC Silverbox, Server, Gaming Power Supply, Industrial, TV, Lighting 	<p>Product Summary</p> <table border="0"> <tr> <td>$V_{DS} @ T_{j,max}$</td> <td>800V</td> </tr> <tr> <td>I_{DM}</td> <td>44A</td> </tr> <tr> <td>$R_{DS(ON),max}$</td> <td>< 0.45Ω</td> </tr> <tr> <td>$Q_{g,typ}$</td> <td>20nC</td> </tr> <tr> <td>$E_{oss} @ 400V$</td> <td>2.5μJ</td> </tr> </table> <p>100% UIS Tested 100% R_g Tested</p> 	$V_{DS} @ T_{j,max}$	800V	I_{DM}	44A	$R_{DS(ON),max}$	< 0.45 Ω	$Q_{g,typ}$	20nC	$E_{oss} @ 400V$	2.5 μ J
$V_{DS} @ T_{j,max}$	800V										
I_{DM}	44A										
$R_{DS(ON),max}$	< 0.45 Ω										
$Q_{g,typ}$	20nC										
$E_{oss} @ 400V$	2.5 μ J										



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOWF450A70	TO262F	Tube	1000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	700	V
Gate-Source Voltage	V_{GS}	± 20	V
Gate-Source Voltage (dynamic) AC($f > 1\text{Hz}$)	V_{GS}	± 30	V
Continuous Drain Current	$T_C=25^\circ\text{C}$	11*	A
	$T_C=100^\circ\text{C}$	7.1*	
Pulsed Drain Current ^C	I_{DM}	44	
Avalanche Current ^C	I_{AR}	2.5	A
Repetitive avalanche energy ^C	E_{AR}	3.1	mJ
Single pulsed avalanche energy ^G	E_{AS}	30	mJ
MOSFET dv/dt ruggedness	dv/dt	100	V/ns
Peak diode recovery dv/dt		20	
Power Dissipation ^B	$T_C=25^\circ\text{C}$	26	W
	Derate above 25°C	0.2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

Thermal Characteristics				
Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	55	65	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.9	4.8	$^\circ\text{C}/\text{W}$

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	700			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		800		
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.6		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =700V, V _{GS} =0V			1	μA
		V _{DS} =560V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	2.4	3	3.6	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =2.3A		0.405	0.45	Ω
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =2.3A		5		S
V _{SD}	Diode Forward Voltage	I _S =2.3A, V _{GS} =0V		0.8	1.2	V
I _S	Maximum Body-Diode Continuous Current				11	A
I _{SM}	Maximum Body-Diode Pulsed Current ^C				44	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		1115		pF
C _{oss}	Output Capacitance			30		pF
C _{o(er)}	Effective output capacitance, energy related ^H	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz		28		pF
C _{o(tr)}	Effective output capacitance, time related ^I			122		pF
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		2		pF
R _g	Gate resistance	f=1MHz		6.7		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =5.5A		20		nC
Q _{gs}	Gate Source Charge			6.8		nC
Q _{gd}	Gate Drain Charge			5.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =400V, I _D =5.5A, R _G =5Ω		25		ns
t _r	Turn-On Rise Time			15		ns
t _{D(off)}	Turn-Off DelayTime			45		ns
t _f	Turn-Off Fall Time			20		ns
t _{rr}	Body Diode Reverse Recovery Time			275		ns
I _{rm}	Peak Reverse Recovery Current	I _F =5.5A, di/dt=100A/μs, V _{DS} =400V		21		A
Q _{rr}	Body Diode Reverse Recovery Charge			3.5		μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. This is the absolute maximum rating. Parts are 100% tested at T_J=25° C, L=60mH, I_{AS}=1A, V_{DD}=150V, R_G=25Ω.

H. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

I. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

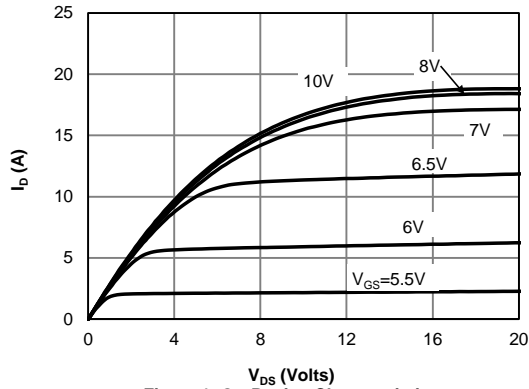


Figure 1: On-Region Characteristics

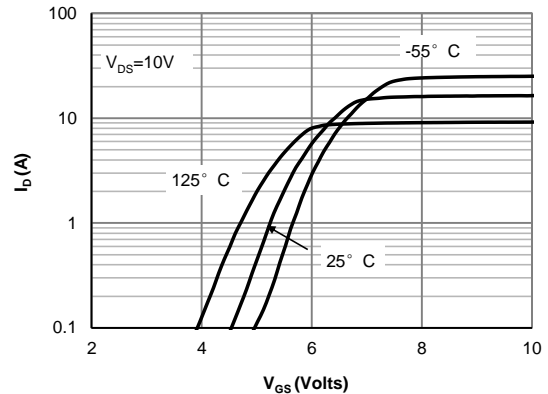


Figure 2: Transfer Characteristics

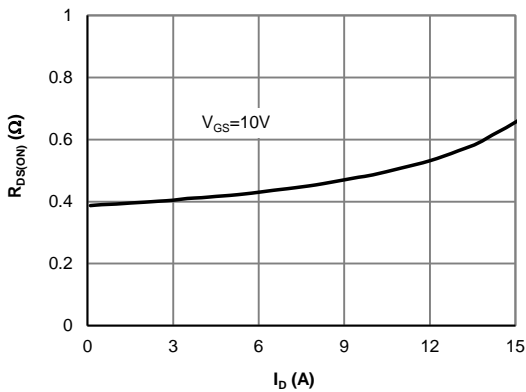


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

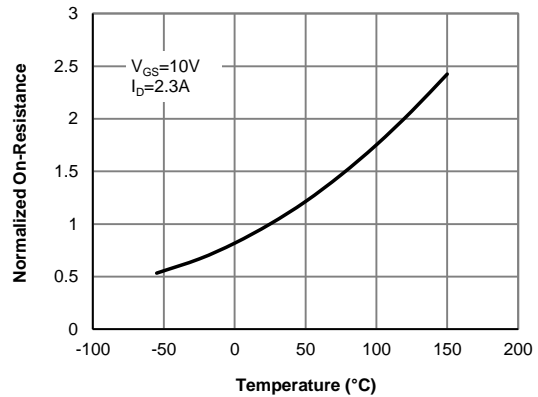


Figure 4: On-Resistance vs. Junction Temperature

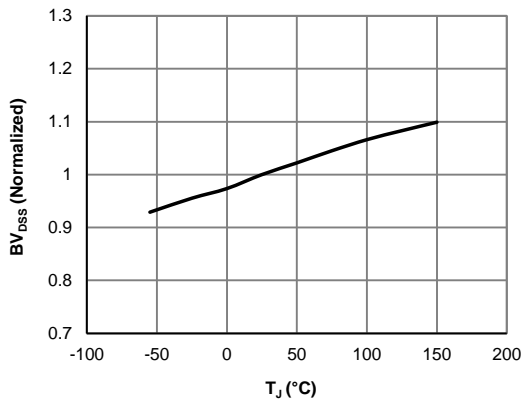


Figure 5: Break Down vs. Junction Temperature

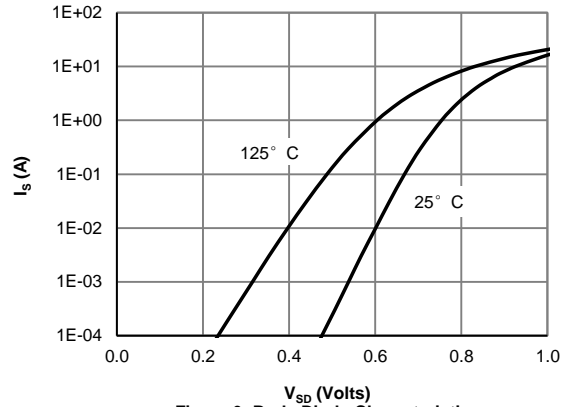


Figure 6: Body-Diode Characteristics

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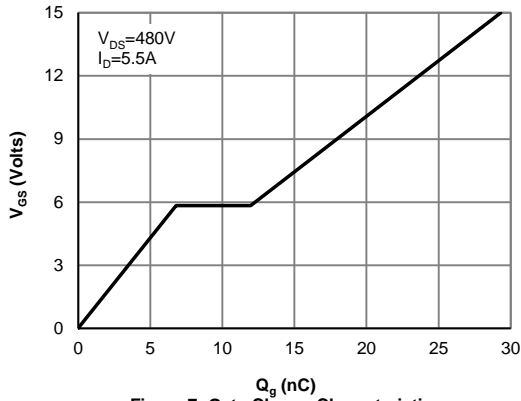


Figure 7: Gate-Charge Characteristics

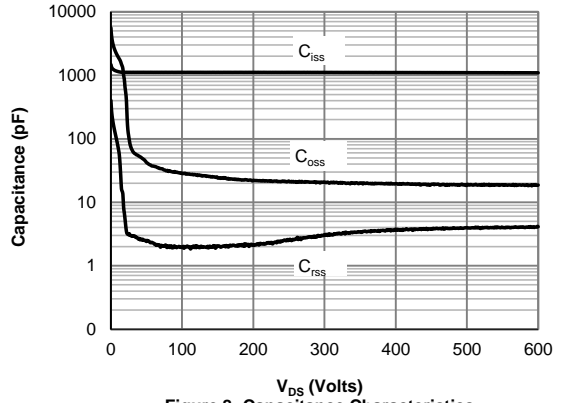


Figure 8: Capacitance Characteristics

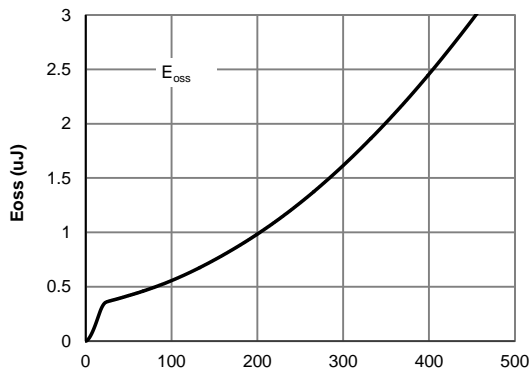


Figure 9: Coss stored Energy

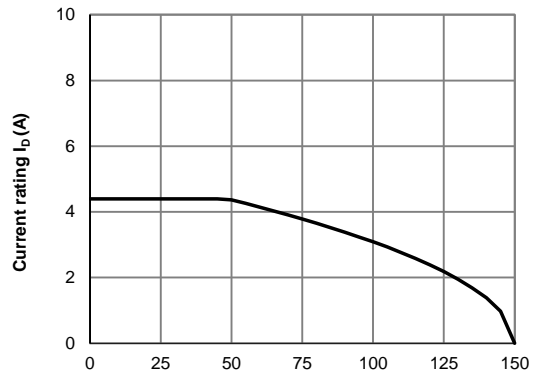


Figure 10: Current De-rating (Note F)

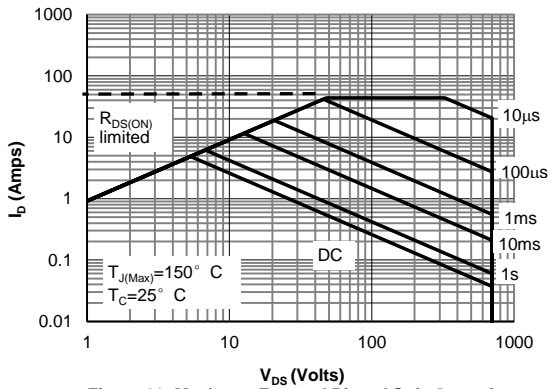


Figure 11: Maximum Forward Biased Safe Operating Area (Note F)

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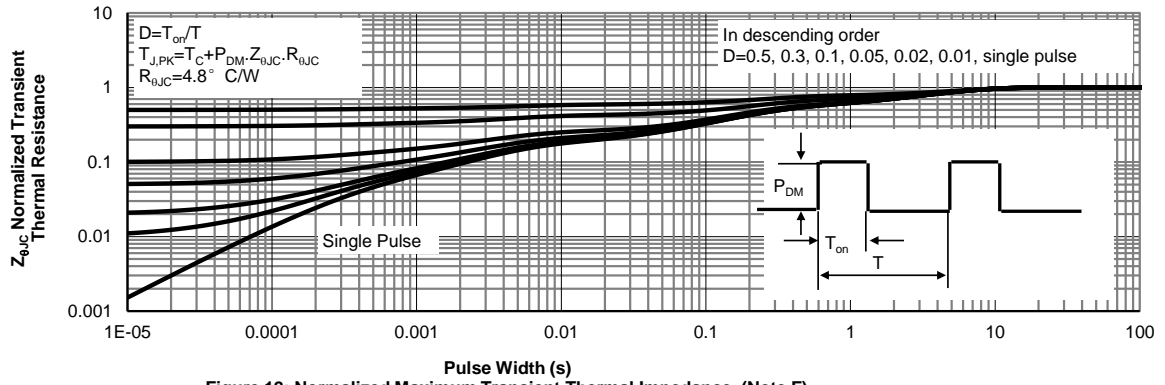
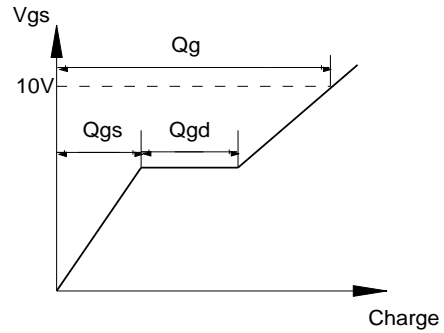
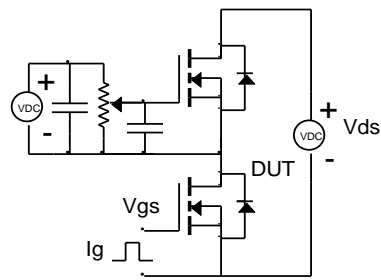
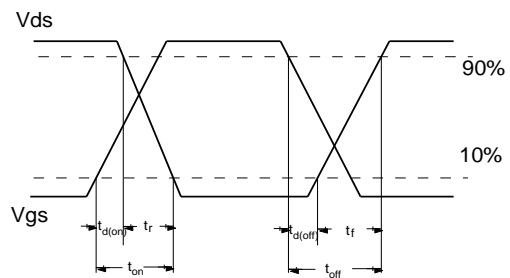
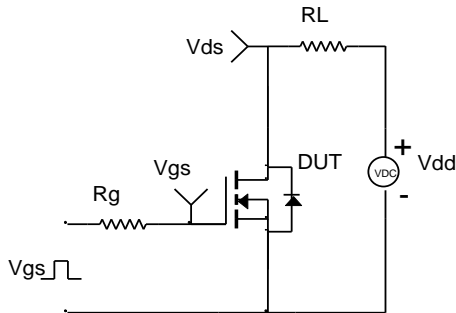


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

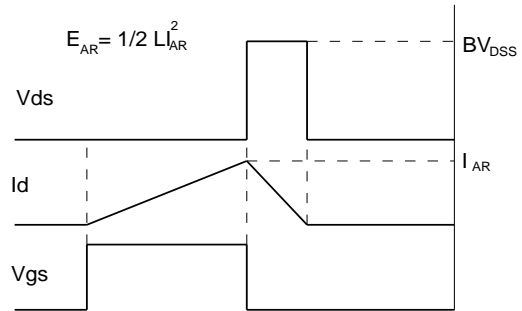
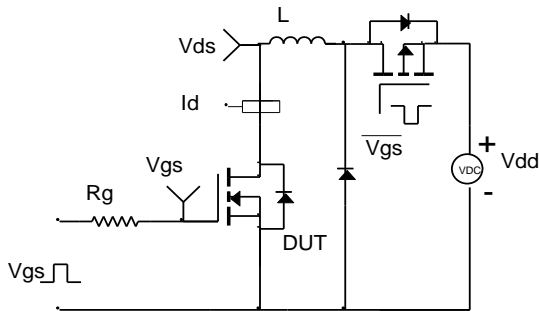
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

