LM98519 10-bit 65 MSPS 6 Channel Imaging Signal Processor

1 Features

- 3.3-V Single Supply Operation
- CDS or S/H Processing with Negative Input Signal Polarity
- 32.5-MHz Channel Rate
- Enhanced ESD Protection on Host Interface Pins: SHP, SHD, CLPIN, BLKCLP, AGC_ONB, MCLK, RESETB, SENB, SCLK, SDI, SDO
- Low Power CMOS Design
- 4-Wire Serial interface
- 2 Channel Symmetrical Architecture
- Independent Gain and Offset Correction for Each Channel
- Digital Black Level Calibration for Each Channel
- Digital White Level Calibration for Each Channel
- Programmable Input Clamp

2 Applications

- Digital Color Copiers
- Scanners
- Image Processing Polarity applications
- **Key Specifications**
  - Maximum Input Level:
    - 1.19 Vp-p (CDS Gain = 1.0)
    - 0.58 Vp-p (CDS Gain = 2.1)
  - Input Sample Rate:
    - 5 to 32.5 MSPS – 6ch Mode
    - 10 to 32.5 MSPS – 3ch Mode
  - PGA Gain Range: 1x to 10x (0 to 20 dB)
  - CDS/SH Gain Settings: 1x or 2.1x
  - Total Channel Gain: 1x to 20x (0 to 26 dB)
  - PGA Gain Resolution: 8 Bits – Analog
  - ADC Resolution: 10 Bits
  - ADC Sampling Rate: 10 to 65 MSPS
  - SNR: 67.5 dB (Gain = 1x)
  - Offset DAC Range:
    - ±111 mV or ±60 mV – FDAC
    - ±277 mV – CDAC
  - Offset DAC Resolution:
    - ±10 Bits – FDAC
    - ±4 Bits – CDAC
  - Supply Voltage: 3.0 V to 3.6 V
  - Power Dissipation: 1.04 W (Typical)

3 Description

The LM98519 is a fully integrated, high performance 10-Bit, 65 MSPS signal processing solution for digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative six channel architecture utilizing Correlated Double Sampling (CDS), or Sample and Hold (SH) type sampling. 1x or 2x gain settings are available in the CDS/SH input stage. Each channel has a dedicated 1x to 10x (8 bit) PGA that allows accurate gain adjustment of each channel. The Digital White Level auto calibration loop can automatically set the PGA value to achieve a selected white target level. Each channel also has a ±4-bit coarse and ±10-bit fine analog offset correction DAC that allows offset correction before the sample-and-hold amplifier. These correction values can be controlled by an automated Digital Black Level correction loop. The PGA and offset DACs for each channel are programmed independently allowing unique values of gain and offset for each of the six channels. A 2-to-1 multiplexing scheme routes the signals to three 65-MHz high performance ADCs. The fully differential processing channels achieve exceptional noise immunity, having a very low noise floor of -67.5 dB. The 10-bit analog-to-digital converters have excellent dynamic performance making the LM98519 transparent in the image reproduction chain.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM98519	TQFP (80)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

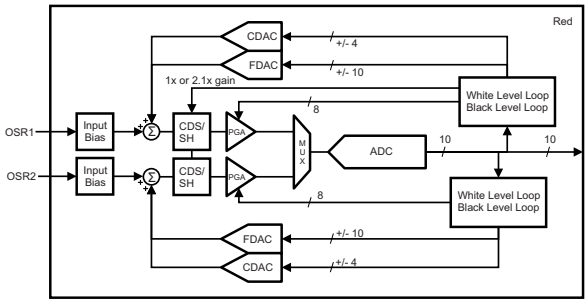


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C — **Page**

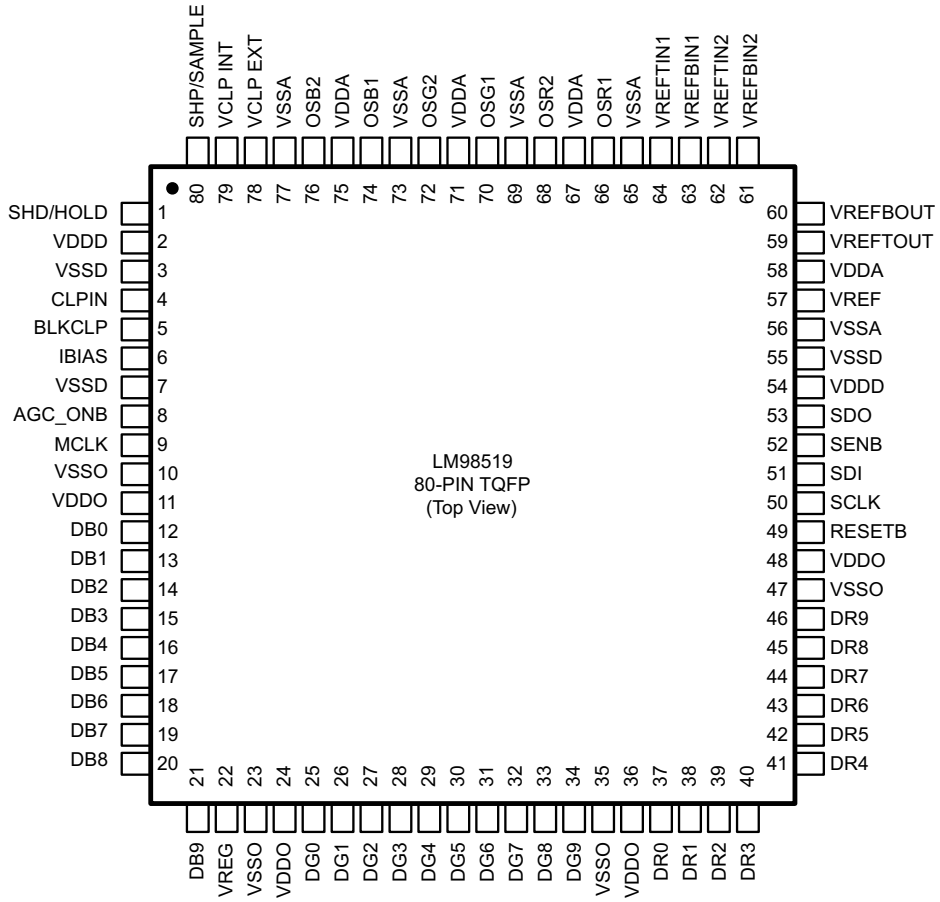
- Added, updated, or revised the following sections: Device Information Table, *Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1
- Changed 68 db to 67.5 db in *Description* section. ... 1

Changes from Revision A (April 2013) to Revision B — **Page**

- Changed layout of National data sheet to TI format ... 1

5 Pin Configuration and Functions

80-Pin
PFC Package
(Top View)



Pin Functions[1]

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	SHD/ HOLD	DI	Data Clamp Pulse
2, 54	VDDD	PI	Digital Power Supply
3, 7, 55	VSSD	PI	Digital Power Supply Ground
4	CLPIN	DI	Input Pulse That Invokes an Input Clamp Switch
5	BLKCLP	DI	Input Pulse that Invokes a Black Clamp Calibration Loop Pulldown 108kΩ
6	IBIAS	AO	Optional IBIAS resistor connection. To minimize device to device power consumption variation, connect an 11k Ohm 1% resistor to VSSA. If no resistor is used, the internal bias and power supply currents will be subject to normal device to device variation.
8	AGC_ONB	DI	Input Pulse that Invokes the White Calibration Loop. Tie high to disable White Clamp. Pulse Low to initiate White Clamp. (Active Low) Pulldown 108kΩ

(1) A – Analog, D – Digital, P – Power, I – Input, O – Output, PD – Pull-down resistor to VSSD, PU – Pull-up resistor to VDDD

Pin Functions[1] (continued)

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
9	MCLK	DI	Master Clock Input
10, 23, 35, 47	VSSO	PI	Output Driver Power Supply Ground
11, 24, 36, 48	VDDO	PI	Output Driver Power Supply
12-21	DB0–DB9	DO	Bit 0 – Bit 9 of the Blue Channel
22	VREG	PO	Decoupling connection for VREG – Internal Voltage for Logic
25-34	DG0–DG9	DO	Bit 0 – Bit 9 of the Green Channel
37-46	DR0–DG9	DO	Bit 0 – Bit 9 of the Red Channel
39	DR2 (TESTO0)	DO	Bit 2 of Red Channel Data or TESTO0 timing monitor output (Timing monitor output selected by setting Register 0x00, Bit 1 = 1)
40	DR3 (TESTO1)	DO	Bit 3 of Red Channel Data or TESTO1 timing monitor output (Timing monitor output selected by setting Register 0x00, Bit 1 = 1)
49	RESETB	DI	Master Reset Input (Active Low) Pulldown 108 kΩ
50	SCLK	DI	Serial Clock for the 4-wire Serial Interface
51	SDI	DI	Serial Input Data for the 4-wire Serial Interface
52	SENB	DI	Serial Enable (Active Low) for the 4-wire Serial Interface Pulldown 108 kΩ
53	SDO	DO	Serial Output Data for the 4-wire Serial Interface
56, 65, 69, 73, 77	VSSA	PI	Analog Power Supply Ground
57	VREF	AO	Reference Voltage Bypass
58, 67, 71, 75	VDDA	PI	Analog Power Supply
59	VREFTOUT	AO	Top Reference Bypass. Connect to bypass capacitors (see applications section) and VREFTINx. – Approx. 2.23 V output[2]
60	VREFBOUT	AO	Bottom Reference Bypass. Connect to bypass capacitors (see applications section) and VREFBINx. – Approx. 0.98 V output[2]
61	VREFBIN2	AI	Bottom Reference Input Voltage for the ADC. Connect to VREFBOUT.
62	VREFTIN2	AI	Top Reference Input Voltage for the ADC. Connect to VREFTOUT.
63	VREFBIN1	AI	Bottom Reference Input Voltage for the AFE. Connect to VREFBOUT.
64	VREFTIN1	AI	Top Reference Input Voltage for the AFE. Connect to VREFTOUT.
66	OSR1	AI	Input Voltage 1 for the Red Channel
68	OSR2	AI	Input Voltage 2 for the Red Channel
70	OSG1	AI	Input Voltage 1 for the Green Channel
72	OSG2	AI	Input Voltage 2 for the Green Channel
74	OSB1	AI	Input Voltage 1 for the Blue Channel
76	OSB2	AI	Input Voltage 2 for the Blue Channel
78	VCLP_EXT	AI	External Clamp Voltage
79	VCLP_INT	AO	Internally Supplied V-Clamp Voltage
80	SHP/ SAMPLE	DI	Pedestal Clamp Pulse

(2) Voltages provided for debugging only. Not an ensured specification.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply Voltage	–0.3	4.2	V
Voltage at any Pin (except VREG)	–0.3	VDDD + 0.3	V
Voltage at VREG Pin	–0.3	2.1	V
Input Current at any Pin(2)		±25	mA
Package Input Current(2)		±50	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When the input voltage (VIN) at any pin exceeds the power supplies [VIN < (GND – 0.3 V) or VIN > (VDDA + 0.3 V)], the DC current at that pin should be limited to ±25 mA. The 50 mA DC maximum package input current means that a maximum of two pins can simultaneously have input currents that equal 25 mA.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)		2500	V
		Human body model (HBM, rated for the following pins only: SHP, SHD, CLPIN, BLKCLP, AGC_ONB, MCLK, RESETB, SENB, SCLK, SDI, SDO).(3)		7500	
		Machine model (MM)		250	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(4)		1000	

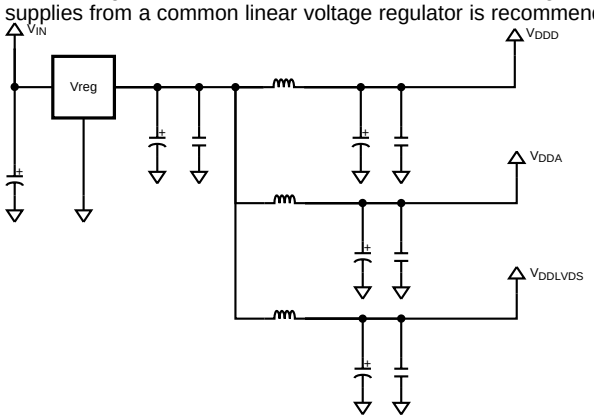
(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device. Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin. Charged device model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 2500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 7500-V HBM allows safe manufacturing with a standard ESD control process
(4) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 1000-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Analog Supply Voltage Range		3.0		3.6	V
Digital Supply Voltage Range		3.0		3.6	V
Output Supply Voltage Range		2.25		VDDD	V
DC Power Supply Voltage Relationships(1)	VDDD ≥ VDDA, VDDD ≥ VDDO				
Voltage at any Digital I/O Pin		0		VDDD	V
Voltage at any Analog Input Pin		0		VDDA	V
Voltage at any Data Output Pin		0		VDDO	V
Specified Temperature Range		0		70	°C

(1) Static voltage levels on VDDD must be at the same voltage or slightly higher than VDDO or VDDA. Therefore, driving all three power supplies from a common linear voltage regulator is recommended. Please see the following diagram.



6.4 Thermal Information

THERMAL METRIC(1)		LM98519 PFC 80 TERMINALS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

The following specifications apply for VDDA = VDDD = VDDO = 3.3 V; F_{MCLK} = 65 Ms/s and T_A =+25°C unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits apply for T_A =+25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC/AFE						
	Resolution	No missing codes			10	bits
	INL	Gain = 1x	**–2.4**	–0.75 to 0.9	**1.95**	lsb
		Gain = 6x		–1.85 to 2.0		
	DNL	Gain = 1x	**–0.99**	–0.55 to 0.7	**1.5**	lsb
		Gain = 6x		–0.65 to 0.85		
	Noise Floor (SNR)(1)	Gain = 1x		67.5		dB
		Gain = 6x		55		
	Analog Input Range	Peak-to-peak, CDS gain = 1x	**1.12**	1.19	**1.29**	V
		Peak-to-peak, CDS gain = 2.1x	**0.55**	0.58	**0.62**	
	Analog Input Leakage (Osx inputs)	GND < Vin < VDDA Source Follower Enabled – OVP off	**–330**	±25	**140**	nA
R_{CLAMP}	Input Clamp Impedance	From bench and design		43		Ω
	Conversion Ratio	CDS/SH Gain Setting = 1x PGA gain setting = Min (Typical values by design)(2)	**0.78**	0.85	**0.92**	lsb/mV
	Conversion Ratio Color to Color Error			0.26%		
	Conversion Ratio Ch1 to Ch2 Error			0.13%		
	Crosstalk – Color to Color	R1,B1 to G1; R1,G1 to B1, etc. R2, B2, to G2; R2, G2, to B2, etc. Gain = 20x setting		0.8%		
	Crosstalk – Ch1 to Ch2	R1 to R2, R2 to R1, G1 to G2, G2 to G1, B1 to B2, B2 to B1 Gain = 20x setting		0.3%		
P_D	Active Mode Power Consumption	3.3 V		1041	**1271**	mW
I_{DDA}		3.3 V			**257**	mA
I_{DDD}		3.3 V			**58**	mA
I_{DDO}		3.3 V			**70**	mA
P_D	Power-Down Mode Power Consumption	3.3 V – MCLK Active		153	**201**	mW
PGA (8 bits) Gain = 283/(283-M)						
	PGA Gain Range(3)	Max Setting/Min Setting	**19.5**	20	**20.9**	dB
	PGA Max Stepsize	Largest PGA Step		0.3		dB
	PGA Monotonicity				**Monotonic**	
	PGA Error (Difference from ideal curve)			1.15%		
CDS/SH						
	CDS/SH Gain	Gain at 2x / Gain at 1x	**2**	2.1	**2.13**	V/V

(1) SNR = 20log(1024/Output Noise(lsb rms)) with input = DC
(2) For conversion ratio min/max, variation and error, Conversion ratio is: (Digital Max – Digital Min)/(Vin Max – Vin Min). Measured at gain setting of 1x
(3) PGA gain range is: [(ADC_OUT(PGA at 1111111111)) / (ADC_OUT(PGA at 0000000000))]

Electrical Characteristics (continued)

The following specifications apply for VDDA = VDDD = VDDO = 3.3 V; F_{MCLK} = 65 Ms/s and T_A =+25°C unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits apply for T_A =+25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET FDAC (±10 bits)						
	DAC Full Scale (input referred)	Large FDAC range	**102**	110.5	**120**	±mV
		Small FDAC range	**51**	59.5	**68**	
	DAC Monotonicity				**Monotonic**	
OFFSET CDAC (±4 bits)						
	DAC Full Scale (input referred)		**255**	277	**300**	±mV
	DAC Monotonicity				**Monotonic**	
LOGIC I/O DC PARAMETERS						
V_{IH}	Logic Input Voltage High SHP, SHD, CLPIN, BLKCLP, AGC_ONB, MCLK, SCLK, SDI, SENB		**2.0**			V
V_{IL}	Logic Input Voltage Low SHP, SHD, CLPIN, BLKCLP, AGC_ONB, MCLK, SCLK, SDI, SENB				**0.8**	
I_{IN}	Logic Input Leakage	Excludes AGC_ONB, BLKCLP, SENB, RESETB due to pull-ups or pull-downs on those pins	**–100**	65	**100**	nA
V_{OH}	Logic Output Voltage High	VDDD = 3.6 V, Iout = -0.5 mA	**3.3**	3.56		V
		VDDD = 3.0 V, Iout = -0.5 mA	**2.7**	2.9		
V_{OL}	Logic Output Voltage Low	VDDD = 3.6 V, Iout = 1.6 mA		0.11	**0.2**	V
		VDDD = 3.0 V, Iout = 1.6 mA		0.11	**0.2**	
V_{RES}	Power On Reset Threshold	From simulation	**1.18**	1.5		V
AFE/ADC TIMING						
f_{MCLK}	MCLK frequency	6 channel mode	**10**		**65**	MHz
		3 channel mode	**10**		**32.5**	
	MCLK Duty Cycle		**45%**		**55%**	
	Input Sampling Rate	6 Channel Mode	**5**		**32.5**	MS/s
		3 Channel Mode	**10**		**32.5**	
t_{RESET}	RESETB Pulse Width	MCLK Present Mode	**2**			t_{MCLK}
		MCLK Idle Mode	**50**			ns
t_{RESET_CLR}	RESETB Clear Time	MCLK Present Mode (ensured by design)			**3**	t_{MCLK}
		MCLK Idle Mode (ensured by design)			**10**	ns
t_{SHD}	SHP/SHD high period	Ensured by design	**8.2**			ns

Electrical Characteristics (continued)

The following specifications apply for VDDA = VDDD = VDDO = 3.3 V; F_{MCLK} = 65 Ms/s and T_A =+25°C unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits apply for T_A =+25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{MCS_MIN}	MCLK high to SAMPLE high (Minimum)(4)	SH3 Mode – ADC Rate MCLK		9	**13**	ns(5)
		SH2 Mode		10.5	**14.5**	
		SH1b Mode		2.4	**5**	
		CDSb Mode		1.8	**4**	
t_{HMC_MIN}	HOLD high to MCLK high (Minimum)(4)	SH3 Mode – ADC Rate MCLK		0.7	**3.5**	ns(5)
		SH2 Mode		–0.7	**3**	
		SH1b Mode		–2.1	**2**	
		CDS Mode		–3.1	**1**	
t_{MCH_MIN}	MCLK high to HOLD high (Minimum)(4)	SH3 Mode – ADC Rate MCLK		1	**5**	ns
t_{AD}	Aperture delay		**4**	5	**6.9**	ns
	Aperture delay variation			0.2	**1**	
$t_{BCLPINB}$, t_{BLKCLP}	CLPIN/BLKCLP Pulse Width	(high or low)	**2**			t_{MCLK}
t_{IS}	CLPIN/BLKCLP Setup		**3**			ns
t_{IH}	CLPIN/BLKCLP Hold		**3**			ns
t_{C_B}	CLPIN neg. edge to BLKCLP start	6 Channel mode		16		Pixels
		3 Channel mode		10		
$t_{LAT(1)}$	6 Channel Mode	6 Channel Mode, ADC Rate MCLK		11		t_{MCLK}
	Channel 1 Latency	6 Channel Mode, Pixel Rate MCLK		5		
$t_{LAT(2)}$	6 Channel Mode	6 Channel Mode, ADC Rate MCLK		12		t_{MCLK}
	Channel 2 Latency	6 Channel Mode, Pixel Rate MCLK		5.5		
t_{LAT}	3 Channel Mode Latency	3 Channel Mode ADC=Pixel Rate MCLK		11		t_{MCLK}
t_{OD}	Output Data Delay	Pixel Rate MCLK:				ns(6)
		6 Channel Mode – Channel 1	**2**	5.2	**8**	
		6 Channel Mode – Channel 2	**2**	5	**8**	
		ADC Rate MCLK:				ns
		6 Channel Mode – Channel 1	**3**	6	**9**	
		6 Channel Mode – Channel 2	**3**	6	**9**	
		3 Channel Mode	**2**	5.4	**9**	

(4) Refer to *Sampling Timing Diagrams*
(5) Measured with AFEPHASE = 11. For other AFEPHASE settings,these sample input timings will shift earlier with respect to MCLK as follows. (t_{HMC} will increase by these amounts, t_{MCH} will decrease by these amounts):
  (a) AFEPHASE = 10 – Earlier by ¼ pixel period
  (b) AFEPHASE = 01 – Earlier by ½ pixel period
  (c) AFEPHASE = 00 – Earlier by ¾ pixel period
(6) In Pixel Rate MCLK mode, the output data delay for Channel 2 data may be different under certain conditions of low MCLK duty cycle (< 50%). In that case the approximate output data delay t_{OD} will increase by the following: (50 – MCLK Duty Cycle Percent)/100 * T_{MCLK}

6.6 Serial Interface Timing

		MIN	TYP	MAX	UNIT
t_{CP}	SCLK period	**50**			ns
t_{WH}	SCLK High width	**20**			ns
t_{WL}	SCLK Low width	**20**			ns
t_{IS}	SDI Setup time	**5**			ns
t_{IH}	SDI Hold time	**5**			ns
t_{SENSC}	SENB low before SCLK rising	**5**			ns
t_{SCSEN}	SENB high after SCLK rising	**5**			ns
t_{SENW}	SENB high width(1)	**50**			ns
		5			t_{MCLK}
t_{OD}	SDO Output delay	**2**		**10**	ns

(1) SENB high pulse width should be > 50 ns when MCLK is not supplied. It should be > 5 MCLK when MCLK_ALIVE bit is set to 1 and MCLK is supplied.

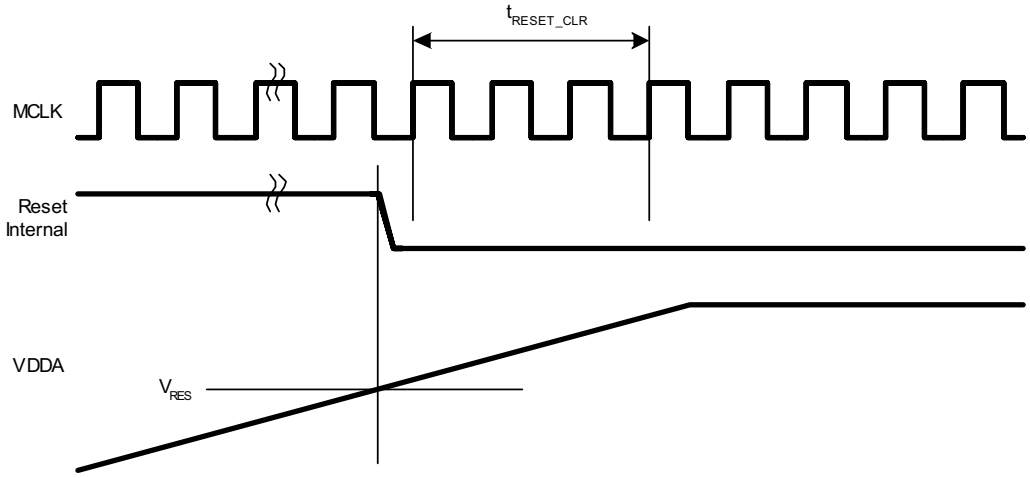


Figure 1. POR - Power On Reset

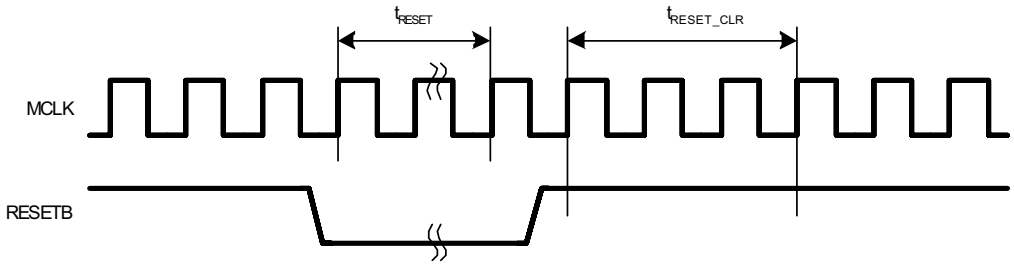
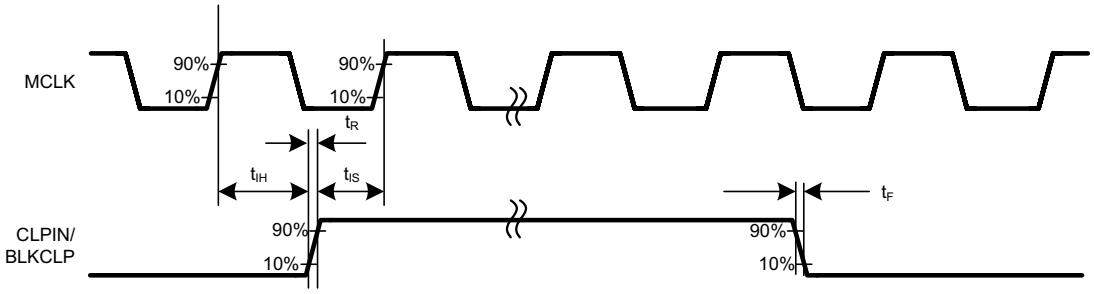
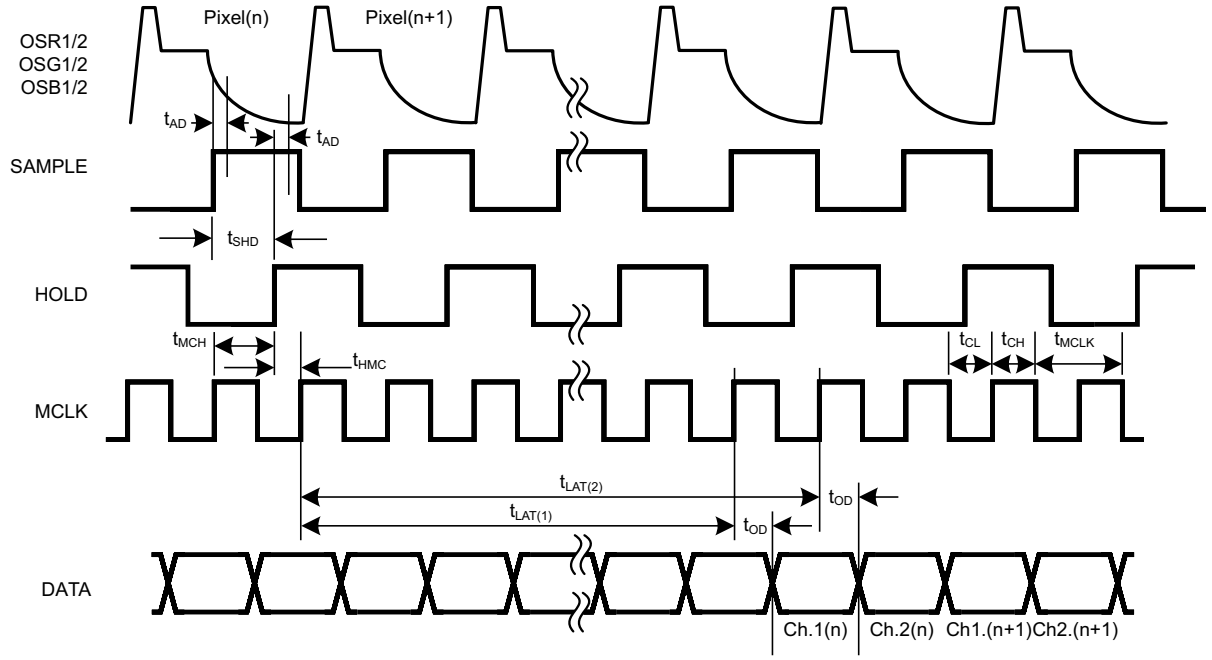


Figure 2. RESETB Input Timing



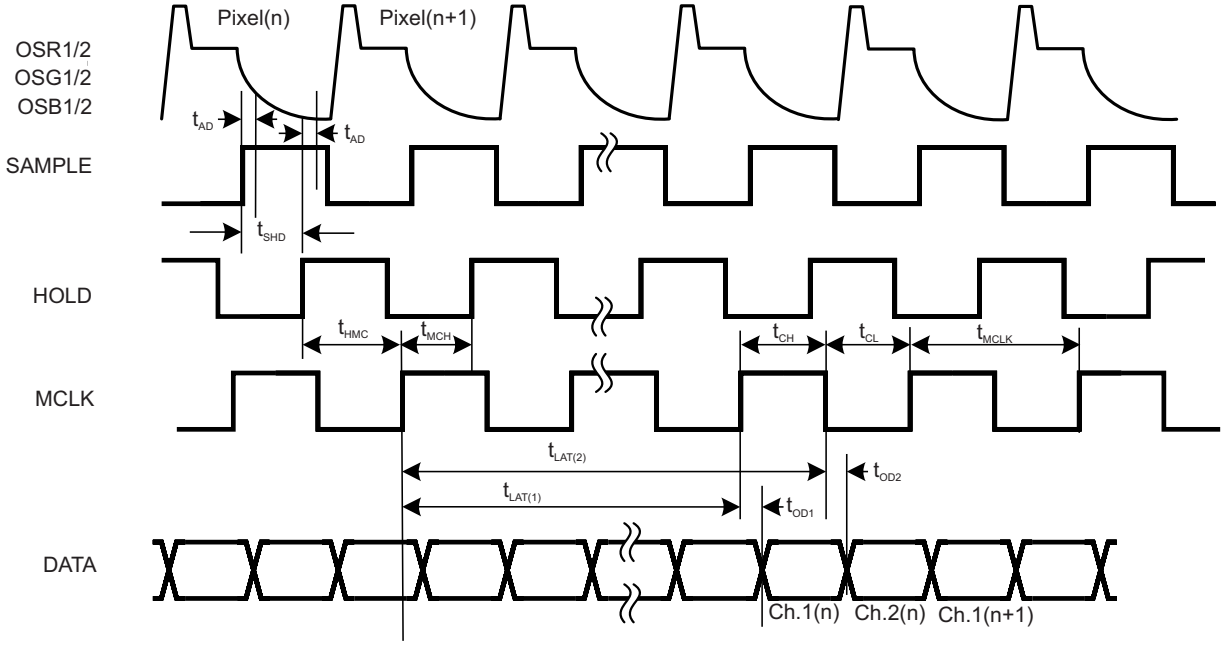
Note: CLPIN and BLKCLP are sampled or latched on the rising edge of MCLK by default .

Figure 3. Input Setup and Hold Timing



Above timing relationships between SAMPLE, HOLD and MCLK are for AFEPHASE = 11.
For other AFEPHASE settings, the sampling timing can move earlier by ¼, ½ or ¾ pixel period with respect to MCLK, but the latency as shown above will remain constant.

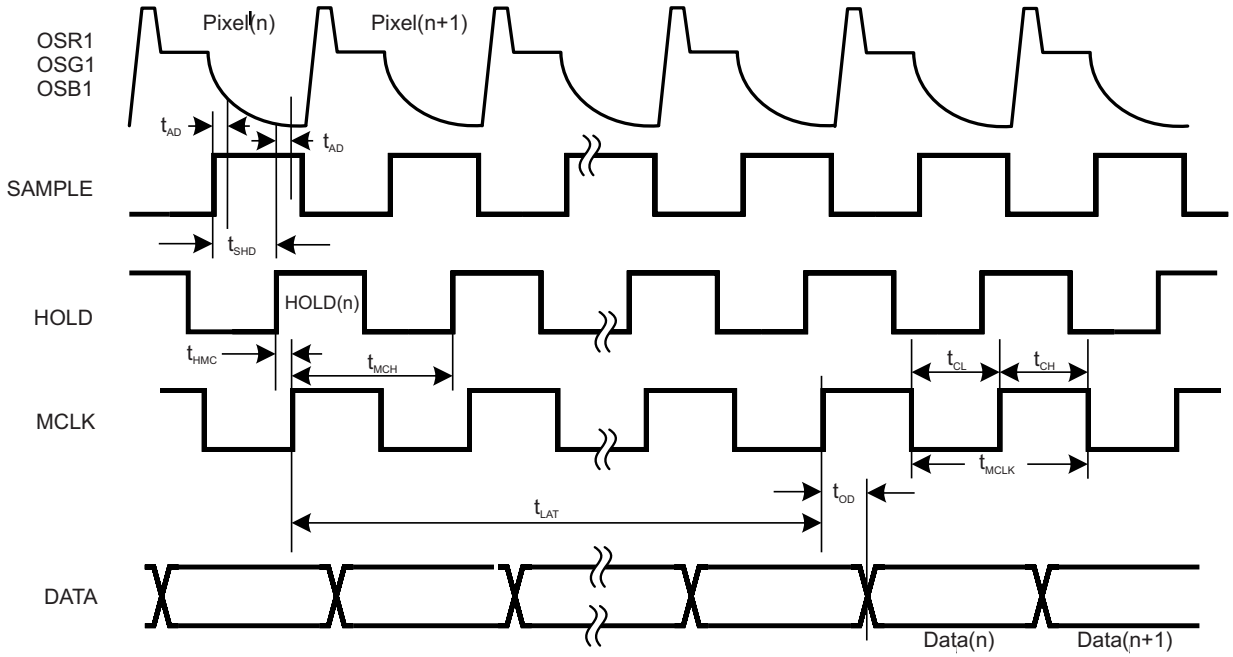
Figure 4. Output Latency and Timing – 6 Channel Mode – ADC Rate MCLK



Above timing relationships between SAMPLE, HOLD and MCLK are for AFEPHASE = 11.

For other AFEPHASE settings, the sampling timing can move earlier by ¼, ½, or ¾ pixel period with respect to MCLK, but the latency as shown above will remain constant.

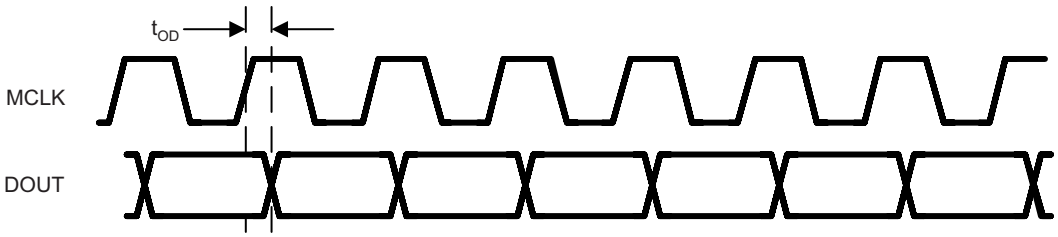
Figure 5. Output Latency and Timing – 6 Channel Mode – Pixel Rate MCLK



Above timing relationships between SAMPLE, HOLD, and MCLK are for AEPHASE = X1.

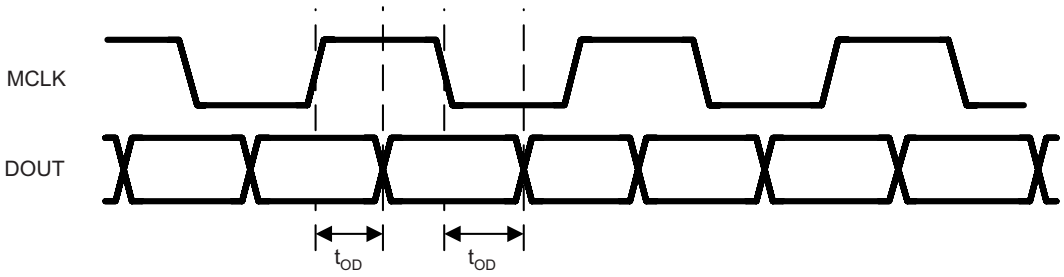
For other AEPHASE setting X0, the sampling timing can move earlier by ½ pixel period with respect to MCLK, but the latency as shown above will remain constant.

Figure 6. Output Latency and Timing – 3 Channel Mode



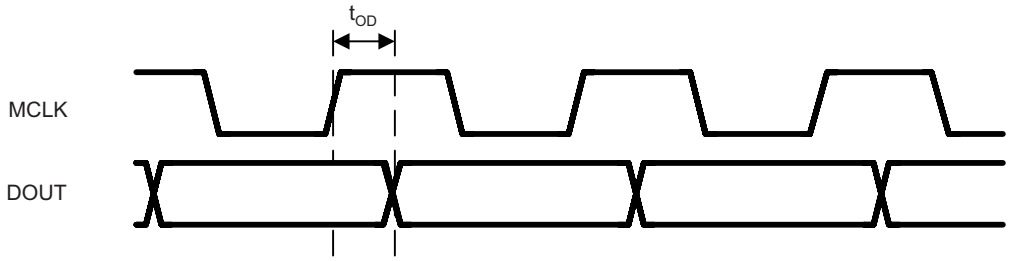
Output data is updated on the rising edge of MCLK. Data can be latched using the falling edge of MCLK.

Figure 7. Data Capture Timing – 6 Channel – ADC Rate MCLK



Output data is updated on both edges of MCLK. Due to the internal timing delays in the LM98519, from MCLK to DOUT, the data can be safely latched using both edges of MCLK.

Figure 8. Data Capture Timing – 6 Channel – Pixel Rate MCLK



Output data is updated on the rising edge of MCLK and can be latched using the falling edge of MCLK.

Figure 9. Data Capture Timing – 3 Channel

7 Detailed Description

7.1 Overview

The LM98519 is a fully integrated, high performance 10-Bit, 65 MSPS signal processing solution for digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative six channel architecture utilizing Correlated Double Sampling (CDS), or Sample and Hold (SH) type sampling.

7.2 Functional Block Diagrams

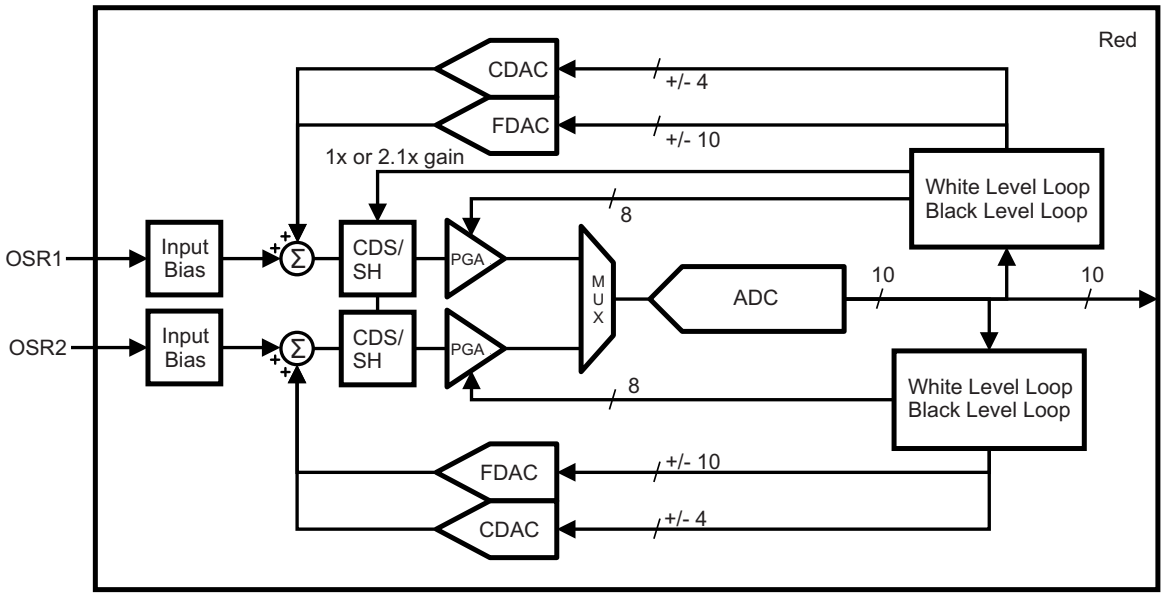


Figure 10. Channel Block Diagram

Functional Block Diagrams (continued)

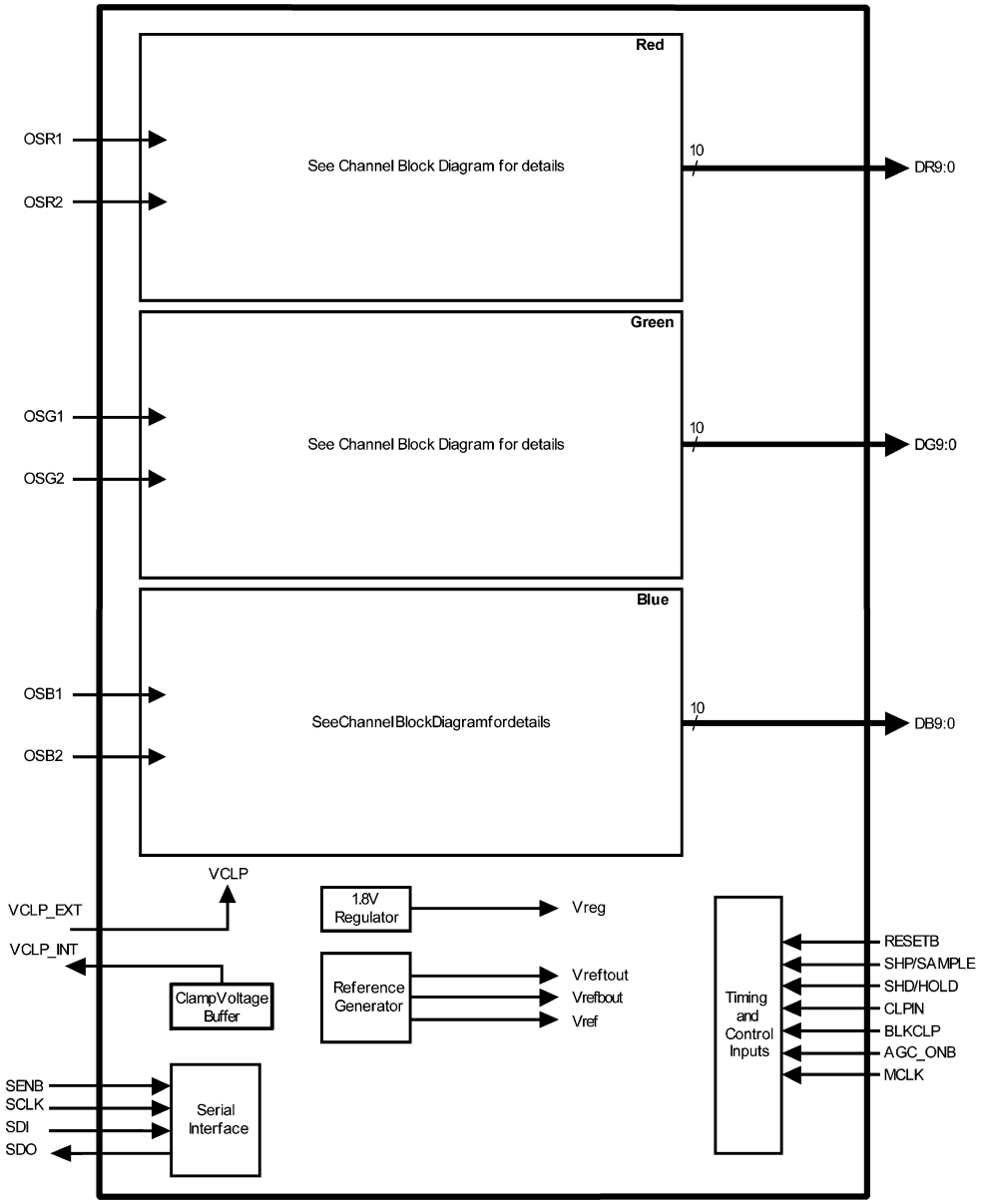


Figure 11. Chip Block Diagram

7.3 Feature Description

7.3.1 Input Clamping and Biasing Circuitry

Many sensor input signals will be at a different common mode voltage than that of the LM98519 input circuitry. In these applications, AC coupling is used to block the DC voltage difference between the source and the AFE inputs. Input clamp circuits are used to set the AFE input at the proper common mode voltage.

Initial coarse clamping should be done using the PIB (Passive Input Bias) and/or AIB (Active Input Bias) circuitry. Setting the PIB enable bit connects 1-kΩ pull-up and pull-down resistors to the inputs to rapidly charge them to VDDA/2. Setting the AIB bit connects the VCLPEXT reference voltage to the inputs via low impedance switches. Either method will bring the input voltage very close to the desired level of VDDA/2.

The AIB and PIB must be disabled during normal operations.

During image capture, black level clamping is done by connecting the input pins to an internal reference voltage through a low impedance switch. The clamp is turned on periodically to correct any droop in the DC input voltage and minimize conversion errors.

The clamp switch will be turned on during the “Black” portion of the input signal when the input is at a known voltage level. The clamp will connect the inputs to a reference level of approximately 1.65 V. Optionally, a customer supplied reference voltage can be applied at the VCLPEXT pin. Clamp timing is controlled by the CLPIN input signal in combination with the register bit ANDen and the internal SAMPLE timing signal.

CLPIN can directly control the internal Clamp, or the combination of CLPIN and SAMPLE can be used. Clamping only during SAMPLE ensures that the input is clamped to the “Black” level rather than the average of “Black”, “Reset” and reset noise feed through signals.

Feature Description (continued)

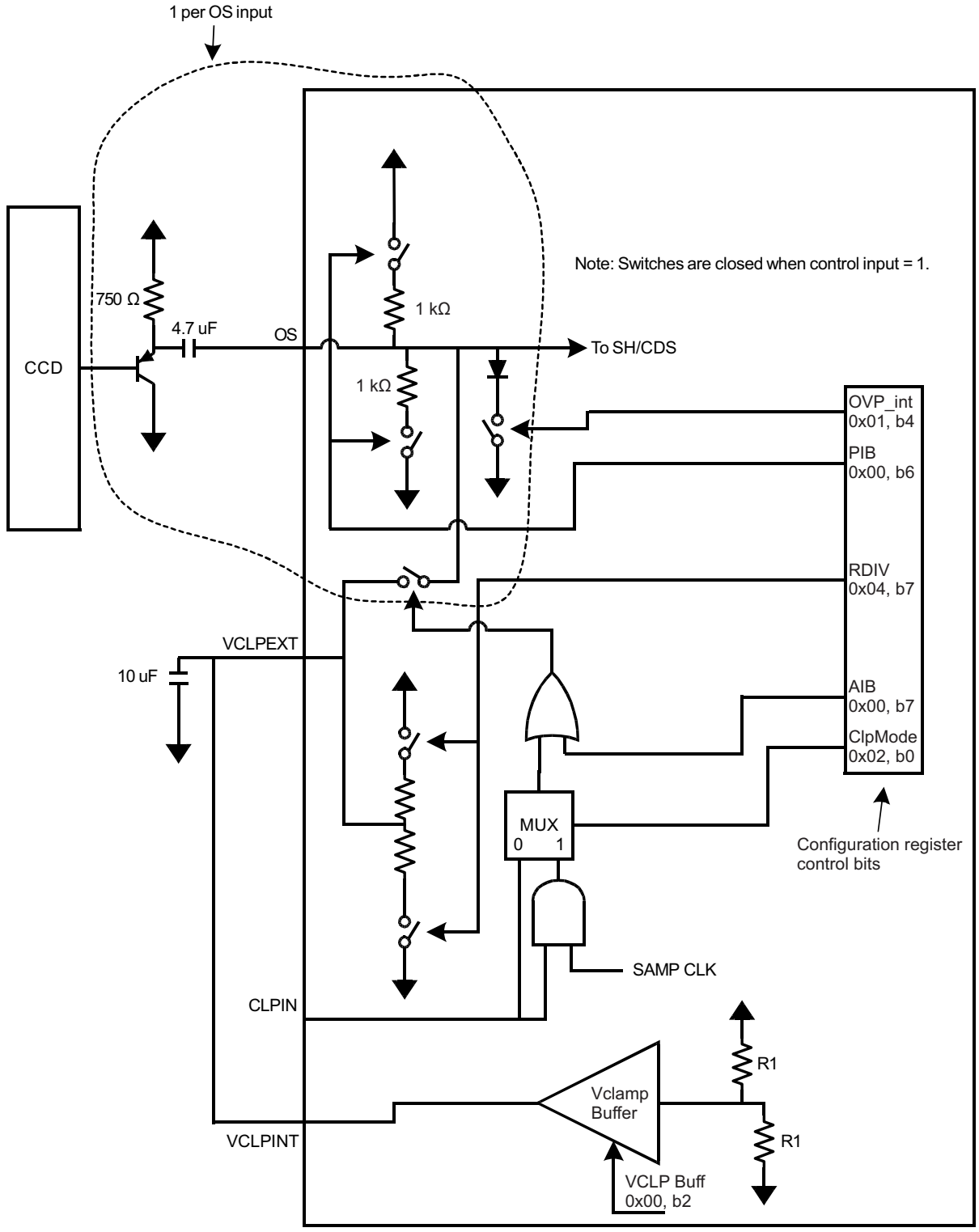
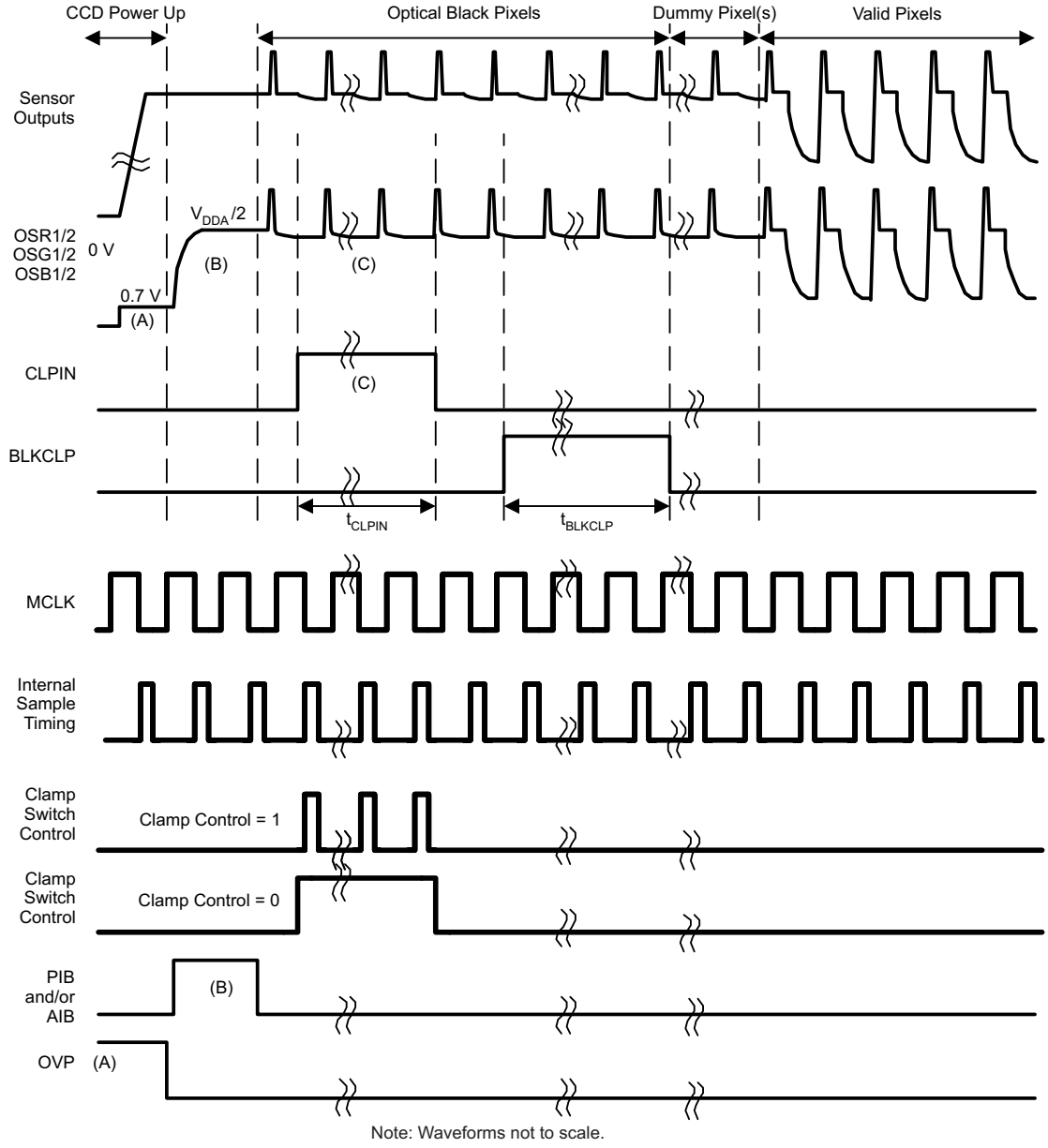


Figure 12. Input Protection and Clamping and Biasing Circuit

Feature Description (continued)



Waveforms not to scale

Figure 13. Input Protection Clamping and Biasing – Operation Example

Input clamping happens in two stages as indicated by A and B in Figure 13:

(A) During initial system power up, the OVP clamp circuit should be enabled by register setting (Register 0x01, Bit 4 = 1). This provides a path for current to flow as the sensor is powered up, and the large common mode voltage output of the sensor reaches a steady state value. Once the sensor voltages have stabilized, the OVP circuit can be disabled. At this point the OS inputs will still be approximately 0.7 V above ground. Settling to 99% of final voltage will take approximately 18 ms for a 4.7-µF capacitance, assuming a 750-Ω diode/switch impedance.

(B) Then, the PIB and/or AIB circuits should be enabled to bring the OS inputs up to approximately VDDA/2 volts. After the OS voltages have charged to this level, the PIB and AIB biasing should be turned off. Settling to within 1mV of VDDA/2 will take approximately 18 ms for a 4.7-µF capacitance, assuming a 500-Ω charging resistance.

Feature Description (continued)

(C) During image acquisition, accurate DC clamping is provided by the CLPIN switch. This switch is enabled when the CLPIN input is asserted. In most applications, the Clamp Control bit (Register 0x02, Bit 0) should be set to gate the CLPIN signal with the internal sampling pulse. This will ensure that clamping is only done during the image portion of the optical black pixels. Settling to 1 mV for a 10 mV ΔV between the pedestal and black will take:

(1/(%dwell) × 1/(% samp time) × Rsw × Cin × 5) (1)

Settling Time = (1/(32/7600 pixels)) × 1/(50%) × 40 Ω × 4.7 µF × 5 = 447 ms. (2)

Smaller input capacitors will result in proportionally smaller settling times for all clamping modes.

7.3.2 Input Connections for 3 Channel Operation

For three channel only applications, the unused inputs should be connected with 10-kΩ resistors to VCLP_EXT to minimize noise coupling into the active inputs.

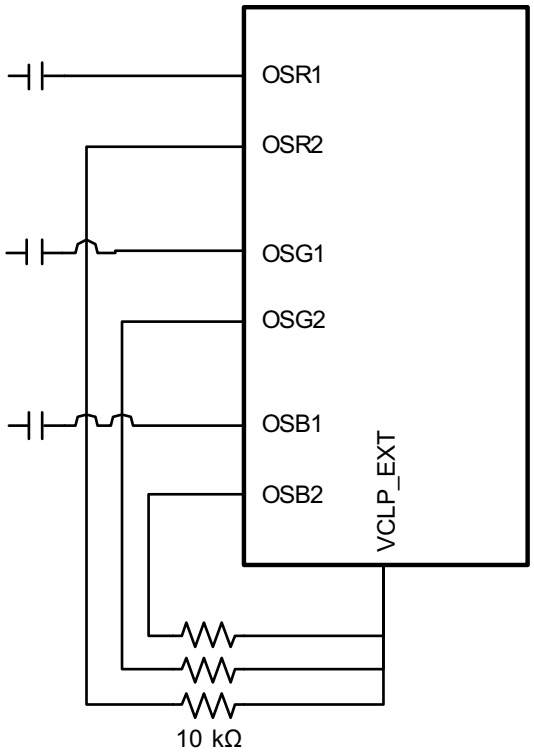


Figure 14. Input Connections for 3 Channel Operation

Feature Description (continued)

7.3.3 AFE References

A low noise reference structure is incorporated in the LM98519. Outputs (VREFTOUT approx. 2.23 V, VREFBOUT approx. 0.98V) and inputs (VREFTIN1, VREFTIN2, VREFBIN1, VREFBIN2) are provided to allow decoupling capacitors to be connected. VREFTOUT should be connected to VREFTIN1 and VREFTIN2. VREFBOUT should be connected to VREFBIN1 and VREFBIN2. Recommended capacitance is 1.0 µF between the top and bottom reference source, with 0.1 µF to AGND from both the top and bottom reference source. Connection and decoupling capacitor traces should all be as short as possible, and digital signals should be kept away from this area. Internal connections from VREFTOUT to VREFTIN1,2 and VREFBOUT to VREFBIN1,2 are present to reduce the impedance between outputs and inputs, but external connections should still be used for the best performance

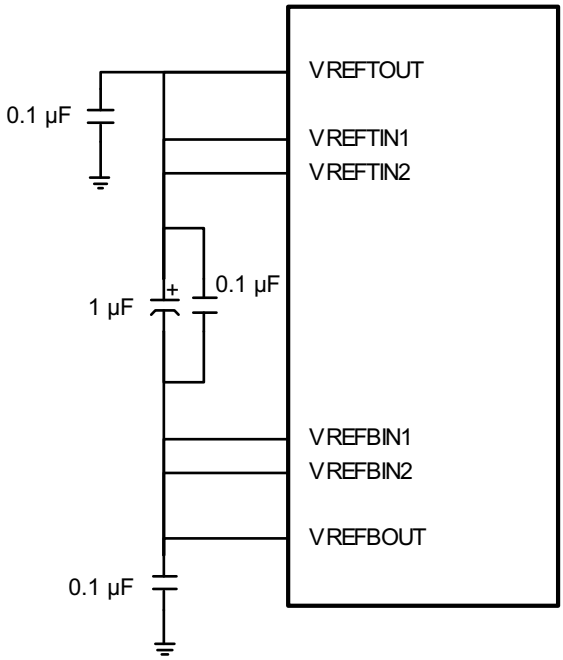


Figure 15. Reference Decoupling Example

Feature Description (continued)

7.3.4 Offset Control

Analog offset is provided before the ADC.

Two offset DACs are used to provide a coarse (CDAC) and fine (FDAC) offset that is applied prior to the CDS/SH stage.

- The offset CDAC (Coarse DAC) provides ±277 mV with ±4 bits of resolution in offset binary format.
- The offset FDAC (Fine DAC) provides ±111 mV (Large FDAC range) or ±60 mV (Small FDAC range) with ±10 bits of resolution in offset binary format. The FDAC range is controlled by the FDAC range bit for each color channel, in Register 0x03h, bits 3, 4, 5.

Table 1. Offset Binary Format

CDAC (±4 bit) Offset Binary Format			FDAC (±10 bit) Offset Binary Format			
Hex.	Dec.	Offset Voltage (mV)	Hex.	Dec.	Offset Voltage (mV)	Offset Voltage (mV)
1F	+15	+277	7FF	+1023	+111	+60
11	+1	+18.5	401	+1	+0.109	+0.059
10	0	0	400	0	0	0
0F	–1	–18.5	3FF	–1	–0.109	–0.059
01	–15	–277	001	–1023	–111	–60
00	–16	–277	000	–1024	–111	–60

Table 2. CDAC Step Sizes

CDS/SH+PGA Gain	CDAC LSB	ADC LSB
1x	1	15.7
10x	1	157
20x	1	314

Table 3. FDAC Step Sizes

FDAC Range	CDS/SH+PGA Gain	FDAC LSB	ADC LSB
Small	1x	1	0.05
Small	10x	1	0.50
Small	20x	1	1.00
Large	1x	1	0.09
Large	10x	1	0.93
Large	20x	1	1.8

7.3.5 Black Level Calibration (Offset)

Black level correction may be performed through one of two available methods: automatic or manual.

7.3.5.1 Manual Offset Adjustment

The manual method is intended for use with processing systems where the desired black level correction loop is external to the LM98519. In this mode the external processor controls the Black Level Offset registers.

Offset adjustment should be done using the average data from multiple Black pixels. The offset will be adjusted to set the Black pixel data as close as possible to the desired target value.

First the CDAC is adjusted until the error is reduced as much as possible given the CDAC step size for the current channel gain. (1 CDAC lsb = (15.7 to 314) ADC lsb depending on gain). Once the error is minimized with the CDAC, the FDAC is used to further converge the Black pixel data towards the target value.

After changing the channel gain, it may be desirable to repeat the offset adjustment.

7.3.5.2 Automatic Offset Adjustment

NOTE

During Automatic Offset Adjustment, the CDAC and FDAC register settings are Read Only.

During automatic black level calibration, the CDAC (coarse analog offset DAC) is used to bring the black level as close to the target as possible given the CDAC resolution.

Then the FDAC (Fine analog offset DAC) is applied to further converge the output to the desired black level target.

Two basic modes are available:

- CDAC and FDAC enabled – Used to converge to accurate Black target level as quickly as possible.
- FDAC Only mode – Used to maintain Black target level while avoiding large changes to offset. In FDAC only mode, the CDAC value is fixed, and the automatic adjustments only affect the FDAC.

CDAC and FDAC mode should be used to set the gain after power up and between scanning operations. FDAC Only mode should be used during scanning, to prevent large changes in offset from occurring in the image data. When using CDAC and FDAC mode, the value stored in Registers 0x25 and 0x26 is used to optimize trading of CDAC and FDAC steps. The default value is 321 decimal. To achieve the best trading, this value can be changed to 314 decimal. If the large FDAC range is enabled, this value should be changed to 184 decimal.

Use of the automatic mode involves enabling the black level offset auto-calibration bit in the black level clamp control register through the serial interface.

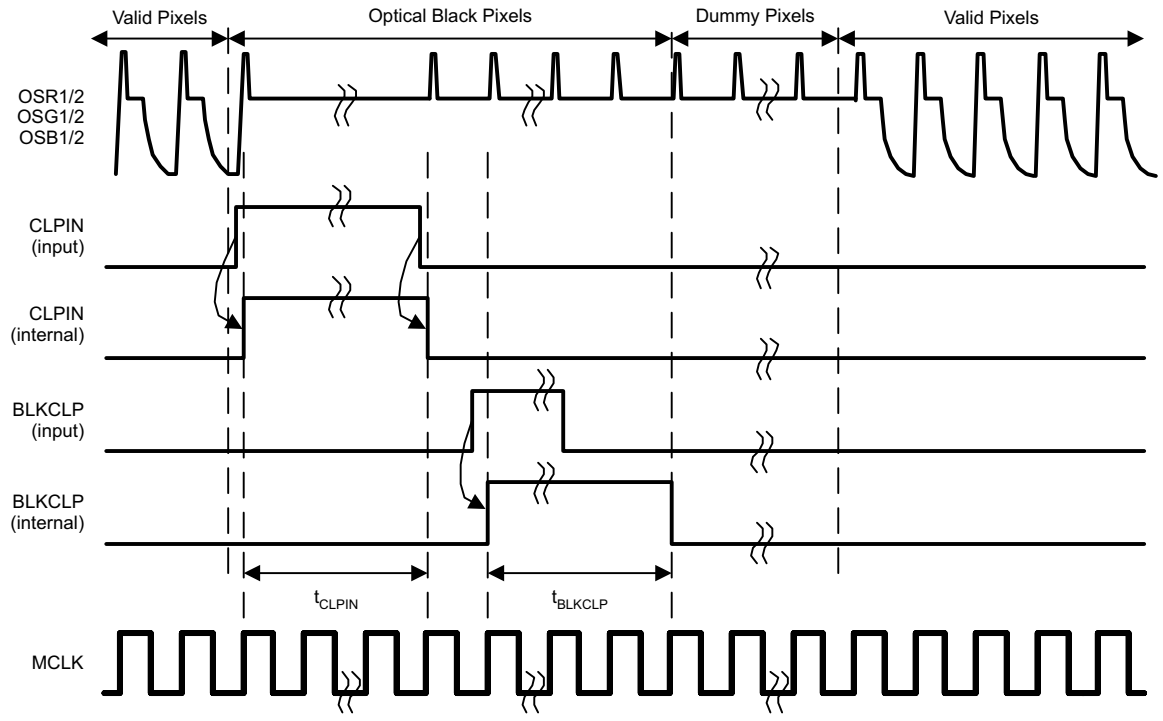
The ADC output value is averaged over the programmed number of pixels and subtracted from the desired black level code stored in the target black level register. The result of the subtraction may then be integrated by a preset scaling factor, effectively smoothing any sharp transitions present in the black level signal, before the resulting calculated offset is finally applied. The offset integration scaling factor is stored in the black level loop control register. The integration scaling values range from offset/2 to offset/128.

High Speed mode can be enabled to provide rapid initial convergence, with slower, more accurate convergence to the target value. High Speed mode is enabled by setting Register 0x23, Bit 1 = 1. The High Speed Mode offset integration value is set at Register 0x23, Bit 4. Two other parameters control the regions of operation around the target black value. The High Speed Mode Threshold and Hysteresis registers control the points where the transition from High Speed Mode to normal mode is made. When operating in High Speed Mode, the chip will transition to normal mode when Black Error < High Speed Threshold. When operating in Normal Mode, the chip will transition to High Speed Mode when Black Error > (High Speed Threshold + Hysteresis).

In automatic mode, the black level is determined from the ADC output during the Optical Black Pixels. The BLKCLP input pin is used to identify when the black pixels are being input to the IC. The rising edge of the BLKCLP input signal signals the beginning of the Optical Black Pixels. Alternatively, the Auto BLKCLP Pulse Generation (Register 0x23h, Bit 3) can be set to 1 to generate this signal internally. In that case, the BLKCLP pulse will begin 16 (6 channel mode) or 10 (3 channel mode) pixels after the falling edge of the CLPIN signal. Regardless of the source providing the BLKCLP start signal, the BLKCLP pulse duration is controlled by the Pixel Averaging setting in the BLKCLP_CTRL Register (0x24h, Bits 5:3).

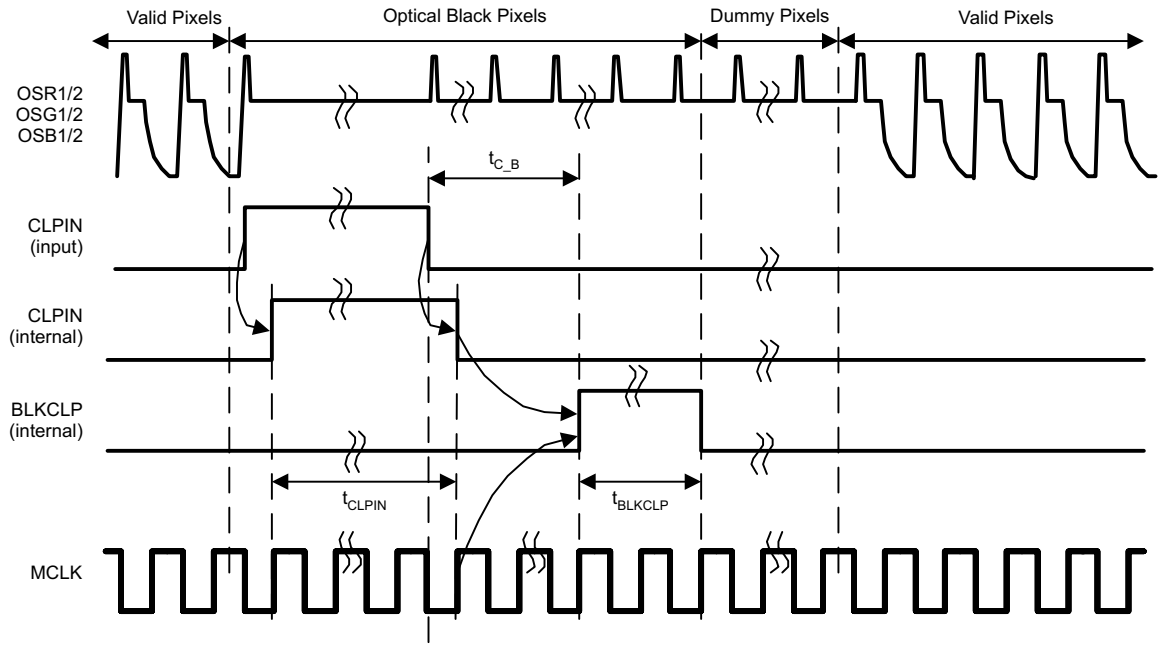
NOTE

At high gain settings, it is possible that the Automatic Offset Adjustment may reach the full scale CDAC setting and fail to recover. In this case, the Automatic Offset Adjustment should be disabled, the CDAC and FDAC settings should be centered, and then the Automatic Offset Adjustment should be enabled.



Note: t_{BLKCLP} is controlled by BLKCLP_CTRL Register (0x24h, Bits 7:3)

Figure 16. Black Calibration Timing – Manual BLKCLP



Note: t_{BLKCLP} is controlled by BLKCLP_CTRL Register (0x24h, Bits 7:3)

Figure 17. Black Calibration Timing – Automatic BLKCLP

7.3.5.3 Gain Control

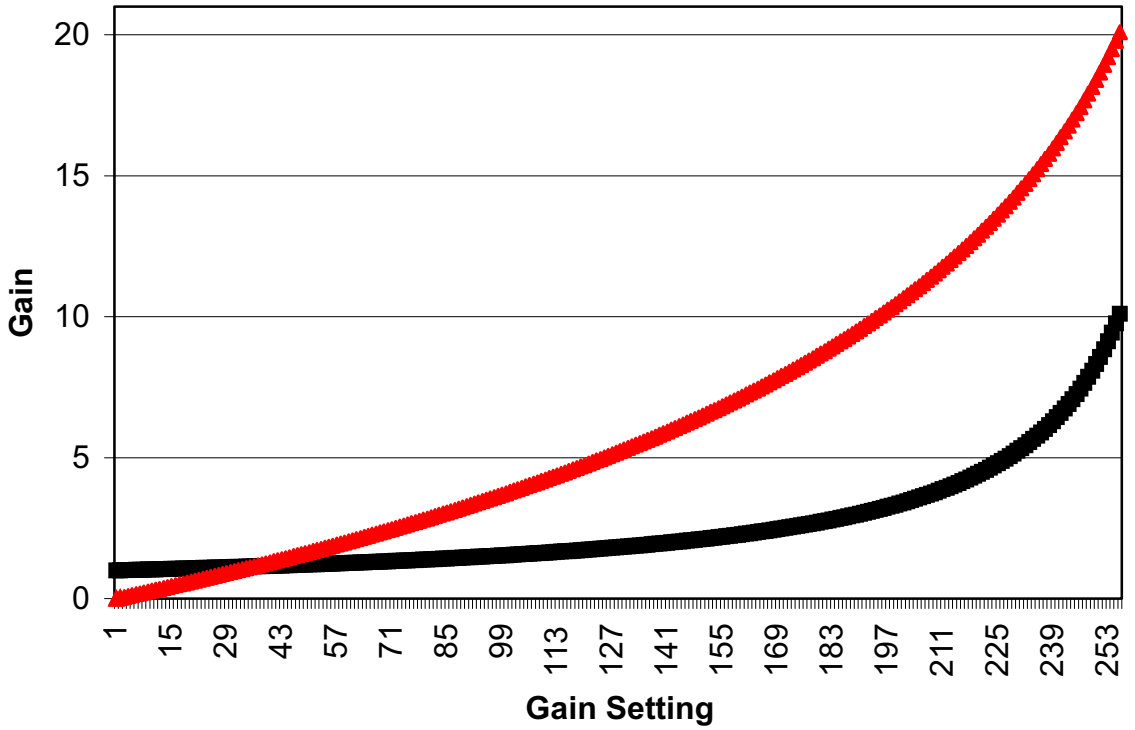
The PGA provides a range from 1x to 10x gain with 8 bits of resolution. The gain curve is nominally:

Gain = 283/(283-M)

where

- M is the 8-bit gain setting value from 0 to 255 (3)

In addition, the CDS/SH stage provides a 1x or 2.1x gain, giving an overall channel gain of 1x to 20x (0 dB to 26 dB).



(1) Min gain=1.0, max gain=10, max step=0.300dB; CDS Gain set to 2x.

(2) **Red** = gain in dB; **Black** = Gain by Ratio

(3) PGA Gain = 283/(283-M); M = 0 to 255

Figure 18. LM98519 8-Bit PGA Gain Curve

7.3.5.4 White Level Calibration (AGC - Automatic Gain Control)

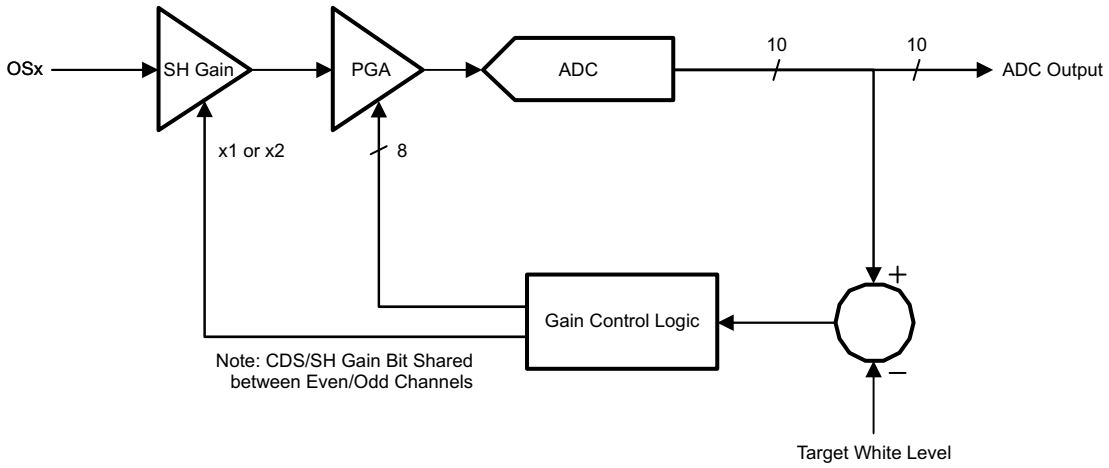


Figure 19. White Level Calibration

During Automatic Gain Adjustment, the PGA and CDS/SH gain settings are Read Only.

The white calibration loop allows the LM98519 to automatically set the gain for the desired maximum ADC output. A digital input pin or configuration register bit is used to start the loop. This would normally be done once per page, or as needed for the particular system design. When triggered, the loop processes the output data during the defined white pixel range. The pixel range can be selected from a minimum of 1 pixel to a maximum of 65535 pixels. The starting pixel can be selected via the PK_DET_ST register at 0x2Ah, 0x2Bh and is referred to the rising edge of either the CLPIN or BLKCLP signal. The number of pixels is selected by the PK_DET_WID register at 0x2Ch, 0x2Dh.

During processing, a moving window average is performed. The size of the window is set by the PK_AVE register at 0x29, Bits 2:0. The window size is adjustable from 1 (no averaging) to 32 pixels. As each window average is calculated, the value is compared to the previous Peak White value (at the start of the line, the initial Peak White value is set to 0). If the new average is larger than the previous Peak White value, the Peak White value is replaced with the new average value. The window position is then incremented by 1 pixel and the process is repeated until the window average has processed all PK_DET_WID pixels.

If the AGC_ONB input is pulsed, the white calibration loop will operate for a fixed number of lines at the beginning of the scan. This duration is selected via the AGCDuration register at 0x2Eh. Valid settings are from 1 to 255 decimal. A duration setting of 0 will cause the loop to not run.

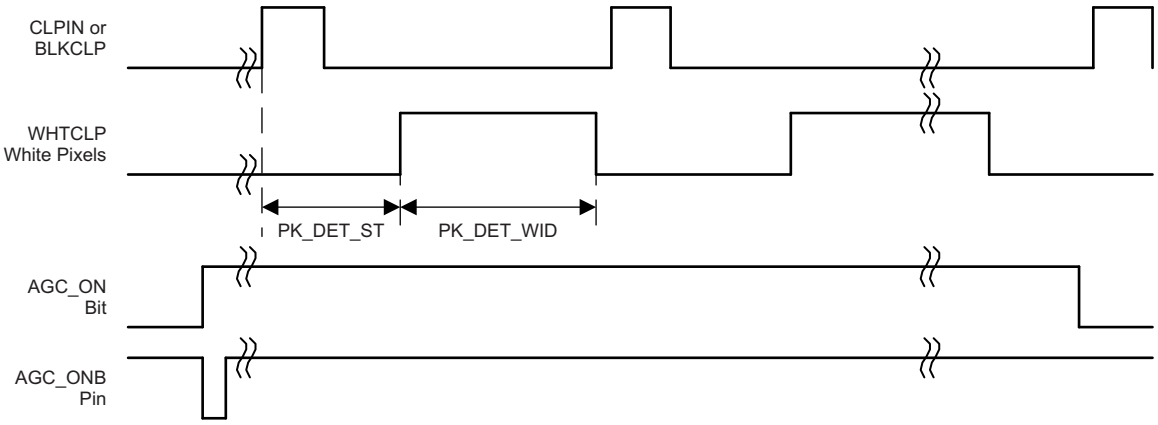


Figure 20. AGC Loop

When the AGC_ONB input is pulsed, the register bit AGC_ON is set. The AGC_ON bit is cleared when the loop is terminated, which is when the number of lines allocated for the loop are exhausted. The AGC_ONB pin should be asserted for minimum of two pixels and should be deasserted before the loop is complete and the AGC_ON register bit is cleared.

Register 0x01, Bit 5 selects the polarity of the AGC_ONB input. The default is 0 for active low.

When the AGC loop begins operation, the AGC STATUS at Register 0x33, will be automatically cleared (as long as the serial interface mode bit at Register 0x01, Bit 3 is set to 1, MCLK present). At the end of the AGC loop operation, the AGC STATUS register can be read to check that the loop successfully converged for all channels. The status value should be 0x00 to indicate no Convergence Errors.

While the AGC loop is operating, a timing source is needed to provide a consistent reference point at the beginning of each line of pixels. Register 0x28, Bit 5 is used to select either the CLPIN or BLKCLP as the timing source. If Bit 5 = 0, the timing reference is the rising edge of CLPIN. If Bit 5 = 1, the timing reference is the rising edge of BLKCLP. The register setting PK_DET_ST selects the number of pixel after this timing reference that pixel averaging begins. The register setting PK_DET_WID selects the number of pixels after PK_DET_ST that are processed.

The purpose of the white loop is to find the correct gain setting so the brightest white pixels are at a specific ADC code target. The target value is set in the AGCTargetMSB and AGCTargetLSB registers. The target value is calculated from the register value as shown:

AGC_TARG = 512d + (AGCTargetMSB[7:0]+AGCTargetLSB[7]) (4)

Table 4. AGC Target Values

AGCTargetMSB (REGISTER 0x2F)	AGCTargetLSB (REGISTER 0x30)	AGC_TARG BINARY	AGC_TARG DECIMAL
11111111	1	1111111111	1023
11111111	0	1111111110	1022
10000000	1	1100000001	769
10000000	0	1100000000	768
00000000	1	1000000001	513
00000000	0	1000000000	512

7.3.6 Operating Mode Description

The white loop provides two different techniques for converging to the target value, Binary Search, and Incremental Search.

The Binary Search algorithm is intended to provide a rapid convergence to the target value. During initial operation, large changes in the channel gain are allowed. After each line, the allowed change is reduced significantly. For final convergence, the algorithm switches to the Incremental Search mode, to achieve low error.

The Incremental or Linear Search algorithm is intended to provide a low error, but will converge more slowly than the Binary method. The changes (if any) in channel gain are always done in 1 lsb increments to provide low overshoot and high accuracy of convergence.

7.4 Device Functional Modes

7.4.1 AFEPHASEn Details for SHP/SHD Input Mode

The SHP (sample reference) and SHD (sample signal) inputs are combined with the selected AFEPHASEn signal to generate the internal CLAMP and SAMPLE signals respectively. The SHP signal is ANDed with AFEPHASEn. The SHD signal is ANDed with the inverted AFEPHASEn signal.

The best performance will be achieved by selecting the AFEPHASEn timing that has the high period completely overlapping the SHP input timing, and the low period completely overlapping the SHD timing.

Device Functional Modes (continued)

7.4.2 AFEPHASEn Details for SAMPLE and HOLD Input Mode

In Sample/Hold mode, the SAMPLE and HOLD inputs are used. The rising edge of SAMPLE defines the start of the sample control pulse, and the rising edge of HOLD defines the end of the sample control pulse. This sample control pulse is then gated by the low period of the AFEPHASEn signal to generate the resulting SAMPLE signal used internally.

The AFEPHASEn signal which has the low period overlapping the sample control pulse will give the best performance.

7.4.3 AFEPHASEn: 6 Channel and 3 Channel Modes

In 6 Channel Mode, there are two full cycles of MCLK and ADCCLK for each sensor pixel period. This allows the two AFE channels to be multiplexed into the single ADC. In this mode, there are 4 possible AFEPHASEn timings available.

In 3 Channel Mode, there is only one cycle of MCLK and ADCCLK per pixel period. Because of this, there are only 2 choices for AFEPHASEn, as shown in Figure 21 through Figure 23.

7.4.4 LM98519 AFEPHASE Synchronization

There are three main modes of operation for the LM98519

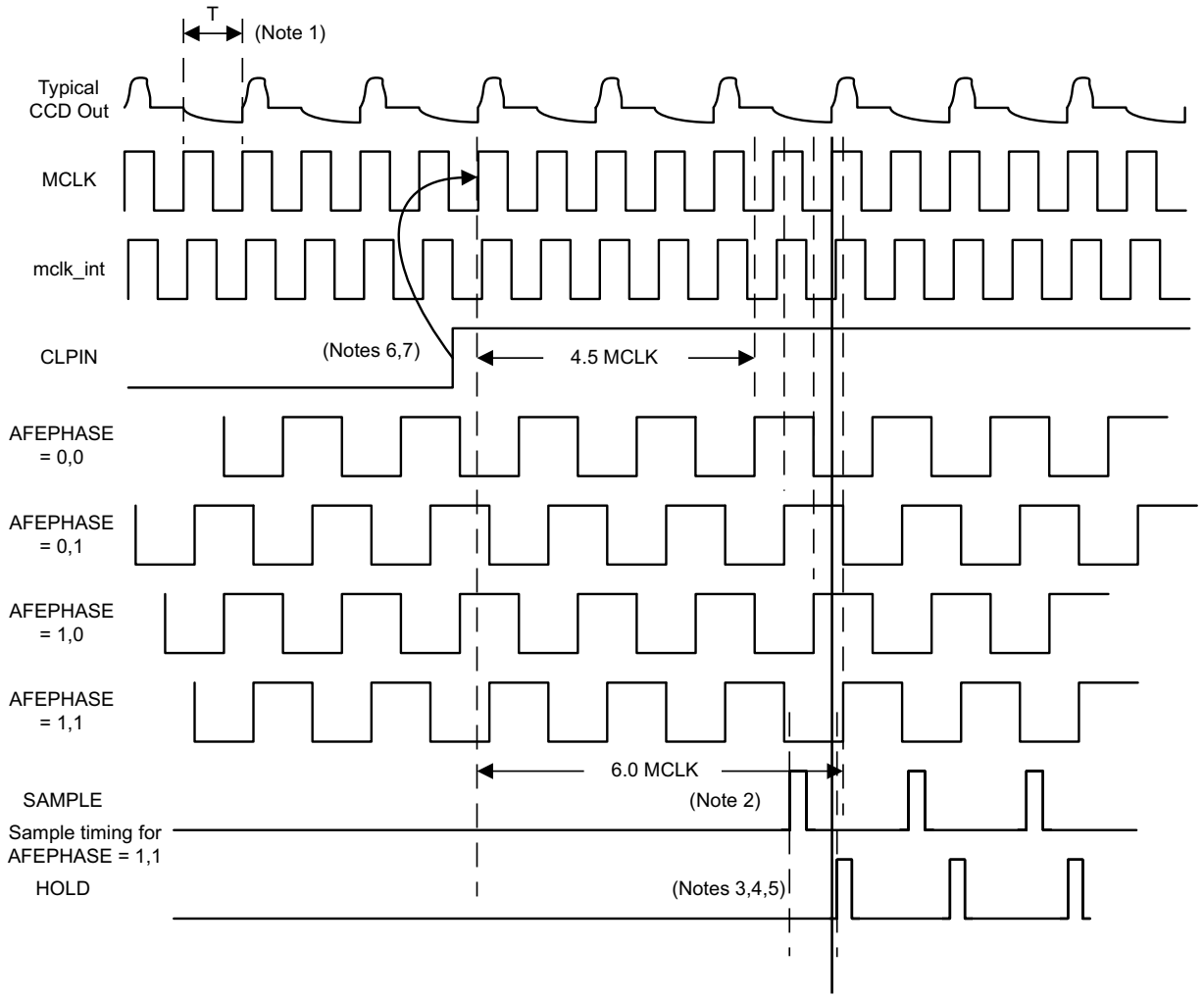
1. 6 channel mode using ADC Rate MCLK – Clock Doubler is bypassed
2. 6 channel mode using Pixel Rate MCLK – Clock Doubler is used
3. 3 channel mode using Pixel Rate MCLK – Clock Doubler is bypassed

In case #1, where an ADC rate (2x of pixel rate) clock is input, the LM98519 needs one additional signal to ensure synchronization between the internal sampling phases and the pixel rate input signal.

This synchronization is done using the CLPIN input signal in combination with MCLK. The CLPIN input generates an internal reset signal that sets the internal AFEPHASE state machine into a known relationship with MCLK and CLPIN. This ensures the AFEPHASE sampling is synchronized to the host sensor timing.

Figure 21 through Figure 23 indicate the phase relationship between MCLK and AFEPHASE when CLPIN is used for synchronization.

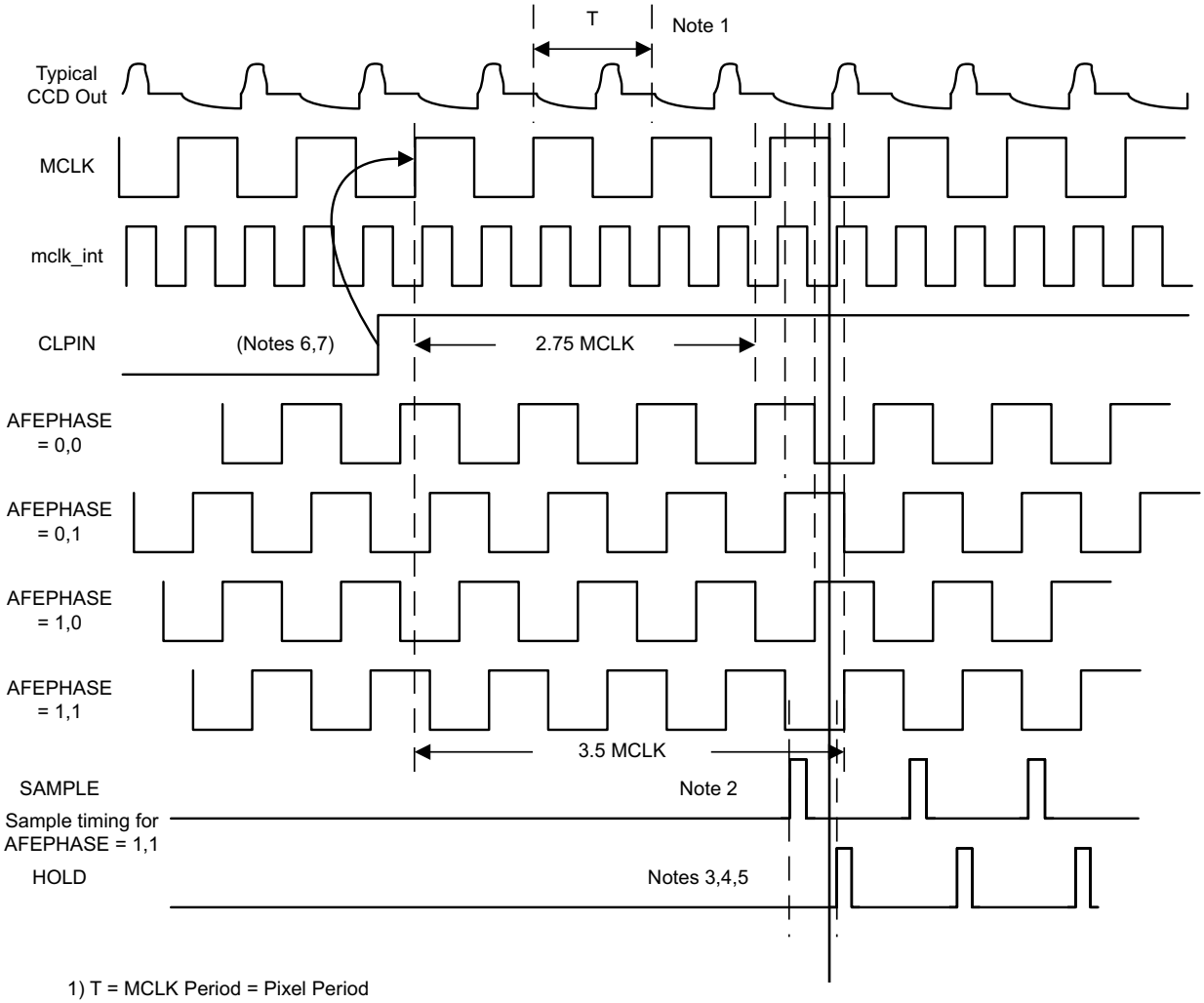
Device Functional Modes (continued)



1) T = MCLK Period = 1/2 Pixel Period
2) Rising edge of SAMPLE must be at least 8 ns before rising edge of HOLD
3) Rising edge of HOLD can be up to t_{MCH} after rising edge of MCLK (AFEPHASE = 1,1)
4) In SH1a,SH1b modes, the rising edge of HOLD can be up to t_{HMC} before the rising edge of MCLK (AFEPHASE = 1,1)
5) In SH2 mode, HOLD can be up to t_{HMC} ns before the rising edge of MCLK (AFEPHASE=1,1)
6) CLPIN must be high or low for at least 2 input MCLK cycles
7) CLPIN is latched by the rising or falling edge of MCLK selectable by Register 0x04h, Bit 5.

Figure 21. 6 Channel Mode – ADC Rate MCLK

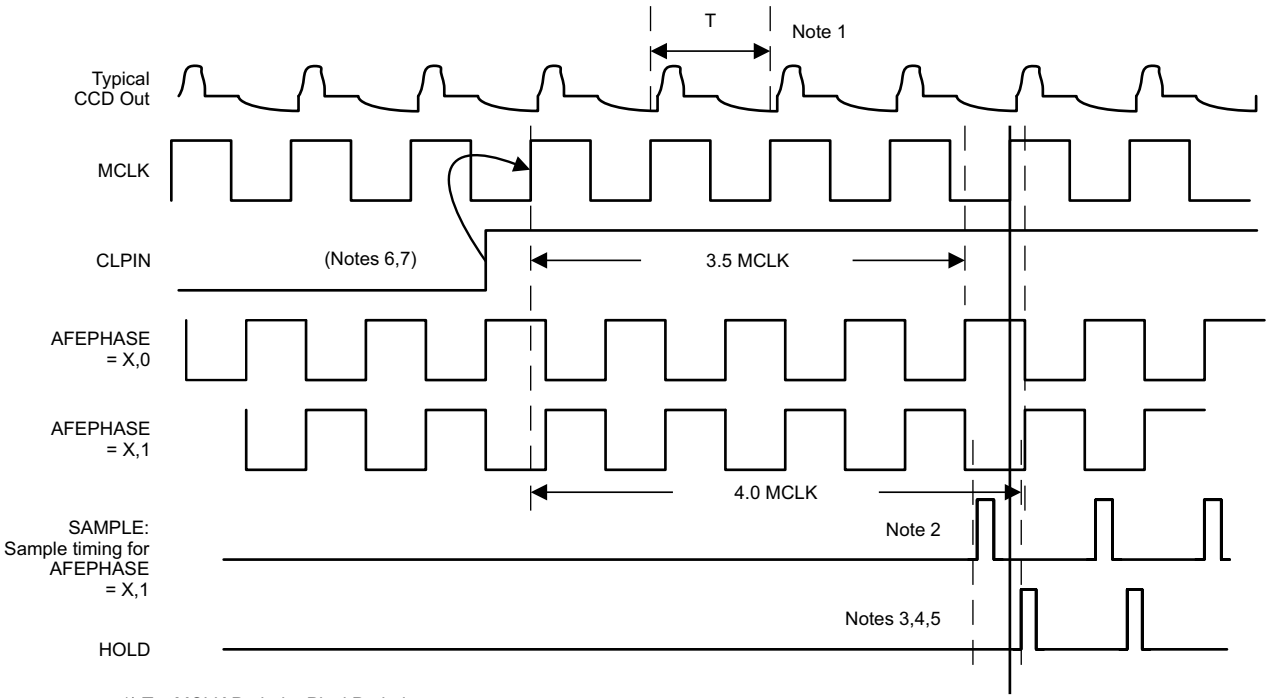
Device Functional Modes (continued)



1) T = MCLK Period = Pixel Period
2) Rising edge of SAMPLE must be at least 8 ns before rising edge of HOLD
3) Rising edge of HOLD can be up to t_{MCH} after falling edge of MCLK (AFEPHASE = 1,1)
4) In SH1a,SH1b modes, the rising edge of HOLD can be up to t_{HMC} before the falling edge of MCLK (AFEPHASE = 1,1)
5) In SH2 mode, HOLD can be up to t_{HMC} before the rising edge of MCLK (AFEPHASE=1,1)
6) CLPIN must be high or low for at least 2 input MCLK cycles
7) CLPIN is latched by the rising or falling edge of MCLK selectable by Register 0x04h, Bit 5.

Figure 22. 6 Channel Mode – Pixel Rate MCLK

Device Functional Modes (continued)



1) T = MCLK Period = Pixel Period
2) Rising edge of SAMPLE must be at least 8 ns before rising edge of HOLD
3) Rising edge of HOLD can be up to t_{MCH} after falling edge of MCLK (AFEPHASE = 1,1)
4) In SH1a, SH1b modes, the rising edge of HOLD can be up to t_{HMC} before the rising edge of MCLK (AFEPHASE = 1,1)
5) In SH2 mode, HOLD can be up to t_{HMC} before the rising edge of MCLK (AFEPHASE = 1,1)
6) CLPIN must be high or low for at least 2 input MCLK cycles
7) CLPIN is latched by the rising or falling edge of MCLK selectable by Register 0x04h, Bit 5.

Figure 23. 3 Channel Mode – Pixel Rate = ADC Rate MCLK

7.4.5 Sampling Timing Diagrams

NOTE

4 (6 Channel Mode) or 2 (3 Channel Mode) AFEPHASE settings are available to provide flexibility of sample timing.

For ease of use, AFEPHASE = 11 is the default setting in 6 channel mode, and AFEPHASE = X1 is the default setting for 3 channel mode, as shown in select diagrams. Specified values for these timings are measured at AFEPHASE = 11. For other AFEPHASE settings,these sample input timings will shift earlier with respect to MCLK as follows:

- AFEPHASE = 10 – Earlier by ¼ pixel period
- AFEPHASE = 01 – Earlier by ½ pixel period
- AFEPHASE = 00 – Earlier by ¾ pixel period

Device Functional Modes (continued)

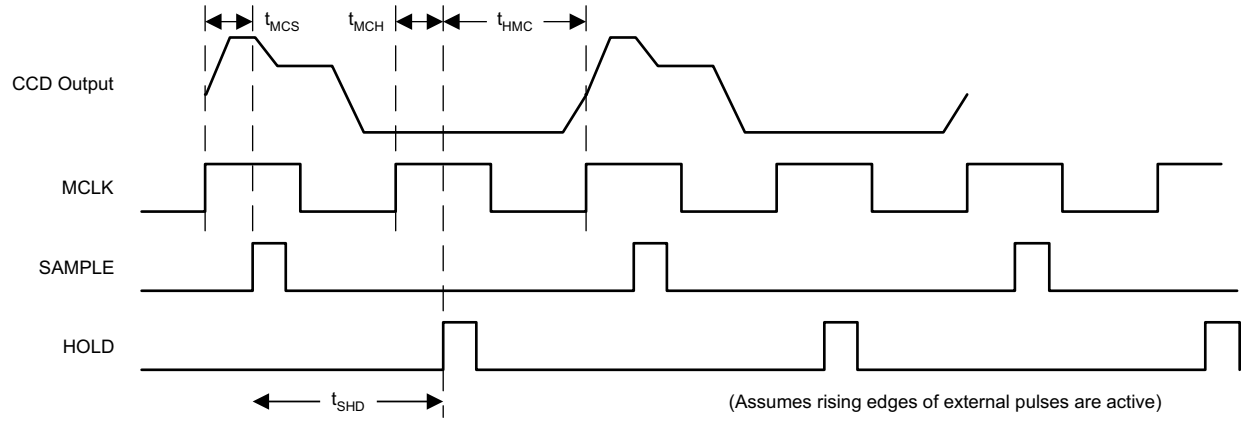


Figure 24. SH3 Timing Mode – ADC Rate Clock Input (Pixel Rate MCLK not Supported in SH3)

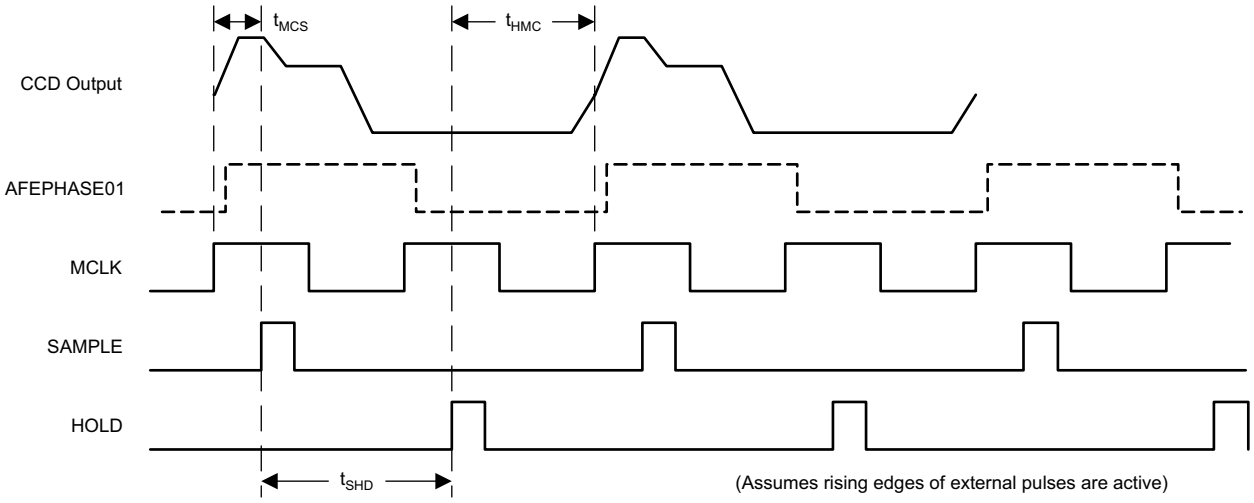


Figure 25. SH2 Timing Mode – ADC Rate Clock Input

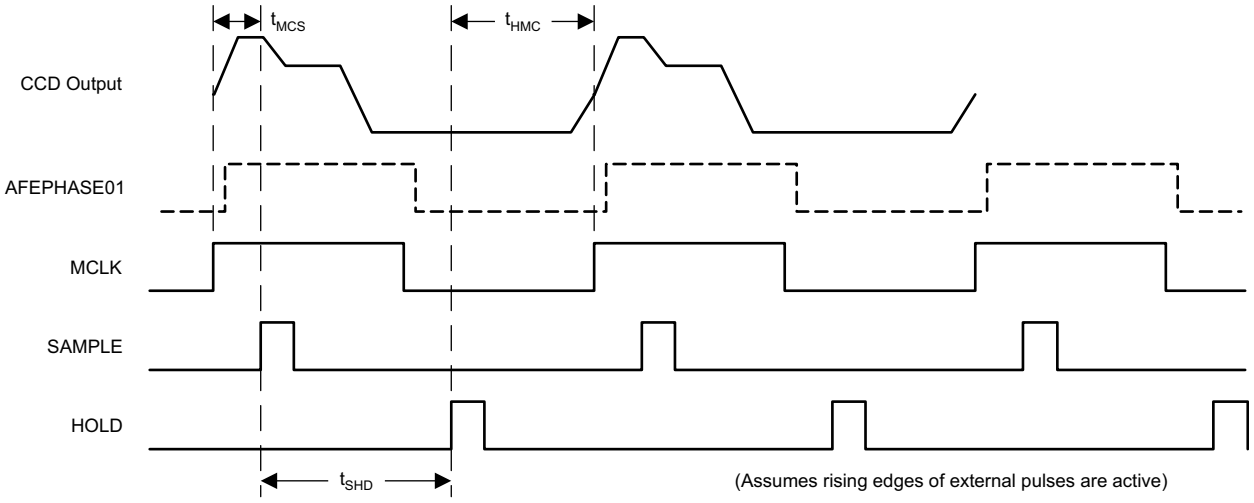


Figure 26. SH2 Timing Mode – Pixel Rate Clock Input

Device Functional Modes (continued)

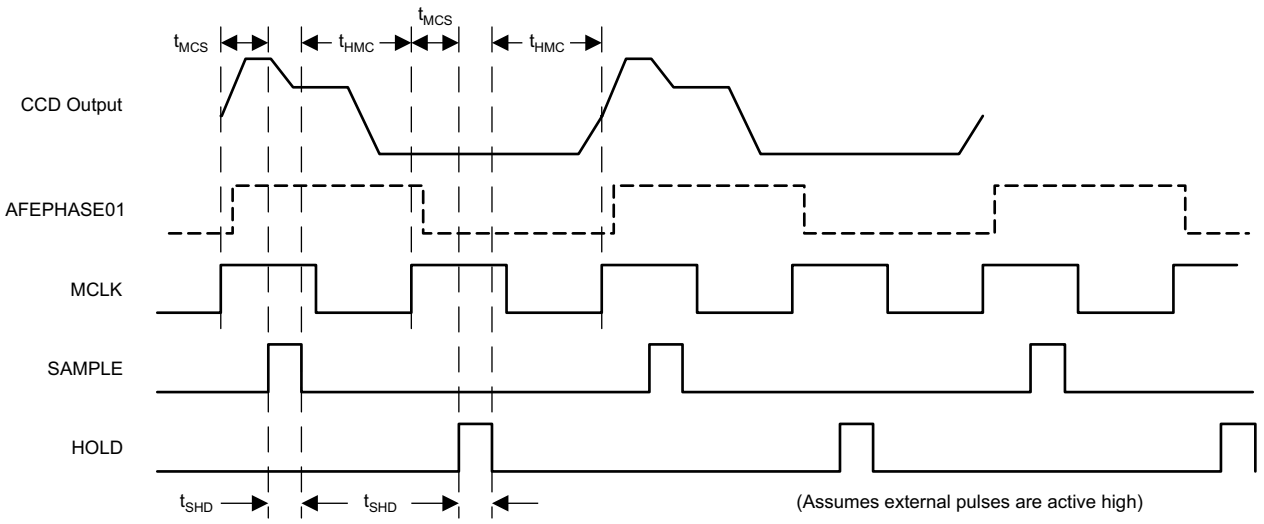


Figure 27. SH1b/CDSb Timing Mode – ADC Rate Clock Input

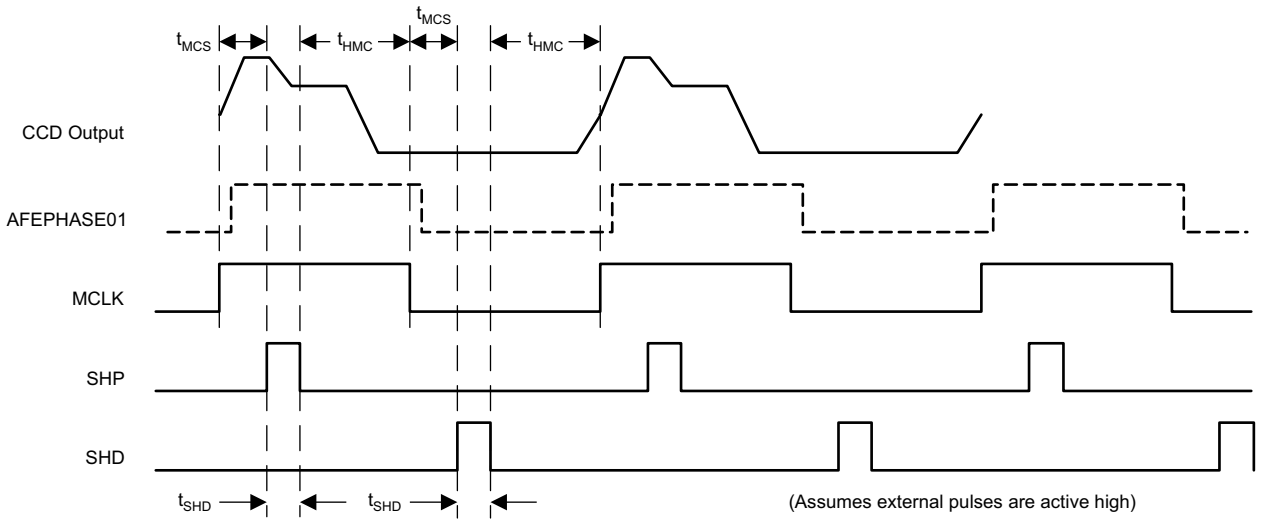


Figure 28. SH1b/CDSb Timing Mode – Pixel Rate Clock Input

7.5 Programming

7.5.1 Using Black Pixel Average

In most applications, the Black Pixel Average bit should be set.

During loop operation, the ADC_MAX or average maximum ADC value is found during the white pixels. The Black Pixel Average value is then subtracted from this ADC_MAX value to find the present white value. This ADC_WHT value is then used for comparison to the target white pixel value TARG_WHT. This is done to eliminate the effects that changes in the system gain will have on the Black Pixel Average value. As gain is increased or decreased, the previously calibrated Black Pixel Average value will change also. When the white loop operation is complete, the gain is set to provide the proper white level referenced to the Black Pixel Average value. Then the Black Loop will be run once more to set the Black Pixel Average at the desired level, and the White level will still be calibrated to the proper level.

Programming (continued)

In addition, the following registers should be initialized before starting the loop:

Table 5. Initialize Registers Before Loop

REGISTER	FUNCTION
PK_DET_ST (0x2Ah, 0x2Bh)	Start of the white pixel averaging in pixels from rising edge of CLPIN or BLKCLP
PK_DET_WID (0x2Ch, 0x2Dh)	Number of pixels in each line over which white pixels are averaged
AGCDuration (0x2Eh)	Duration in number of lines the loop should run. **If set to 0, the loop will not run.** Valid settings are 1 to 255.
AGCTarget (0x2Fh, 0x30h)	AGC target, between 512 to 1023
AGCTolerance (0x31h)	Allowed error margin from the target value
AGC_BLKINT (0x32h)	Black Offset Integration, if used
AGC_CONFIG (0x28h)	Select reference edge CLPIN or BLKCLP rising edge, Enable/Disable AGC_ONB Pin, Incremental Search Enable, Black Offset Enable

After all registers are initialized, the AGC_ON bit (0x28h, b0) can be set, or the AGC_ONB pin can be pulsed to start the white loop.

7.5.2 Sample Timing Control

Sample timing is controlled through the combination of the selected internal AFEPHASEn signal, and one or several user inputs.

The input timing control pins can operate in two different modes:

SAMPLE and HOLD (Used with S/H mode sampling only)

In this mode, the rising edge of the SAMPLE signal controls the start of the sampling, while the rising edge of HOLD stops sampling and holds the signal. This mode cannot be used with CDS operation.

SHP and SHD (Used with CDS and S/H modes of sampling)

In this mode, the SHP pulse is used to sample the reference level of the signal, while the SHD pulse is used to sample the signal (brightness) information when CDS mode is used. If CDS is turned off, then SHD is used to control the signal sample timing and SHP is not used.

The different input timing modes are selected by bits in Registers 0x00, 0x02, and 0x04, as shown in Table 6:

Table 6. Input Timing Modes

MODE	REG 0x04[1]	REG 0x02[7]	REG 0x02[3:2]	REG 0x02[1]	REG 0x00[0]	DESCRIPTION
SH3 (Default)	0	1	See (1)	0	0	Sample and Hold mode, clocked by SAMPLE and HOLD clocks (2)
SH2	1	1		0	0	Sample and Hold mode, clocked by SAMPLE and HOLD clocks (3)
SH1a	1	0		1	0	Sample and Hold mode, clocked by AFEPHASE (3)
SH1b	1	1		1	0	Sample and Hold mode, clocked by SHD (3)
CDSa	1	0		1	1	CDS mode, sampled by AFEPHASE (3)
CDSb	1	1		1	1	CDS mode, sampled by SHP and SHD clocks (3)

(1) AFEPHASE bits should be set to “11” in SH3 mode (both 3ch and 6ch operation)
(2) AFEPHASE is automatically set by the HOLD input timing. Only ADC Rate MCLK is allowed.
(3) AFEPHASE is synchronized by MCLK and CLPIN inputs

In modes SH1a and CDSa, the internal Sample or Clamp and Sample timing signals are generated from the selected AFEPHASEn signal.

In modes SH1b and CDSb, the input SHD or SHD and SHP signals are 'gated' by the internal AFEPHASEn signal to create the internal Sample and Clamp signals.

In mode SH2, the SAMPLE and HOLD timing signals are directly input to the sampling stage of the AFE. Subsequent stages are still clocked by the selected AFEPHASEn and MCLK.

In mode SH3, the SAMPLE and HOLD timing signals are directly input to the sampling stage of the AFE, **and are also used to set the internal AFEPHASE timing for subsequent stages**. In this mode, **CLPIN is not required to set the AFEPHASE timing. SH3 mode only supports ADC Rate MCLK**.

Please refer to the timing diagrams in Figure 21 through Figure 23 to see the relationship between the sample timing inputs and the internal AFEPHASEn signal.

7.5.3 Timing Monitor Outputs

In timing monitor mode, the internal CLAMP and SAMPLE (CDS Mode) or SAMPLE (S/H Mode) timing signals are output on the DR[3:2] pins. This enables easy confirmation of the actual internal timing configuration. Timing monitor mode is enabled by setting Register 0x00, Bit 1 = 1.

Table 7 describes the signals present on the DR[2] and DR[3] outputs in the different timing modes:

Table 7. Signal Presets

SAMPLE MODE	DR[2]	DR[3]
SH2, SH3	SH Sample Signal	PGA Sample B (active low)
SH1a, SH1b	SH Sample Signal	SH Sample Signal
CDSa, CDSb	Sample Signal Level	Sample Reference Level

7.5.4 Output Data Test Pattern Generation

Special test patterns will be generated to help in testing data processing. Four basic types of waveform can be generated and they are:

- Fixed Pattern
- Horizontal Gradation Pattern (main scan)
- Vertical Gradation Pattern (sub-scan)
- Lattice Pattern

By varying the parameters, waveforms of different timing and amplitude can be created. Parameters for the test patterns are programmable and the following registers are defined:

Table 8. Register Definitions for Test Pattern Parameters

REGISTER	DEFINITION
PK_DET_ST	This register defines the start of the Valid Pixel region from the rising edge of CLMPIN or BLKCLP, in Pixels.
PK_DET_WID	This register defines the duration (pixels) of the Valid Pixel region.
PATSW	Enable/Disable test pattern output.
PATMODE	Sets which test pattern mode is used: • 00 = Fixed code • 01 = Horizontal Gradation • 10 = Vertical Gradation • 11 = Lattice
PATREGSEL	Test pattern can be initiated on a single color or all three colors at the same time. When only one color is selected, the other colors are set to maximum 1023 code. • 00 = All colors • 01 = Red • 10 = Green • 11 = Blue
TESTPLVL	Output code 0 to 1023. In Fixed Pattern it is code output during the Valid Pixel range. During Horizontal Gradation and Vertical Gradation it is used as the initial code. In Lattice Pattern it is the level during the Valid Pixel range except for the first pixel every PATW pixels in the horizontal range and for first line every PATW lines.

Table 8. Register Definitions for Test Pattern Parameters (continued)

REGISTER	DEFINITION
PATW	Gradation pitch, this is interval at which the pattern Code Step provided in PATS register is applied.
PATS	Pattern Code Step, this contains the code step increment applied every PATW interval.
LINE_INT	Test pattern output delay. This defines the delays in number of lines between Red to Green and Green to Blue. This sequence is fixed, R->G->B, and when this register is 0, all colors switch simultaneously. This delay is used only on the initial start and the sequence of colors is fixed.

7.5.5 Fixed Pattern

Outputs fixed code in the TESTPLVL register during Valid Pixel range.

7.5.6 Horizontal Gradation

Code in the TESTPLVL is outputted initially in the PATW pixels of the Valid Pixel region, and then code is incremented by PATS value every PATW pixels for the rest of the active region. If the code reaches the maximum (less than or equal to 1023), it is reset to the initial value in TESTPLVL and pattern repeated. Same sequence is repeated for the all the lines.

7.5.7 Vertical Gradation

Code in the TESTPLVL is outputted initially in the first PATW lines of the scan and fixed for all of the Valid Pixel region, and then the code is incremented by PATS value every PATW lines and the new code is applied during active region till the next increment. This is repeated till code reaches the maximum (less than or equal to 1023) then the code is reset to the initial value and the sequence repeated.

7.5.8 Lattice Pattern

This is combination of Horizontal and Vertical Gradation pattern. Here the register PATW defines interval in pixels for horizontal scan and in lines for the vertical scan. At start of the test the output is set to PATS level for the whole first line and every line at PATW interval. In rest of the lines of the output goes to PATS for the first pixel then goes TESTPLVL for PATW-1 pixels, then goes back to PATS for one pixel and then to TESTPLVL for PATW-1 pixels, the cycle repeats till the end of line.

All test pattern generation continues once initiated by setting of PATSW till it is reset.

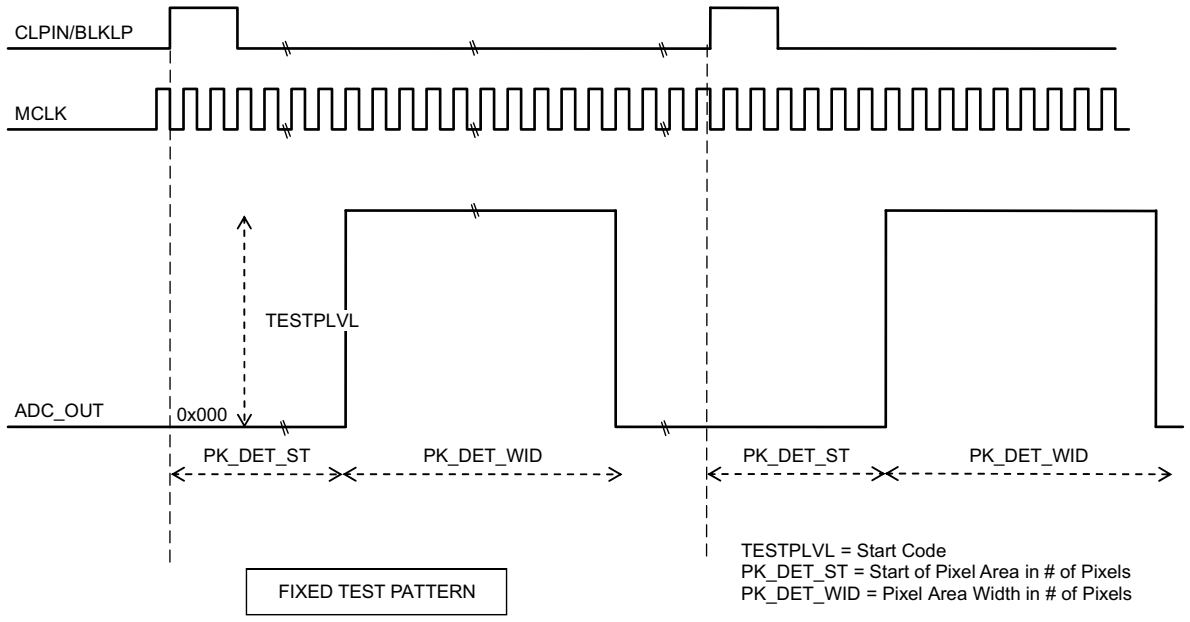


Figure 29. Fixed Test Pattern

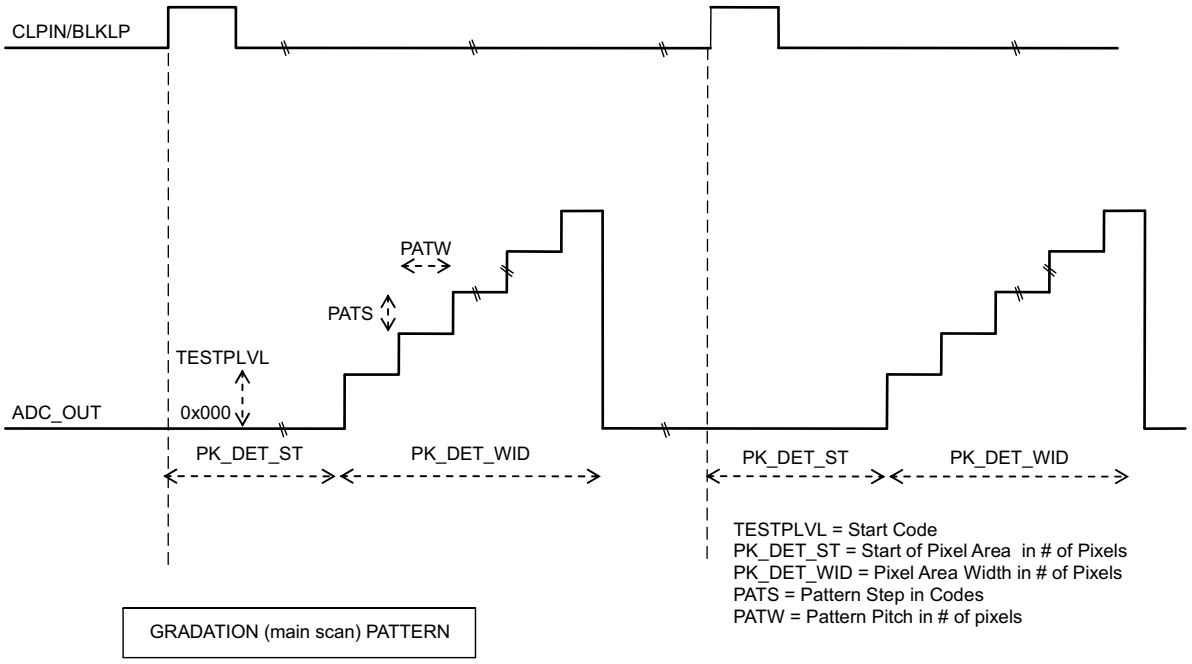


Figure 30. Gradation (Main Scan) Pattern

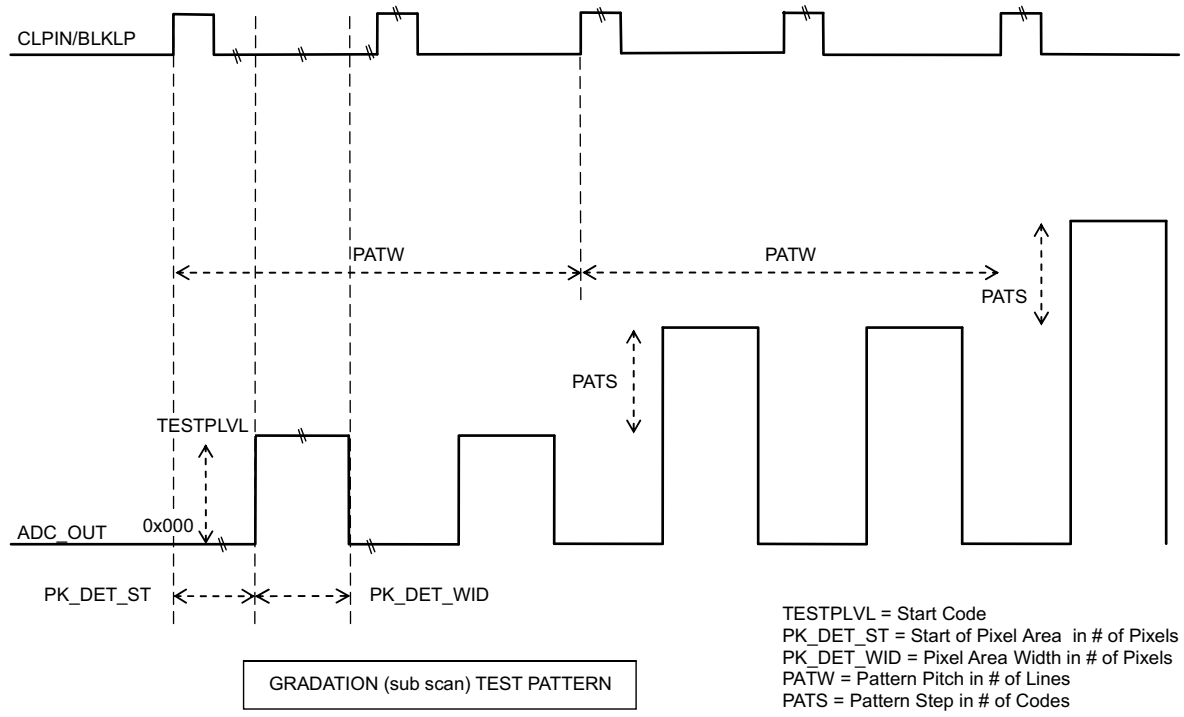


Figure 31. Gradation (Sub Scan) Test Pattern

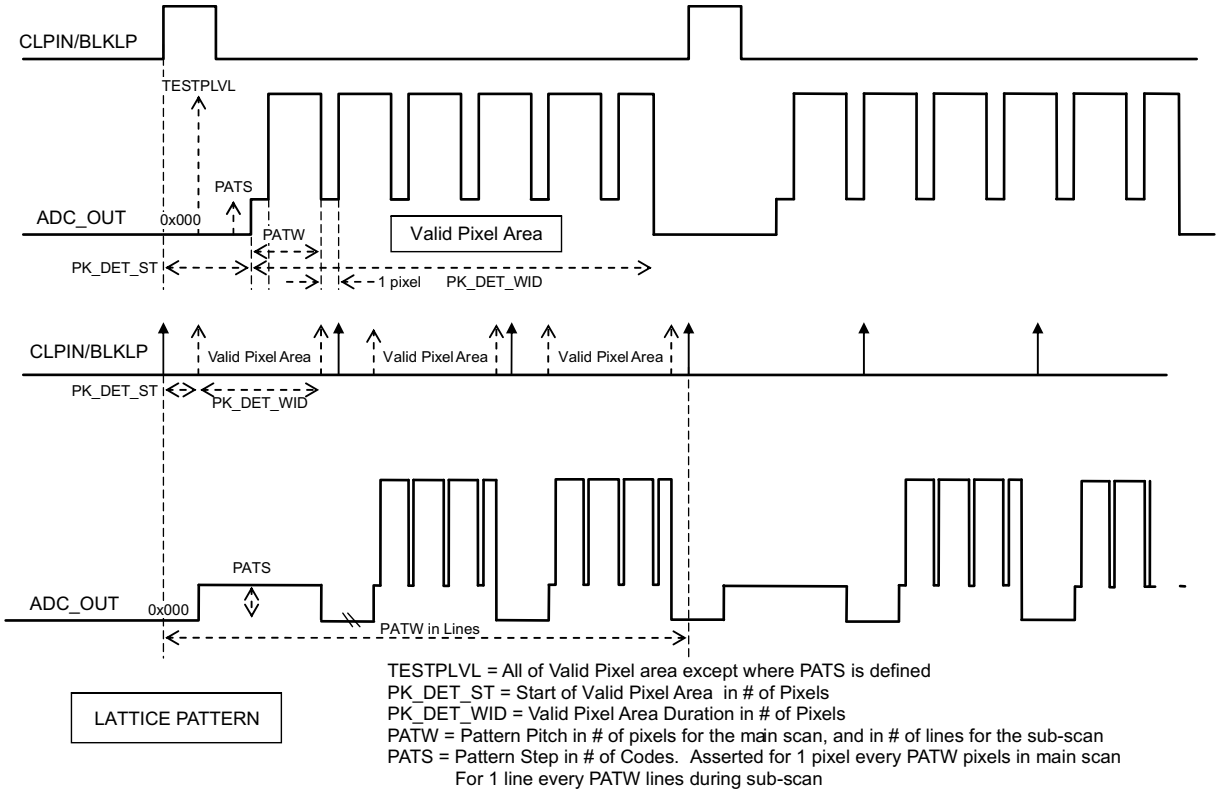


Figure 32. Lattice Pattern

7.5.9 Serial Interface

The serial control interface is based on the common microwire interface with a few specific timing details, as shown below. Bits A5, A4, A3, A2, A1, A0 select the configuration register currently being written to or read within the flat register space.

NOTE

The serial interface is initially configured to work in the absence of MCLK. Once MCLK is established, the configuration can be changed to work with MCLK. This is done by setting the Serial Interface Mode bit in Register 0x01, bit 3 = 1. Operation with MCLK will reduce any timing restrictions required in the non-MCLK mode. In addition, the Auto Clear of AGC Status will only work in MCLK Present mode.

7.5.10 Serial Write

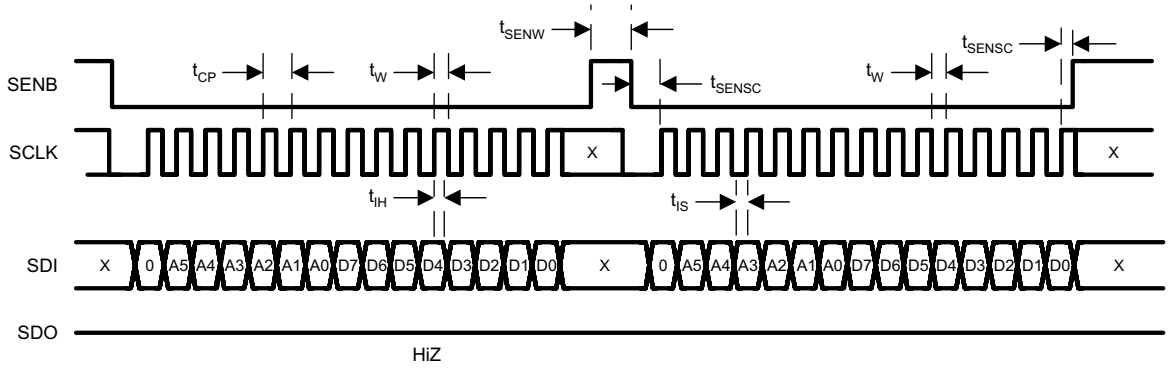


Figure 33. Serial Write

- The positive edge of SCLK is used to receive data on SDI.
- Last 15 bits of data before SEN toggled high will be loaded into AFE.
- A command whose length is less than 15 bits will be discarded.
- SDO will be Hi-Z during write operation.
- At the second cycle shown above, either read or write command is possible.
- The MODE bit must be “0” when writing to registers.
- A Write command consists of one MODE bit, 6 address bits and 8 data bits.
- While SEN is high, the AFE will accept either high or low with respect to SCLK and SDI.

7.5.11 Serial Read

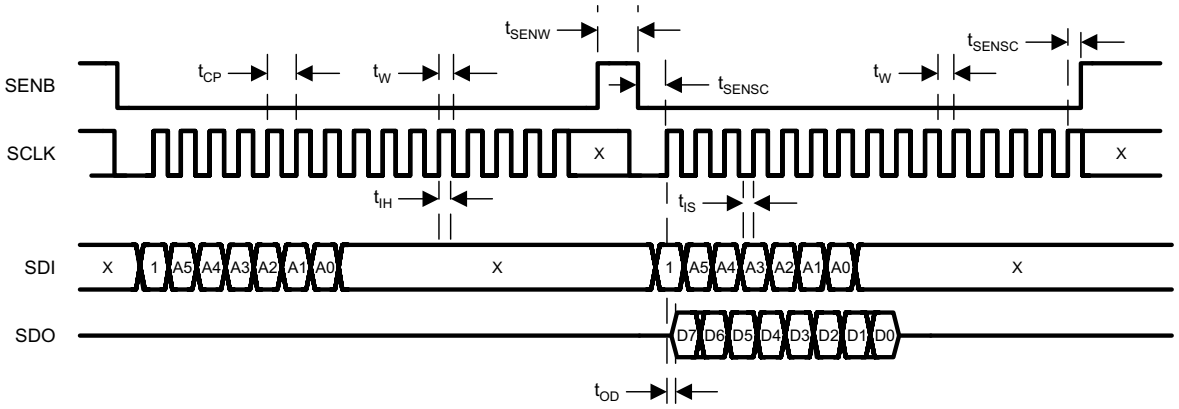


Figure 34. Serial Read

- The positive edge of SCLK is used to receive data on SDI.
- Last 15 bits of data before SEN goes high will be loaded.
- Command whose length is less than 15 bits will be discarded.
- Readout data will appear on SDO at the second cycle above.
- The readout data is clocked at the positive edge of SCLK.
- SDO is Hi-Z except when read out data appears on SDO.
- At the second cycle shown above, either read or write command is possible.
- The MODE bit must be “1” when reading from registers.
- A Read command will contain one MODE bit, 6 address bits, and 8 dummy data bits which are ignored.
- While SEN is high, the AFE will accept either high or low with respect to SCLK and SDI.

7.6 Register Maps

7.6.1 Configuration Registers

Table 9. Register Summary

HEX ADDRESS (A5-A0)	REGISTER NAME	COMMENTS
0x00 to 0x06	Configuration 0 to 6	Configuration settings
0x07	Device Revision	
0x08	GA_R1	OS_R1 Channel Gain and Offset Registers (CDS / SH Gain is NOT located here)
0x09	C_OFFS_R1	
0x0A	F_OFFS_R1_MSB	
0x0B	F_OFFS_R1_LSB	
0x0C	GA_R2	OS_R2 Channel Gain and Offset Registers
0x0D	C_OFFS_R2	
0x0E	F_OFFS_R2_MSB	
0x0F	F_OFFS_R2_LSB	
0x10 to 0x13		OS_G1 Channel Gain and Offset Registers
0x14 to 0x17		OS_G2 Channel Gain and Offset Registers
0x18 to 0x1B		OS_B1 Channel Gain and Offset Registers
0x1C to 0x1F		OS_B2 Channel Gain and Offset Registers
0x20	TARG_BLK_R	
0x21	TARG_BLK_G	
0x22	TARG_BLK_B	
0x23	Black Level Loop Control	
0x24	Black Level Loop Settings	
0x25	CDAC Threshold for BLK LP MSB	
0x25	CDAC Threshold for BLK LP LSB	
0x27	Fast Mode	
0x28	White Level Loop Control	
0x29	PK_AVG	
0x2A	PK_DET_ST_MSB	
0x2B	PK_DET_ST_LSB	
0x2C	PK_DET_WID_MSB	
0x2D	PK_DET_WID_LSB	
0x2E	AGCDuration	
0x2F	AGCTargetMSB	
0x30	AGCTargetLSB	
0x31	AGCTolerance	
0x32	AGC_BLKINT	
0x33	AGC STATUS	
0x34 to 0x37	TBD	
0x38	Test Pattern Mode	
0x39	Test Pattern Settings 1	
0x3A	Test Pattern Settings 2	
0x3B	PATW	
0x3C	PATS	
0x3D	LINE_INTVL	
0x3E	Reserved	
0x3F	Reserved	

7.6.2 Configuration Register Details

Table 10. Configuration Registers Details

ADDR (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x00 - 0x07 CONFIGURATION REGISTERS			
0x00	ANLG_CONFG	0x28	Main Configuration • [7] = Active Input Bias (AIB) - Used for initial DC biasing of OS inputs. Disabled during image capture. – (0:Disabled, 1:OSx connected to VREF_EXT during input clamping) • [6] = Passive Input Bias (PIB) - Used for initial DC biasing of OS inputs. Disabled during image capture. – (0:Disabled, 1:Osx connected to Vdd/2 resistor ladder during input clamping) • [5] = Source Follower Enable - Used to provide higher impedance at OS inputs. Should be enabled for most applications. – (0:Disabled, 1:Enabled) • [4] = Analog Power Down – (0:Normal, 1:Powered Down) • [3] = Input Mode Select – (0:3-channel; 1:6-channel) – In 3-ch mode, OSR1, OSG1, OSB1 inputs are used. • [2] = VCLP Internal Buffer Disable – (0:Enable VCLP Buffer, 1:Disable VCLP Buffer) • [1] = Sample Timing Pulses routed to TESTO outputs – (0:Tristate, 1:Enable) – CDSa & CDSb modes: – SH SAMPLE Timing routed to TESTO_0 – SH CLAMP Timing routed to TESTO_1 – SH1a & SH1b modes: – SH SAMPLE Timing routed to TESTO_0 & TESTO_1 – SH1a & SH1b modes: – SH SAMPLE Timing routed to TESTO_0 & TESTO_1 – SH2 & SH3 modes: – SH SAMPLE Timing routed to TESTO_0 – PGA SAMPLE Timing routed to TESTO_1 • [0] = Sampling Mode Control – See Table 6 in *Sample Timing Control*.
0x01	INTF_CONFG	0x10	Interface Configuration • [7:6] = Reserved • [5] = AGC_ON pin polarity – 0 = Active LOW, 1= Active HIGH • [4] = OVP Input Protection Enable (clamp signal inputs to 1 diode drop) – (0:Disabled, 1:Enabled) • [3] = Serial Interface Mode – *In MCLK idle mode the AGC Status Auto Clear will not function. Set to MCLK present to utilize this feature. – (0:MCLK idle, 1:MCLK present) • [2:1] = Reserved – Set to 00 • [0] = Red/Blue data swap – (0:normal, 1:R/B swapped)

Table 10. Configuration Registers Details (continued)

ADDR (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x02	CLP_CONFG Sample Timing Control	0x9C	Clamp Control • [7] = Sampling Mode Control – See Table 6 in *Sample Timing Control*. • [6] = SAMPLE edge selection – (0: Rising, 1:Falling) • [5] = HOLD edge selection – (0: Rising, 1:Falling) • [4] = SHP/SHD input polarity select – (0:Active Low, 1:Active High) • [3:2] = AFEPHASEn setting (00 to 11) – (Default is 11 in 6 channel mode) – (Default is X1 in 3 channel mode) Value is 11, but upper bit is ignored in 3 channel mode. • [1] = Sampling Mode Control – See Table 6 in *Sample Timing Control*. • [0] = Clamp Control – (0:CLPIN input, 1:Clamp gated by internal sampling pulse)
0x03	CDSG_CONFIG CDS / SH Gain Enable FDAC Range Select	0x00	FDAC Range, CDS Gain Selection • [7:6] = Reserved • [5] = Blue Channel FDAC Range Select • [4] = Green Channel FDAC Range Select • [3] = Red Channel FDAC Range Select – 0: 1 CDAC LSB = 314 FDAC LSBs (Range = +/- 64 mV) – 1: 1 CDAC LSB = 184 FDAC LSBs (Range = +/- 117 mV) • [2] = Blue Channels 1 & 2 Gain Enable (0:1x; 1:2.1x-typ) • [1] = Green Channels 1 & 2 Gain Enable (0:1x; 1:2.1x-typ) • [0] = Red Channels 1 & 2 Gain Enable (0:1x; 1:2.1x-typ)
0x04	Main Configuration 4	0x00	• [7] = pbufen (passive buffer enable) – 0: disable resistor divider at VCLP_ext – 1: enable resistor divider at VCLP_ext • [6] = pd_ref – Power down VREFT/VREFB buffer only – 0: buffer = power up – 1: buffer = power down • [5] = CLPIN Sampling Edge Select – 0: sampled by the rising edge of MCLK – 1: sampled by the falling edge of MCLK • [4] = Digital Inputs Sampling Edge Select – 0: sampled by the rising edge of MCLK – 1: sampled by the falling edge of MCLK • [3:2] = Clock Range Select (TXCLK and ADCCLK are the same frequency. In 6 channel mode, TXCLK and ADCCLK are 2x the pixel rate.) – 11,10: TXCLK/ADCCLK running at 10MHz – 20 MHz – 01: TXCLK/ADCCLK running at 20MHz – 40 MHz – 00: TXCLK/ADCCLK running at 40MHz – 65 MHz • [1] = Sampling Mode Control – See Table 6 in *Sample Timing Control*. – 1: SH3 mode is disabled. – 0: SH3 mode is enabled • [0] = clock doubler select – 1: TXCLK and ADCCLK are 2x MCLK – 0: TXCLK and ADCCLK are same freq. as MCLK
0x05	Main Configuration 5	0x77	• [7:3] = Reserved (Must be kept with power on default value) • [2] = Output Enable for Blue Channels • [1] = Output Enable for Green Channels • [0] = Output Enable for Red Channels (0:Disable, 1: Enable)

Table 10. Configuration Registers Details (continued)

ADDR (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x06	SRESET	0x00	Soft Reset • [1] = FSM Reset, programmable registers are not disturbed. • [0] = REG Reset, reset all FSM, except micro-wire interface and programmable registers
0x07	Device Revision	0x10	Read Only This number reflects the device revision and updated every time any major or minor change is made to the silicon.
0x08 – 0x0F Red CHANNEL PGA GAIN, CDAC and FDAC OFFSETS			
0x08	GA_R1	0x00	• [7:0] = Red Channel 1 PGA Gain – Gain = 283/(283 - [7:0]) – Gain range is from 1x to 10x
0x09	C_OFFS_R1	0x10	• [4:0] = Red Channel 1 Offset DAC Code – Offset binary format
0x0A	F_OFFS_R1	0x80	• [7:0] = Red Channel 1 Fine Offset DAC code [10:3] – Offset binary format
0x0B	F_OFFS_R1 LSB	0x00	• [7:5] = Red Channel 1 Fine Offset DAC code [2:0] • [4:0] = Reserved
0x0C	GA_R2	0x00	• [7:0] = Red Channel 2 PGA Gain – Gain = 283/(283 - [7:0]) – Gain range is from 1x to 10x
0x0D	C_OFFS_R2	0x10	• [4:0] = Red Channel 2 Offset DAC Code – Offset binary format
0x0E	F_OFFS_R2	0x80	• [7:0] = Red Channel 2 Fine Offset DAC code [10:3] – Offset binary format
0x0F	F_OFFS_R2 LSB	0x00	• [7:5] = Red Channel 2 Fine Offset DAC code [2:0] • [4:0] = Reserved
0x10 – 0x17 GREEN CHANNEL PGA GAIN, CDAC and FDAC OFFSETS			
0x10	GA_G1	0x00	• [7:0] = Green Channel 1 PGA Gain – Gain = 283/(283 - [7:0]) – Gain range is from 1x to 10x
0x11	C_OFFS_G1	0x10	• [4:0] = Green Channel 1 Offset DAC Code – Offset binary format
0x12	F_OFFS_G1	0x80	• [7:0] = Green Channel 1 Fine Offset DAC code [10:3] – Offset binary format
0x13	F_OFFS_G1 LSB	0x00	• [7:5] = Green Channel 1 Fine Offset DAC code [2:0] • [4:0] = Reserved
0x14	GA_G2	0x00	• [7:0] = Green Channel 2 PGA Gain – Gain = 283/(283 - [7:0]) – Gain range is from 1x to 10x
0x15	C_OFFS_G2	0x10	• [4:0] = Green Channel 2 Offset DAC Code – Offset binary format
0x16	F_OFFS_G2	0x80	• [7:0] = Green Channel 2 Fine Offset DAC code [10:3] – Offset binary format
0x17	F_OFFS_G2 LSB	0x00	• [7:5] = Green Channel 2 Fine Offset DAC code [2:0] • [4:0] = Reserved

Table 10. Configuration Registers Details (continued)

ADDR (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x18 – 0x1F BLUE CHANNEL PGA GAIN, CDAC and FDAC OFFSETS			
0x18	GA_B1	0x00	• [7:0] = Blue Channel 1 PGA Gain – Gain = 283/(283 - [7:0]) – Gain range is from 1x to 10x
0x19	C_OFFS_B1	0x10	• [4:0] = Blue Channel 1 Offset DAC Code – Offset binary format
0x1A	F_OFFS_B1	0x80	• [7:0] = Blue Channel 1 Fine Offset DAC code [10:3] – Offset binary format
0x1B	F_OFFS_B1 LSB	0x00	• [7:5] = Blue Channel 1 Fine Offset DAC code [2:0] • [4:0] = Reserved
0x1C	GA_B2	0x00	• [7:0] = Blue Channel 2 PGA Gain – • Gain = 283/(283 - [7:0]) – • Gain range is from 1x to 10x
0x1D	C_OFFS_B2	0x10	• [4:0] = Blue Channel 2 Offset DAC – Offset binary format Code
0x1E	F_OFFS_B2	0x80	• [7:0] = Blue Channel 2 Fine Offset DAC code [10:3] – Offset binary format
0x1F	F_OFFS_B2 LSB	0x00	• [7:5] = Blue Channel 2 Fine Offset DAC code [2:0] • [4:0] = Reserved
0x20 - 0x27 BLACK LEVEL OFFSET CALIBRATION REGISTERS			
0x20	TARG_BLK_R	0x20	• [7] = Reserved • [6:0] = Target black level – Red Channel
0x21	TARG_BLK_G	0x20	• [7] = Reserved • [6:0] = Target black level – Green Channel
0x22	TARG_BLK_B	0x20	• [7] = Reserved • [6:0] = Target black level – Blue Channel
0x23	BLKCLP_CTL0	0x0C	Black Level Loop Control • [7:6] = # of lines black clamp compensation applied. – 00 – infinite # of lines (default) – 01 – 16 lines – 10 – 32 lines – 11 – 64 lines • [5] = Reserved • [4] = High Speed Mode Offset Integration Select – 1: Divide-by-2 – 0: Divide-by-4/3 • [3] = Auto BLKCLP Pulse Generation (0:Disable, 1:Enable • [2] = Auto black loop Enable (0:Disable. 1:Enable) • [1] = High Speed Mode Enable • [0] = Auto black loop mode – 1: Update FDAC offset correction only – 0: Update CDAC and FDAC Offset Corrections

Table 10. Configuration Registers Details (continued)

ADDR (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x24	BLKCLP_CTRL1	0x84	Digital Black Level Clamp Control • [7:3] = Pixel Averaging o 00000 4 pixels o 00001 8 pixels – 00010 12 pixels – 00011 16 pixels – 00100 20 pixels – 00101 24 pixels – 00110 28 pixels – 10000 32 pixels – 10001 64 pixels – 10010 96 pixels – 10011 128 pixels – 10100 160 pixels – 10101 192 pixels – 10110 224 pixels – 10111 256 pixels – 11000 288 pixels – 11001 320 pixels – 11010 352 pixels – 11011 384 pixels – 11100 416 pixels – 11101 448 pixels – 11110 480 pixels – 11111 512 pixels – other combinations are Reserved • [2:0] = Offset Integration – 000:Divide-by-2 – 001:Divide-by-4 – 010:Divide-by-8 – 011:Divide-by-16 – 100:Divide-by-32 – 101:Divide-by-64 – 110:Divide-by-128 – Reserved
0x25	CDAC_THLD_MSB	0x50	CDAC Threshold for BLK LP MSB Default value is 321d, so loop will change FDAC by 321 to compensate for change of 1 in CDAC. To optimize even further, this can be changed to 314d. If FDAC is set to the large range, then this value should be changed to 184d. • [7:0] = Threshold[9:2]
0x26	CDAC_THLD_LSB	0x40	CDAC Threshold for BLK LP LSB • [7:6] = Threshold[1:0] • [5:0] = Reserved. Set to 0.
0x27	High Speed Mode	0x88	• [7:5] = High Speed Mode Hysteresis • [4:0] = High Speed Mode Threshold

Table 10. Configuration Registers Details (continued)

ADDR (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x28 – 0x37 WHITE LEVEL GAIN CALIBRATION REGISTERS			
0x28	AGC_CONFG	0x00	• [7] = Incremental Search Enable – 0: Binary Search – 1: Incremental Search • [6] = Black Offset Enable – 0: Do not Use BLK_AVG during White Level Gain Calibration Loop – 1: Use BLK_AVG as offset during White Level Gain Calibration Loop (Recommended) • [5] = CLPIN or BLKCLP White Loop Trigger Select – 0: CLPIN initiates White Loop each line – 1: BLKCLP initiates White Loop each line • [4] = AGC_ON pin disable – = 0 Enable use of AGC_ON pin – = 1 Disable use of AGC_ON pin to start white calb.loop. • [3:1] = Reserved • [0] = AGC_ON. Write to 1 to enable White Level Loop. (0:Ready, 1:Enabled) – White Loop can also be enabled by asserting AGC_ON pin of pin is enabled via. Register 0x28, b4.
0x29	PK_AVE	0x04	Number of pixels in running average during white calibration loop • [2:0] = – 000: No average (1 pixel) – 001: 2 pixels – 010: 4 pixels – 011: 8 pixels – 100: 16 pixels – 101: 32 pixels
0x2A	PK_DET_ST_MSB	0x00	Starting pixel for peak detection. 16 bit value. Number of pixels after rising edge trigger event. (CLPIN or BLKCLP) (0 to 65535)
0x2B	PK_DET_ST_LSB	0x00	
0x2C	PK_DET_WID_MSB	0x00	Duration of peak detection after PK_DET_ST. 16 bit value (0 to 65535)
0x2D	PK_DET_WID_LSB	0x00	
0x2E	AGCDuration	0x10	• [7:0] = Number of lines for AGC to operate. Loop will run continuously if AGC_ON pin is held high. (0 to 255)
0x2F	AGCTargetMSB	0xE0	• [7:0] = MSB of Target Value for AGC loop (Default AGCTarget=960d) AGC_TARG = 512d + (AGCTargetMSB[7:0],AGCTargetLSB[7])
0x30	AGCTargetLSB	0x00	• [7] = LSb of Target Value for AGC loop • [6:0] = Reserved
0x31	AGCTolerance	0x28	• [7:6] = Reserved • [5:0] = Allowable error for AGC loop

Table 10. Configuration Registers Details (continued)

ADDR (HEX)	REGISTER NAME	DEFAULT (HEX)	DESCRIPTION
0x32	AGC_BLKINT	0x00	AGC Offset Integration • [2:0] = Offset Integration setting for the Black Level Loop while the AGC is on (i.e. white level loop) – 000:Divide-by-2 – 001:Divide-by-4 – 010:Divide-by-8 – 011:Divide-by-16 – 100:Divide-by-32 – 101:Divide-by-64 – 110:Divide-by-128 – Reserved
0x33	AGC STATUS	0x00	AGC Status – Read Only • [7:6] = 0 • [5] = Convergence Error Blue Ch2 • [4] = Convergence Error Blue Ch1 • [3] = Convergence Error Green Ch2 • [2] = Convergence Error Green Ch1 • [1] = Convergence Error Red Ch2 • [0] = Convergence Error Red Ch1
0x34	Reserved	0x32	Must be kept with Power-on-default values.
0x35	Reserved	0x54	Must be kept with Power-on-default values.
0x36	Reserved	0x00	Must be kept with Power-on-default values.
0x37	Reserved	0x00	Must be kept with Power-on-default values.
0X38 to 0X3F USER TEST PATTERNS REGISTERS			
0x38	TEST_PAT_CTL	0x00	Test Pattern Mode • [7] = Test Pattern Enable (PATSW) – (0:Normal Data Output, 1:Test Pattern Output Enabled) • [6:5] = Test Pattern Mode Select (PTRMODE) – 00:Fixed Code – 01:Gradation Pattern (Main Scanning) – 10:Gradation Pattern (Sub Scanning) – 11:Grid Pattern • [4:3] = Test Pattern Output Channel (PTRGBSEL) – 00:All colors – 01:Red (Other color data at 1023d) – 10:Green (Other color data at 1023d) – 11:Blue (Other color data at 1023d) • [2:0] = Reserved
0x39	TESTPLVL_MSB	0x00	• [7:0] = 8 MSb of fixed output code (TESTPLVL)
0x3A	TESTPLVL_LSB	0x00	• [7:6] = 2 LSb of fixed output code (TESTPLVL)
0x3B	PATW	0x00	• [7:0] = Gradation Pattern Pitch (0 to 255 lines)
0x3C	PATS	0x00	• [7:0] = Gradation Pattern Increment Step (0 to 255)
0x3D	LINE_INTVL	0x00	• [3:0] = Test Pattern Output Color Delay, Red to Green, Green to Blue (0 to 15 line delay)
0x3E	Reserved		
0x3F	Reserved		

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Design Requirements

See Figure 36 for an example circuit and the required minimum circuitry around the LM98519.

All power supply voltages should be provided from clean linear regulator outputs, NOT switching power supplies.

8.2 Detailed Design Procedure

1. 3.3-V Power for Analog, Digital, and Outputs (VDDA, VDDD, and VDDO) supplies. It is recommended to use a common LDO regulator for al 3.3 V supplies, using EMI filter devices and dedicated coupling to isolate any noise between buses.
2. Input Timing Signals (Ground referenced logic signal with: 2.0 V < VHigh < 3.3 V)
   (a) MCLK: Continuous clock signal at pixel rate or ADC rate of LM98519
   (b) CLPIN: Once per scan line signal used to control input clamp for DC restoration of AC coupled CCD input signals
   (c) BLKCLP: Once per scan line signal used to indicate beginning of black pixels for Black (Offset) Level Calibration
   (d) AGC_ONB – Input signal used to initiate start of White (Gain) Calibration
   (e) SHP/SAMPLE: Once per pixel signal used to control pixel sample timing
   (f) SHD/HOLD: Once per pixel signal used to control pixel sample timing
3. CCD signals at OS Inputs – These are connected to the outputs from the CCD sensor emitter follower buffer circuits. The signals are AC coupled to the AFE inputs using 0.1 uF capacitors.
4. Serial control interface from data processing module to LM98519 (Ground referenced logic signal with: 2.0 V < V_{high} < 3.3 V):
   (a) SENB – Serial enable to LM98519
   (b) SCLK – Serial clock input to LM98519
   (c) SDI – Data input to LM98519
   (d) SDO – Data output from LM98519
5. Serialized data lines connected to FPGA or chip on data processing module
6. Adjust and reconfigure the configuration register settings as needed

9 Power Supply Recommendations

9.1 Over Voltage Protection on OS Inputs

The OS inputs are protected from damage caused by transients from the sensor circuitry during power up/down. When the chip has just been powered up, the protective clamp circuits are enabled by setting Register 0x01, Bit 4 to 1. This clamps the OS inputs to VSSA with internal PMOS devices. The protective clamp circuits are disabled by setting the OVPB enable bit to 0.

The maximum voltage and input current specifications for the OS inputs when OVP is enabled are the same as those listed in *Absolute Maximum Ratings*.

Positive input signals will be clamped by the internal switch through a diode to VSSA. Negative input signals will be clamped by the internal ESD protection diode to one diode drop below VSSD. Typically this will be about 0.7 V below ground.

Table 11. OVP Enable Bit Settings

OVP ENABLE BIT (Register 0x01, Bit 4)	OVER VOLTAGE PROTECTION INPUT CLAMPING
0	Disabled
1	Enabled

10 Layout

10.1 Layout Guidelines

1. Use Figure 35 configuration for powering the device.

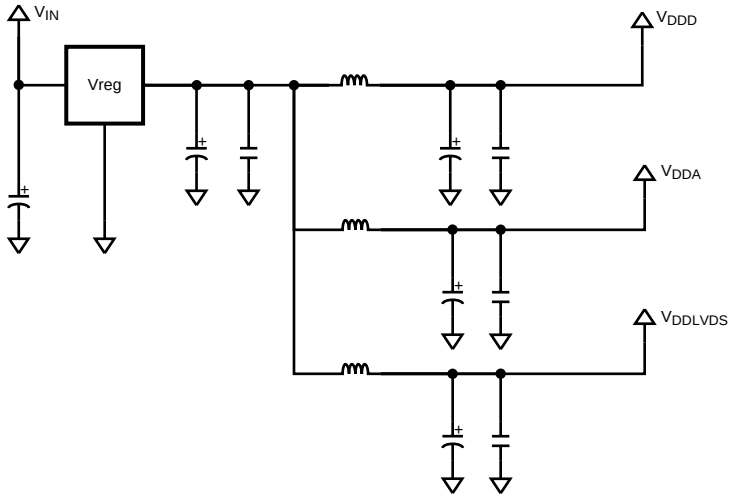


Figure 35. Recommended Setup for Powering Device

2. Place decoupling cap(s) next to every supply pin to the ground plane close by.
3. Use a multi-layer boards as shown in Figure 35 to ease routing, and to provide a low inductance ground plane.
4. Beware of via inductance and when necessary increase the number and / or diameter of vias to reduce inductance
5. Use ground plane “keep out” areas under sensitive nodes to minimize parasitic capacitance

10.2 Layout Example

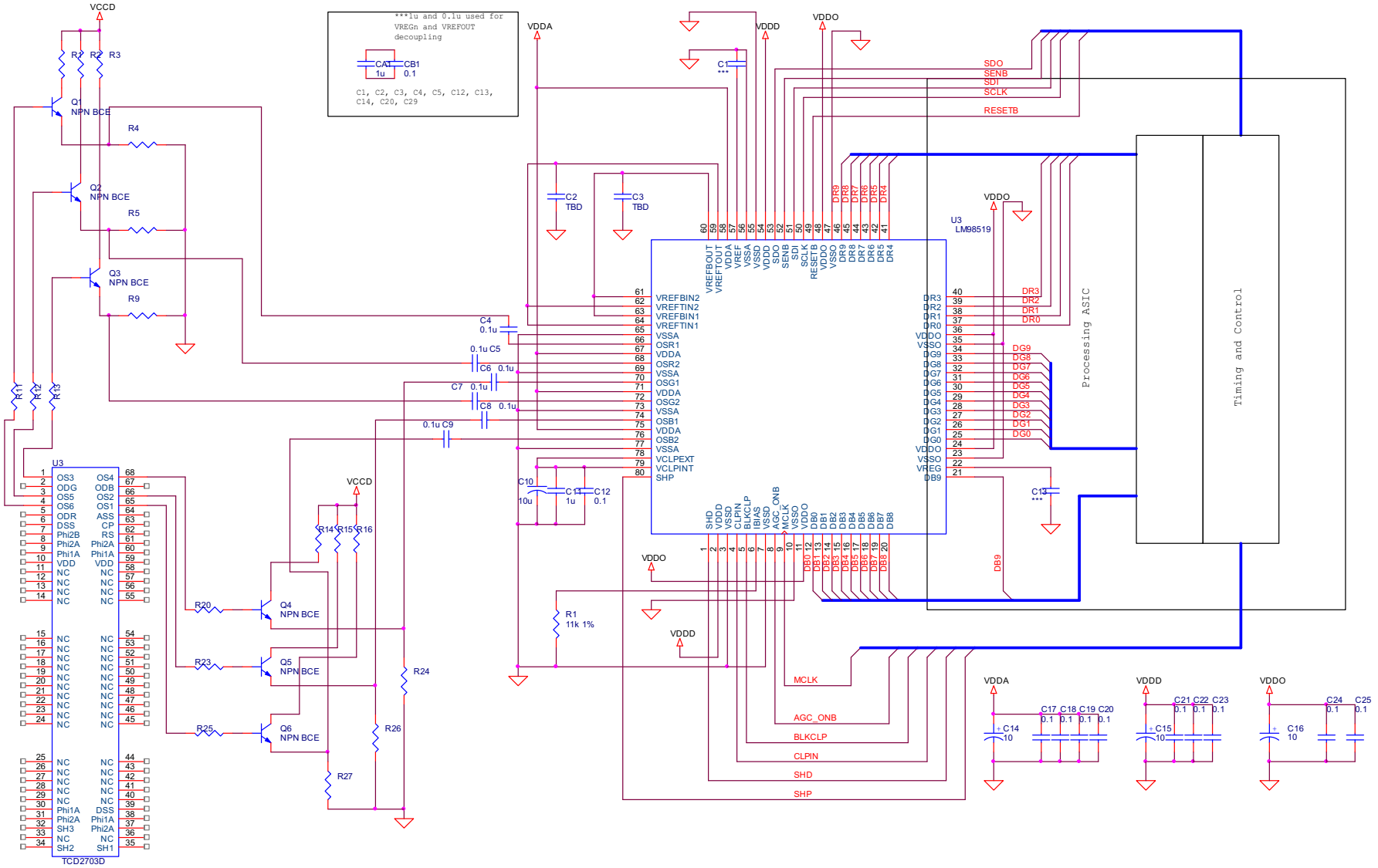


Figure 36. LM98519 Typical Application

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM98519VHB/NOPB	ACTIVE	TQFP	PFC	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	LM98519VHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

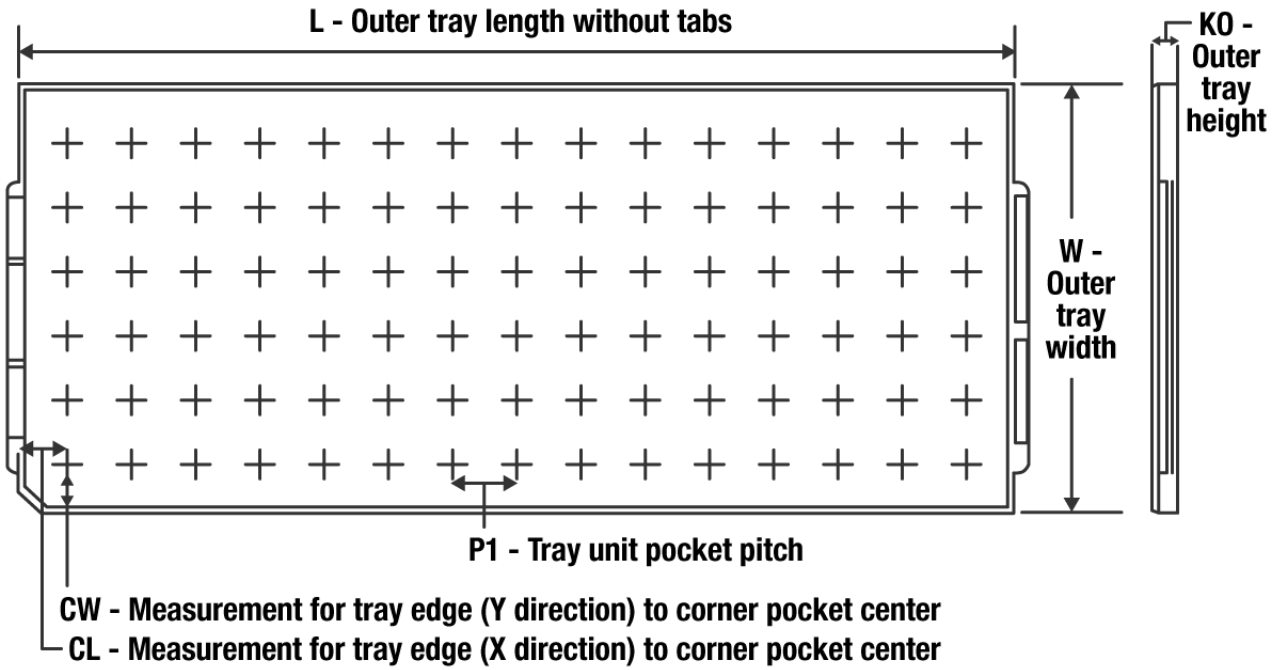
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

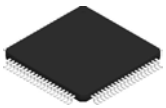
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LM98519VHB/NOPB	PFC	TQFP	80	119	7X17	150	322.6	135.9	7620	17.9	14.3	13.95

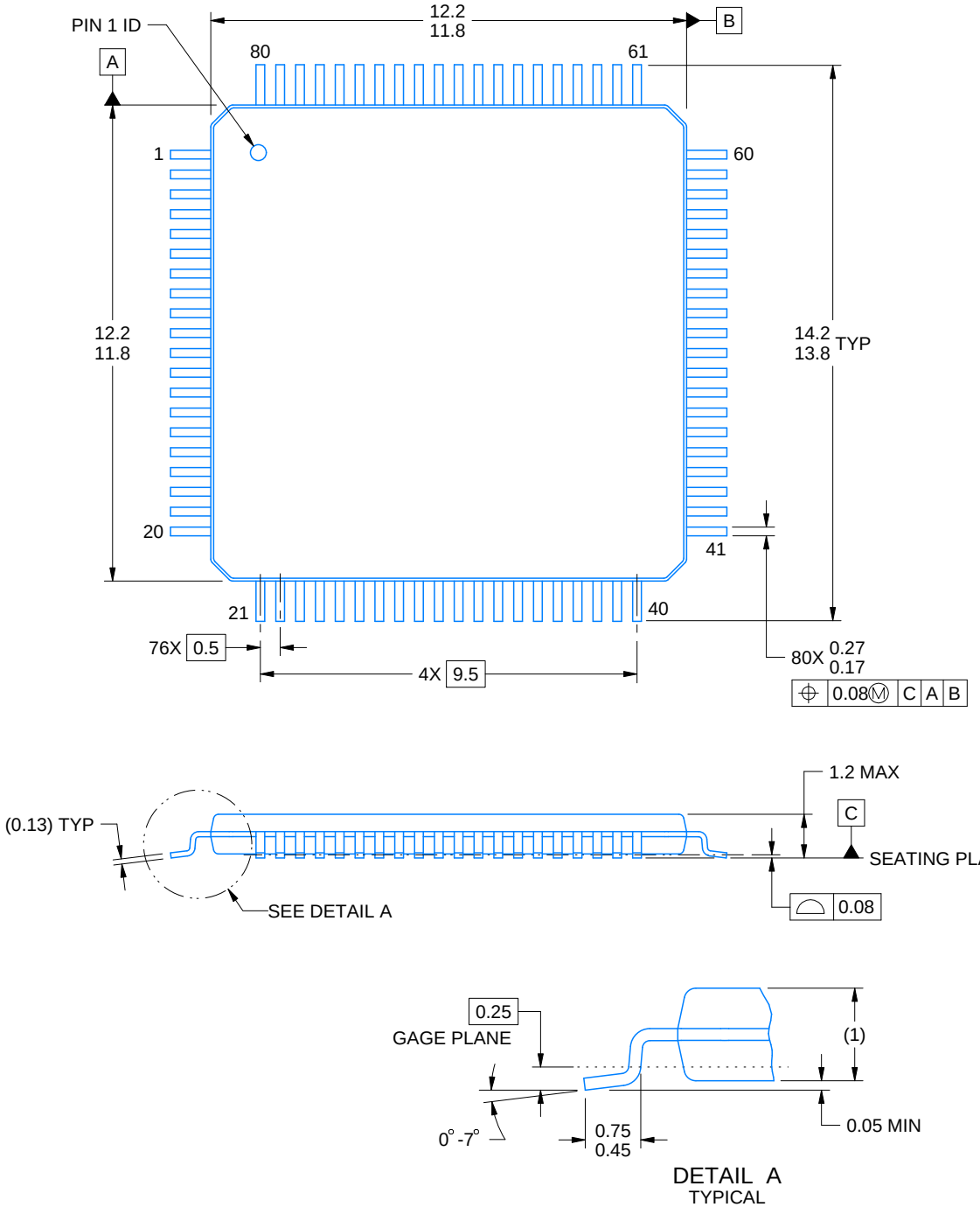


PACKAGE OUTLINE

PFC0080A

TQFP - 1.2 mm max height

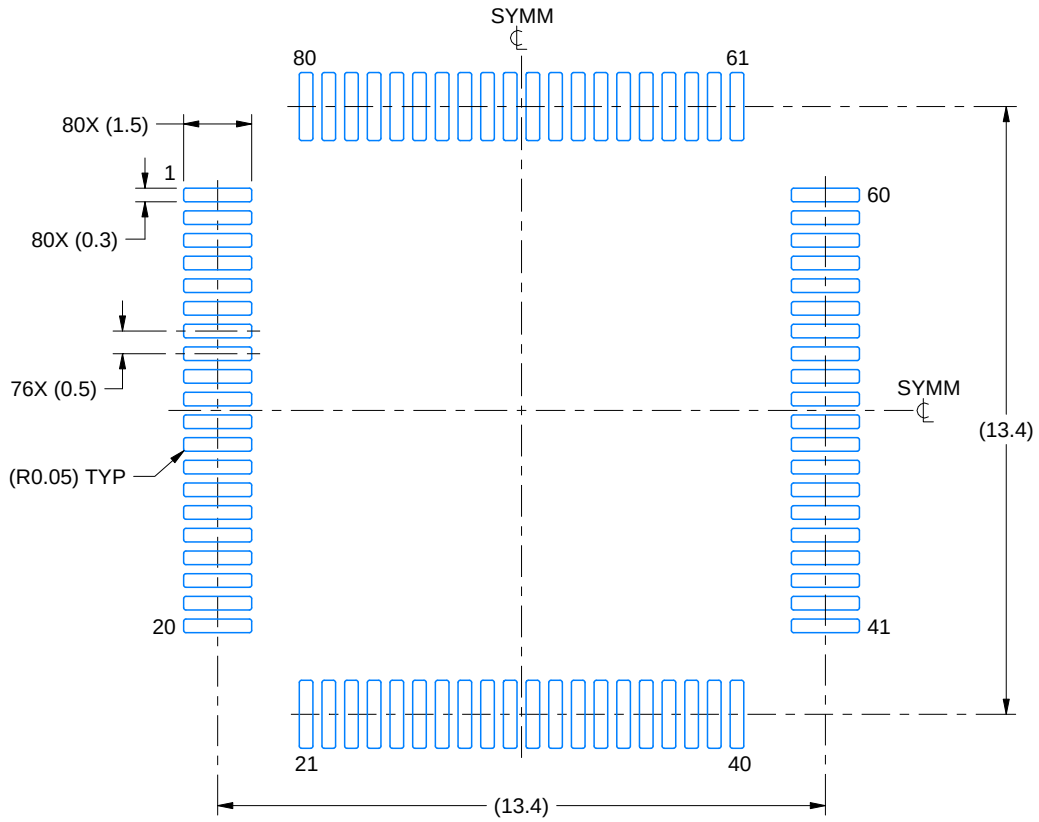
PLASTIC QUAD FLATPACK



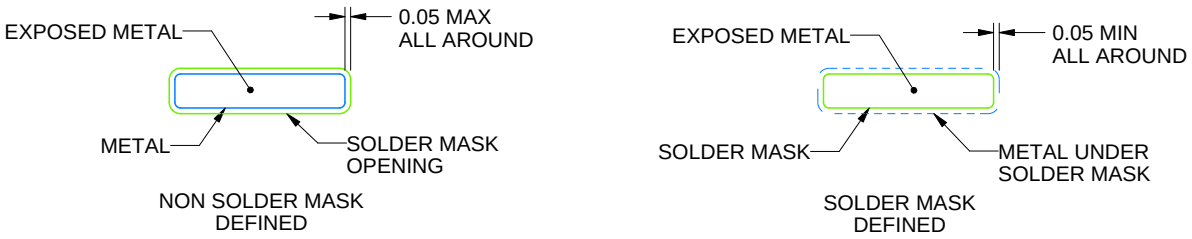
4215165/B 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

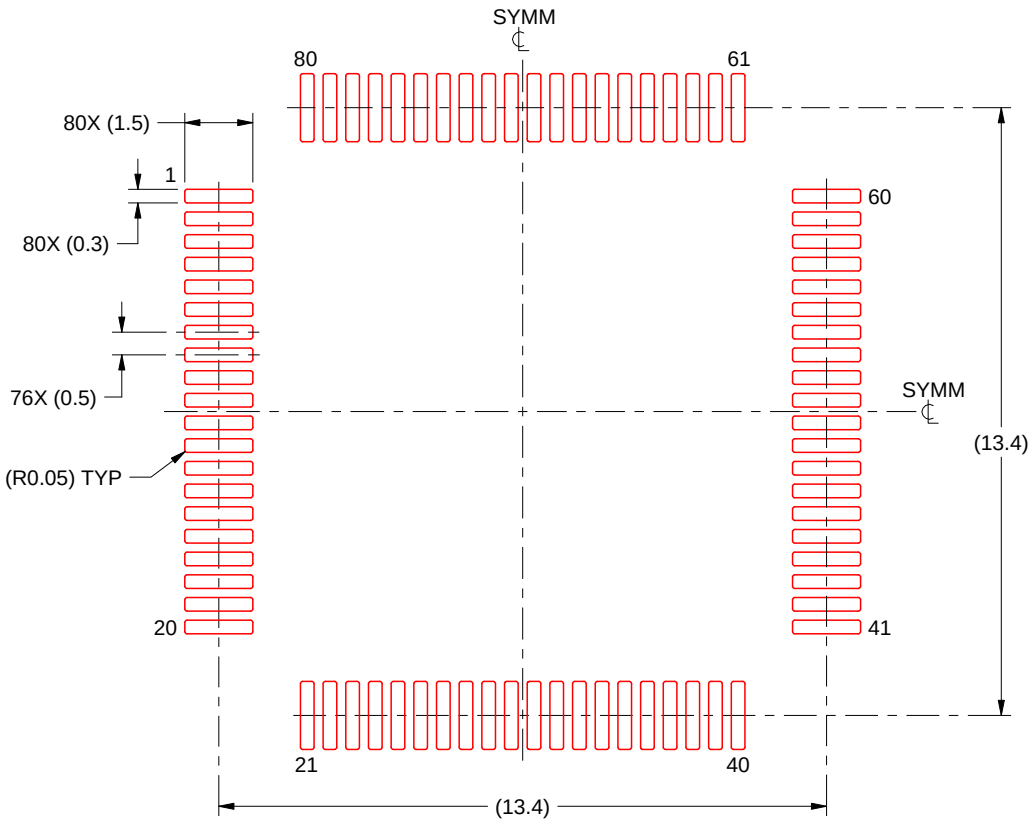


SOLDER MASK DETAILS

4215165/B 06/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215165/B 06/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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