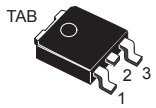
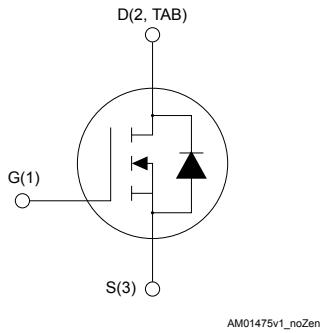
# N-channel 650 V, 425 mΩ typ., 11 A MDmesh II Power MOSFET in a DPAK package




DPAK




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STD11NM65N | 650 V | 455 mΩ | 11 A |

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

STPOWER

| Product status link |
|---|
| STD11NM65N |

| Product summary | |
|---|---|
| **Order code** | STD11NM65N |
| **Marking** | 11NM65N |
| **Package** | DPAK |
| **Packing** | Tape and reel |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 650 | V |
| $V_{GS}$ | Gate-source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 11 | A |
| | Drain current (continuous) at $T_C$ = 100 °C | 7 | |
| $I_{DM}$ (1) | Drain current (pulsed) | 44 | A |
| $P_{TOT}$ | Total power dissipation at $T_C$ = 25 °C | 110 | W |
| $I_{AR}$ | Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max) | 3 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 147 | mJ |
| dv/dt (2) | Peak diode recovery voltage slope | 15 | V/ns |
| $T_{stg}$ | Storage temperature range | -55 to 150 | °C |
| $T_J$ | Operating junction temperature range | | °C |

1. *Pulse width limited by safe operating area.*
2. *$I_{SD}$ ≤ 11 A, di/dt ≤ 400 A/µs, $V_{DS}$ (peak) ≤ $V_{(BR)DSS}$.*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Thermal resistance, junction-to-case | 1.14 | °C/W |
| $R_{thJA}$ (1) | Thermal resistance, junction-to-ambient | 50 | °C/W |

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

# 2 Electrical characteristics

$T_C$ = 25 °C unless otherwise specified.

**Table 3. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 V | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V, $T_C$ = 125 °C (1) | | | 100 | |
| $I_{GSS}$ | Gate body leakage current | $V_{GS}$ = ±25 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 5.5 A | | 425 | 455 | mΩ |

1. *Specified by design, not tested in production.*

**Table 4. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz,$V_{GS}$ = 0 V | - | 800 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 50 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.9 | - | pF |
| $C_{oss\ eq.}$ (1) | Equivalent output capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 520 V | - | 133 | - | pF |
| $R_g$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 A | - | 4.2 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 11 A, $V_{GS}$ = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 29 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 3.9 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 16 | - | nC |

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 5. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 325 V, $I_D$ = 5.5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 15.5 | - | ns |
| $t_r$ | Rise time | | - | 10.8 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 11 | - | ns |
| $t_f$ | Fall time | | - | 47 | - | ns |

**Table 6. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 11 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 44 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 11 A, $V_{GS}$ = 0 V | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 11 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 418 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 4.4 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 21 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 11 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_J$ = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 530 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 5.6 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 21 | | A |

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

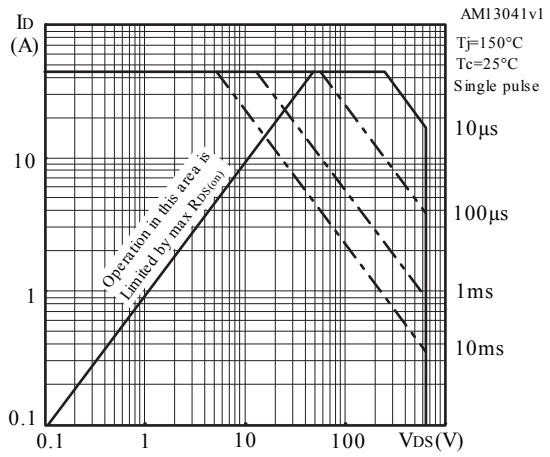



**Figure 2. Normalized transient thermal impedance**

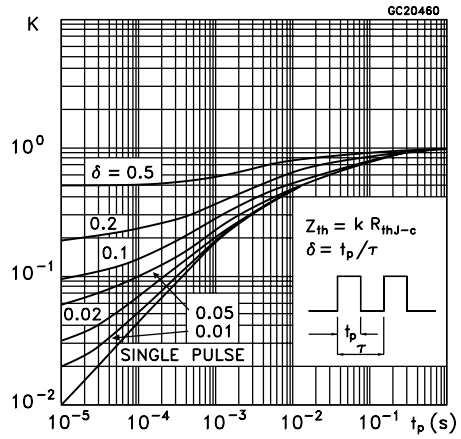



**Figure 3. Typical output characteristics**

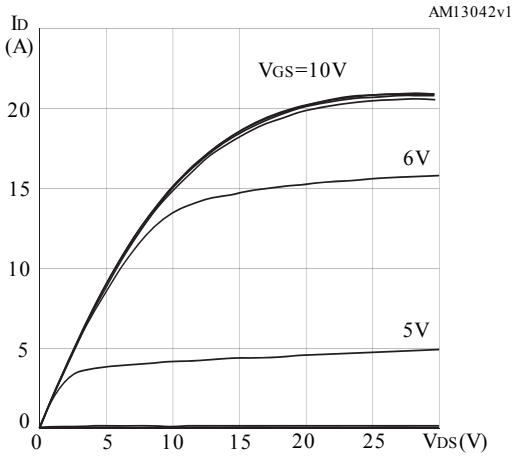



**Figure 4. Typical transfer characteristics**

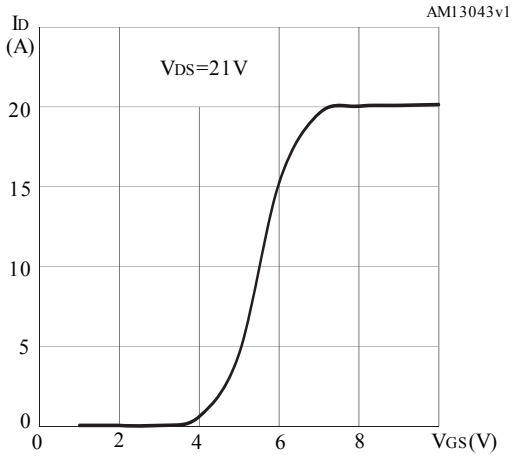



**Figure 5. Typical gate charge characteristics**

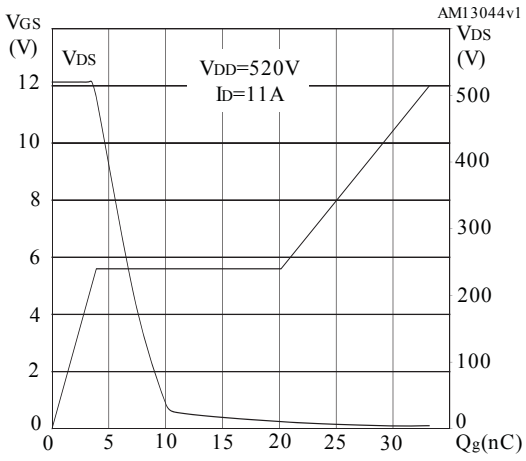



**Figure 6. Typical drain-source on-resistance**

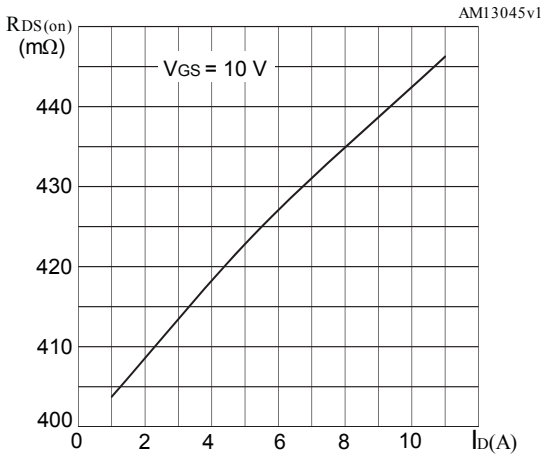


**Figure 7. Typical capacitance characteristics**

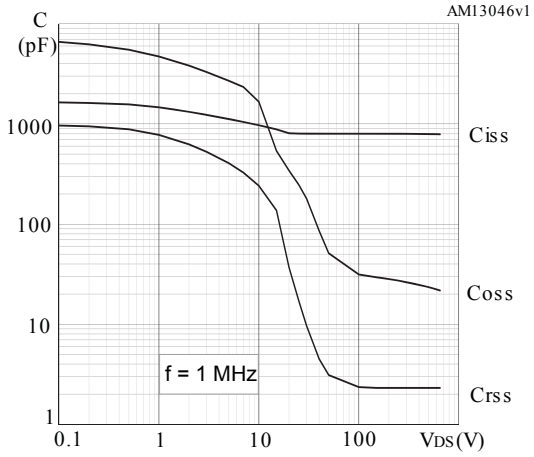



**Figure 8. Typical output capacitance stored energy**

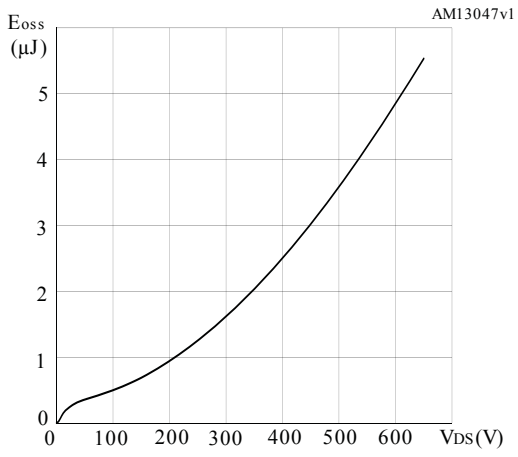



**Figure 9. Normalized gate threshold vs temperature**

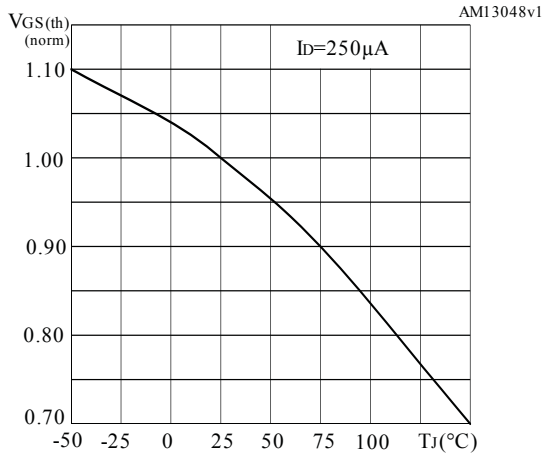



**Figure 10. Normalized on-resistance vs temperature**

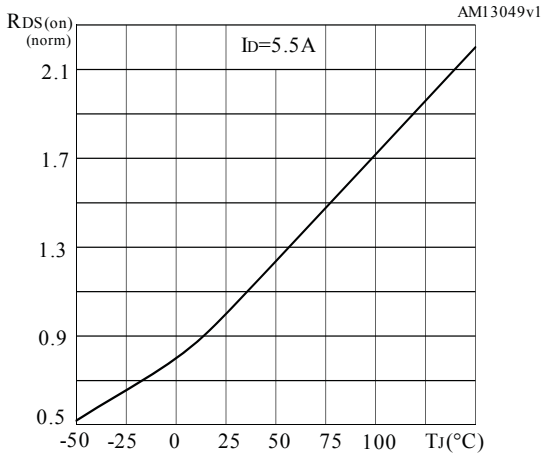



**Figure 11. Normalized breakdown voltage vs temperature**

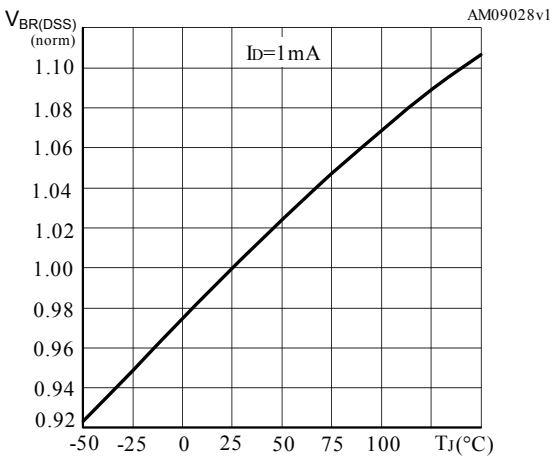
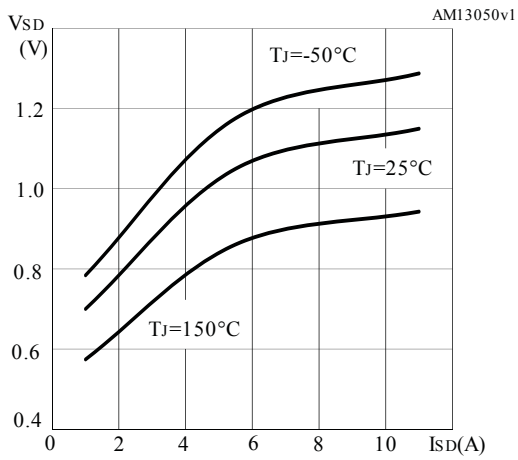



**Figure 12. Typical reverse diode forward characteristics**



# 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

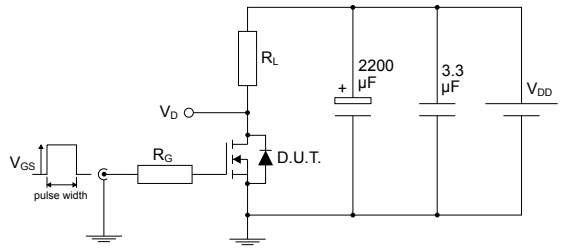



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**Figure 14. Test circuit for gate charge behavior**

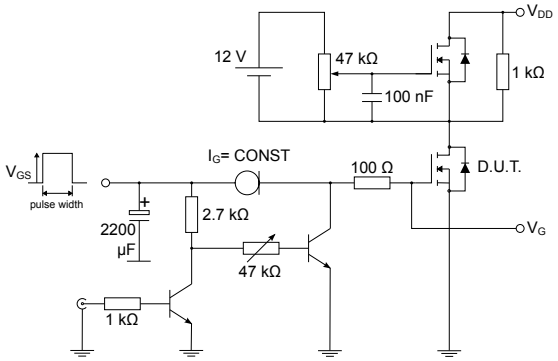


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**Figure 15. Test circuit for inductive load switching and diode recovery times**

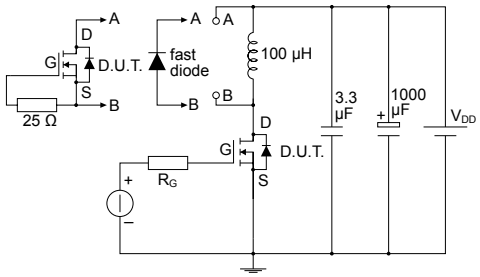


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**Figure 16. Unclamped inductive load test circuit**

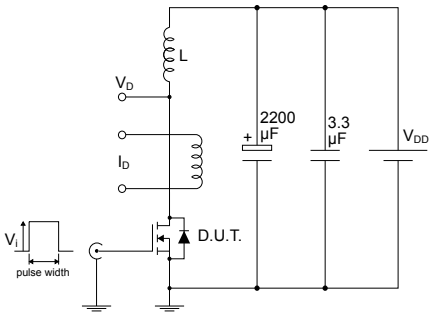


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**Figure 17. Unclamped inductive waveform**

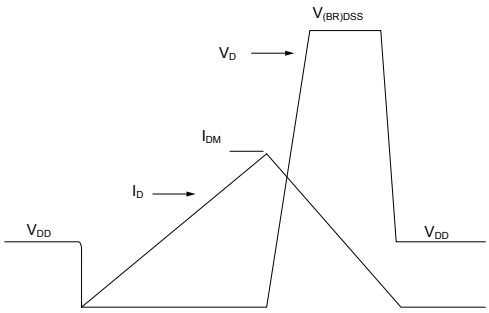


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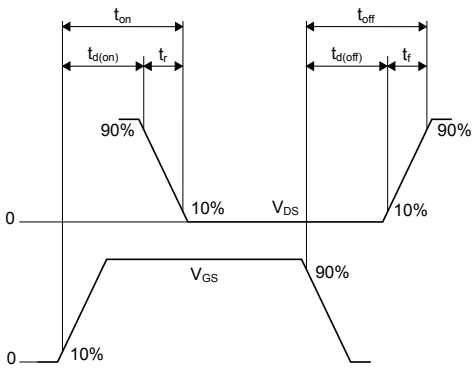
**Figure 18. Switching time waveform**

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# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 4.1 DPAK (TO-252) type A2 package information

**Figure 19. DPAK (TO-252) type A2 package outline**

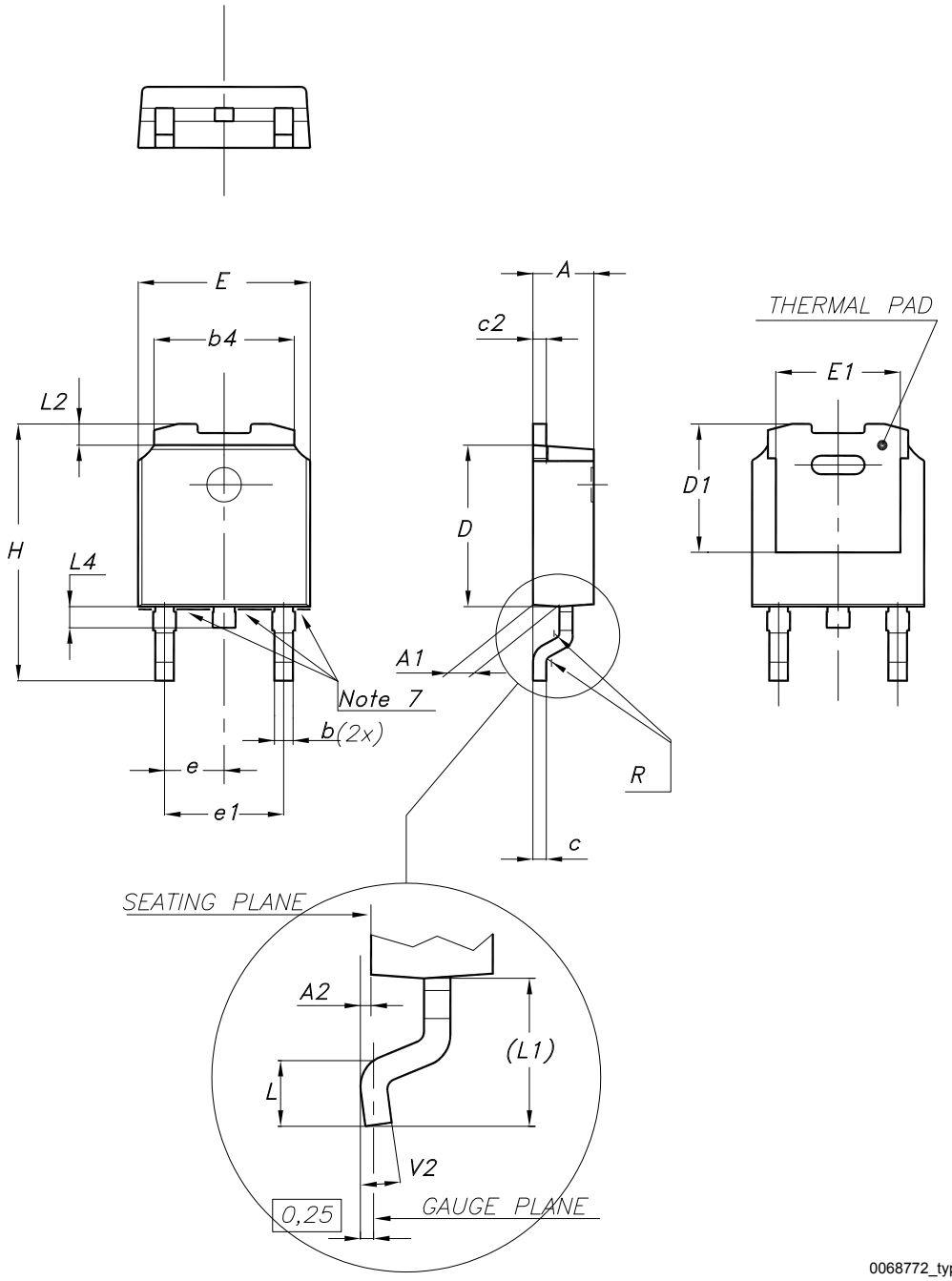


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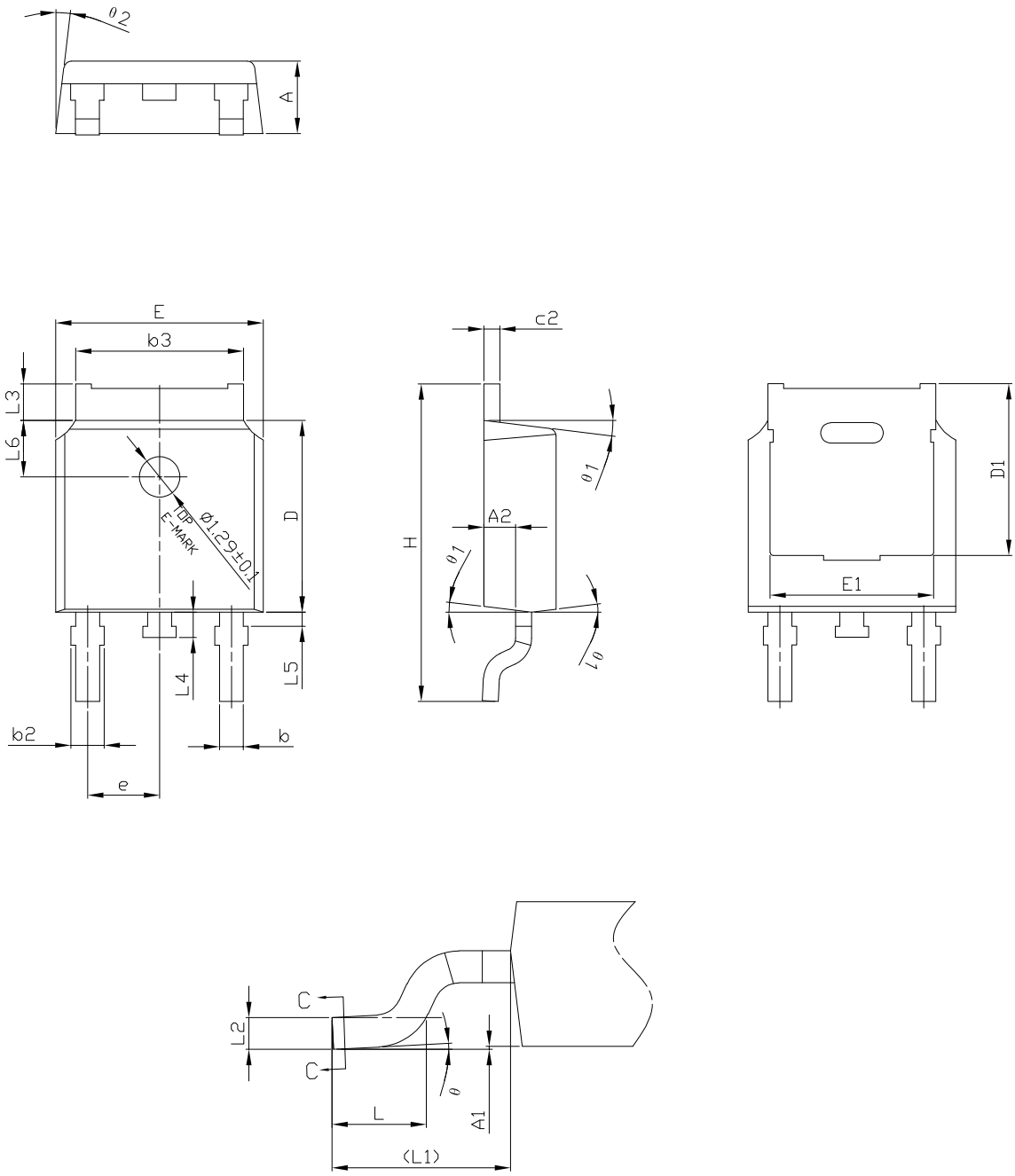
Table 7. **DPAK (TO-252) type A2 mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 5.10 | 5.20 | 5.30 |
| e | 2.159 | 2.286 | 2.413 |
| e1 | 4.445 | 4.572 | 4.699 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| L1 | 2.60 | 2.80 | 3.00 |
| L2 | 0.65 | 0.80 | 0.95 |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

## 4.2 DPAK (TO-252) type C3 package information

Figure 20. **DPAK (TO-252) type C3 package outline**

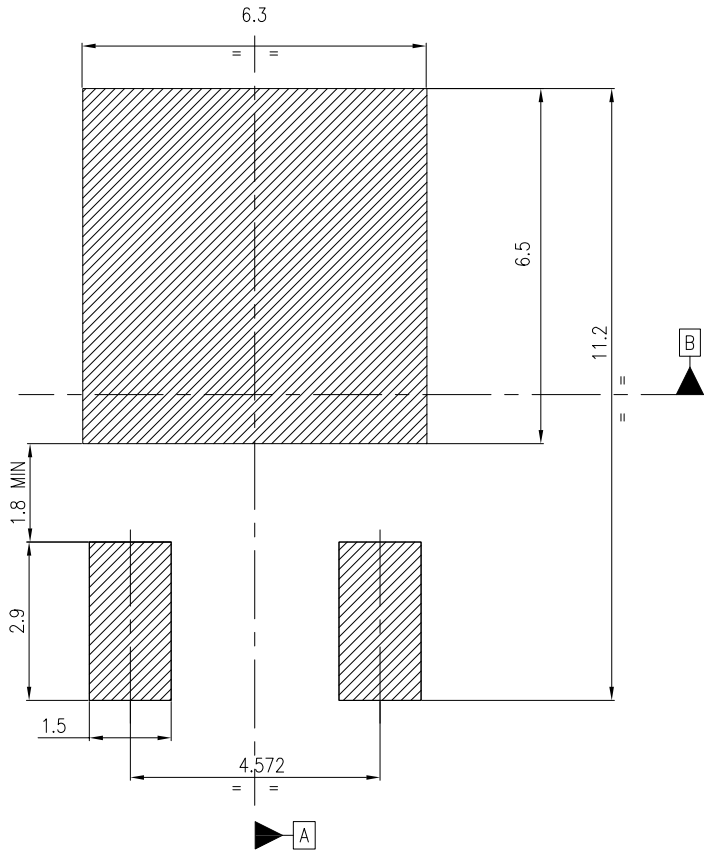



0068772_type-C3_rev34

Table 8. **DPAK (TO-252) type C3 mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | 2.30 | 2.38 |
| A1 | 0.00 | | 0.10 |
| A2 | 0.90 | 1.01 | 1.10 |
| b | 0.72 | | 0.85 |
| b2 | 0.72 | | 1.10 |
| b3 | 5.13 | 5.33 | 5.46 |
| c | 0.47 | | 0.60 |
| c2 | 0.47 | | 0.60 |
| D | 6.00 | 6.10 | 6.20 |
| D1 | 5.20 | 5.45 | 5.70 |
| E | 6.50 | 6.60 | 6.70 |
| E1 | 5.00 | 5.20 | 5.40 |
| e | 2.186 | 2.286 | 2.386 |
| H | 9.80 | 10.10 | 10.40 |
| L | 1.40 | 1.50 | 1.70 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.90 | | 1.25 |
| L4 | 0.60 | 0.80 | 1.00 |
| L5 | 0.15 | | 0.75 |
| L6 | 1.80 REF | | |
| θ | 0° | | 8° |
| θ1 | 5° | 7° | 9° |
| θ2 | 5° | 7° | 9° |

Figure 21. **DPAK (TO-252) recommended footprint (dimensions are in mm)**




Notes:

1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664−1)

2) The device must be positioned within ⌖ 0.05 A B

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## 4.3 DPAK (TO-252) packing information

Figure 22. **DPAK (TO-252) tape outline**

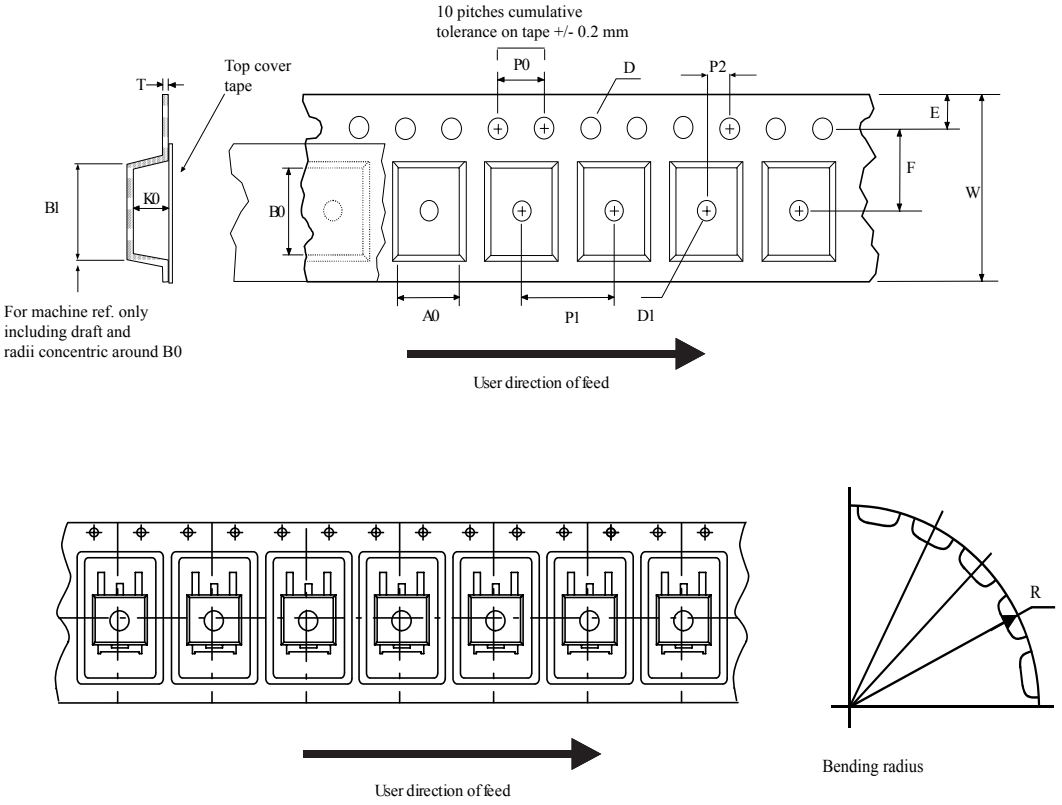

Figure 23. **DPAK (TO-252) reel outline**

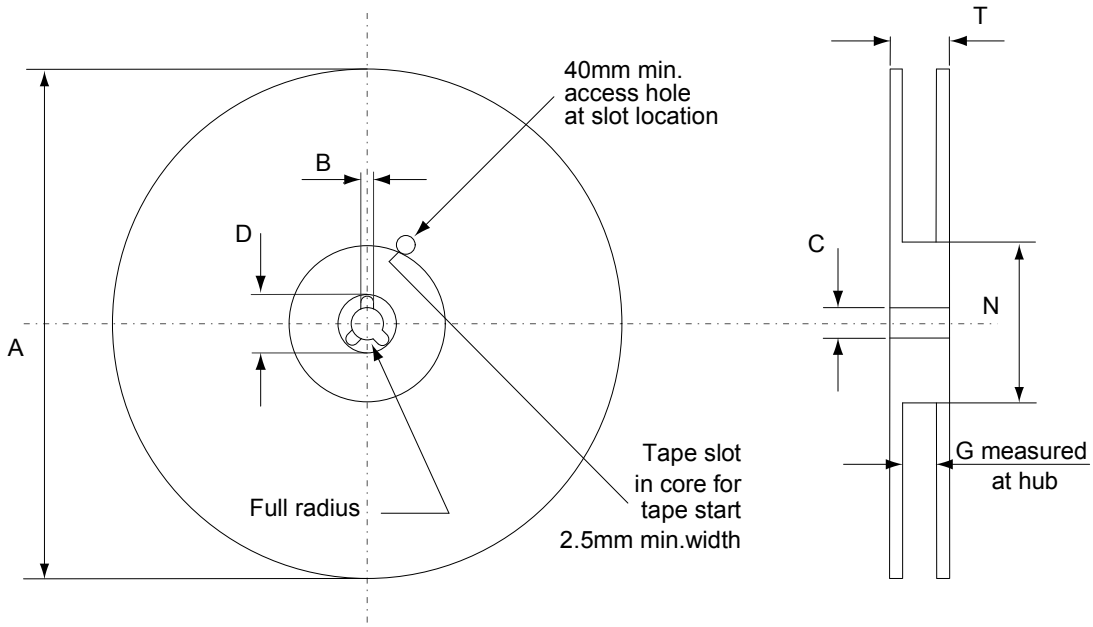


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Table 9. **DPAK (TO-252) tape and reel mechanical data**

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

## Revision history

Table 10. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 01-Jun-2007 | 1 | First release. |
| 03-Oct-2007 | 2 | Added device in D2PAK and updated *Figure 12: Capacitance variations* |
| 20-Jul-2012 | 3 | Document status promoted from preliminary to production data.<br>Updated *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data*.<br>Minor text changes. |
| 15-Jul-2013 | 4 | Updated *Table 1: Device summary* and *Section 4: Package mechanical data.* |
| 09-May-2023 | 5 | The part numbers STF11NM65N, STFI11NM65N and STP11NM65N have been moved to separate datasheet and the document has been updated accordingly.<br>Updated Section 4.1 DPAK (TO-252) type A2 package information.<br>Added Section 4.2 DPAK (TO-252) type C3 package information.<br>Minor text changes. |

# Contents