MOSFET - Power, Single N-Channel, TOLL

NTBLS1D5N08MC

80 V, 1.53 mΩ, 298 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	80	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	298	A
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	P_D	250	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	32	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	2.9	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	4487	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	192	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 31 A, L = 3 mH)			E_{AS}	1441	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.5	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	43	

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ON Semiconductor®

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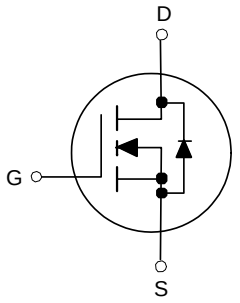
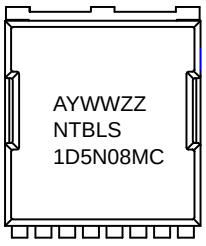
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	1.53 mΩ @ 10 V	298 A
	3.7 mΩ @ 6 V	



MO−299A
TOLL
CASE 100CU

MARKING DIAGRAM



NTBLS1D5N08MC = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

Table 1. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 250 μA, V_{GS} = 0 V		80	−	−	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C		−	78	−	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V	T_J = 25°C	−	−	1	μA
			T_J = 125°C	−	−	100	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		−	−	±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 710 μA		2.0	3.0	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$	I_D = 710 μA, ref to 25°C		−	−8.3	−	mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 80 A		−	1.30	1.53	mΩ
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 6 V, I_D = 63 A		−	2.0	3.7	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 80 A		−	220	−	S
Gate−Resistance	R_G	T_A = 25°C		−	0.7	−	Ω
CHARGES & CAPACTIANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		−	8170	−	pF
Output Capacitance	C_{oss}			−	3025	−	pF
Reverse Transfer Capacitance	C_{rss}			−	82	−	pF
Total Gate Charge	$Q_{G(tot)}$	V_{GS} = 10 V, V_{DS} = 40 V, I_D = 80 A		−	111	−	nC
Threshold Gate Charge	$Q_{G(th)}$			−	22	−	
Gate−to−Source Charge	Q_{gs}			−	35	−	
Gate−to−Drain Charge	Q_{gd}			−	23	−	
Output Charge	Q_{oss}			−	166	−	
Sync Charge	Q_{sync}			−	94	−	
Plateau Voltage	V_P			−	5	−	V
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 40 V, I_D = 80 A, R_G = 6 Ω		−	38	−	ns
Rise Time	t_r			−	34	−	ns
Turn−Off Delay Time	$t_{d(off)}$			−	74	−	ns
Fall Time	t_f			−	37	−	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	I_S = 80 A, V_{GS} = 0 V	T_J = 25°C	−	0.8	1.3	V
		I_S = 80 A, V_{GS} = 0 V	T_J = 125°C	−	0.7	−	V
Reverse Recovery Time	t_{rr}	I_F = 40 A, di/dt = 300 A/μs		−	19	−	nS
Reverse Recovery Charge	Q_{rr}			−	42	−	nC
Reverse Recovery Time	t_{rr}	I_F = 40 A, di/dt = 1000 A/μs		−	17	−	nS
Reverse Recovery Charge	Q_{rr}			−	121	−	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

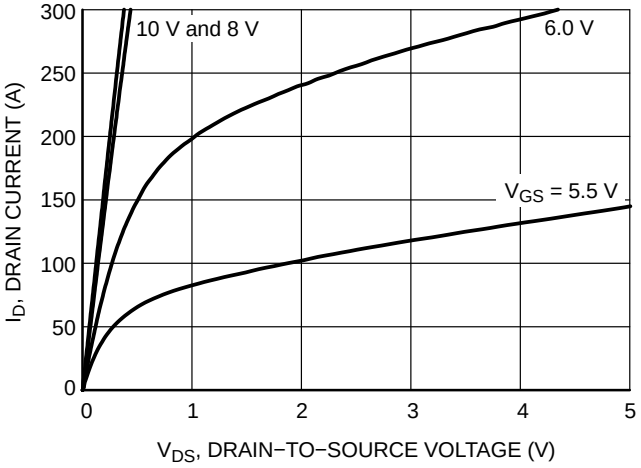


Figure 1. On−Region Characteristics

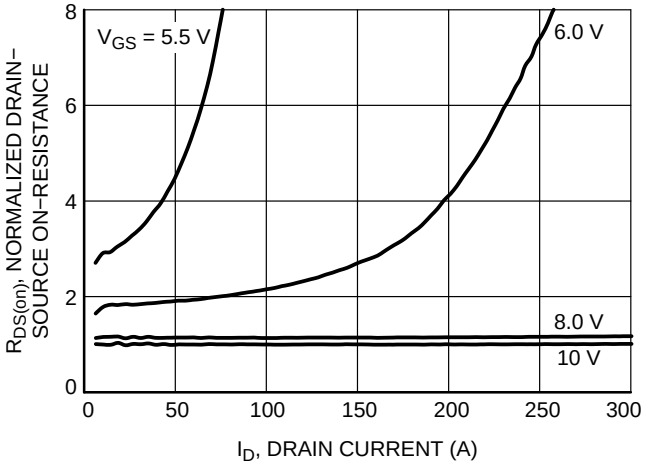


Figure 2. $R_{DS(on)}$ Normalized vs. I_D

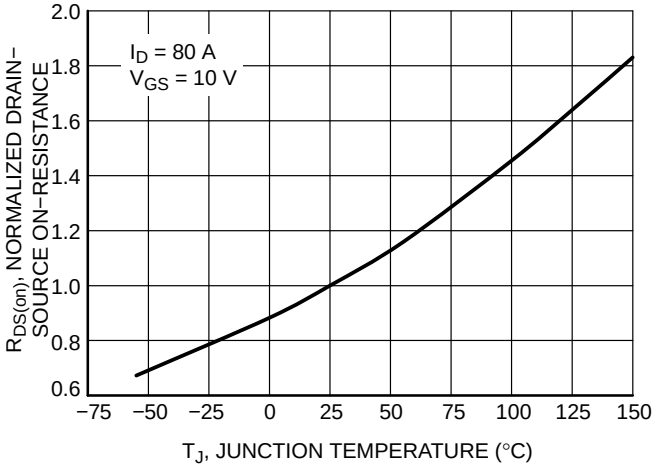


Figure 3. $R_{DS(on)}$ vs. Junction Temperature

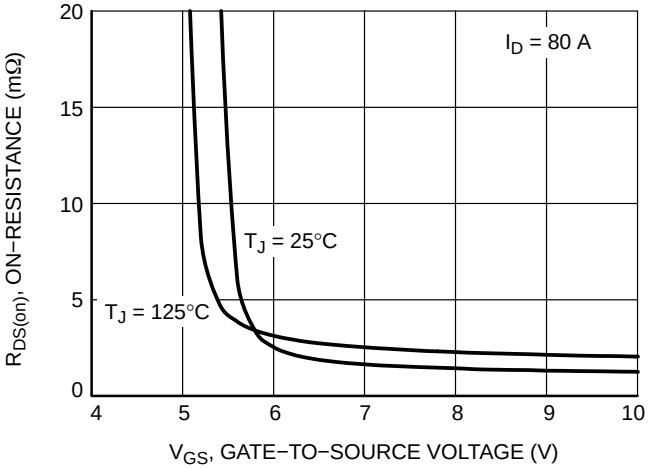


Figure 4. On−Resistance vs. Gate−to−Source Voltage

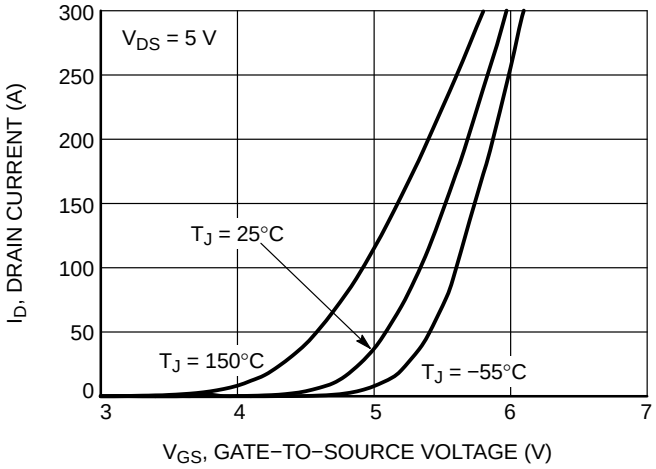


Figure 5. Drain Current vs. Gate−to−Source Voltage

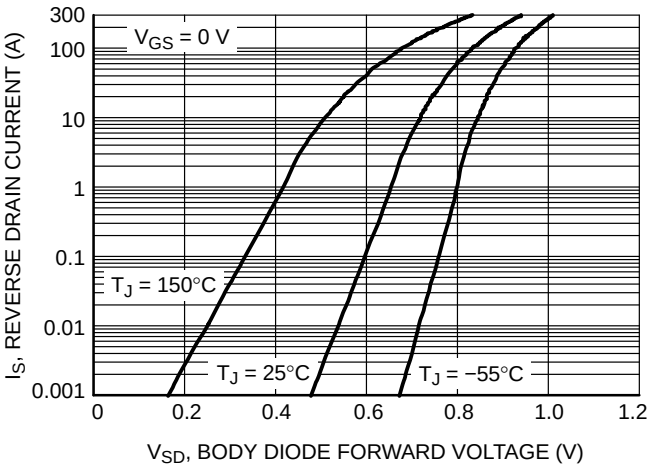


Figure 6. Reverse Drain Current vs. Body Diode Forward Voltage

TYPICAL CHARACTERISTICS

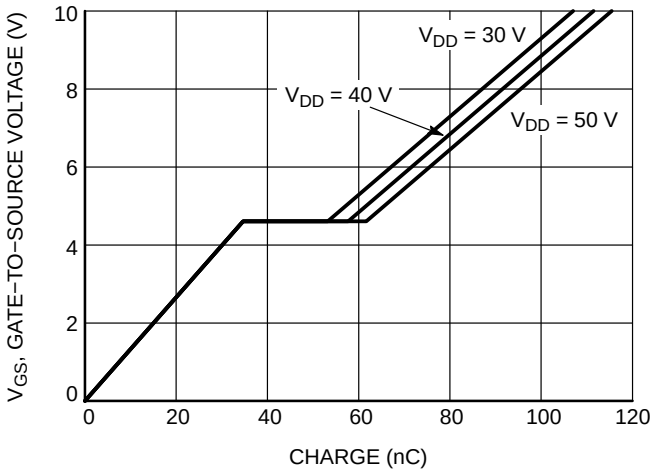


Figure 7. Gate Charge

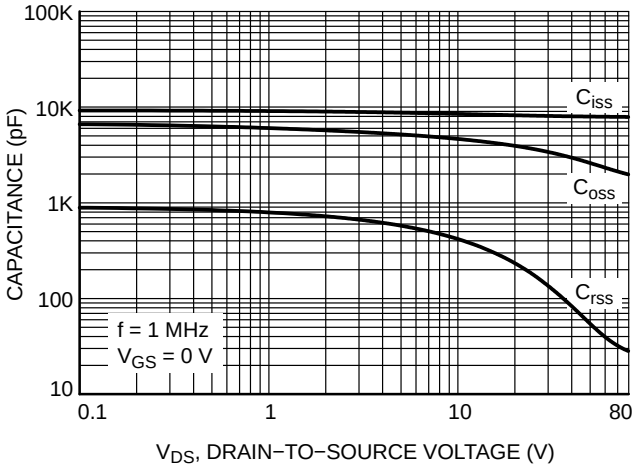


Figure 8. Capacitance Variation

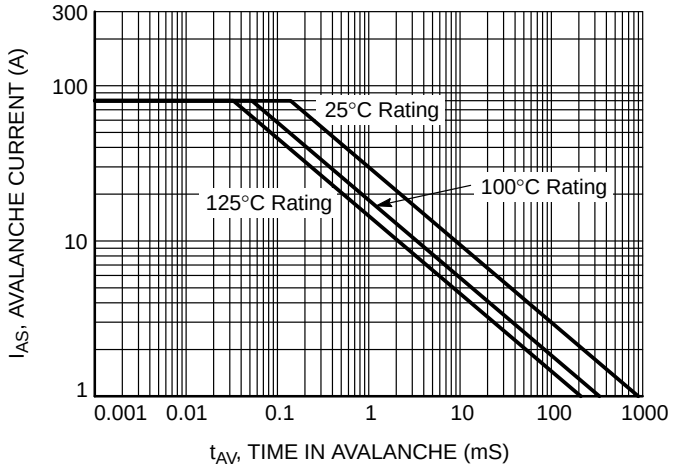


Figure 9. UIL

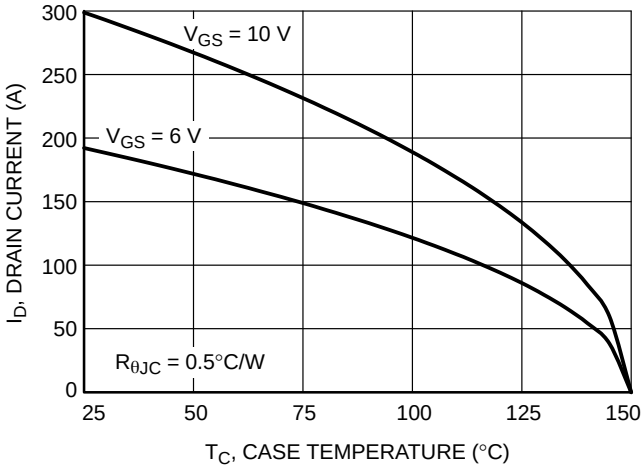


Figure 10. Drain Current vs. Case Temperature

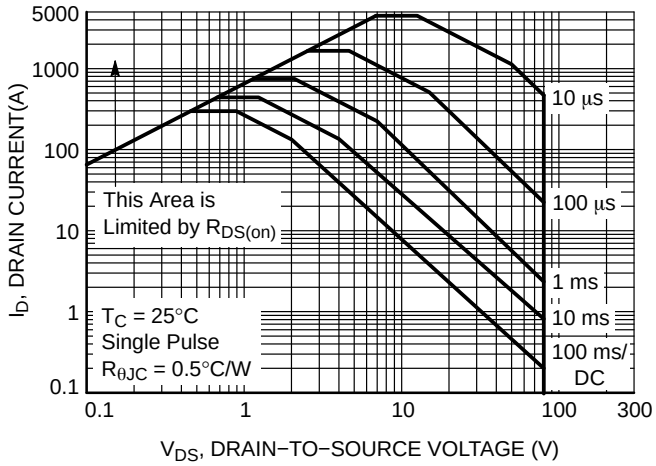


Figure 11. Maximum Rated Forward Biased Safe Operating Area

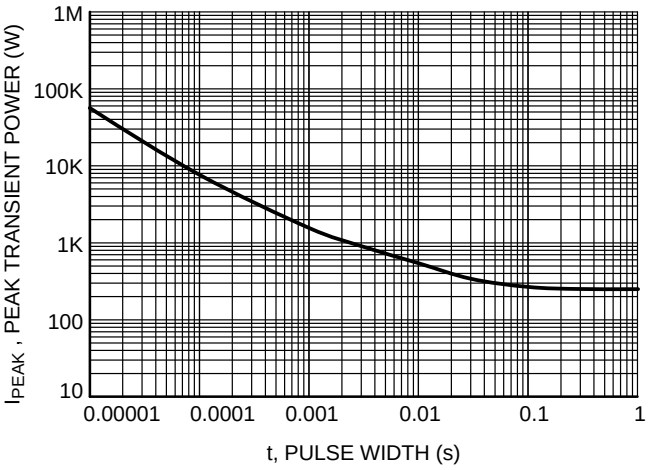


Figure 12. Peak Power

TYPICAL CHARACTERISTICS

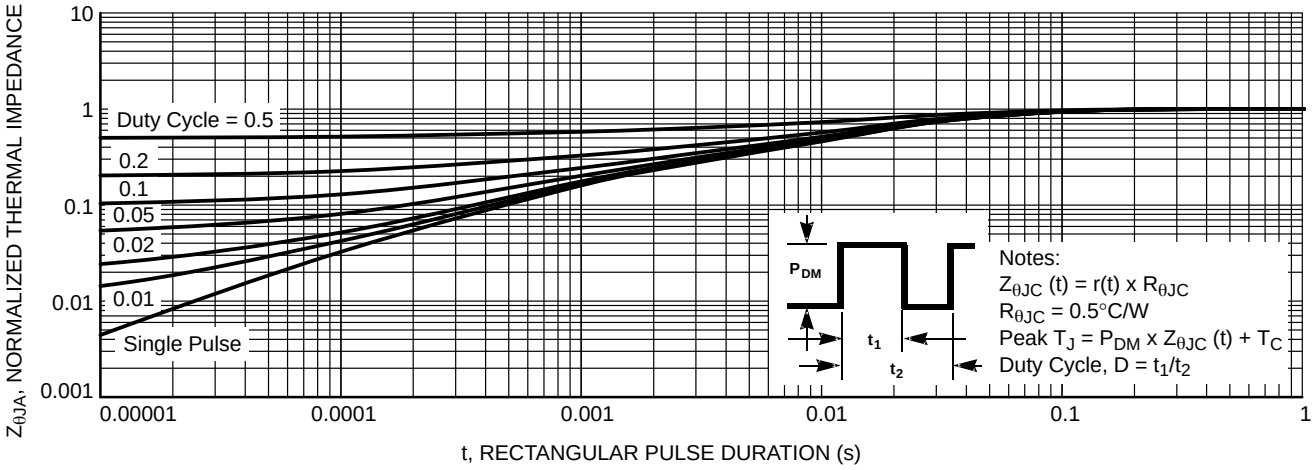


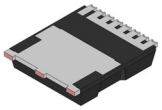
Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTBLS1D5N08MC	NTBLS 1D5N08MC	M0−299A (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



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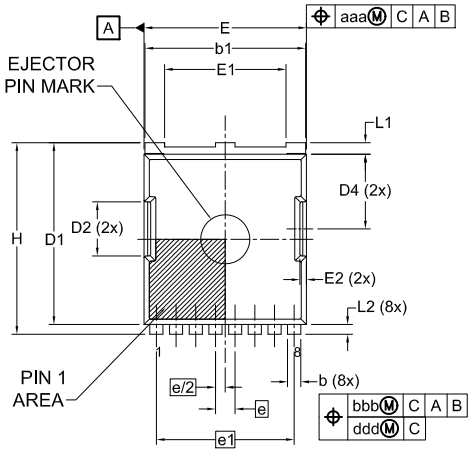
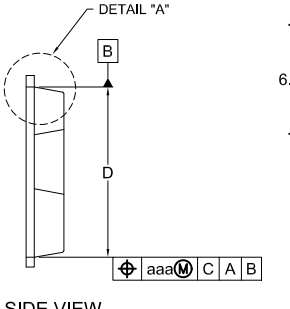
CASE 100CU
ISSUE C

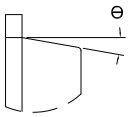
DATE 22 MAY 2023



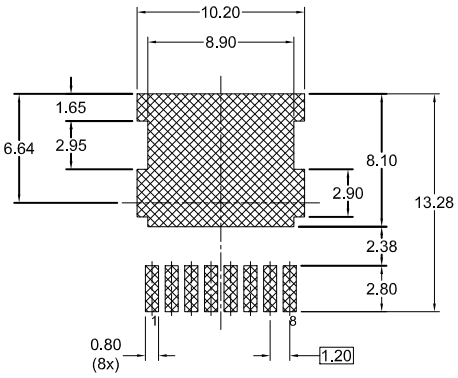
TOP VIEW



SIDE VIEW

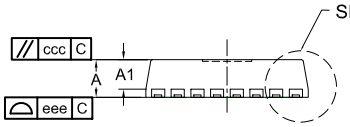


DETAIL "A"
SCALE: 2X

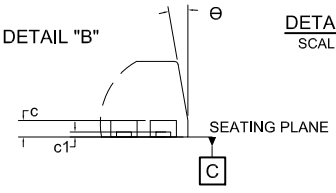


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



FRONT VIEW



DETAIL "B"
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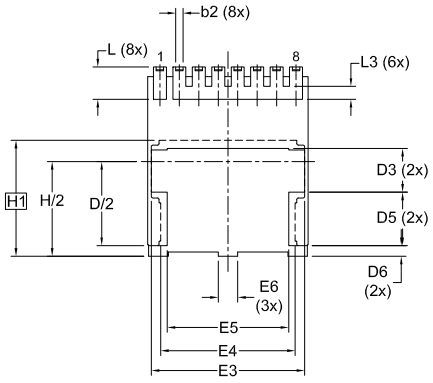


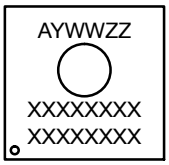
BOTTOM VIEW

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13813G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**H−PSOF8L 11.68x9.80**	**PAGE 1 OF 1**

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