



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-AAS/13/8018
Dated 22 Jul 2013

L272D Wafer diameter , assembly and test changes

Table 1. Change Implementation Schedule

Forecasted implementation date for change	31-Jul-2013
Forecasted availability date of samples for customer	31-Jul-2013
Forecasted date for STMicroelectronics change Qualification Plan results availability	31-Jul-2013
Estimated date of changed product first shipment	21-Oct-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	L272D
Type of change	Waferfab technology change, Package assembly location change, Package assembly material change, Testing location change, Test program / platform change
Reason for change	Production capacity rationalization - Halogen content reduction
Description of the change	1) As part of the running program to convert to 6" wafers the silicon lines diffused on the bipolar processes in the Ang Mo Kio plant, the wafer diameter for the product L272D (diffused on LAMT process) will be changed from 5" to 6". 2) For the L272D (housed in SO16 Narrow package) also the following changes regarding the assembly and test will be done: 2.1) Transfer of the assembly and final test from ST Muar (Malaysia) to ST Shenzhen (PRC). 2.2) Change of bonding wires material from GOLD to COPPER 2.3) Implementation of ECOPAK2 "green" molding compound (change from Nitto MP8000 H4-2A to Sumitomo EME 630AY) 2.4) Die attach glue (change from Hitachi EN4900 to Ablebond 8601S-25) 2.5) A Super High Density frame (SHD) will be implemented.
Change Product Identification	Traceability Code (first digit "K") -
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN AMS-AAS/13/8018					
Please sign and return to STMicroelectronics Sales Office		Dated 22 Jul 2013					
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="padding: 2px;">Name:</td></tr> <tr><td style="padding: 2px;">Title:</td></tr> <tr><td style="padding: 2px;">Company:</td></tr> <tr><td style="padding: 2px;">Date:</td></tr> <tr><td style="padding: 2px;">Signature:</td></tr> </table>		Name:	Title:	Company:	Date:	Signature:
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L272D Wafer diameter , assembly and test changes

WHAT

- 1) As part of the running program to convert to 6” wafers the silicon lines diffused on the bipolar processes in the Ang Mo Kio plant, the wafer diameter for the product L272D (diffused on LAMT process) will be changed from 5” to 6”.

- 2) For the L272D (housed in SO16 Narrow package) also the following changes regarding the assembly and test will be done:
 - 2.1) Transfer of the assembly and final test from ST Muar (Malaysia) to ST Shenzhen (PRC).
 - 2.2) Change of bonding wires material from GOLD to COPPER
 - 2.3) Implementation of ECOPAK2 “green” molding compound (change from Nitto MP8000 H4-2A to Sumitomo EME 630AY)
 - 2.4) Die attach glue (change from Hitachi EN4900 to Ablebond 8601S-25)
 - 2.5) A Super High Density frame (SHD) will be implemented.

WHY

- 1)-To rationalize the wafer production capacity.
- 2)-To improve the supply chain and to have a lower impact on the ambient.

HOW

1)-The bipolar LAMT diffusion process family is qualified and running in volumes on 6” wafers.

The qualification has been done through test vehicles belonging to the same process family (namely LM317 and L2722).

2)-The PDIP package family is qualified in Shenzhen plant through test vehicles: relevant L4931ABD50 ; L78L05ACD ; U329 and L6910.

Reliability tests on the L272D device are done as well (see the following report).

The alignment of electrical parameters of the L272D will be monitored as well.

Reliability Report

L272D:wafer diameter and assembly changes

General Information	
Product Lines	<i>L272</i>
Product Description	<i>Dual power operational amplifier</i>
Finished Good Codes	<i>L272D</i>
Product division	<i>AMS Analog and Audio Systems</i>
Package	<i>SO16 narrow</i>
Silicon process technology	<i>BIP>6um -LA MT</i>
Raw Line Code :	<i>A3Q7*L272AAE</i>

Locations	
Wafer fab location	<i>AMJ9</i>
Assembly fab location	<i>Shenzen</i>
Reliability assessment	<i>Qualification ongoing. Positive preliminary results.</i>

DOCUMENT HISTORY

Version	Date	Pages	Authors	Comment
1.0	12/07/2013	9	1. Fabio Fiabane 2. Sandro Storti	

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluation performed on *L272D, assembled in SO16 Narrow package*, in order to qualify the following changes:

- 1) Die related:
 - 1.1)-Wafer diameter change from 5" to 6"
- 2) Assembly related
 - 2.1)-Transfer of the assembly from ST Muar (Malaysia) to ST Shenzhen (PRC).
 - 2.2)-Change of bonding wires material from GOLD to COPPER.
 - 2.3)-Implementation of ECOPAK2 "green" molding compound (change from Nitto MP8000 H4-2A to Sumitomo EME630AY).
 - 2.4)-Die attach glue (change from Hitachi EN4900 to Ablebond 8601S-25).
 - 2.5)-A Super High Density frame (SHD) will be implemented.

1.2 Preliminary conclusions

All reliability tests have been completed or have intermediate positive results.
Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die oriented test showed a good stability of the main electrical monitored parameters.

Die and package oriented tests have not put in evidence any criticality regarding the wafer diameter change nor regarding the FE/BE compatibility.

Furthermore, the qualification of devices diffused on 6" wafers on bipolar processes belonging to the same family (test vehicles) has been considered to reinforce the reliability assessment about the wafer diameter change, namely L2722 (same process and application) and LM317.
See annex 4 for the details.

On the same way, the qualifications of the packages belonging to the same family SO8 - SO14 - SO16 has been considered. The most relevant test vehicles are L4931ABD50 ; L78L05ACD ; U329 and L6910.
See annex 4 for the details.

2 DEVICE CHARACTERISTICS

2.1 Device description


L272

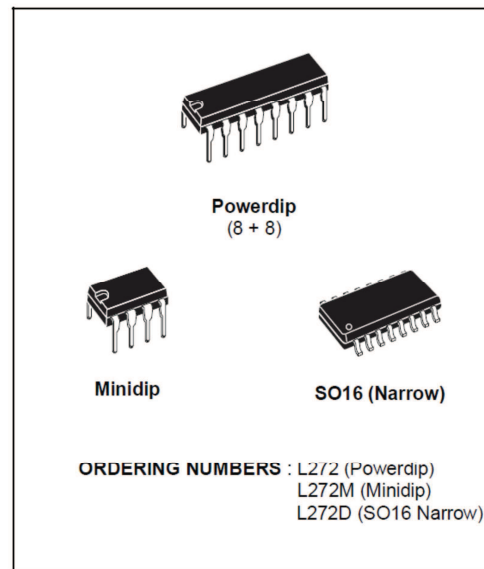
DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1 A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

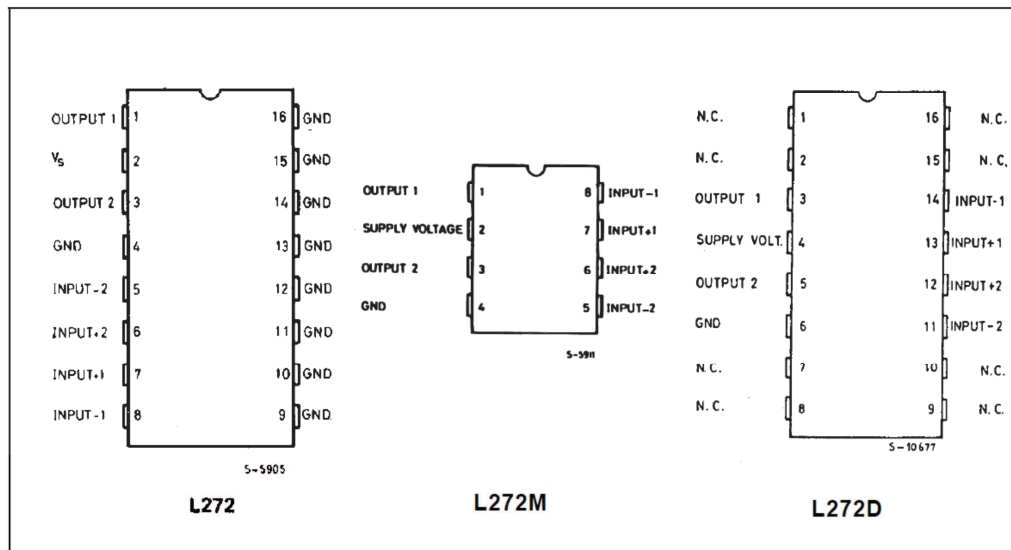
DESCRIPTION

The L272 is a monolithic integrated circuits in Powerdip, Minidip and SO packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



PIN CONNECTIONS (top view)



2.2 Traceability

Wafer fab information	
Device	L272D
Wafer fab manufacturing location	AMJ9
Wafer diameter	6
Silicon process technology	BIP (>6um) - MT
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size [μm x μm]	1910 x 2450
Metal levels	1

Assembly Information	
Device	L272D
Assembly fab location	ST Shenzhen
Package description	SO 16 Narrow
Molding compound	RESIN SUMITOMO EME-G630AY
Die attach material	GLUE ABLEBOND 8601S-25
Wirebonding material	COPPER
Frame	FRAME SO 16L 94x200 (Super High Density)

3 TESTS DESCRIPTION & DETAILED RESULTS

3.1 Die and Package tests description

TEST NAME	DESCRIPTION	PURPOSE
PC : Preconditioning (solder simulation)	The device is submitted to a typical temperature profile used for surface mounting, after controlled moisture absorption.	To investigate in general the effect of customer manufacturing soldering enhanced by package water absorption. As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.
AC :Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity
TC : Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding wire-bonds failure.
HTS : High Temperature Storage	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wirebonds solder joint ageing, data retention faults, metal stress-voiding.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity	To evaluate the package moisture resistance
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence
HTB High Temperature Bias	The device is biased in static configuration approaching the max. voltage ratings and stored at controlled conditions of ambient temperature approaching the maximum	This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.

3.2 LOT Information

Qualification lot number	RL code	Diffusion Lot Number	Package
1	A3Q7*L272AAE	W226N4E	SO16

3.3 Detailed results

L272D

N	TEST NAME	CONDITION/METHOD	STEPS	FAILS/SS
1	Preconditioning ML3	REFLOW PROFILE = J-STD-020C (Tmax=260°C)	Final	0/40
2	AC	Pa = 2 Atm Ta = 121°C JESD22a102	96 hrs	0 / 77
3	TC	Ta Cycling: -50°C/+150°C JESD22a104	500 Cy	0 / 77
			1000 Cy	ONGOING
4	HTS	Ta = +150°C JESD22a103	1000 hrs	0 / 77
5	HTB	125 °C Tj as minimum at Vcc Max JESD22-A108	1000 hrs	0 / 77

4 ANNEX

4.1 -Test Vehicles for wafer diameter change.

Following the construction analysis and the test matrix.

	1 - L2722	2 - LM317
Front End Techno	Bipolar>6/um LAMT	Bipolar>6/um LAAT
Metal	Al-Si – 3/um	Al-Si - 3/um
Passivation	Silicon Nitride	Silicon Nitride
Backside finishing	Cr-Ni-Au	Cr-Ni-Au
Package	DIP8	D2PACK
Wires	Au – 1mil	Cu – 2mils

N	NAME	CONDITION/METHOD	DURATION	1 - L2722	2 -LM317
1	PC	Reference specification = JEDEC J-STD-020 - MSL3		pass	pass
2	AC	Pa=2Atm / Ta=121°C JESD22A-102	168 hrs	-	0/77
3	TC	Ta Cycling: -50°C/+150°C JESD22a104	1000 cycles	0/77	-
		Ta Cycling: -65°C/+150°C JESD22a104	1000 cycles	-	0/77
4	HTS	Ta = 150°C JESD22A-103	1000 hrs	-	0/45
5	THB	Ta = 85°C, RH = 85% JESD22A-101	1000 hrs	-	0/77
6	HTB	125 °C Tj as minimum at Vcc Max JESD22-A108	1000 hrs	0/77	-
7	HTOL	Tj = 125°C JESD22A-108	1000 hrs	-	0/77

Note: results from the reliability reports with the following references:

1. L2722 (reliability report RR002613CS6103)
2. LM317 (reliability report REL - 6043- 189.11W)

4.2 - Test vehicles for the assembly related changes.

Following the construction analysis and the reliability test matrix of the most relevant to cover the impacted FE technologies and assembly materials.

	1 - L4931ABD50	2 - L78L05ACD	3 - U329	4 - L6910
Frame	SO 8L 94x125 SHD	SO 8L 94x125 SHD	SO 16L 94x150 SHD	SO 16L 94x150 SHD
Molding Compound	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC	SUMITOMO EME-G630AY	SUMITOMO EME-G630AY
Die attach	ABLEBOND 8601S-25	ABLEBOND 8601S-25	HITACHI ENX49VA-S(15)	HITACHI ENX49VA-S(15)
Wires	Cu D1.3	Cu D1.0	Cu D1.0	Au D1
Front End Techno	Bip>6/um - BTI	Bip>6/um - AT	BCD-OFFLINE	BCD5
Metal	Al-Si - 3/um	Al-Si - 3/um	Al-Si-Cu - 1/um	3 metal layers
Passivation	Silicon Nitride	Silicon Nitride	Silicon Nitride	Teos+SiOn+PIX
Backside finishing	Cr-Ni-Au	Silicon	Cr-Ni	Silicon

	Test		1 - L4931ABD50	2 - L78L05ACD	3 - U329	4 - L6910
1	PC	Reference specification = JEDEC J-STD-020 - MSL3	Pass (3 lots)	Pass (3 lots)	Pass	Pass
2	AC	Ta=121C P=2atm JESD22 A-102	168 hrs	0/77 x 3 lots	0/77 x 3 lots	0/77
3	TC	Ta=-65/+150C -JESD22 A-104	500 cycles	0/77 x 3 lots	0/77 x 3 lots	0/77
4	HTSL	Ta=150°C - JESD22 A-103	1000 hrs	0/45 x 3 lots	0/45 x 3 lots	0/77
5	THS	85°C/85%RH, JESD22A-105	1000 hrs	-	-	0/77
6	THB	Ta=85C RH=85% JESD22 A-101	1000 hrs	-	0/77 x 3 lots	0/77
7	HTB	JESD22A-108	1000 hrs	-	-	0/45
8	HTOL	Tj = 125°C,	1000 hrs	-	0/77	-

Note: results from reliability reports with the following references:

1. L4931ABD50: (reliability report REL-6043W180.11) ,
2. L78L05ACD (reliability report QASOHFK1) ,
3. U329, (reliability report RR000112CT6004).
4. L6910 (reliability report RR000112CT6004).

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