

## FEATURES

High small signal gain: 16.0 dB

High PAE: 55% typical

Instantaneous bandwidth: 0.01 GHz to 2.8 GHz

Supply voltage:  $V_{DD} = 28\text{ V}$  at 100 mA

Internal prematching

Simple and compact external tuning for optimal performance

32-lead, 5 mm × 5 mm, LFCSP package

## APPLICATIONS

Extended battery operation for public mobile radios

Power amplifier stage for wireless infrastructures

Test and measurement equipment

Commercial and military radars

General-purpose transmitter amplification

## GENERAL DESCRIPTION

The **HMC8500** is a gallium nitride (GaN), broadband power amplifier delivering >10 W with up to 55% power added efficiency (PAE) across an instantaneous bandwidth of 0.01 GHz to 2.8 GHz, and with a  $\pm 1.0$  dB typical gain flatness.

The **HMC8500** is ideal for pulsed or continuous wave (CW) applications, such as wireless infrastructure, radars, public mobile radios, and general-purpose amplification.

## FUNCTIONAL BLOCK DIAGRAM

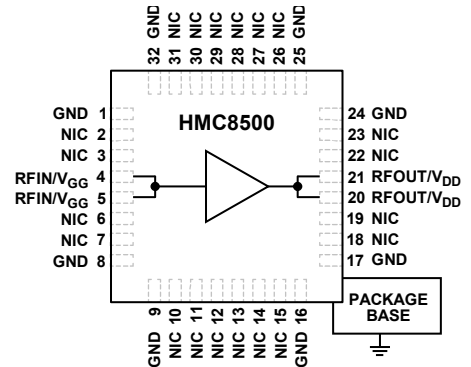


Figure 1.

14684-001

The **HMC8500** amplifier is externally tuned using low cost, surface-mount components and is available in a compact LFCSP package.

Note that throughout this data sheet, multifunction pins, such as RFIN/V<sub>GG</sub>, are referred to either by the entire pin name or by a single function of the pin, for example, RFIN, when only that function is relevant.

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**REVISION HISTORY**

**8/2018—Rev. 0 to Rev. A**

Changed CG-32-1 to CG-32-2 .....	Throughout
Changes to Figure 5.....	7
Updated Outline Dimensions .....	16
Changes to the Ordering Guide.....	16

**1/2017—Revision 0: Initial Version**

**SPECIFICATIONS****ELECTRICAL SPECIFICATIONS**

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 28\text{ V}$ ,  $I_{DD} = 100\text{ mA}$ , frequency range = 0.01 GHz to 0.8 GHz.

**Table 1.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.01		0.8	GHz	
GAIN						
Small Signal Gain		18.0	20.0		dB	
Gain Flatness			$\pm 1.5$		dB	
RETURN LOSS						
Input			7		dB	
Output			7		dB	
POWER						
Output Power at 30 dBm Input Power	$P_{OUT}$		40		dBm	
Power Added Efficiency	PAE		55		%	
OUTPUT THIRD-ORDER INTERCEPT	IP3		48		dBm	Measurement taken at $P_{OUT}/\text{tone} = 30\text{ dBm}$
NOISE FIGURE	NF		5		dB	
TOTAL SUPPLY CURRENT	$I_{DD}$		100		mA	Adjust the gate bias control voltage ( $V_{GG}$ ) between $-8\text{ V}$ and $0\text{ V}$ to achieve $I_{DD} = 100\text{ mA}$ typical

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 28\text{ V}$ ,  $I_{DD} = 100\text{ mA}$ , frequency range = 0.8 GHz to 1.5 GHz.

**Table 2.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.8		1.5	GHz	
GAIN						
Small Signal Gain		14.0	16.0		dB	
Gain Flatness			$\pm 1.0$		dB	
RETURN LOSS						
Input			8		dB	
Output			8		dB	
POWER						
Output Power at 30 dBm Input Power	$P_{OUT}$		40		dBm	
Power Added Efficiency	PAE		55		%	
OUTPUT THIRD-ORDER INTERCEPT	IP3		50		dBm	Measurement taken at $P_{OUT}/\text{tone} = 30\text{ dBm}$
NOISE FIGURE	NF		4.5		dB	
TOTAL SUPPLY CURRENT	$I_{DD}$		100		mA	Adjust the gate bias control voltage ( $V_{GG}$ ) between $-8\text{ V}$ and $0\text{ V}$ to achieve $I_{DD} = 100\text{ mA}$ typical

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 28\text{ V}$ ,  $I_{DD} = 100\text{ mA}$ , frequency range = 1.5 GHz to 2.8 GHz.

**Table 3.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		1.5		2.8	GHz	
GAIN						
Small Signal Gain		12.0	15.0		dB	
Gain Flatness			$\pm 0.75$		dB	
RETURN LOSS						
Input			10		dB	
Output			10		dB	
POWER						
Output Power at 30 dBm Input Power	$P_{OUT}$		40		dBm	
Power Added Efficiency	PAE		60		%	
OUTPUT THIRD-ORDER INTERCEPT	IP3		47		dBm	Measurement taken at $P_{OUT}/\text{tone} = 30\text{ dBm}$
NOISE FIGURE	NF		4.5		dB	
TOTAL SUPPLY CURRENT	$I_{DD}$		100		mA	Adjust the gate bias control voltage ( $V_{GG}$ ) between $-8\text{ V}$ and $0\text{ V}$ to achieve $I_{DD} = 100\text{ mA}$ typical

### TOTAL SUPPLY CURRENT BY $V_{DD}$

**Table 4.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT	$I_{DD}$					Adjust the gate bias control voltage ( $V_{GG}$ ) between $-8\text{ V}$ and $0\text{ V}$ to achieve $I_{DD} = 100\text{ mA}$ typical
$V_{DD} = 24\text{ V}$			100		mA	
$V_{DD} = 28\text{ V}$			100		mA	
$V_{DD} = 32\text{ V}$			100		mA	

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter <sup>1</sup>	Rating
Drain Bias Voltage (V <sub>DD</sub> )	35 V dc
Gate Bias Voltage (V <sub>GG</sub> )	–8 V to 0 V dc
Radio Frequency (RF) Input Power (RFIN)	33 dBm
Maximum Voltage Standing Wave Ratio (VSWR) <sup>2</sup>	6:1
Channel Temperature	225°C
Maximum Peak Reflow Temperature (MSL3) <sup>3</sup>	260°C
Continuous Power Dissipation, P <sub>DISS</sub> (T <sub>A</sub> = 85°C, Derate 108.6 mW/°C Above 85°C)	12.5 W
Storage Temperature Range	–40°C to +125°C
Operating Temperature Range	–40°C to +85°C
ESD Sensitivity (Human Body Model)	Class 1B, passed 500 V

<sup>1</sup> When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the Absolute Maximum Rating is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

<sup>2</sup> Restricted by maximum power dissipation.

<sup>3</sup> See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$  is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	$\theta_{JC}$	Unit
CG-32-2 <sup>1</sup>	9.2	°C/W

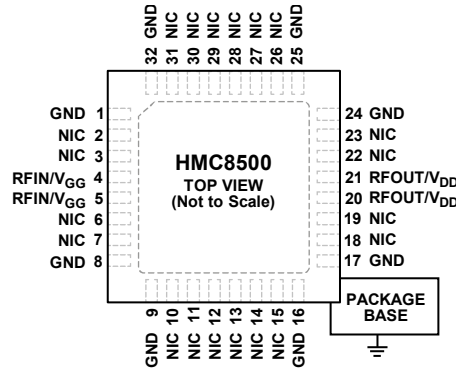
<sup>1</sup> Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with 36 thermal vias. See JEDEC JESD51.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



**NOTES**  
 1. NO INTERNAL CONNECTION. THESE PINS ARE NOT CONNECTED INTERNALLY. HOWEVER, ALL DATA WAS MEASURED WITH THESE PINS CONNECTED TO RF/DC GROUND EXTERNALLY.  
 2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF/DC GROUND.

14694-002

Figure 2. Pin Configuration

Table 7. Pad Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16, 17, 24, 25, 32	GND	Ground. These pins must be connected to RF/dc ground. See Figure 3 for the GND interface schematic.
2, 3, 6, 7, 10 to 15, 18, 19, 22, 23, 26 to 31	NIC	No Internal Connection. These pins are not connected internally. However, all data was measured with these pins connected to RF/dc ground externally.
4, 5	RFIN/V <sub>GG</sub>	RF Input/Gate Bias Control Voltage. This pin is a multifunction pin. The RFIN/V <sub>GG</sub> pin is dc-coupled with internal prematching and requires external matching to 50 Ω, as shown in Figure 41. See Figure 4 for the RFIN/V <sub>GG</sub> interface schematic.
20, 21	RFOUT/V <sub>DD</sub>	RF Output/Drain Bias Voltage. This is a multifunction pin. The RFOUT/V <sub>DD</sub> pin is dc-coupled and requires external matching to 50 Ω, as shown in Figure 41. See Figure 4 for the RFOUT/V <sub>DD</sub> interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

### INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

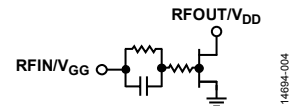


Figure 4. RFIN/V<sub>GG</sub> and RFOUT/V<sub>DD</sub> Interface Schematic

### TYPICAL PERFORMANCE CHARACTERISTICS

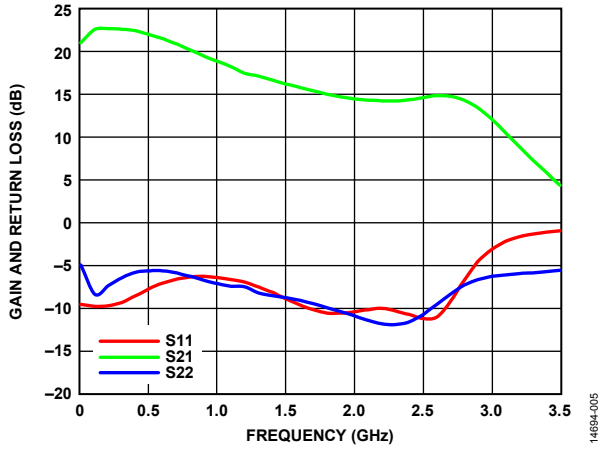


Figure 5. Gain and Return Loss vs. Frequency

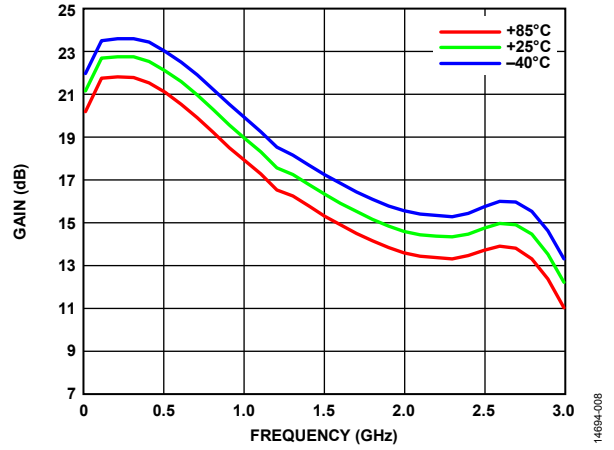


Figure 8. Gain vs. Frequency at Various Temperatures

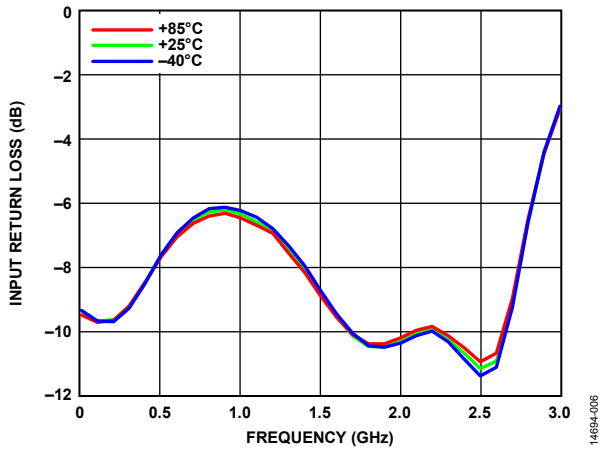


Figure 6. Input Return Loss vs. Frequency at Various Temperatures

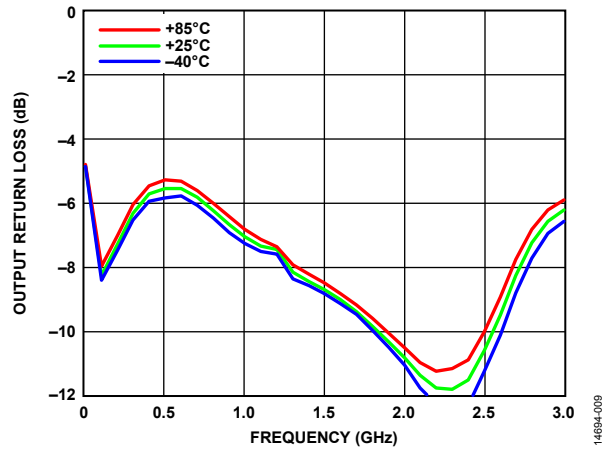


Figure 9. Output Return Loss vs. Frequency at Various Temperatures

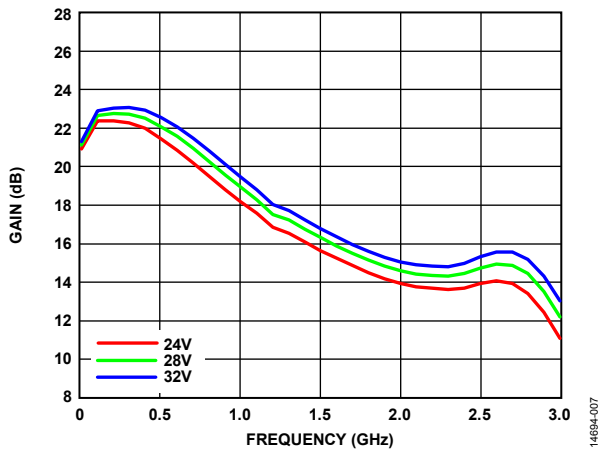


Figure 7. Gain vs. Frequency at Various Supply Voltages

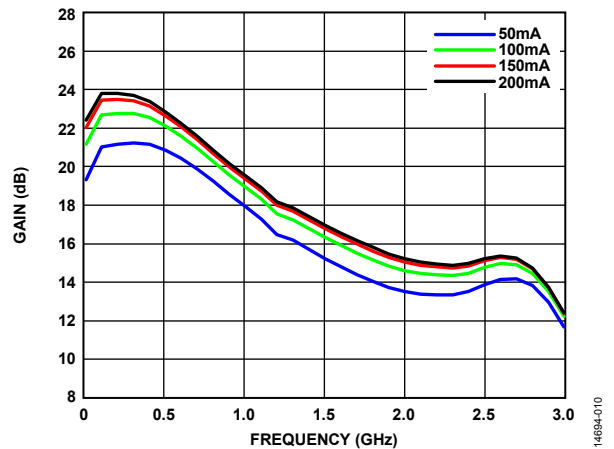


Figure 10. Gain vs. Frequency at Various Supply Currents

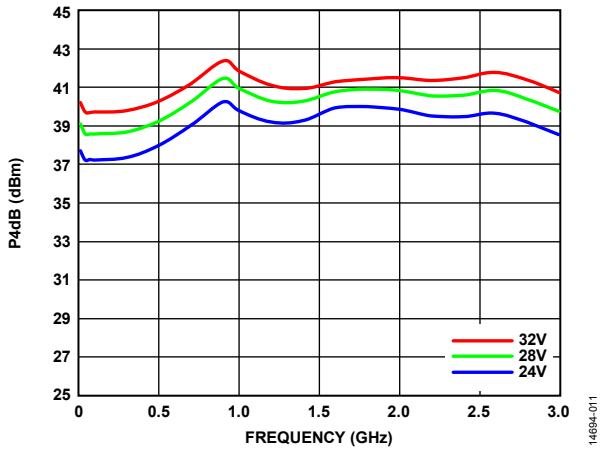


Figure 11. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Supply Voltages

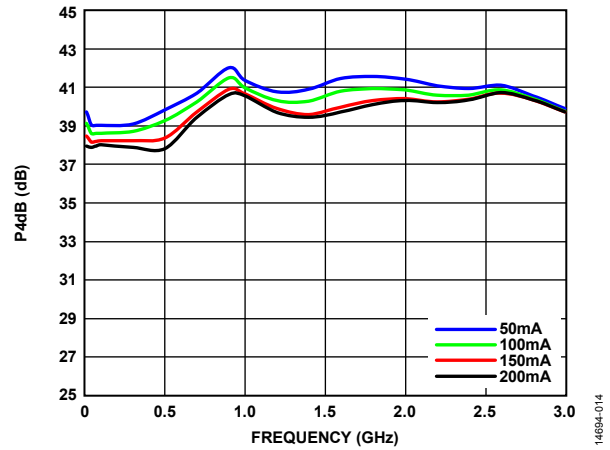


Figure 14. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Supply Currents

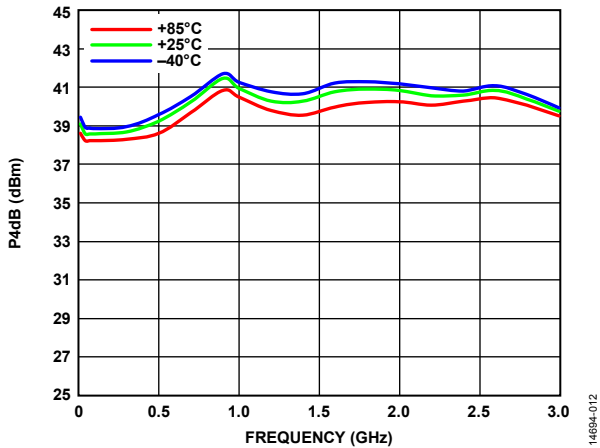


Figure 12. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Temperatures

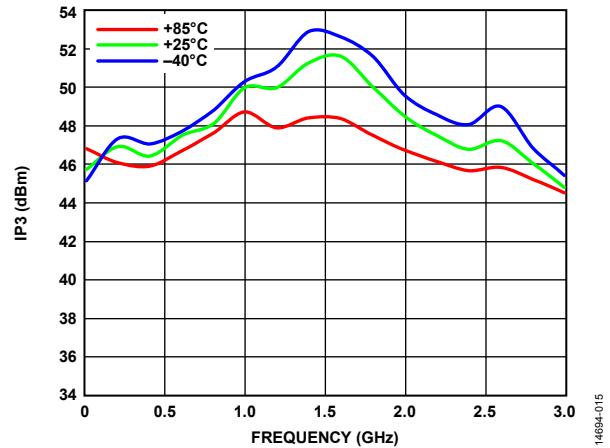


Figure 15. Output Third-Order Intercept (IP3) vs. Frequency at Various Temperatures,  $P_{Out}/Tone = 30 \text{ dBm}$

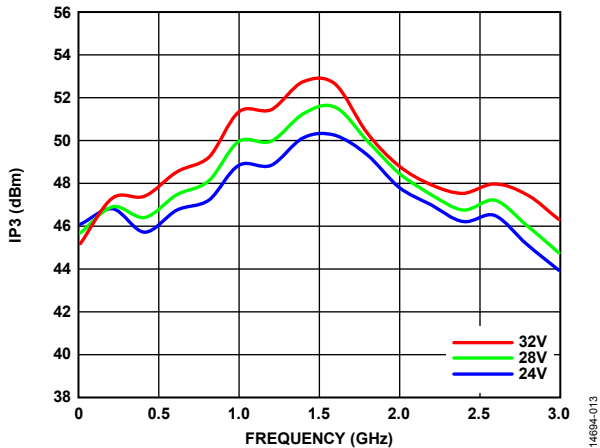


Figure 13. Output Third-Order Intercept (IP3) vs. Frequency at Various Supply Voltages,  $P_{Out}/Tone = 30 \text{ dBm}$

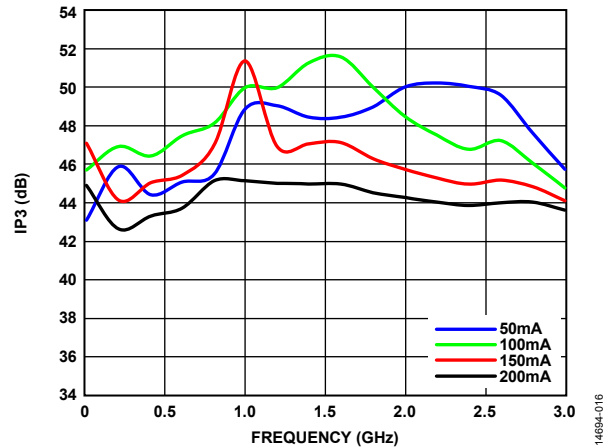


Figure 16. Output Third-Order Intercept (IP3) vs. Frequency at Various Supply Currents,  $P_{Out}/Tone = 30 \text{ dB}$



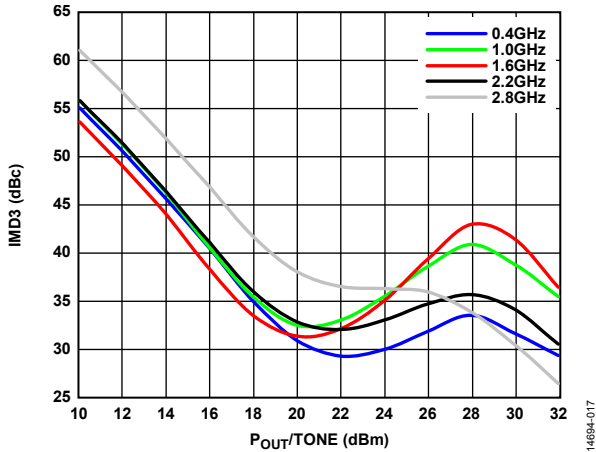


Figure 17. Output Third-Order Intermodulation (IMD3) vs.  $P_{OUT}/Tone$  at  $V_{DD} = 24 V$

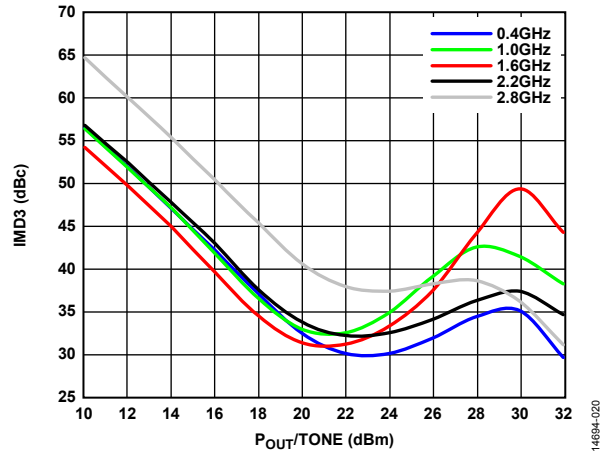


Figure 20. Output Third-Order Intermodulation (IMD3) vs.  $P_{OUT}/Tone$  at  $V_{DD} = 32 V$

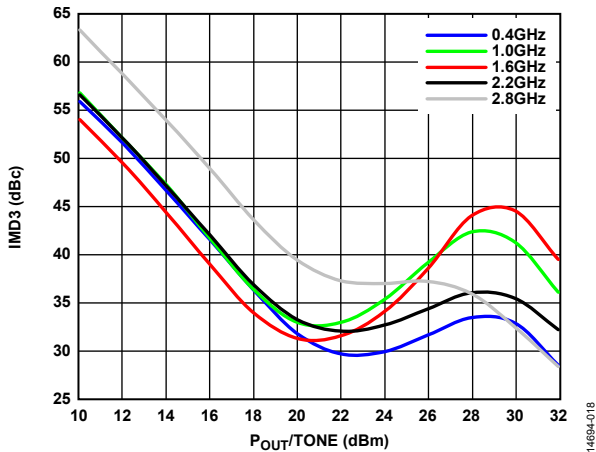


Figure 18. Output Third-Order Intermodulation (IMD3) vs.  $P_{OUT}/Tone$  at  $V_{DD} = 28 V$

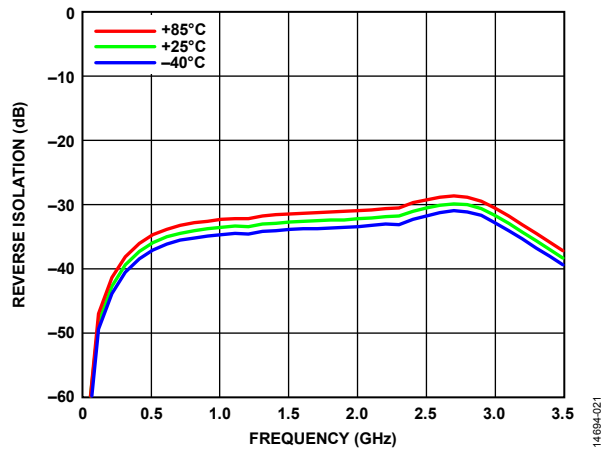


Figure 21. Reverse Isolation vs. Frequency at Various Temperatures

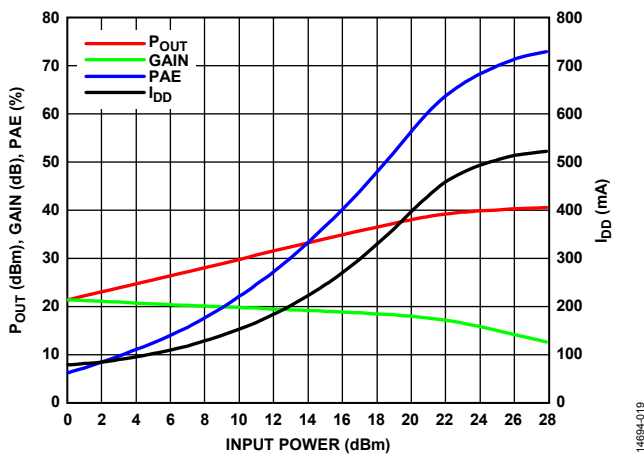


Figure 19. Power Output ( $P_{OUT}$ ), Gain, Power Added Efficiency (PAE), and Total Supply Current ( $I_{DD}$ ) vs. Input Power at 0.5 GHz

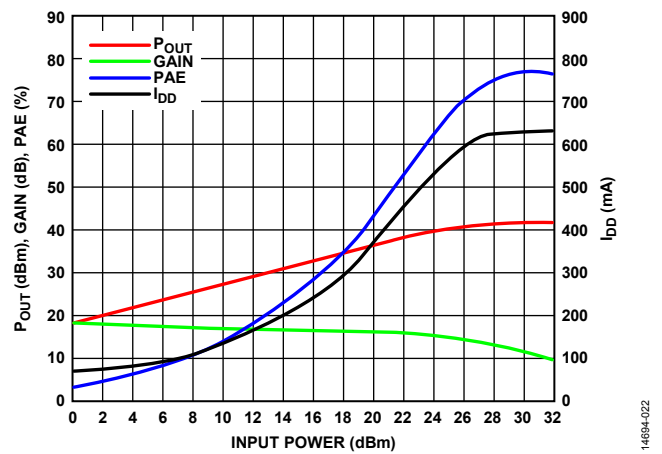


Figure 22. Power Output ( $P_{OUT}$ ), Gain, Power Added Efficiency (PAE), and Total Supply Current ( $I_{DD}$ ) vs. Input Power at 1 GHz

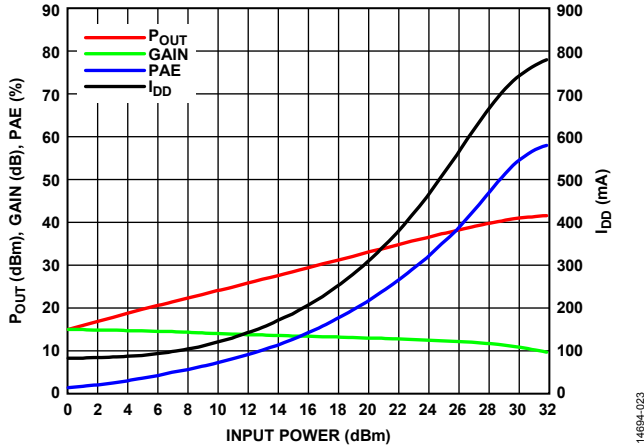


Figure 23. Power Output ( $P_{OUT}$ ), Gain, Power Added Efficiency (PAE), and Total Supply Current ( $I_{DD}$ ) vs. Input Power at 1.8 GHz

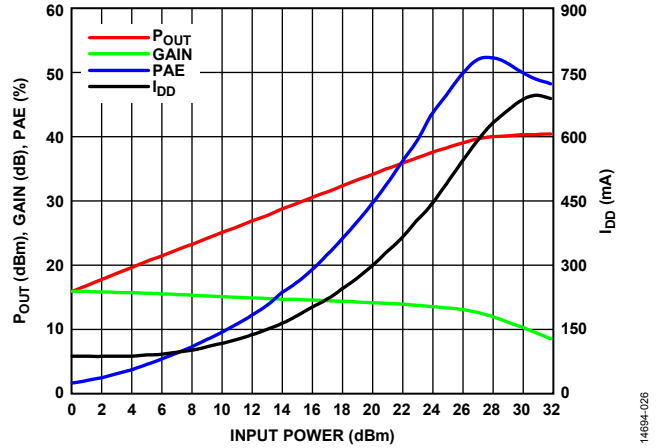


Figure 26. Power Output ( $P_{OUT}$ ), Gain, Power Added Efficiency (PAE), and Total Supply Current ( $I_{DD}$ ) vs. Input Power at 2.8 GHz

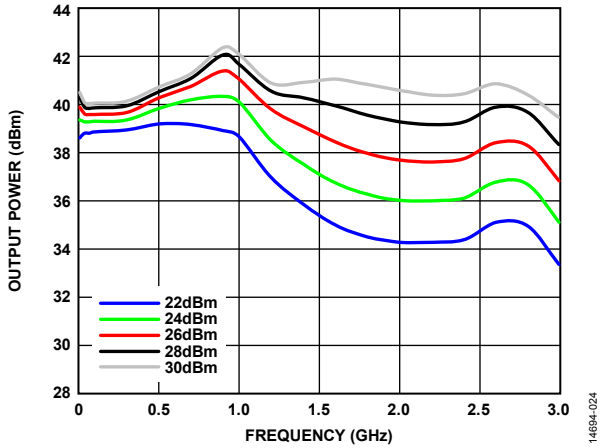


Figure 24. Output Power vs. Frequency at Various Input Powers

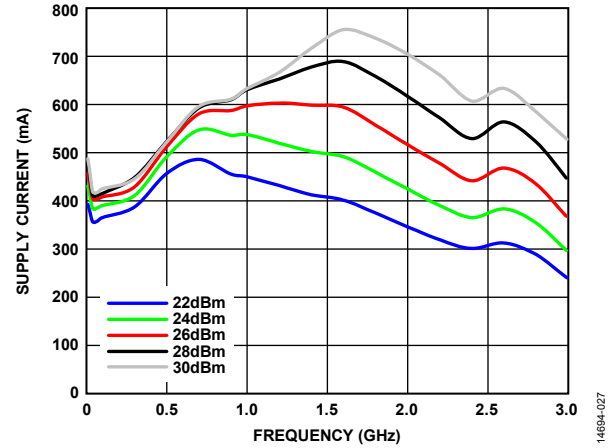


Figure 27. Supply Current vs. Frequency at Various Input Powers

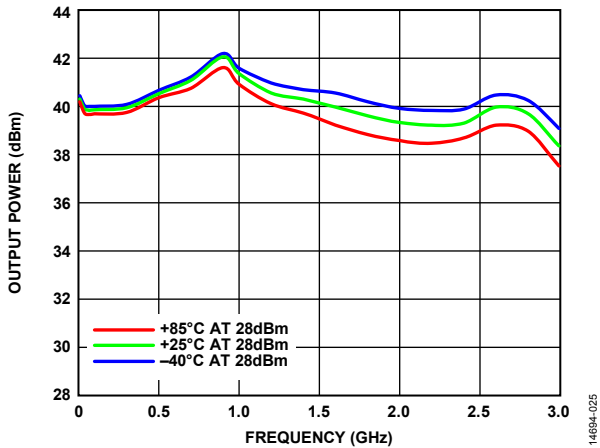


Figure 25. Output Power vs. Frequency at Various Temperatures at 28 dBm Input Power

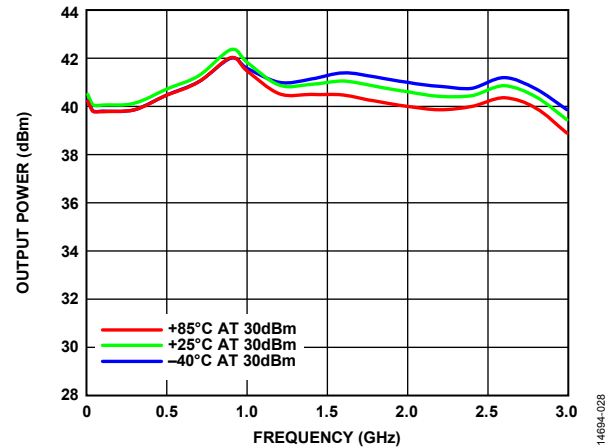


Figure 28. Output Power vs. Frequency at Various Temperatures at 30 dBm Input Power

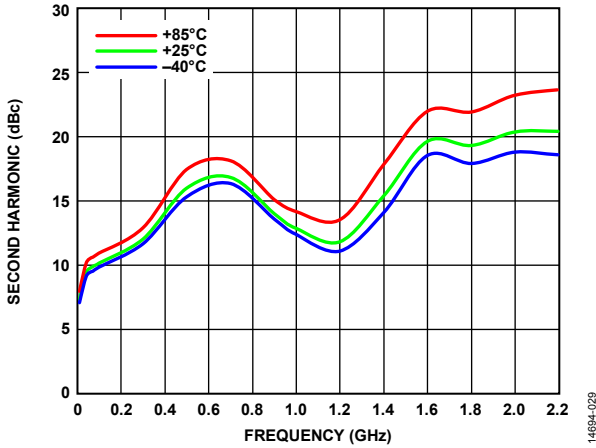


Figure 29. Second Harmonic vs. Frequency at Various Temperatures

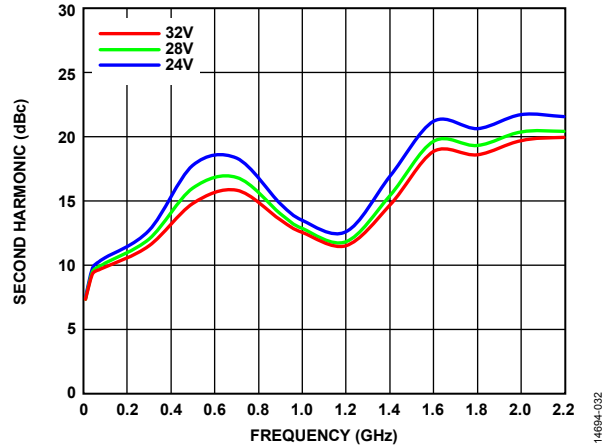


Figure 32. Second Harmonic vs. Frequency at Various Supply Voltages

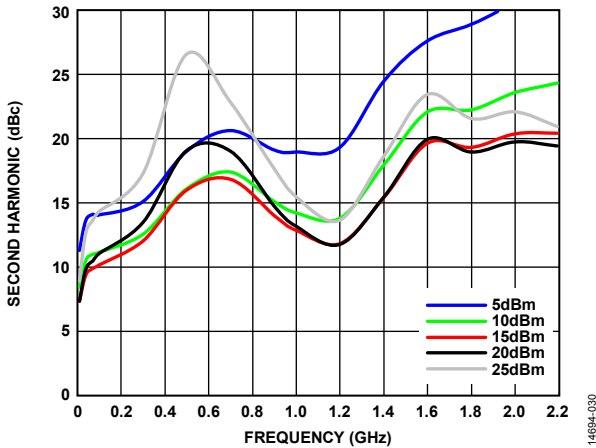


Figure 30. Second Harmonic vs. Frequency at Various Input Power Levels

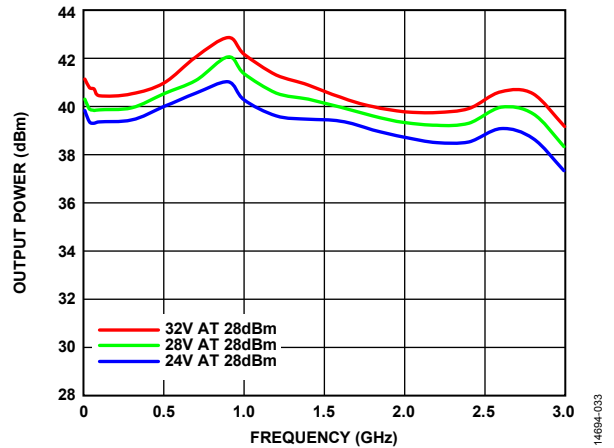


Figure 33. Output Power vs. Frequency at Various Supply Voltages at 28 dBm Input Power

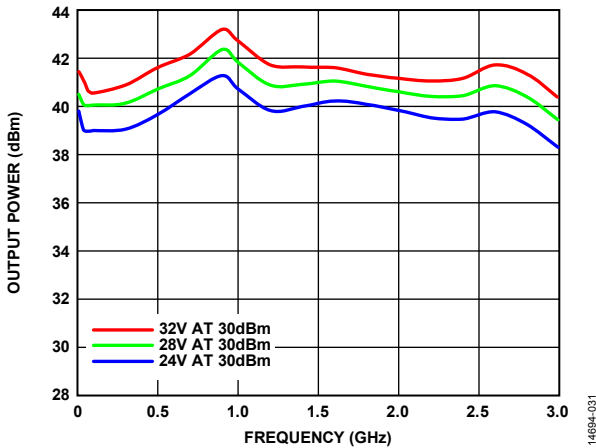


Figure 31. Output Power vs. Frequency at Various Supply Voltages at 30 dBm Input Power

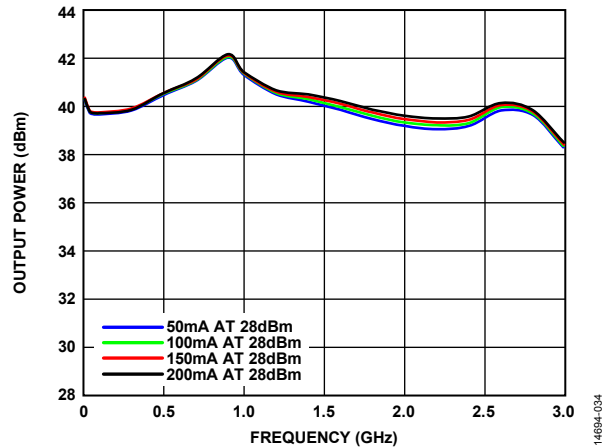


Figure 34. Output Power vs. Frequency at Various Supply Currents at 28 dBm Input Power

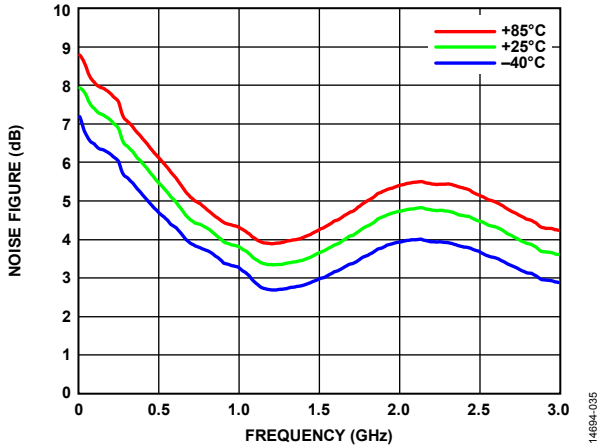


Figure 35. Noise Figure vs. Frequency at Various Temperatures

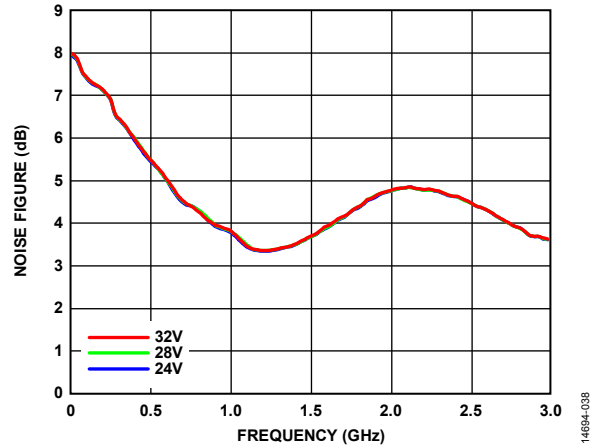


Figure 38. Noise Figure vs. Frequency at Various Supply Voltages

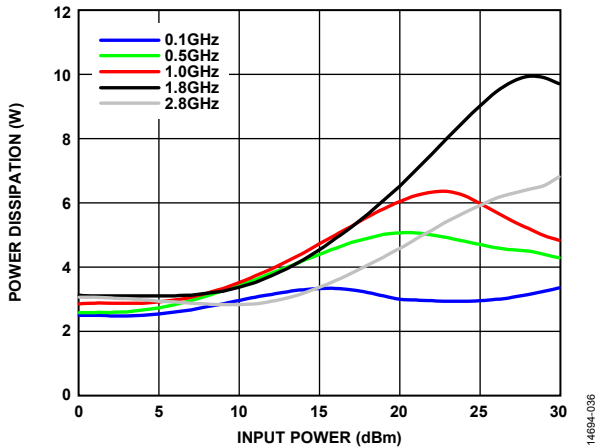


Figure 36. Power Dissipation vs. Input Power at Various Frequencies,  $T_A = 85^\circ\text{C}$

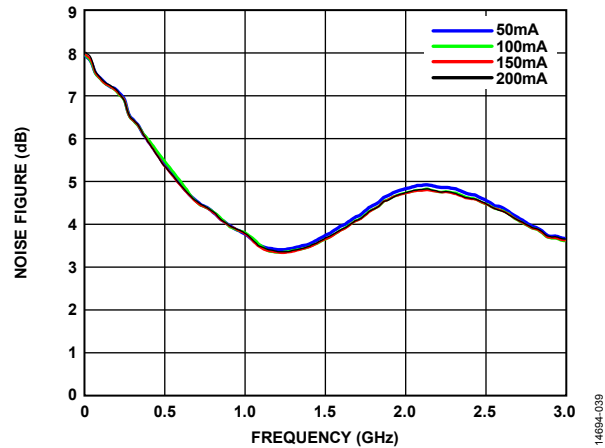


Figure 39. Noise Figure vs. Frequency at Various Supply Currents

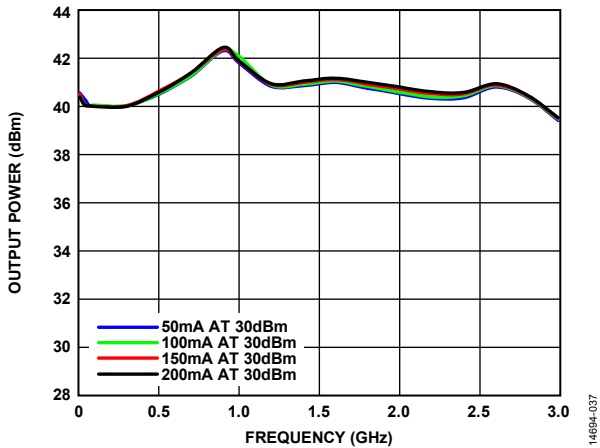


Figure 37. Output Power vs. Frequency at Various Supply Currents at 30 dBm Input Power

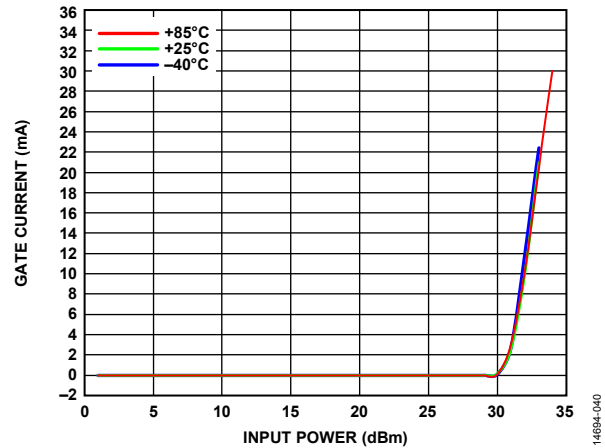


Figure 40. Gate Current vs. Input Current at Various Temperatures

## THEORY OF OPERATION

The HMC8500 is a >10 W, gallium nitride (GaN), power amplifier that consists of a single gain stage that effectively operates like a single field effect transistor (FET). The device is internally prematched so that simple, external matching networks at the RF input and RF output ports optimize the performance across

the entire operating frequency range. The recommended dc bias conditions place the device in deep Class AB operation, resulting in high saturated output power (41 dBm typical) at improved levels of power efficiency (55% typical).

### APPLICATIONS INFORMATION

The drain bias voltage is applied through the RFOUT/V<sub>DD</sub> pin, and the gate bias voltage is applied through the RFIN/V<sub>GG</sub> pin. For operation of a single application circuit across the entire frequency range, it is recommended to use the external matching components specified in the typical application circuit (L1, C1, C8, C11, and R2) shown in Figure 41. If operation is only required across a narrower frequency range, performance can be optimized additionally through the implementation of alternate matching networks. Capacitive bypassing of V<sub>DD</sub> and V<sub>GG</sub> is recommended.

The recommended power-up bias sequence follows:

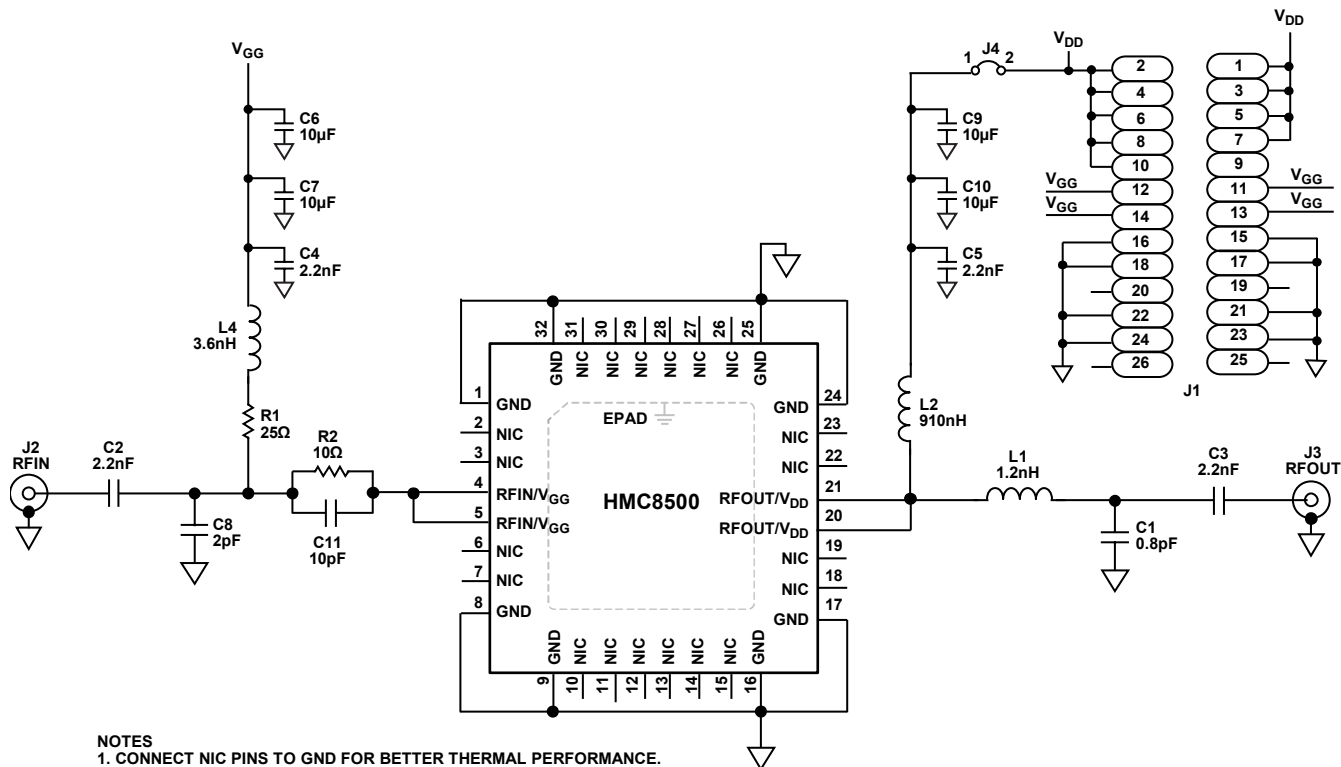
1. Connect the power supply ground to circuit ground.
2. Set V<sub>GG</sub> to -8 V to pinch off the drain current.
3. Set V<sub>DD</sub> to 28 V (drain current is pinched off).
4. Adjust V<sub>GG</sub> more positive (approximately -2.5 V to -3.0 V) until a quiescent of I<sub>DD</sub> = 100 mA is obtained.
5. Apply the RF signal.

The recommended power-down bias sequence follows:

1. Turn off the RF signal.
2. Set V<sub>GG</sub> to -8 V to pinch off the drain current.
3. Set V<sub>DD</sub> to 0 V.
4. Set V<sub>GG</sub> to 0 V.

All measurements for this device were taken using the typical application circuit, configured as shown in the assembly diagram (see Figure 41). The bias conditions shown in the electrical specifications table (see Table 1 to Table 3) are the operating points recommended to optimize the overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the HMC8500 under other bias conditions may provide performance that differs from that shown in the Typical Performance Characteristics section.

The evaluation PCB provides the HMC8500 in its typical application circuit, allowing easy operation using standard dc power supplies and 50 Ω RF test equipment.



NOTES  
1. CONNECT NIC PINS TO GND FOR BETTER THERMAL PERFORMANCE.

Figure 41. Typical Application Circuit

14684-041

## EVALUATION BOARD

The **HMC8500** evaluation board is a 2-layer board fabricated using Rogers 4350 and using best practices for high frequency RF design. The RF input and RF output traces have a 50  $\Omega$  characteristic impedance. The board is attached to a heat sink using an electrically and thermally conductive epoxy providing a low thermal and low dc resistance path. Components are mounted using SN63 solder allowing rework of the surface-mount components without compromising the circuit board to heat sink attachment.

The evaluation board and populated components are designed to operate over the ambient temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . During operation, attach the evaluation board to a temperature controlled plate to control the temperature of the **HMC8500** during operation. For the proper bias sequence, see the Applications Information section.

A fully populated and tested evaluation board, shown in Figure 42, is available from Analog Devices, Inc., upon request.

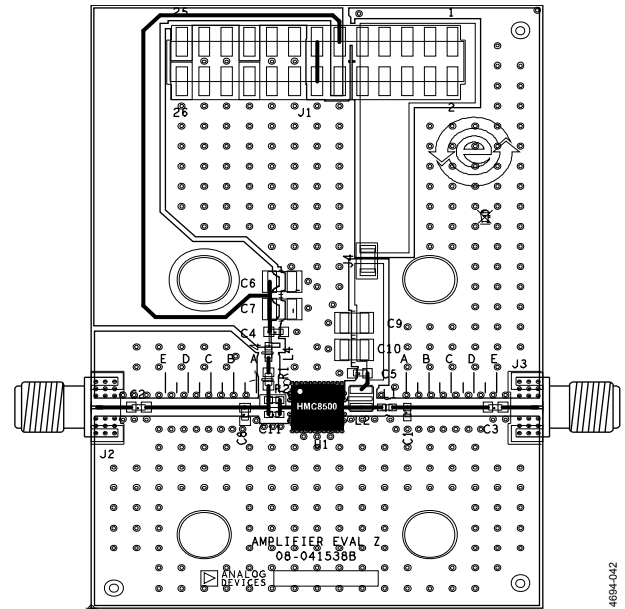


Figure 42. Evaluation PCB

Table 8. Bill of Materials for Evaluation PCB **EV1HMC8500LP5D**

Item	Description	Manufacturer/Part Number
J2, J3	K connector	SRI/25-146-1000-92
J1	Preform surface terminal strip	SAMTEC/TSM-113-01-L-DV
J4	Surface-mount jumper	Components corporation/SJ-1206-01-T
C1	0.8 pF capacitor, 0402 package	Murata/GRM1555C1HR80BA01D
C2, C3, C4, C5	2.2 nF capacitors, 0603 package	TDK/C1608C0G1H222J
C6, C7, C9, C10	10 $\mu\text{F}$ capacitors, 1210-2 package	TDK/ C3225X7S1H106K250AB
C8	2 pF capacitor, 0603 package	Murata/GQM1875C2E2R0BB12
C11	10 pF capacitor, 0402 package	Phycomp (Yageo)/CC0402JRNPO9BN100
L1	1.2 nH inductor, 0402 package	Panasonic/ ELJ-RF1N2DF
L2	910 nH inductor, 1008CS package	Coilcraft/1008CS-911XGLB
L4	3.6 nH inductor, 0603 package	Coilcraft/0603CS-3N6XGLU
R1	25 $\Omega$ high precision resistor, 0603package	Vishay/P0603E25R0BNT
R2	10 $\Omega$ resistor, 0402 package	Panasonic/ERJ-2RKF10R0X
Heat sink	Used for thermal transfer from the HMC8500 amplifier	Not applicable
U1	Amplifier	Analog Devices/HMC8500
PCB	<b>EV1HMC8500LP5D</b> Circuit board material: Rogers 4350	Analog Devices/ <b>EV1HMC8500LP5D</b>

OUTLINE DIMENSIONS

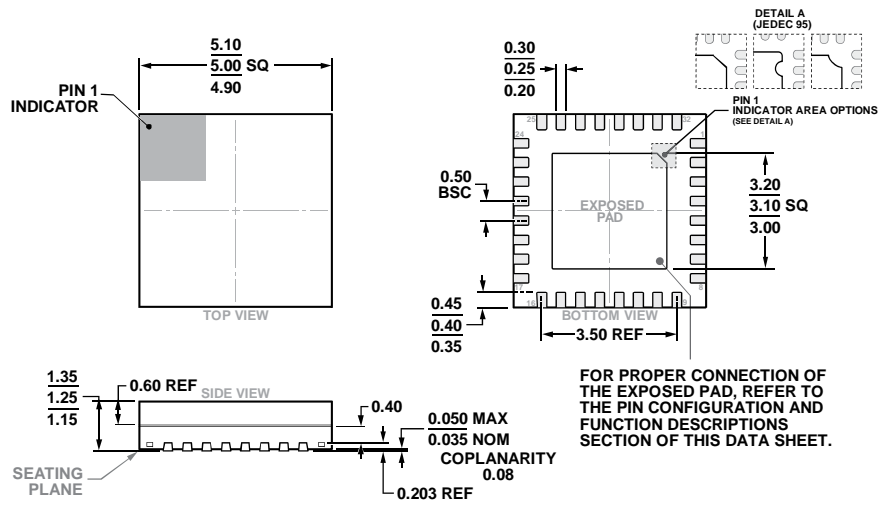


Figure 43. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP\_CAV]  
 5 mm x 5 mm Body and 1.25 mm Package Height  
 (CG-32-2)  
 Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1,2</sup>	Temperature	MSL Rating <sup>3</sup>	Description <sup>4</sup>	Package Option
HMC8500LP5DE	-40°C to +85°C	MSL3	32-Lead LFCSP_CAV	CG-32-2
HMC8500LP5DETR	-40°C to +85°C	MSL3	32-Lead LFCSP_CAV	CG-32-2
EV1HMC8500LP5D			Evaluation PCB	

<sup>1</sup> The HMC8500LP5DE and the HMC8500LP5DETR are LFCSP premolded copper alloy lead frame and RoHS compliant.

<sup>2</sup> When ordering the evaluation board only, reference the model number, EV1HMC8500LP5D.

<sup>3</sup> See the Absolute Maximum Ratings section for additional information.

<sup>4</sup> The lead finish of the HMC8500LP5DE and the HMC8500LP5DETR is nickel palladium gold (NiPdAu).