# CY91460C Series

# FR60 32-bit Microcontroller

CY91460C series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.

This series contains the LIN-USART and CAN controllers.

## Features

### FR60 CPU Core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

### Internal Peripheral Resources

- General-purpose ports : Maximum 104 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously.
  - 2 transfer sources (internal peripheral/software)
  - Activation source can be selected using software
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Transfer data size selectable from 8/16/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200H to 240H, 1000H to 1024H)
- A/D converter (successive approximation type)
  - 10-bit resolution: 30 channels
  - Conversion time: minimum 1 µs
- External interrupt inputs : 15 channels
  - 8 channels shared with CAN RX or $I^2C$ pins
- Bit search module (for REALOS)
  - Function to search the first bit position of “1”, “0”, “changed” from the MSB (most significant bit) within one word
- LIN-USART (full duplex double buffer): 5 channels
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
- $I^2C$ bus interface (supports 400 kbps): 3 channels
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 3 channels
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- Stepper motor controller : 6 channels
  - 4 high current output to each channel
  - 2 synchronized PWMs per channel (8/10-bit)
- Sound generator : 1 channel
  - Tone frequency : PWM frequency divide-by-two (reload value + 1)
- Alarm comparator : 1 channel
  - Monitor external voltage
  - Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer : 12 channels
- 16-bit PFM timer : 1 channel
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: 8 channels (operates in conjunction with the free-run timer)
- Output compare: 4 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 3 channels (3*8-bit or 2*16-bit)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Low voltage detection circuit
- Clock supervisor
  - Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor

- Sub-clock calibration
  - Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer
  - Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
  - Sub-oscillator stabilization timer
  - Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

### Package and Technology

- Package: QFP-144
- CMOS 180 nm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 105°C

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## 1. Product Lineup

| Feature | CY91V460 | CY91F463CA | CY91F465CA | CY91F467CA<br>CY91F467CB |
|---|---|---|---|---|
| Max. core frequency (CLKB) | 80 MHz | 100 MHz | 100 MHz | 100 MHz |
| Max. resource frequency (CLKP) | 40 MHz | 50 MHz | 50 MHz | 50 MHz |
| Max. external bus frequency (CLKT) | 40 MHz | - | - | - |
| Max. CAN frequency (CLKCAN) | 20 MHz | 50 MHz | 50 MHz | 50 MHz |
| Max. FlexRay frequency (SCLK) | - | - | - | - |
| Technology | 0.35µm | 0.18µm | 0.18µm | 0.18µm |
| Watchdog timer | yes | yes | yes | yes |
| Watchdog timer (RC osc. based) | yes (disengageable) | yes | yes | yes |
| Bit Search | yes | yes | yes | yes |
| Reset input (INITX) | yes | yes | yes | yes |
| Hardware standby input (HSTX) | yes | no | no | no |
| Clock Modulator | yes | yes | yes | yes |
| Clock Monitor | yes | yes | yes | yes |
| Low Power Mode | yes | yes | yes | yes |
| DMA | 5 ch | 5 ch | 5 ch | 5 ch |
| MMU/MPU | MPU (16 ch)[*1] | MPU (4 ch)[*1] | MPU (8 ch)[*1] | MPU (8 ch)[*1] |
| | | | | |
| Flash memory | Emulation SRAM<br>32bit read data | 288 KByte | 544 KByte | 1088 KByte |
| Satellite Flash memory | - | - | - | - |
| Flash Protection | - | yes | yes | yes |
| | | | | |
| D-RAM | 64 KByte | 16 KByte | 16 KByte | 32 KByte |
| ID-RAM | 64 KByte | 8 KByte | 16 KByte | 32 KByte |
| Flash-Cache (Instruction cache) | 16 KByte | 4 KByte | 8 KByte | 8 KByte |
| Boot-ROM / BI-ROM | 4 KByte fixed | 4 KByte | 4 KByte | 4 KByte |
| | | | | |
| RTC | 1 ch | 1 ch | 1 ch | 1 ch |
| Free Running Timer | 8 ch | 8 ch | 8 ch | 8 ch |
| ICU | 8 ch | 8 ch | 8 ch | 8 ch |
| OCU | 8 ch | 4 ch | 4 ch | 4 ch |
| Reload Timer | 8 ch | 8 ch | 8 ch | 8 ch |
| PPG 16-bit | 16 ch | 12 ch | 12 ch | 12 ch |
| PFM 16-bit | 1 ch | 1 ch | 1 ch | 1 ch |
| Sound Generator | 1 ch | 1 ch | 1 ch | 1 ch |
| Up/Down Counter (8/16 bit) | 4 ch (8-bit) / 2 ch (16-bit) | 3 ch (8-bit) / 2ch (16-bit) | 3 ch (8-bit) / 2ch (16-bit) | 3 ch (8-bit) / 2ch (16-bit) |
| | | | | |
| C_CAN | 6 ch<br>(128msg) | 3 ch<br>(32msg) | 3 ch<br>(32msg) | 3 ch<br>(32msg) |
| LIN-USART | 4 ch + 4 ch FIFO<br>+ 8 ch | 1 ch + 4 ch FIFO | 1 ch + 4 ch FIFO | 1 ch + 4 ch FIFO |

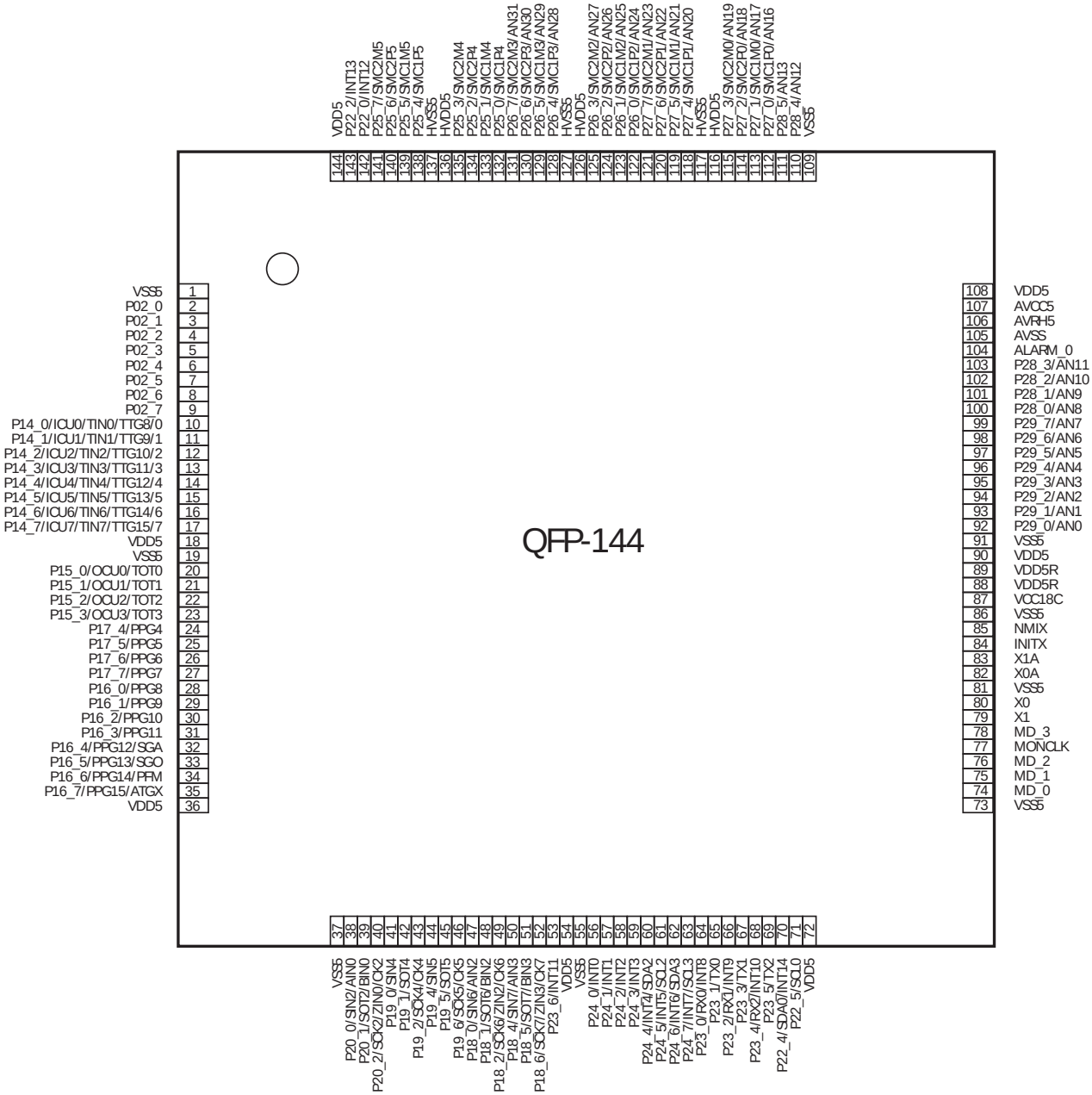
| Feature | CY91V460 | CY91F463CA | CY91F465CA | CY91F467CA<br>CY91F467CB |
|---|---|---|---|---|
| $I^2C$ (400K) | 4 ch | 3 ch | 3 ch | 3 ch |
| | | | | |
| FR external bus | yes (32bit addr, 32bit data) | - | - | - |
| External Interrupts | 16 ch | 15 ch | 15 ch | 15 ch |
| NMI Interrupts | 1 ch | 1 ch | 1 ch | 1 ch |
| | | | | |
| SMC | 6 ch | 6 ch | 6 ch | 6 ch |
| LCD controller (40x4) | 1 ch | - | - | - |
| | | | | |
| ADC (10-bit) | 32 ch | 30 ch | 30 ch | 30 ch |
| Alarm Comparator | 2 ch | 1 ch | 1 ch | 1 ch |
| | | | | |
| Supply Supervisor (low voltage detection) | yes | yes | yes | yes |
| Clock Supervisor | yes | yes | yes | yes |
| | | | | |
| Main clock oscillator | 4 MHz | 4 MHz | 4 MHz | 4 MHz |
| Sub clock oscillator | 32kHz | 32kHz | 32kHz | 32kHz |
| RC oscillator | 100kHz | 100kHz / 2MHz | 100kHz / 2MHz | 100kHz / 2MHz |
| PLL | x 20 | x 25 | x 25 | x 25 |
| | | | | |
| DSU4 | yes | no | no | no |
| EDSU | yes (32 BP)*1 | yes (8 BP)*1 | yes (16 BP)*1 | yes (16 BP)*1 |
| | | | | |
| Supply voltage | 3V/5V | 3V/5V | 3V/5V | 3V/5V |
| Regulator | yes | yes | yes | yes |
| Power consumption | n.a. | < 1 W | < 1 W | < 1 W |
| Temperature Range (Ta) | 0.70 C | -40.105 C | -40.105 C | -40.105 C |
| | | | | |
| Package | BGA660 | QFP-144 | QFP-144 | QFP-144 |
| | | | | |
| Power on to PLL run | < 20 ms | < 20 ms | < 20 ms | < 20 ms |
| Flash Download Time | n.a. | < 5 sec. typical | < 5 sec. typical | < 6 sec typical |
| | | | | |

*1: MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

## 2. Pin Assignment

### 2.1 CY91F463CA, CY91F465CA, CY91F467Cx

(TOP VIEW)




(LQS144)

# 3. Pin Description

## 3.1 CY91F463CA, CY91F465CA, CY91F467Cx

| Pin No. | Pin Name | I/O | I/O Circuit Type* | Function |
|---|---|---|---|---|
| 2 to 9 | P02_0 to P02_7 | I/O | A | General-purpose input/output ports |
| 10 to 17 | P14_0 to P14_7 | I/O | A | General-purpose input/output ports |
| | ICU0 to ICU7 | | | Input capture input pins |
| | TIN0 to TIN7 | | | External trigger input pins of reload timer |
| | TTG8/0 to TTG15/7 | | | External trigger input pins of PPG timer |
| 20 to 23 | P15_0 to P15_3 | I/O | A | General-purpose input/output ports |
| | OCU0 to OCU3 | | | Output compare output pins |
| | TOT0 to TOT3 | | | Reload timer output pins |
| 24 to 27 | P17_4 to P17_7 | I/O | A | General-purpose input/output ports |
| | PPG4 to PPG7 | | | Output pins of PPG timer |
| 28 to 31 | P16_0 to P16_3 | I/O | A | General-purpose input/output ports |
| | PPG8 to PPG11 | | | Output pins of PPG timer |
| 32 | P16_4 | I/O | A | General-purpose input/output ports |
| | PPG12 | | | Output pins of PPG timer |
| | SGA | | | SGA output pin of sound generator |
| 33 | P16_5 | I/O | A | General-purpose input/output ports |
| | PPG13 | | | Output pins of PPG timer |
| | SGO | | | SGO output pin of sound generator |
| 34 | P16_6 | I/O | A | General-purpose input/output ports |
| | PPG14 | | | Output pins of PPG timer |
| | PFM | | | Pulse frequency modulator output pin |
| 35 | P16_7 | I/O | A | General-purpose input/output ports |
| | PPG15 | | | Output pins of PPG timer |
| | ATGX | | | A/D converter external trigger input pin |
| 38 | P20_0 | I/O | A | General-purpose input/output ports |
| | SIN2 | | | Data input pin of USART2 |
| | AIN0 | | | Up/down counter input pin |
| 39 | P20_1 | I/O | A | General-purpose input/output ports |
| | SOT2 | | | Data output pin of USART2 |
| | BIN0 | | | Up/down counter input pin |
| 40 | P20_2 | I/O | A | General-purpose input/output ports |
| | SCK2 | | | Clock input/output pin of USART2 |
| | ZIN0 | | | Up/down counter input pin |
| | CK2 | | | External clock input pin of free-run timer 2 |

| Pin No. | Pin Name | I/O | I/O Circuit Type* | Function |
|---|---|---|---|---|
| 41 | P19_0 | I/O | A | General-purpose input/output ports |
| | SIN4 | | | Data input pin of USART4 |
| 42 | P19_1 | I/O | A | General-purpose input/output ports |
| | SOT4 | | | Data output pin of USART4 |
| 43 | P19_2 | I/O | A | General-purpose input/output ports |
| | SCK4 | | | Clock input/output pin of USART4 |
| | CK4 | | | External clock input pin of free-run timer 4 |
| 44 | P19_4 | I/O | A | General-purpose input/output ports |
| | SIN5 | | | Data input pin of USART5 |
| 45 | P19_5 | I/O | A | General-purpose input/output ports |
| | SOT5 | | | Data output pin of USART5 |
| 46 | P19_6 | I/O | A | General-purpose input/output ports |
| | SCK5 | | | Clock input/output pin of USART5 |
| | CK5 | | | External clock input pin of free-run timer 5 |
| 47 | P18_0 | I/O | A | General-purpose input/output ports |
| | SIN6 | | | Data input pin of USART6 |
| | AIN2 | | | Up/down counter input pin |
| 48 | P18_1 | I/O | A | General-purpose input/output ports |
| | SOT6 | | | Data output pin of USART6 |
| | BIN2 | | | Up/down counter input pin |
| 49 | P18_2 | I/O | A | General-purpose input/output ports |
| | SCK6 | | | Clock input/output pin of USART6 |
| | ZIN2 | | | Up/down counter input pin |
| | CK6 | | | External clock input pin of free-run timer 6 |
| 50 | P18_4 | I/O | A | General-purpose input/output ports |
| | SIN7 | | | Data input pin of USART7 |
| | AIN3 | | | Up/down counter input pin |
| 51 | P18_5 | I/O | A | General-purpose input/output ports |
| | SOT7 | | | Data output pin of USART7 |
| | BIN3 | | | Up/down counter input pin |
| 52 | P18_6 | I/O | A | General-purpose input/output ports |
| | SCK7 | | | Clock input/output pin of USART7 |
| | ZIN3 | | | Up/down counter input pin |
| | CK7 | | | External clock input pin of free-run timer 7 |
| 53 | P23_6 | I/O | A | General-purpose input/output ports |
| | INT11 | | | External Interrupt input (CAN wakeup) |

| Pin No. | Pin Name | I/O | I/O Circuit Type* | Function |
|---|---|---|---|---|
| 56 to 59 | P24_0 to P24_3 | I/O | A | General-purpose input/output ports |
| | INT0 to INT3 | | | External Interrupt input |
| 60 | P24_4 | I/O | A | General-purpose input/output ports |
| | INT4 | | | External Interrupt input |
| | SDA2 | | | $I^2C$ bus DATA input/output pin (open drain) |
| 61 | P24_5 | I/O | A | General-purpose input/output ports |
| | INT5 | | | External Interrupt input |
| | SCL2 | | | $I^2C$ bus clock input/output pin (open drain) |
| 62 | P24_6 | I/O | A | General-purpose input/output ports |
| | INT6 | | | External Interrupt input |
| | SDA3 | | | $I^2C$ bus DATA input/output pin (open drain) |
| 63 | P24_7 | I/O | A | General-purpose input/output ports |
| | INT7 | | | External Interrupt input |
| | SCL3 | | | $I^2C$ bus clock input/output pin (open drain) |
| 64 | P23_0 | I/O | A | General-purpose input/output ports |
| | RX0 | | | RX input/output pin of CAN0 |
| | INT8 | | | External Interrupt input (CAN wakeup) |
| 65 | P23_1 | I/O | A | General-purpose input/output ports |
| | TX0 | | | TX output pin of CAN0 |
| 66 | P23_2 | I/O | A | General-purpose input/output ports |
| | RX1 | | | RX input/output pin of CAN1 |
| | INT9 | | | External Interrupt input (CAN wakeup) |
| 67 | P23_3 | I/O | A | General-purpose input/output ports |
| | TX1 | | | TX output pin of CAN1 |
| 68 | P23_4 | I/O | A | General-purpose input/output ports |
| | RX2 | | | RX input/output pin of CAN2 |
| | INT10 | | | External Interrupt input (CAN wakeup) |
| 69 | P23_5 | I/O | A | General-purpose input/output ports |
| | TX2 | | | TX output pin of CAN2 |
| 70 | P22_4 | I/O | A | General-purpose input/output ports |
| | SDA0 | | | $I^2C$ bus DATA input/output pin (open drain) |
| | INT14 | | | External Interrupt input ($I^2C$ wakeup) |
| 71 | P22_5 | I/O | A | General-purpose input/output ports |
| | SCL0 | | | $I^2C$ bus clock input/output pin (open drain) |
| 74 to 76 | MD_0 to MD_2 | I | G | Mode setting pins |
| 77 | MONCLK | O | G | Clock monitor pin |
| 78 | MD_3 | I | G | To be connected to VSS |

| Pin No. | Pin Name | I/O | I/O Circuit Type* | Function |
|---|---|---|---|---|
| 79 | X1 | — | J1 | Clock (oscillation) output |
| 80 | X0 | — | J1 | Clock (oscillation) output |
| 82 | X0A | — | J2 | Sub clock (oscillation) output |
| 83 | X1A | — | J2 | Sub clock (oscillation) output |
| 84 | INITX | I | H | External reset input pin |
| 85 | NMIX | I | H | Non-Maskable Interrupt input |
| 92 to 99 | P29_0 to P29_7 | I/O | B | General-purpose input/output ports |
| | AN0 to AN7 | | | Analog input pins of A/D converter |
| 100 to 103 | P28_0 to P28_3 | I/O | B | General-purpose input/output ports |
| | AN8 to AN11 | | | Analog input pins of A/D converter |
| 104 | ALARM_0 | I | I | Alarm comparator input pin |
| 110, 111 | P28_4, P28_5 | I/O | B | General-purpose input/output ports |
| | AN12 to AN13 | | | Analog input pins of A/D converter |
| 112 | P27_0 | I/O | F | General-purpose input/output ports |
| | SMC1P0 | | | Controller output pin of Stepper motor |
| | AN16 | | | Analog input pins of A/D converter |
| 113 | P27_1 | I/O | F | General-purpose input/output ports |
| | SMC1M0 | | | Controller output pin of Stepper motor |
| | AN17 | | | Analog input pins of A/D converter |
| 114 | P27_2 | I/O | F | General-purpose input/output ports |
| | SMC2P0 | | | Controller output pin of Stepper motor |
| | AN18 | | | Analog input pins of A/D converter |
| 115 | P27_3 | I/O | F | General-purpose input/output ports |
| | SMC2M0 | | | Controller output pin of Stepper motor |
| | AN19 | | | Analog input pins of A/D converter |
| 118 | P27_4 | I/O | F | General-purpose input/output ports |
| | SMC1P1 | | | Controller output pin of Stepper motor |
| | AN20 | | | Analog input pins of A/D converter |
| 119 | P27_5 | I/O | F | General-purpose input/output ports |
| | SMC1M1 | | | Controller output pin of Stepper motor |
| | AN21 | | | Analog input pins of A/D converter |
| 120 | P27_6 | I/O | F | General-purpose input/output ports |
| | SMC2P1 | | | Controller output pin of Stepper motor |
| | AN22 | | | Analog input pins of A/D converter |
| 121 | P27_7 | I/O | F | General-purpose input/output ports |
| | SMC2M1 | | | Controller output pin of Stepper motor |
| | AN23 | | | Analog input pins of A/D converter |

| Pin No. | Pin Name | I/O | I/O Circuit Type* | Function |
|---|---|---|---|---|
| 122 | P26_0 | I/O | F | General-purpose input/output ports |
| | SMC1P2 | | | Controller output pin of Stepper motor |
| | AN24 | | | Analog input pins of A/D converter |
| 123 | P26_1 | I/O | F | General-purpose input/output ports |
| | SMC1M2 | | | Controller output pin of Stepper motor |
| | AN25 | | | Analog input pins of A/D converter |
| 124 | P26_2 | I/O | F | General-purpose input/output ports |
| | SMC2P2 | | | Controller output pin of Stepper motor |
| | AN26 | | | Analog input pins of A/D converter |
| 125 | P26_3 | I/O | F | General-purpose input/output ports |
| | SMC2M2 | | | Controller output pin of Stepper motor |
| | AN27 | | | Analog input pins of A/D converter |
| 128 | P26_4 | I/O | F | General-purpose input/output ports |
| | SMC1P3 | | | Controller output pin of Stepper motor |
| | AN28 | | | Analog input pins of A/D converter |
| 129 | P26_5 | I/O | F | General-purpose input/output ports |
| | SMC1M3 | | | Controller output pin of Stepper motor |
| | AN29 | | | Analog input pins of A/D converter |
| 130 | P26_6 | I/O | F | General-purpose input/output ports |
| | SMC2P3 | | | Controller output pin of Stepper motor |
| | AN30 | | | Analog input pins of A/D converter |
| 131 | P26_7 | I/O | F | General-purpose input/output ports |
| | SMC2M3 | | | Controller output pin of Stepper motor |
| | AN31 | | | Analog input pins of A/D converter |
| 132 | P25_0 | I/O | E | General-purpose input/output ports |
| | SMC1P4 | | | Controller output pin of Stepper motor |
| 133 | P25_1 | I/O | E | General-purpose input/output ports |
| | SMC1M4 | | | Controller output pin of Stepper motor |
| 134 | P25_2 | I/O | E | General-purpose input/output ports |
| | SMC2P4 | | | Controller output pin of Stepper motor |
| 135 | P25_3 | I/O | E | General-purpose input/output ports |
| | SMC2M4 | | | Controller output pin of Stepper motor |
| 138 | P25_4 | I/O | E | General-purpose input/output ports |
| | SMC1P5 | | | Controller output pin of Stepper motor |
| 139 | P25_5 | I/O | E | General-purpose input/output ports |
| | SMC1M5 | | | Controller output pin of Stepper motor |

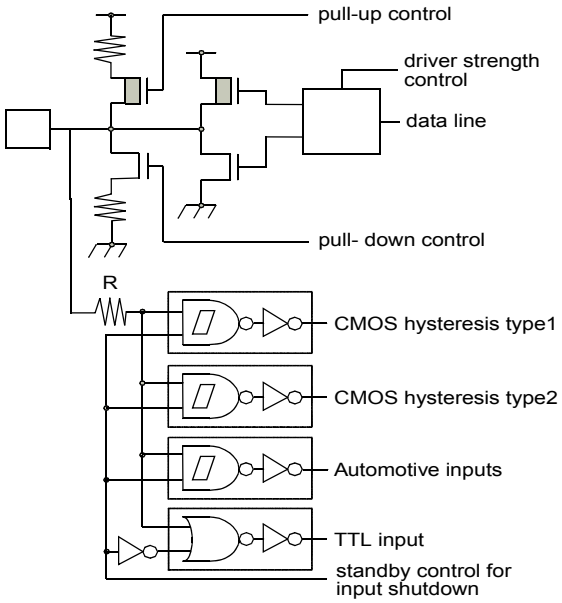
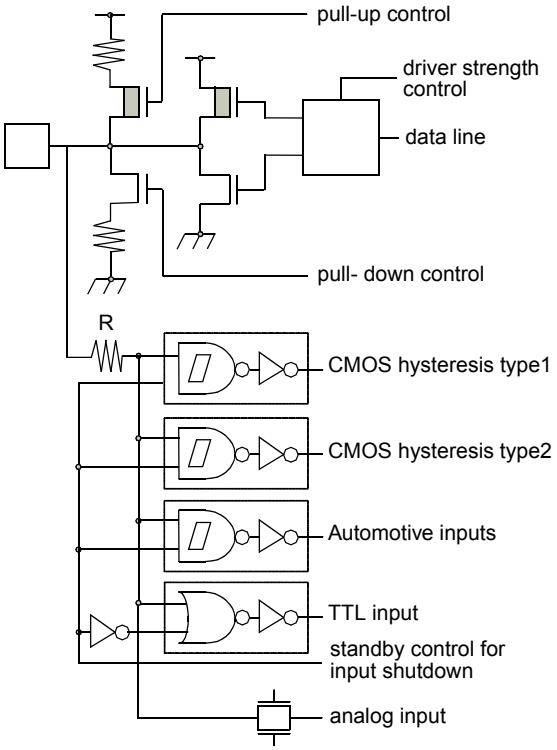
| Pin No. | Pin Name | I/O | I/O Circuit Type* | Function |
|---|---|---|---|---|
| 140 | P25_6 | I/O | E | General-purpose input/output ports |
| | SMC2P5 | | | Controller output pin of Stepper motor |
| 141 | P25_7 | I/O | E | General-purpose input/output ports |
| | SMC2M5 | | | Controller output pin of Stepper motor |
| 142 | P22_0 | I/O | A | General-purpose input/output ports |
| | INT12 | | | External Interrupt input ($I^2C$ wakeup) |
| 143 | P22_2 | I/O | A | General-purpose input/output ports |
| | INT13 | | | External Interrupt input ($I^2C$ wakeup) |

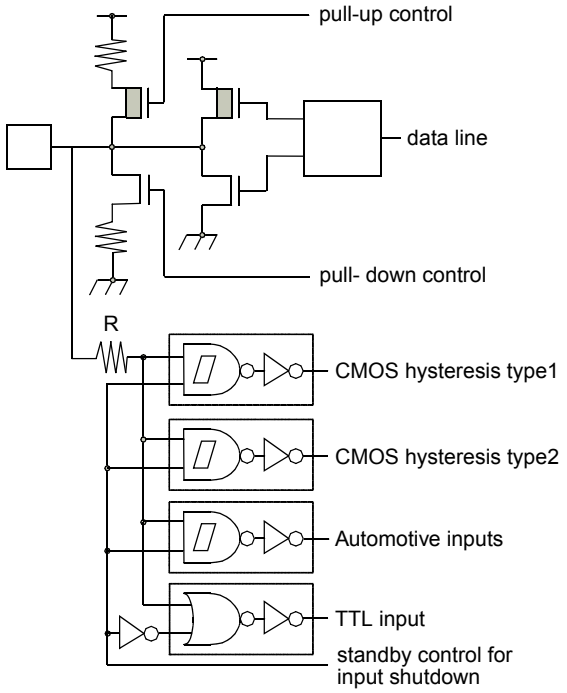
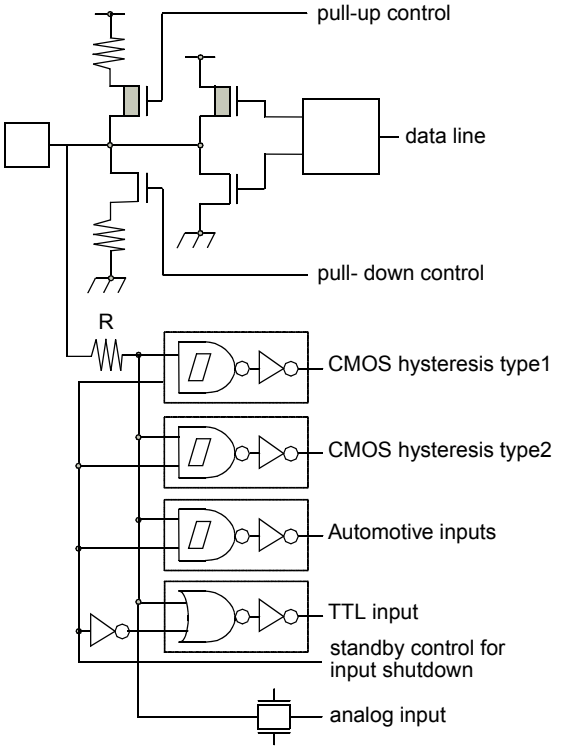
* : For information about the I/O circuit type, refer to “4. I/O Circuit Types”.

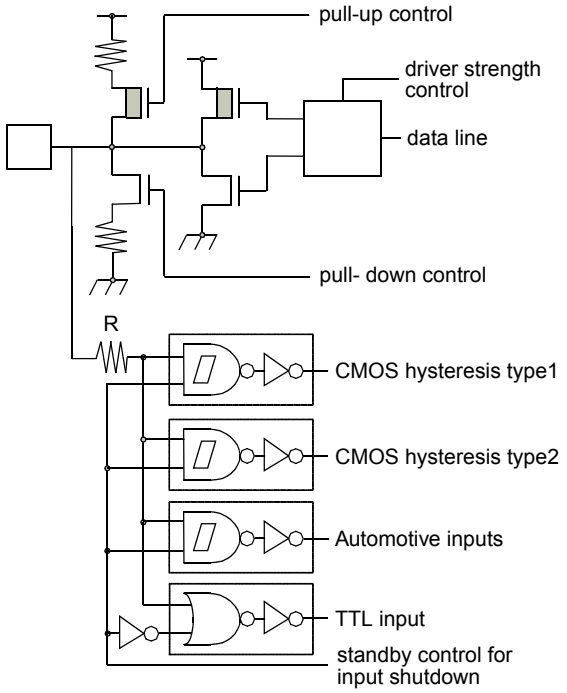
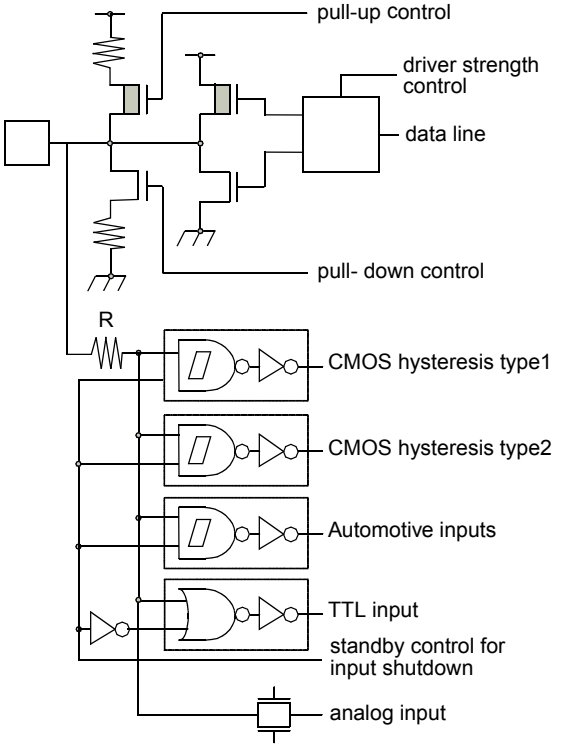
**[Power Supply/Ground Pins]**

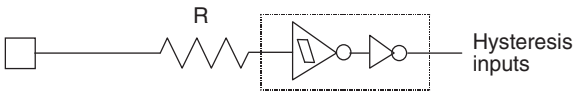
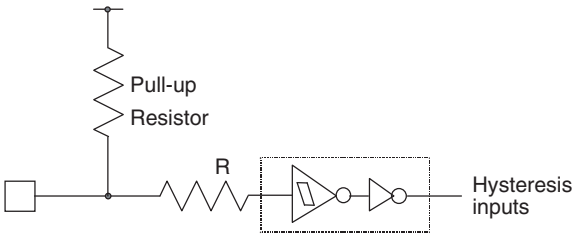
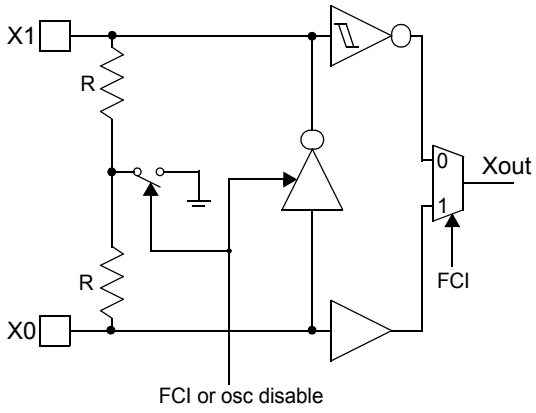
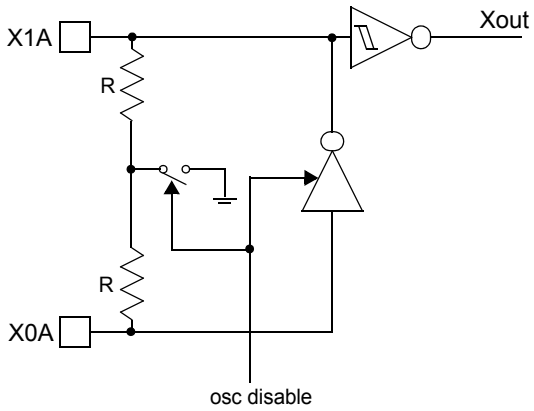
| Pin No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1, 19, 37, 55, 73, 81, 86, 91, 109 | VSS5 | Supply | Ground pins |
| 117, 127, 137 | HVSS5 | | Ground pins for Stepper motor controller |
| 18, 36, 54, 72, 90, 108, 144 | VDD5 | | Power supply pins |
| 116, 126, 136 | HVDD5 | | Power supply pins for Stepper motor controller |
| 88, 89 | VDD5R | | Power supply pins for internal regulator |
| 105 | AVSS5 | | Analog ground pin for A/D converter |
| 107 | AVCC5 | | Power supply pin for A/D converter |
| 106 | AVRH5 | | Reference power supply pin for A/D converter |
| 87 | VCC18C | | Capacitor connection pin for internal regulator |

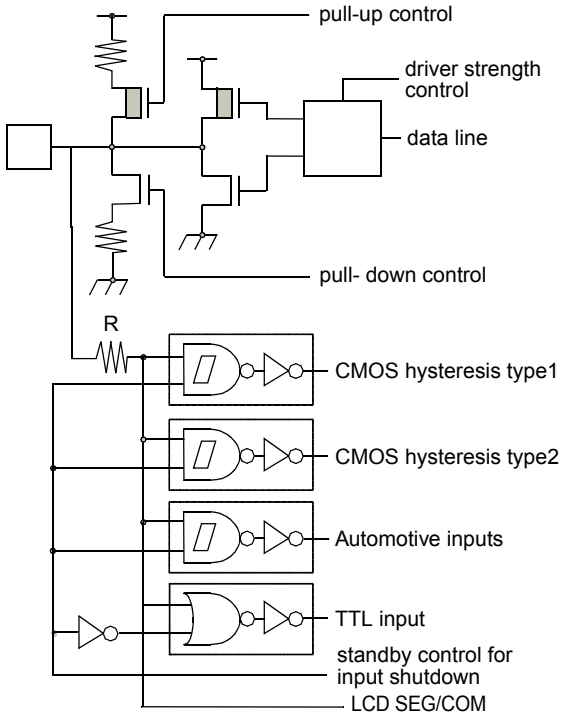
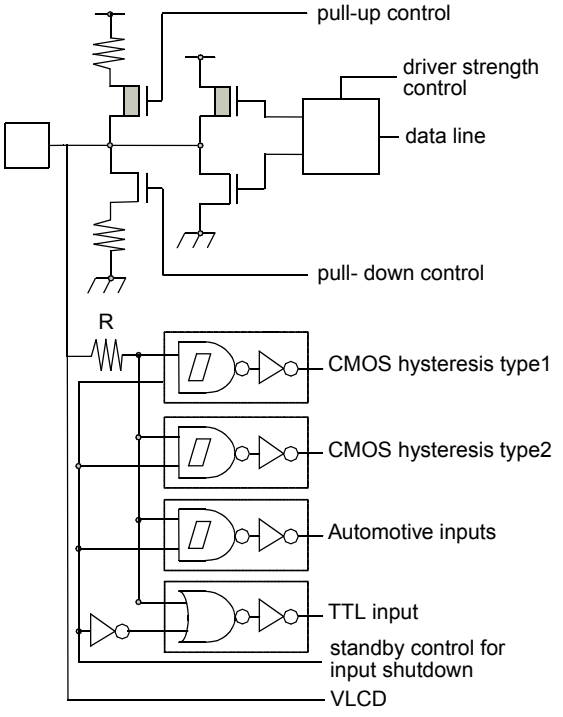
## 4. I/O Circuit Types

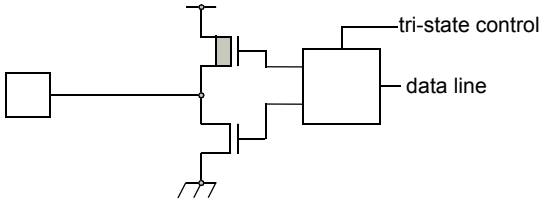
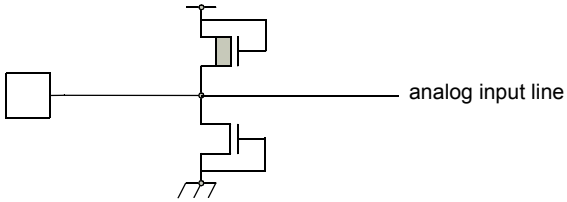
| Type | Circuit | Remarks |
|---|---|---|
| A |  | CMOS level output<br>(programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA<br>and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>2 different CMOS hysteresis inputs with input shutdown function<br>Automotive input with input shutdown function<br>TTL input with input shutdown function<br>Programmable pull-up resistor: 50kΩ approx. |
| B |  | CMOS level output<br>(programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA<br>and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>2 different CMOS hysteresis inputs with input shutdown function<br>Automotive input with input shutdown function<br>TTL input with input shutdown function<br>Programmable pull-up resistor: 50kΩ approx.<br>Analog input |

| Type | Circuit | Remarks |
|---|---|---|
| C |  | CMOS level output ($I_{OL}$ = 3mA, $I_{OH}$ = -3mA)<br>2 different CMOS hysteresis inputs with input shutdown function<br>Automotive input with input shutdown function<br>TTL input with input shutdown function<br>Programmable pull-up resistor: 50kΩ approx. |
| D |  | CMOS level output ($I_{OL}$ = 3mA, $I_{OH}$ = -3mA)<br>2 different CMOS hysteresis inputs with input shutdown function<br>Automotive input with input shutdown function<br>TTL input with input shutdown function<br>Programmable pull-up resistor: 50kΩ approx.<br>Analog input |

| Type | Circuit | Remarks |
|---|---|---|
| E |  | CMOS level output<br>(programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA<br>and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA,<br>and $I_{OL}$ = 30mA, $I_{OH}$ = -30mA)<br>2 different CMOS hysteresis inputs with input shutdown function<br>Automotive input with input shutdown function<br>TTL input with input shutdown function<br>Programmable pull-up resistor: 50kΩ approx. |
| F |  | CMOS level output<br>(programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA<br>and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA,<br>and $I_{OL}$ = 30mA, $I_{OH}$ = -30mA)<br>2 different CMOS hysteresis inputs with input shutdown function<br>Automotive input with input shutdown function<br>TTL input with input shutdown function<br>Programmable pull-up resistor: 50kΩ approx.<br>Analog input |

| Type | Circuit | Remarks |
|---|---|---|
| G |  | Mask ROM and EVA device:<br>CMOS Hysteresis input pin<br>Flash device:<br>CMOS input pin<br>12 V withstand (for MD [2:0]) |
| H |  | CMOS Hysteresis input pin<br>Pull-up resistor value: 50 kΩ approx. |
| J1 |  | High-speed oscillation circuit:<br>• Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)<br>• Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode. |
| J2 |  | Low-speed oscillation circuit:<br>• Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled. |

| Type | Circuit | Remarks |
|---|---|---|
| K |  | CMOS level output<br>(programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA<br>and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>2 different CMOS hysteresis inputs with input shutdown function<br>Automotive input with input shutdown function<br>TTL input with input shutdown function<br>Programmable pull-up resistor: 50kΩ approx.<br>LCD SEG/COM output |
| L |  | CMOS level output<br>(programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA<br>and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>2 different CMOS hysteresis inputs with input shutdown function<br>Automotive input with input shutdown function)<br>TTL input with input shutdown function<br>Programmable pull-up resistor: 50kΩ approx.<br>Analog input<br>LCD Voltage input |

| Type | Circuit | Remarks |
|---|---|---|
| M |  | CMOS level tri-state output ($I_{OL}$ = 5mA, $I_{OH}$ = -5mA) |
| N |  | Analog input pin with protection |

# 5. Handling Devices

## 5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$ *1) or less than ($V_{SS}5$ or $HV_{SS}5$ *1) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note *1: $HV_{DD}5$, $HV_{SS}5$ are available only on devices having Stepper Motor Controller.

## 5.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

## 5.3 Power Supply Pins

In CY91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the CY91460 series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

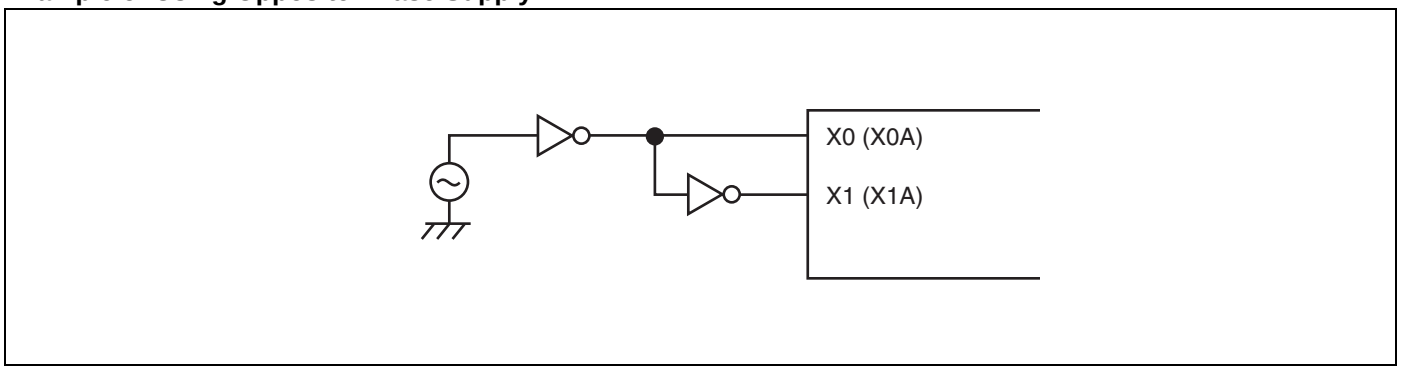
## 5.4 Crystal Oscillator Circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

## 5.5 Notes on Using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

**Example of Using Opposite Phase Supply**




*(Continued)*

*(Continued)*

### 5.6 Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

### 5.7 Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

### 5.8 Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

# 6. Notes on Debugger

## 6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

## 6.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

## 6.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

## 6.4 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

**The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:**

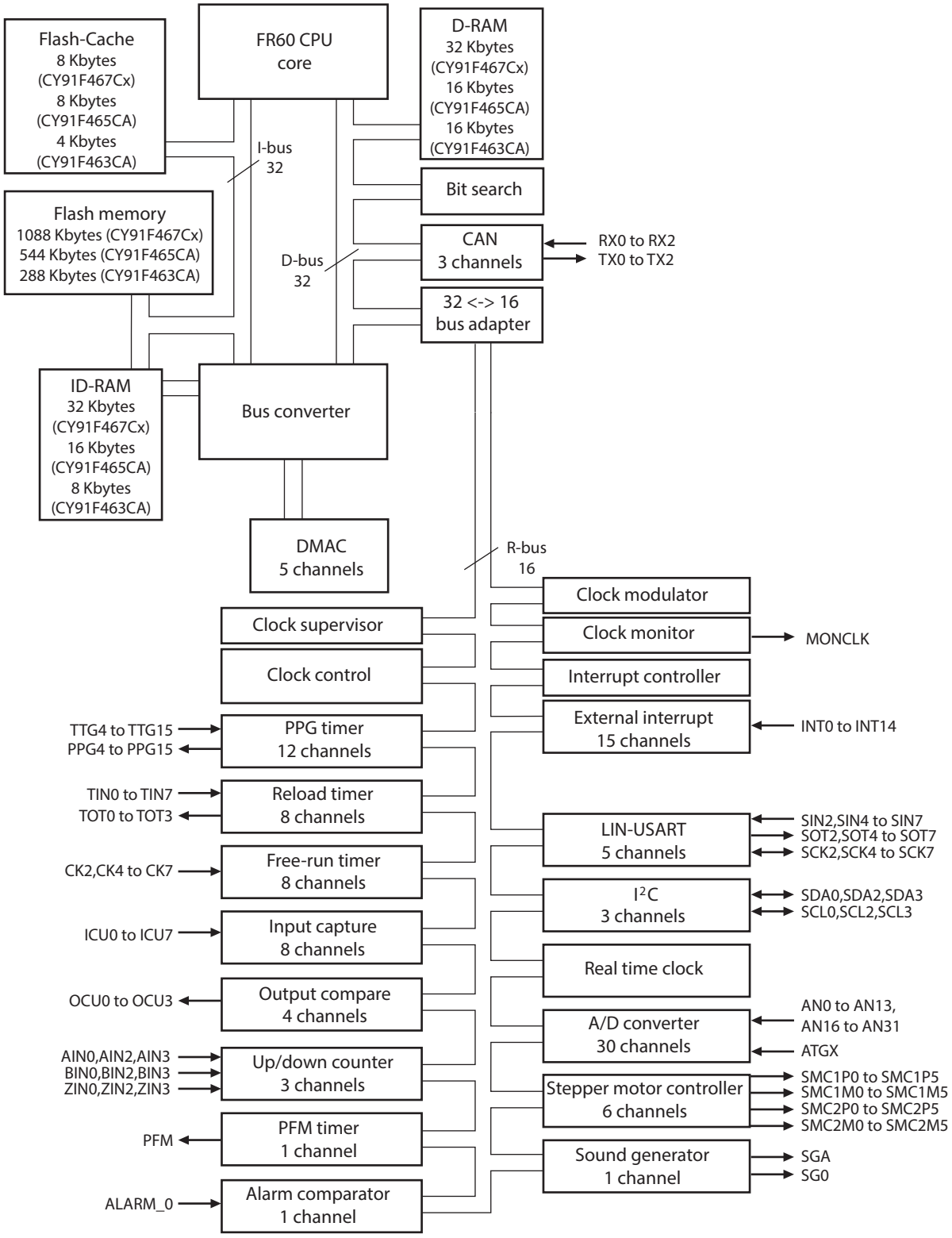
a. a user interrupt or NMI is accepted;
b. single-step execution is performed;
c. execution breaks due to a data event or from the emulator menu.
   1. D0 and D1 flags are updated in advance.
   2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
   3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

**The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.**

1. The PS register is updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

# 7. Block Diagram

## 7.1 CY91F463CA, CY91F465CA, CY91F467Cx



# 8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

## 8.1 Features

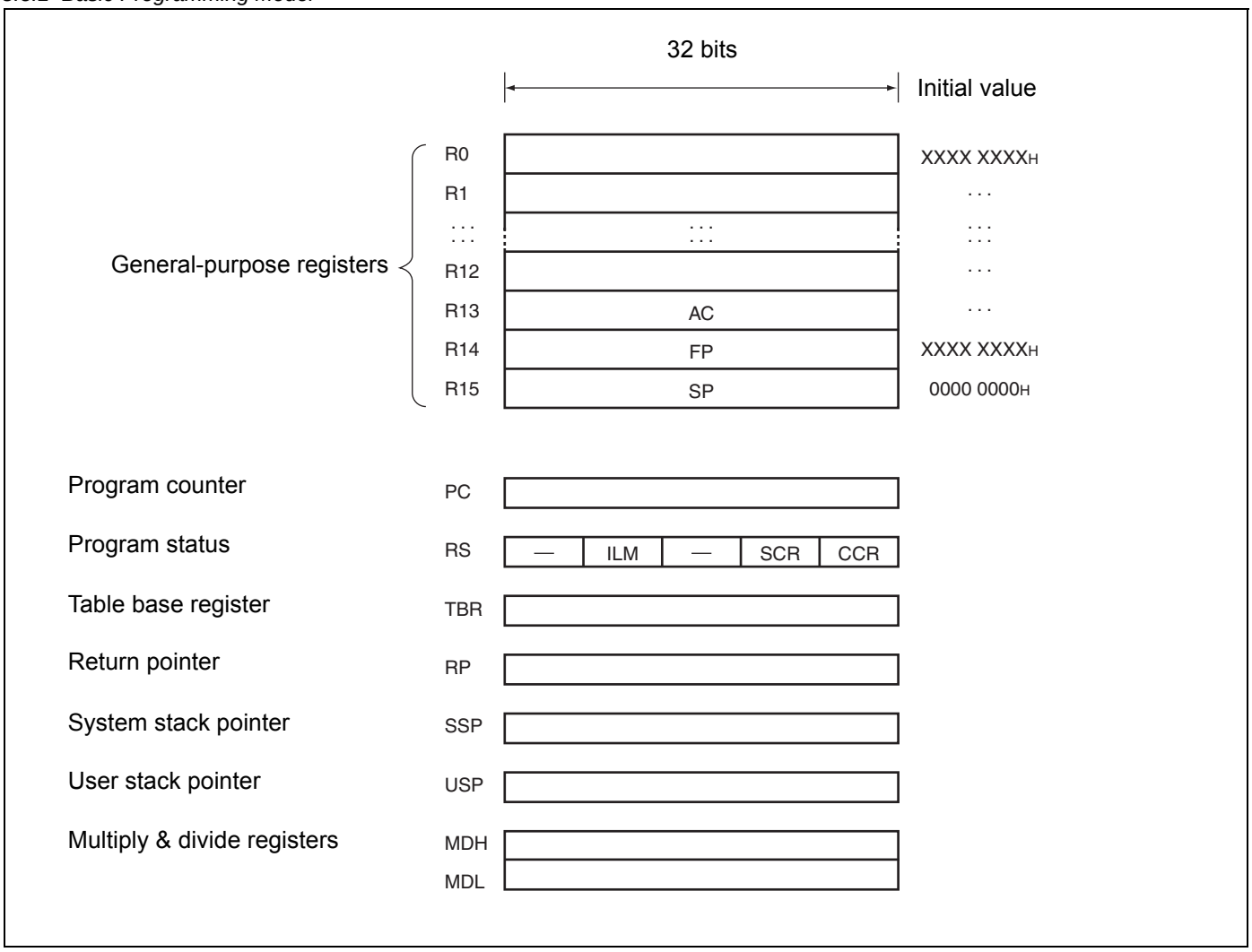
- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

## 8.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

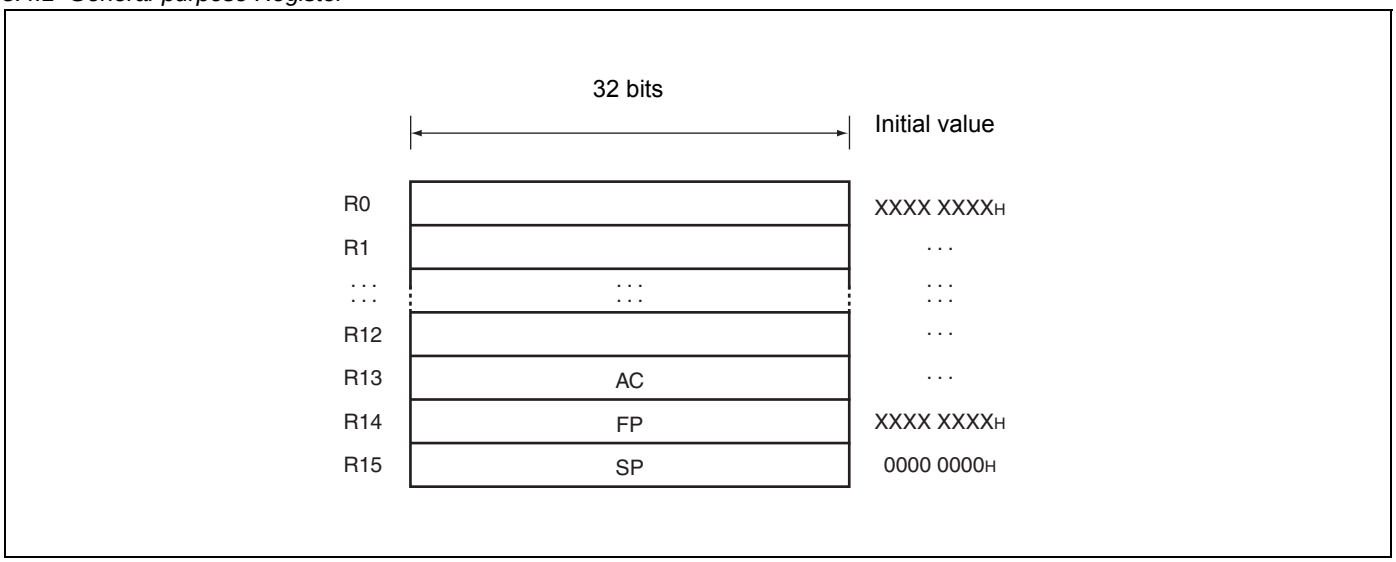
## 8.3 Programming Model

### *8.3.1 Basic Programming Model*



## 8.4 Registers

### *8.4.1 General-purpose Register*




Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

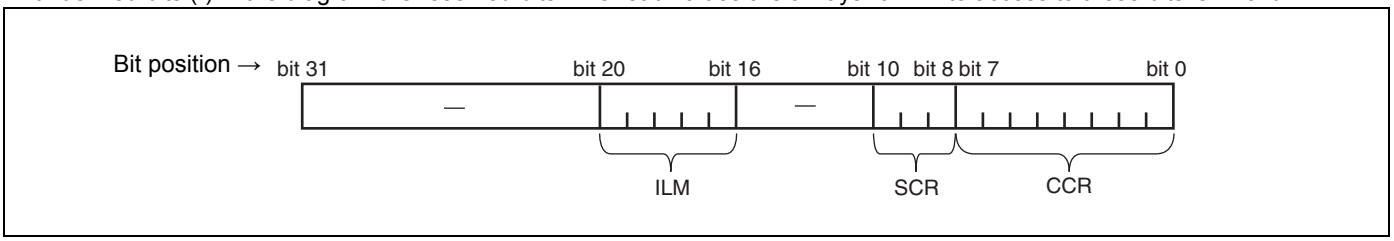
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is $00000000_H$ (SSP value).

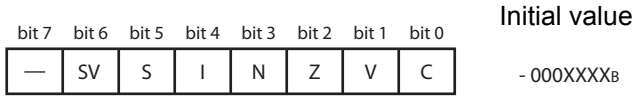
### *8.4.2 PS (Program Status)*

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.

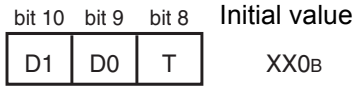


### 8.4.3 CCR (Condition Code Register)




SV : Supervisor flag
S : Stack flag
I : Interrupt enable flag
N : Negative enable flag
Z : Zero flag
V : Overflow flag
C : Carry flag

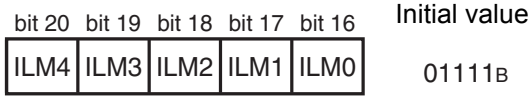
### 8.4.4 SCR (System Condition Register)




Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

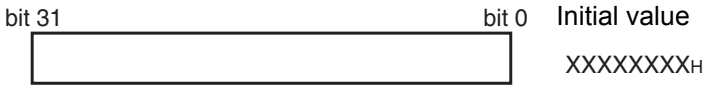
Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

### 8.4.5 ILM (Interrupt Level Mask Register)



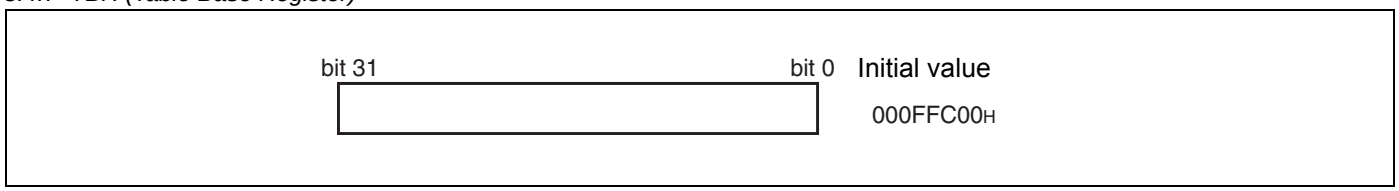

This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.
The register is initialized to value "$01111_B$" at reset.

### 8.4.6 PC (Program Counter)



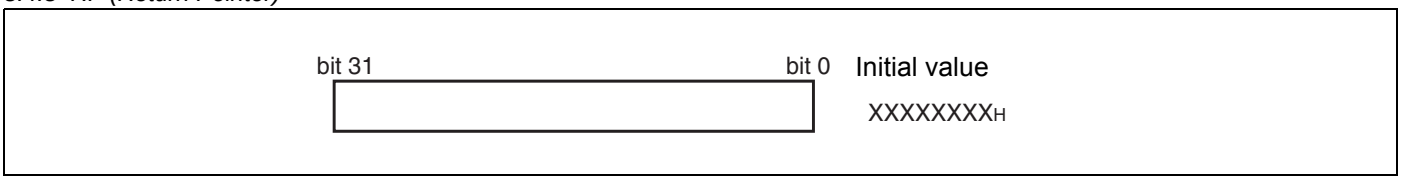

The program counter indicates the address of the instruction that is being executed.
The initial value at reset is undefined.

### 8.4.7 TBR (Table Base Register)



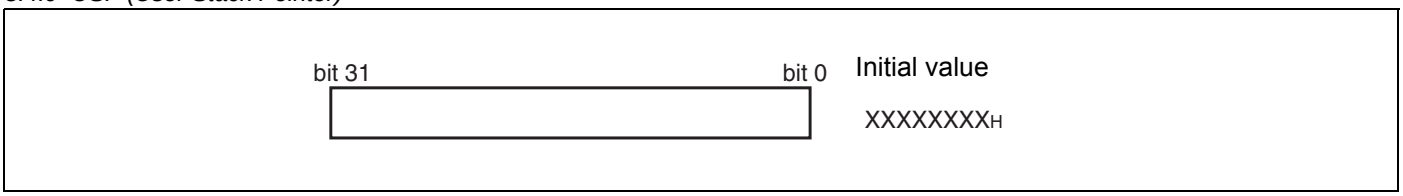

The table base register stores the starting address of the vector table used in EIT processing.
The initial value at reset is $000FFC00_H$.

### 8.4.8 RP (Return Pointer)




The return pointer stores the address for return from subroutines.
During execution of a CALL instruction, the PC value is transferred to this RP register.
During execution of a RET instruction, the contents of the RP register are transferred to PC.
The initial value at reset is undefined.

### 8.4.9 USP (User Stack Pointer)

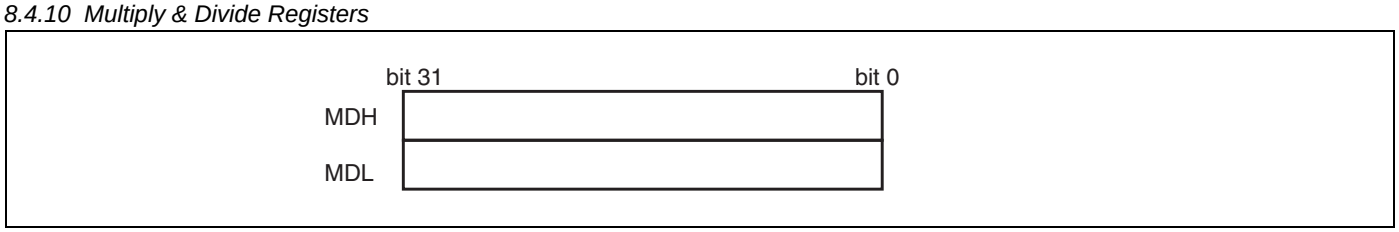



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.

  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

### 8.4.10 Multiply & Divide Registers




These registers are for multiplication and division, and are each 32 bits in length.
The initial value at reset is undefined.

# 9. Embedded Program/data Memory (Flash)

## 9.1 Flash Features

- CY91F467Cx: 1088 Kbytes (16 × 64 Kbytes ＋ 8 × 8 Kbytes = 8.5 Mbits)
- CY91F465CA:544 Kbytes (8 × 64 Kbytes ＋ 4 × 8 Kbytes = 4.25 Mbits)
- CY91F463CA:288 Kbytes (4 × 64 Kbytes + 4 × 8 Kbytes = 2.25 Mbits)
- Programmable wait states for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as CYM29LV400TC (except size and part of sector configuration)

## 9.2 Operation Modes:

(1) 64-bit CPU mode (available on CY91F467Cx only) :
- CPU reads and executes programs in word (32-bit) length units.
- Flash writing is not possible.
- Actual Flash Memory access is performed in d-word (64-bit) length units.

(1) 32-bit CPU mode:
- CPU reads and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

(2) 16-bit CPU mode:
- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in word (16-bit) length units.

Note: The operation mode of the MCU can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 “Flash Access Mode Switching”.

## 9.3 Flash Access in CPU Mode

### *9.3.1 Flash Configuration*

*Flash memory map CY91F467Cx*

| Address | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0014:FFFFh<br>0014:C000h | SA6 (8KB) | | | | SA7 (8KB) | | | | ROMS7 |
| 0014:BFFFh<br>0014:8000h | SA4 (8KB) | | | | SA5 (8KB) | | | | |
| 0014:7FFFh<br>0014:4000h | SA2 (8KB) | | | | SA3 (8KB) | | | | |
| 0014:3FFFh<br>0014:0000h | SA0 (8KB) | | | | SA1 (8KB) | | | | |
| 0013:FFFFh<br>0012:0000h | SA22 (64KB) | | | | SA23 (64KB) | | | | ROMS6 |
| 0011:FFFFh<br>0010:0000h | SA20 (64KB) | | | | SA21 (64KB) | | | | |
| 000F:FFFFh<br>000E:0000h | SA18 (64KB) | | | | SA19 (64KB) | | | | ROMS5 |
| 000D:FFFFh<br>000C:0000h | SA16 (64KB) | | | | SA17 (64KB) | | | | ROMS4 |
| 000B:FFFFh<br>000A:0000h | SA14 (64KB) | | | | SA15 (64KB) | | | | ROMS3 |
| 0009:FFFFh<br>0008:0000h | SA12 (64KB) | | | | SA13 (64KB) | | | | ROMS2 |
| 0007:FFFFh<br>0006:0000h | SA10 (64KB) | | | | SA11 (64KB) | | | | ROMS1 |
| 0005:FFFFh<br>0004:0000h | SA8 (64KB) | | | | SA9 (64KB) | | | | ROMS0 |
| | addr+0 | addr+1 | addr+2 | addr+3 | addr+4 | addr+5 | addr+6 | addr+7 | |
| 16bit read/write | dat[31:16] | | dat[15:0] | | dat[31:16] | | dat[15:0] | | |
| 32bit read/write | dat[31:0] | | | | dat[31:0] | | | | |
| 64bit read | dat[63:0] | | | | | | | | |

*Flash Memory Map CY91F465CA*

| Addr | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0014:FFFFh<br>0014:C000h | SA6 (8KB) | | | | SA7 (8KB) | | | | ROMS7 |
| 0014:BFFFh<br>0014:8000h | SA4 (8KB) | | | | SA5 (8KB) | | | | |
| 0014:7FFFh<br>0014:4000h | SA2 (8KB) | | | | SA3 (8KB) | | | | |
| 0014:3FFFh<br>0014:0000h | SA0 (8KB) | | | | SA1 (8KB) | | | | |
| 0013:FFFFh<br>0012:0000h | SA22 (64KB) | | | | SA23 (64KB) | | | | ROMS6 |
| 0011:FFFFh<br>0010:0000h | SA20 (64KB) | | | | SA21 (64KB) | | | | |
| 000F:FFFFh<br>000E:0000h | SA18 (64KB) | | | | SA19 (64KB) | | | | ROMS5 |
| 000D:FFFFh<br>000C:0000h | SA16 (64KB) | | | | SA17 (64KB) | | | | ROMS4 |
| 000B:FFFFh<br>000A:0000h | SA14 (64KB) | | | | SA15 (64KB) | | | | ROMS3 |
| 0009:FFFFh<br>0008:0000h | SA12 (64KB) | | | | SA13 (64KB) | | | | ROMS2 |
| 0007:FFFFh<br>0006:0000h | SA10 (64KB) | | | | SA11 (64KB) | | | | ROMS1 |
| 0005:FFFFh<br>0004:0000h | SA8 (64KB) | | | | SA9 (64KB) | | | | ROMS0 |
| | addr+0 | addr+1 | addr+2 | addr+3 | addr+4 | addr+5 | addr+6 | addr+7 | |
| 16bit read/write | dat[31:16] | | dat[15:0] | | dat[31:16] | | dat[15:0] | | |
| 32bit read | dat[31:0] | | | | dat[31:0] | | | | |
| Legend | Memory not available in this area | | | | Memory available in this area | | | | |

*Flash Memory Map CY91F463CA*

| Address | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0014:FFFFh<br>0014:C000h | SA6 (8KB) | | | | SA7 (8KB) | | | | ROMS7 |
| 0014:BFFFh<br>0014:8000h | SA4 (8KB) | | | | SA5 (8KB) | | | | |
| 0014:7FFFh<br>0014:4000h | SA2 (8KB) | | | | SA3 (8KB) | | | | |
| 0014:3FFFh<br>0014:0000h | SA0 (8KB) | | | | SA1 (8KB) | | | | |
| 0013:FFFFh<br>0012:0000h | SA22 (64KB) | | | | SA23 (64KB) | | | | ROMS6 |
| 0011:FFFFh<br>0010:0000h | SA20 (64KB) | | | | SA21 (64KB) | | | | |
| 000F:FFFFh<br>000E:0000h | SA18 (64KB) | | | | SA19 (64KB) | | | | ROMS5 |
| 000D:FFFFh<br>000C:0000h | SA16 (64KB) | | | | SA17 (64KB) | | | | ROMS4 |
| 000B:FFFFh<br>000A:0000h | SA14 (64KB) | | | | SA15 (64KB) | | | | ROMS3 |
| 0009:FFFFh<br>0008:0000h | SA12 (64KB) | | | | SA13 (64KB) | | | | ROMS2 |
| 0007:FFFFh<br>0006:0000h | SA10 (64KB) | | | | SA11 (64KB) | | | | ROMS1 |
| 0005:FFFFh<br>0004:0000h | SA8 (64KB) | | | | SA9 (64KB) | | | | ROMS0 |
| | addr+0 | addr+1 | addr+2 | addr+3 | addr+4 | addr+5 | addr+6 | addr+7 | |
| 16bit read/write | dat[31:16] | | dat[15:0] | | dat[31:16] | | dat[15:0] | | |
| 32bit read | dat[31:0] | | | | dat[31:0] | | | | |
| Legend | Memory not available in this area | | | | Memory available in this area | | | | |

### 9.3.2 Flash Access Timing Settings in CPU Mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

*Flash Read Timing Settings (Synchronous Read)*

| Core Clock (CLKB) | ATD | ALEH | EQ | WEXH | WTC | Remark |
|---|---|---|---|---|---|---|
| to 24 MHz | 0 | 0 | 0 | - | 1 | |
| to 48 MHz | 0 | 0 | 1 | - | 2 | |
| to 100 MHz | 1 | 1 | 3 | - | 4 | |

*Flash Write Timing Settings (Synchronous Write)*

| Core Clock (CLKB) | ATD | ALEH | EQ | WEXH | WTC | Remark |
|---|---|---|---|---|---|---|
| to 16 MHz | 0 | - | - | 0 | 3 | |
| to 32 MHz | 0 | - | - | 0 | 4 | |
| to 48 MHz | 0 | - | - | 0 | 5 | |
| to 64 MHz | 1 | - | - | 0 | 6 | |
| to 96 MHz | 1 | - | - | 0 | 7 | |
| to 100 MHz | 1 | - | - | 1 | 8 | |

### 9.3.3 Address Mapping from CPU to Parallel Programming Mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

*Address Mapping CY91F467Cx*

| CPU Address (addr) | Condition | Flash Sectors | FA (flash address) Calculation |
|---|---|---|---|
| 14:0000h to 14:FFFFh | addr[2]==0 | SA0, SA2, SA4, SA6 (8 Kbyte) | FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h |
| 14:0000h to 14:FFFFh | addr[2]==1 | SA1, SA3, SA5, SA7 (8 Kbyte) | FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 05:0000h |
| 04:0000h to 13:FFFFh | addr[2]==0 | SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte) | FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h |
| 04:0000h to 13:FFFFh | addr[2]==1 | SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte) | FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4 + 0C:0000h |

Note: FA result is without 20:0000h offset for parallel Flash programming.
Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

*Address Mapping CY91F463CA, CY91F465CA*

| CPU Address (addr) | Condition | Flash Sectors | FA (flash address) Calculation |
|---|---|---|---|
| 14:8000h to 14:FFFFh | addr[2]==0 | SA4, SA6 (8 Kbyte) | FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h |
| 14:8000h to 14:FFFFh | addr[2]==1 | SA5, SA7 (8 Kbyte) | FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 0D:0000h |
| 08:0000h to 13F:FFFFh | addr[2]==0 | SA12, SA14 (CY91F465CA) SA16, SA18 (64 Kbyte) | FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 |
| 08:0000h to 13F:FFFFh | addr[2]==1 | SA13, SA15 (CY91F465CA) SA17, SA19 (64 Kbyte) | FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4 |

Note: FA result is without 10:0000h offset for parallel Flash programming.
Set offset by keeping FA[20] = 1 as described in section “Parallel Flash programming mode”.

## 9.4 Parallel Flash Programming Mode

### *9.4.1 Flash Configuration in Parallel Flash Programming Mode*

Parallel Flash Programming Mode (MD[2:0] = 111):

CY91F467Cx

| FA[21:0] | |
|---|---|
| 003F:FFFFh<br>003F:0000h | SA23 (64KB) |
| 003E:FFFFh<br>003E:0000h | SA22 (64KB) |
| 003D:FFFFh<br>003D:0000h | SA21 (64KB) |
| 003C:FFFFh<br>003C:0000h | SA20 (64KB) |
| 003B:FFFFh<br>003B:0000h | SA19 (64KB) |
| 003A:FFFFh<br>003A:0000h | SA18 (64KB) |
| 0039:FFFFh<br>0039:0000h | SA17 (64KB) |
| 0038:FFFFh<br>0038:0000h | SA16 (64KB) |
| 0037:FFFFh<br>0037:0000h | SA15 (64KB) |
| 0036:FFFFh<br>0036:0000h | SA14 (64KB) |
| 0035:FFFFh<br>0035:0000h | SA13 (64KB) |
| 0034:FFFFh<br>0034:0000h | SA12 (64KB) |
| 0033:FFFFh<br>0033:0000h | SA11 (64KB) |
| 0032:FFFFh<br>0032:0000h | SA10 (64KB) |
| 0031:FFFFh<br>0031:0000h | SA9 (64KB) |
| 0030:FFFFh<br>0030:0000h | SA8 (64KB) |
| 002F:FFFFh<br>002F:E000h | SA7 (8KB) |
| 002F:DFFFh<br>002F:C000h | SA6 (8KB) |
| 002F:BFFFh<br>002F:A000h | SA5 (8KB) |
| 002F:9FFFh<br>002F:8000h | SA4 (8KB) |
| 002F:7FFFh<br>002F:6000h | SA3 (8KB) |
| 002F:5FFFh<br>002F:4000h | SA2 (8KB) |
| 002F:3FFFh<br>002F:2000h | SA1 (8KB) |
| 002F:1FFFh<br>002F:0000h | SA0 (8KB) |

| 16bit write mode | FA[1:0]=00 | FA[1:0]=10 |
|---|---|---|
| | DQ[15:0] | DQ[15:0] |

Remark: Always keep FA[0] = 0 and FA[21] = 1

CY91F465CA

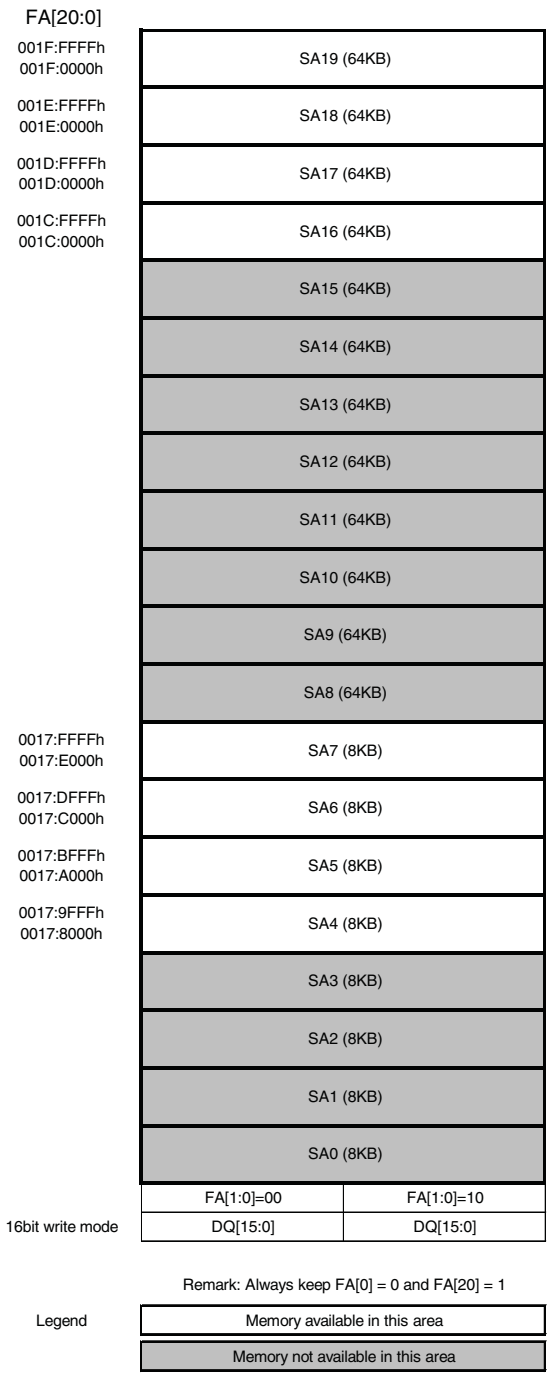
| FA[20:0] | |
|---|---|
| 001F:FFFFh<br>001F:0000h | SA19 (64KB) |
| 001E:FFFFh<br>001E:0000h | SA18 (64KB) |
| 001D:FFFFh<br>001D:0000h | SA17 (64KB) |
| 001C:FFFFh<br>001C:0000h | SA16 (64KB) |
| 001B:FFFFh<br>001B:0000h | SA15 (64KB) |
| 001A:FFFFh<br>001A:0000h | SA14 (64KB) |
| 0019:FFFFh<br>0019:0000h | SA13 (64KB) |
| 0018:FFFFh<br>0018:0000h | SA12 (64KB) |
| | SA11 (64KB) |
| | SA10 (64KB) |
| | SA9 (64KB) |
| | SA8 (64KB) |
| 0017:FFFFh<br>0017:E000h | SA7 (8KB) |
| 0017:DFFFh<br>0017:C000h | SA6 (8KB) |
| 0017:BFFFh<br>0017:A000h | SA5 (8KB) |
| 0017:9FFFh<br>0017:8000h | SA4 (8KB) |
| | SA3 (8KB) |
| | SA2 (8KB) |
| | SA1 (8KB) |
| | SA0 (8KB) |

| 16bit write mode | FA[1:0]=00 | FA[1:0]=10 |
|---|---|---|
| | DQ[15:0] | DQ[15:0] |

Remark: Always keep FA[0] = 0 and FA[20] = 1

| Legend | |
|---|---|
| | Memory available in this area |
| | Memory not available in this area |

CY91F463CA


FA[20:0]
001F:FFFFh
001F:0000h
SA19 (64KB)
001E:FFFFh
001E:0000h
SA18 (64KB)
001D:FFFFh
001D:0000h
SA17 (64KB)
001C:FFFFh
001C:0000h
SA16 (64KB)
SA15 (64KB)
SA14 (64KB)
SA13 (64KB)
SA12 (64KB)
SA11 (64KB)
SA10 (64KB)
SA9 (64KB)
SA8 (64KB)
0017:FFFFh
0017:E000h
SA7 (8KB)
0017:DFFFh
0017:C000h
SA6 (8KB)
0017:BFFFh
0017:A000h
SA5 (8KB)
0017:9FFFh
0017:8000h
SA4 (8KB)
SA3 (8KB)
SA2 (8KB)
SA1 (8KB)
SA0 (8KB)
FA[1:0]=00
FA[1:0]=10
16bit write mode
DQ[15:0]
DQ[15:0]
Remark: Always keep FA[0] = 0 and FA[20] = 1
Legend
Memory available in this area
Memory not available in this area

*9.4.2 Pin Connections in Parallel Programming Mode*

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between CYM29LV400TC and Flash Memory Control Signals

| CYM29LV400TC External Pins | FR-CPU Mode | CY91F465CA, CY91F467Cx External Pins | | | Comment |
|---|---|---|---|---|---|
| | | Flash Memory Mode | Normal Function | Pin Number | |
| — | INITX | — | INITX | 84 | |
| RESET | — | FRSTX | NMIX | 85 | |
| — | — | MD_2 | MD_2 | 76 | Set to ‘1’ |
| — | — | MD_1 | MD_1 | 75 | Set to ‘1’ |
| — | — | MD_0 | MD_0 | 74 | Set to ‘1’ |
| RY/BY | FMCS:RDY bit | RY/BYX | GP28_0 | 100 | |
| BYTE | Internally fixed to ‘H’ | BYTEX | GP28_2 | 102 | |
| WE | Internal control signal + control via interface circuit | WEX | GP28_5 | 111 | |
| OE | | OEX | GP28_4 | 110 | |
| CE | | CEX | GP20_0 | 38 | |
| — | | ATDIN | GP17_7 | 27 | Set to ‘0’ |
| — | | EQIN | GP17_6 | 26 | Set to ‘0’ |
| — | | TESTX | GP28_3 | 103 | Set to ‘1’ |
| — | | RDYI | GP28_1 | 101 | Set to ‘0’ |
| A-1 | Internal address bus | FA0 | GP17_5 | 25 | Set to ‘0’ |
| A0 to A3 | | FA1 to FA4 | GP29_0 to GP29_3 | 92 to 95 | |
| A4 to A7 | | FA5 to FA8 | GP29_4 to GP29_7 | 96 to 99 | |
| A8 to A11 | | FA9 to FA12 | GP16_0 to GP16_3 | 28 to 31 | |
| A12 to A15 | | FA13 to FA16 | GP16_4 to GP16_7 | 32 to 35 | |
| A16 to A18 | | FA17 to FA19 | GP15_0 to GP15_2 | 20 to 22 | |
| A19 | | FA20 | GP15_3 | 23 | Set to ‘1’ on CY91F463CA, CY91F465CA |
| — | | FA21 | GP17_4 | 24 | Set to ‘1’ |
| DQ0 to DQ7 | Internal data bus | DQ0 to DQ7 | GP14_0 to GP14_7 | 10 to 17 | |
| DQ8 to DQ15 | | DQ8 to DQ15 | GP02_0 to GP02_7 | 2 to 9 | |

## 9.5 Power on Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

## 9.6 Flash Security

### *9.6.1 Vector Addresses*

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

### *9.6.2 Security Vector FSV1*

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

*FSV1 (bit31 to bit16)*

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1[31:16]

| FSV1[31:19] | FSV1[18] Write Protection Level | FSV1[17] Write Protection | FSV1[16] Read Protection | Flash Security Mode |
|---|---|---|---|---|
| set all to ‘0’ | set to ‘0’ | set to ‘0’ | set to ‘1’ | Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) |
| set all to ‘0’ | set to ‘0’ | set to ‘1’ | set to ‘0’ | Write Protection (all device modes, without exception) |
| set all to ‘0’ | set to ‘0’ | set to ‘1’ | set to ‘1’ | Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes) |
| set all to ‘0’ | set to ‘1’ | set to ‘0’ | set to ‘1’ | Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) |
| set all to ‘0’ | set to ‘1’ | set to ‘1’ | set to ‘0’ | Write Protection (all device modes, except INTVEC mode MD[2:0]=”000”) |
| set all to ‘0’ | set to ‘1’ | set to ‘1’ | set to ‘1’ | Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes except INTVEC mode MD[2:0]=”000”) |

*FSV1 (bit15 to bit0)*

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1[15:0]

| FSV1 bit | Sector | Enable Write Protection | Disable Write Protection | Comment |
|---|---|---|---|---|
| FSV1[0] | SA0 | set to “0” | set to “1” | Sectors available on CY91F467Cx only |
| FSV1[1] | SA1 | set to “0” | set to “1” | |
| FSV1[2] | SA2 | set to “0” | set to “1” | |
| FSV1[3] | SA3 | set to “0” | set to “1” | |
| FSV1[4] | SA4 | set to “0” | — | Write protection is mandatory! |
| FSV1[5] | SA5 | set to “0” | set to “1” | |
| FSV1[6] | SA6 | set to “0” | set to “1” | |
| FSV1[7] | SA7 | set to “0” | set to “1” | |
| FSV1[15:8] | — | — | — | not available |

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section “9.3. Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

### *9.6.3 Security Vector FSV2*

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

| FSV2 bit | Sector | Enable Write Protection | Disable Write Protection | Comment |
|---|---|---|---|---|
| FSV2[0] | SA8 | set to “0” | set to “1” | Sectors available on CY91F467Cx only |
| FSV2[1] | SA9 | set to “0” | set to “1” | |
| FSV2[2] | SA10 | set to “0” | set to “1” | |
| FSV2[3] | SA11 | set to “0” | set to “1” | |
| FSV2[4] | SA12 | set to “0” | set to “1” | Sectors available on CY91F467Cx and CY91F465CA |
| FSV2[5] | SA13 | set to “0” | set to “1” | |
| FSV2[6] | SA14 | set to “0” | set to “1” | |
| FSV2[7] | SA15 | set to “0” | set to “1” | |
| FSV2[8] | SA16 | set to “0” | set to “1” | Sectors available on CY91F467Cx, CY91F465CA, CY91F463CA |
| FSV2[9] | SA17 | set to “0” | set to “1” | |
| FSV2[10] | SA18 | set to “0” | set to “1” | |
| FSV2[11] | SA19 | set to “0” | set to “1” | |
| FSV2[12] | SA20 | set to “0” | set to “1” | Sectors available on CY91F467Cx only |
| FSV2[13] | SA21 | set to “0” | set to “1” | |
| FSV2[14] | SA22 | set to “0” | set to “1” | |
| FSV2[15] | SA23 | set to “0” | set to “1” | |
| FSV2[31:16] | — | set to “0” | set to “1” | Sectors not available |

Note : See section “9.3. Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

## 10. Memory Space

The FR family has 4 Gbytes of logical address space ($2^{32}$ addresses) available to the CPU by linear access.

### Direct Addressing Area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access : $000_H$ to $0FF_H$

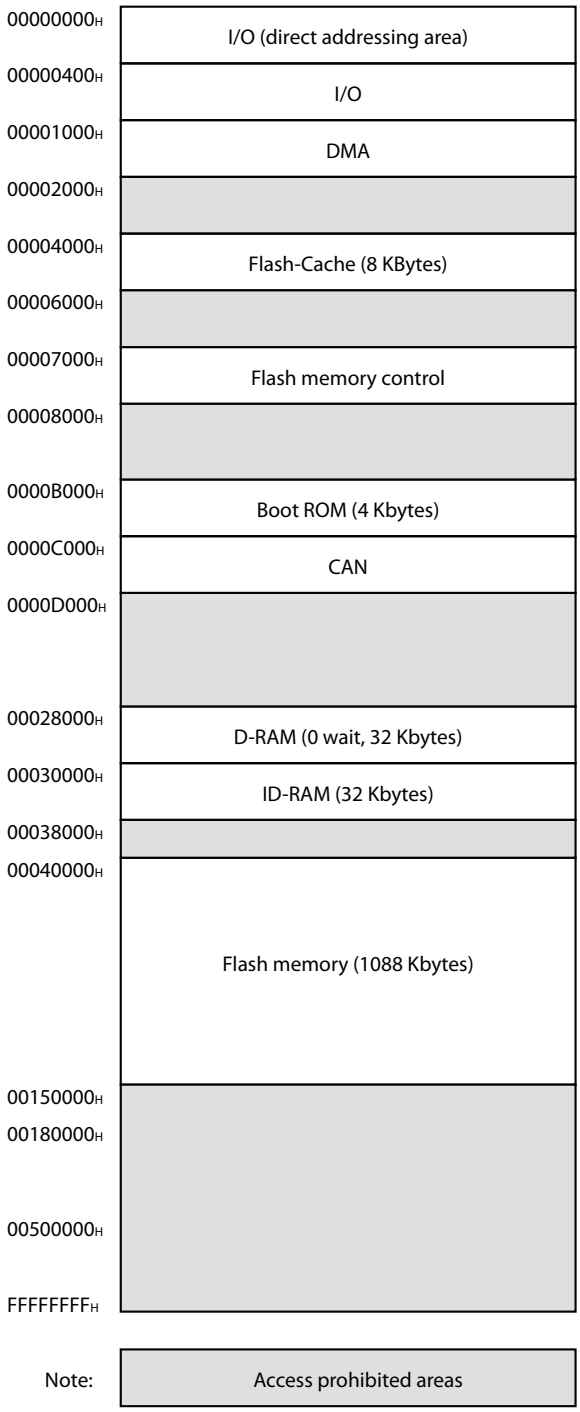
Half word access : $000_H$ to $1FF_H$

Word data access : $000_H$ to $3FF_H$

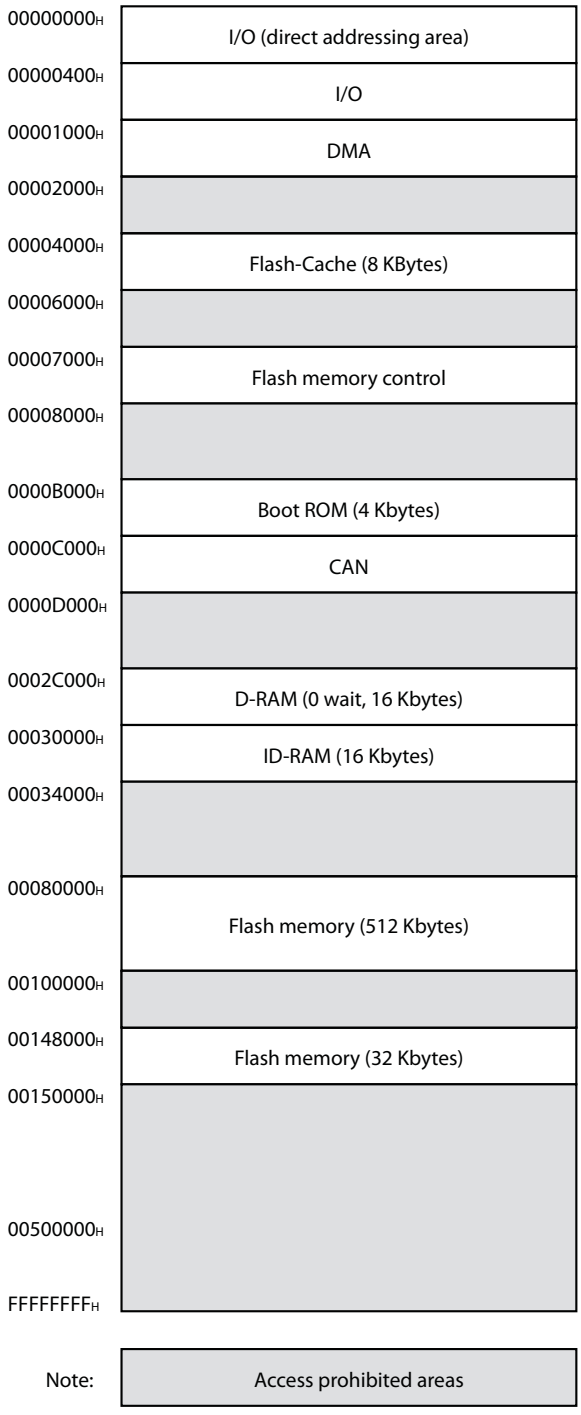
# 11. Memory Maps

## 11.1 CY91F467Cx, CY91F465CA

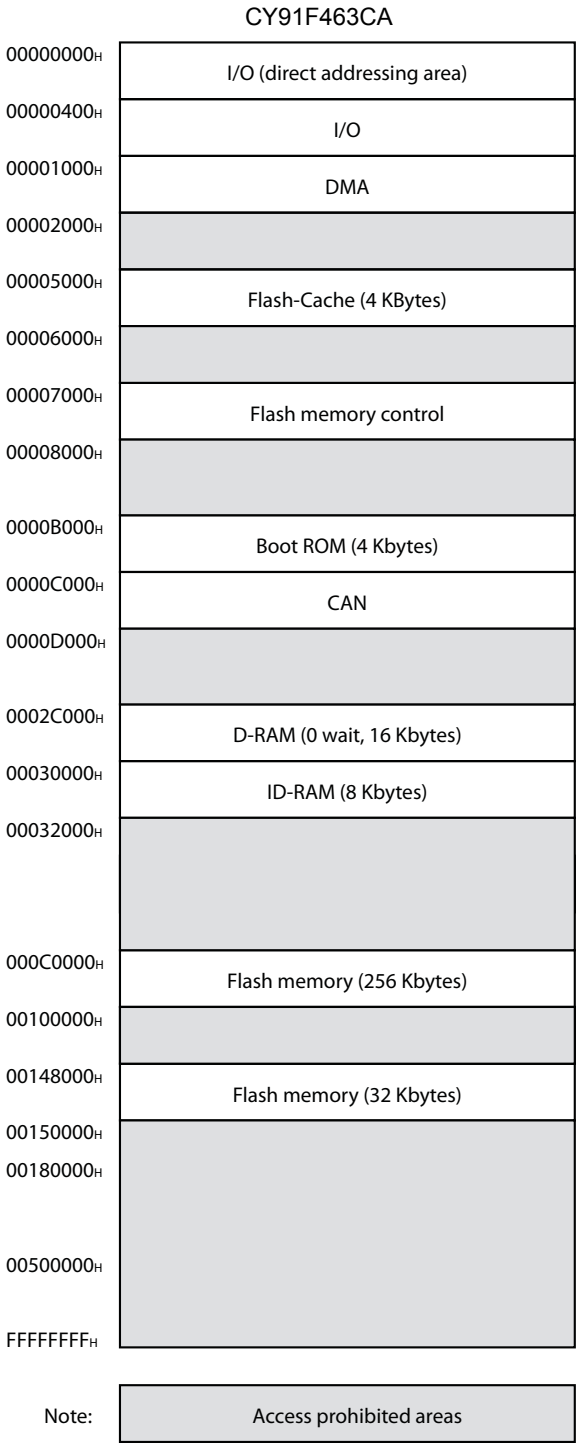
CY91F467Cx




CY91F465CA



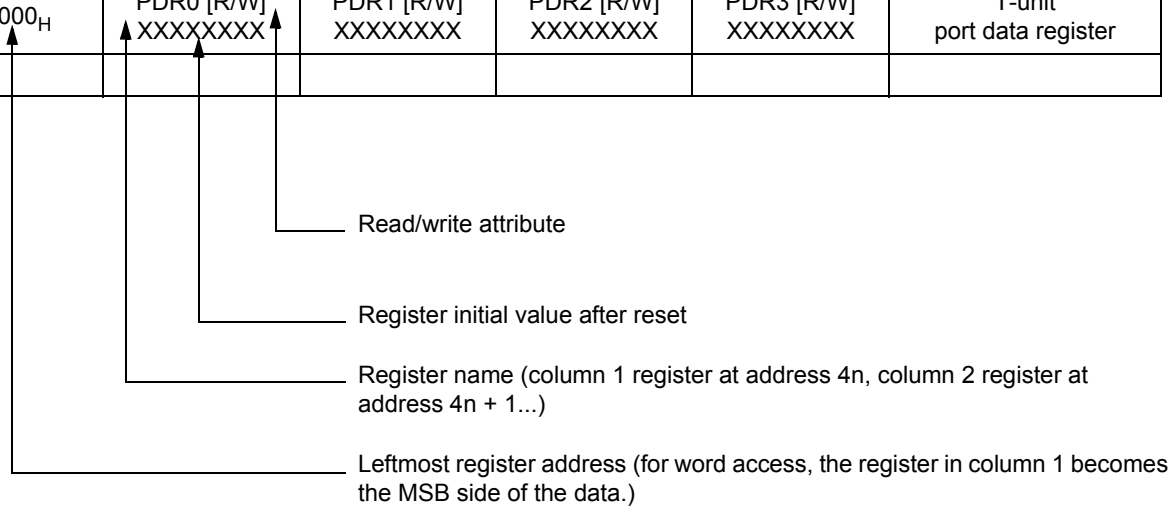
## 11.2 CY91F463CA



# 12. I/O Map

## 12.1 CY91F463CA, CY91F465CA, CY91F467Cx

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | + 0 | + 1 | + 2 | + 3 | |
| $000000_H$ | PDR0 [R/W]<br>XXXXXXXX | PDR1 [R/W]<br>XXXXXXXX | PDR2 [R/W]<br>XXXXXXXX | PDR3 [R/W]<br>XXXXXXXX | T-unit<br>port data register |
| | | | | | |




Note : Initial values of register bits are represented as follows:

" 1 " : Initial value " 1 "
" 0 " : Initial value " 0 "
" X " : Initial value " undefined "
" - " : No physical register at this location
Access is barred with an undefined data access attribute.

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000000_H$ | Reserved | Reserved | PDR02 [R/W] XXXXXXXX | Reserved | R-bus Port Data Register |
| $000004_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000008_H$ | Reserved | Reserved | Reserved | Reserved | |
| $00000C_H$ | Reserved | Reserved | PDR14 [R/W] XXXXXXXX | PDR15 [R/W] - - - - XXXX | |
| $000010_H$ | PDR16 [R/W] XXXXXXXX | PDR17 [R/W] XXXX - - - - | PDR18 [R/W] - XXX - XXX | PDR19 [R/W] - XXX - XXX | |
| $000014_H$ | PDR20 [R/W] - - - - - XXX | Reserved | PDR22 [R/W] - - XX - X - X | PDR23 [R/W] - XXXXXXX | |
| $000018_H$ | PDR24 [R/W] XXXXXXXX | PDR25 [R/W] XXXXXXXX | PDR26 [R/W] XXXXXXXX | PDR27 [R/W] XXXXXXXX | |
| $00001C_H$ | PDR28 [R/W] - -XXXXX | PDR29 [R/W] XXXXXXXX | Reserved | Reserved | |
| $000020_H$ to $00002C_H$ | Reserved | | | | Reserved |
| $000030_H$ | EIRR0 [R/W] XXXXXXXX | ENIR0 [R/W] 00000000 | ELVR0 [R/W] 00000000 00000000 | | External Interrupt (INT 0 to INT 7) |
| $000034_H$ | EIRR1 [R/W] XXXXXXXX | ENIR1 [R/W] 00000000 | ELVR1 [R/W] 00000000 00000000 | | External Interrupt (INT 8 to INT 14) |
| $000038_H$ | DICR [R/W] - - - - - - - 0 | HRCL [R/W] 0 - - 11111 | Reserved | | Delayed Interrupt |
| $00003C_H$ - $00004C_H$ | Reserved | | | | Reserved |
| $000050_H$ | SCR02 [R/W,W] 00000000 | SMR02 [R/W,W] 00000000 | SSR02 [R/W,R] 00001000 | RDR02/TDR02 [R/W] 00000000 | LIN-USART 2 |
| $000054_H$ | ESCR02 [R/W] 00000X00 | ECCR02 [R/W,R,W] -00000XX | Reserved | | |
| $000058_H$ to $00005C_H$ | Reserved | | | | Reserved |
| $000060_H$ | SCR04 [R/W,W] 00000000 | SMR04 [R/W,W] 00000000 | SSR04 [R/W,R] 00001000 | RDR04/TDR04 [R/W] 00000000 | LIN-USART 4 with FIFO |
| $000064_H$ | ESCR04 [R/W] 00000X00 | ECCR04 [R/W,R,W] -00000XX | FSR04 [R] - - - 00000 | FCR04 [R/W] 0001 - 000 | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000068_H$ | SCR05 [R/W,W]<br>00000000 | SMR05 [R/W,W]<br>00000000 | SSR05 [R/W,R]<br>00001000 | RDR05/TDR05<br>[R/W]<br>00000000 | LIN-USART 5<br>with FIFO |
| $00006C_H$ | ESCR05 [R/W]<br>00000X00 | ECCR05<br>[R/W,R,W]<br>-00000XX | FSR05 [R]<br>- - - 00000 | FCR05 [R/W]<br>0001 - 000 | |
| $000070_H$ | SCR06 [R/W,W]<br>00000000 | SMR06 [R/W,W]<br>00000000 | SSR06 [R/W,R]<br>00001000 | RDR06/TDR06<br>[R/W]<br>00000000 | LIN-USART 6<br>with FIFO |
| $000074_H$ | ESCR06 [R/W]<br>00000X00 | ECCR06<br>[R/W,R,W]<br>-00000XX | FSR06 [R]<br>- - - 00000 | FCR06 [R/W]<br>0001 - 000 | |
| $000078_H$ | SCR07 [R/W,W]<br>00000000 | SMR07 [R/W,W]<br>00000000 | SSR07 [R/W,R]<br>00001000 | RDR07/TDR07<br>[R/W]<br>00000000 | LIN-USART 7<br>with FIFO |
| $00007C_H$ | ESCR07 [R/W]<br>00000X00 | ECCR07<br>[R/W,R,W]<br>-00000XX | FSR07 [R]<br>- - - 00000 | FCR07 [R/W]<br>0001 - 000 | |
| $000080_H$ | Reserved | | | | Reserved |
| $000084_H$ | BGR102 [R/W]<br>00000000 | BGR002 [R/W]<br>00000000 | Reserved | Reserved | Baud rate<br>Generator<br>LIN-USART<br>0 to 7 |
| $000088_H$ | BGR104 [R/W]<br>00000000 | BGR004 [R/W]<br>00000000 | BGR105 [R/W]<br>00000000 | BGR005 [R/W]<br>00000000 | |
| $00008C_H$ | BGR106 [R/W]<br>00000000 | BGR006 [R/W]<br>00000000 | BGR107 [R/W]<br>00000000 | BGR007 [R/W]<br>00000000 | |
| $000090_H$ | PWC20 [R/W]<br>- - - - - - XX XXXXXXXX | | PWC10 [R/W]<br>- - - - - - XX XXXXXXXX | | Stepper Motor 0 |
| $000094_H$ | Reserved | Reserved | PWS20 [R/W]<br>-0000000 | PWS10 [R/W]<br>- -000000 | |
| $000098_H$ | PWC21 [R/W]<br>- - - - - - XX XXXXXXXX | | PWC11 [R/W]<br>- - - - - - XX XXXXXXXX | | Stepper Motor 1 |
| $00009C_H$ | Reserved | Reserved | PWS21 [R/W]<br>-0000000 | PWS11 [R/W]<br>- -000000 | |
| $0000A0_H$ | PWC22 [R/W]<br>- - - - - - XX XXXXXXXX | | PWC12 [R/W]<br>- - - - - - XX XXXXXXXX | | Stepper Motor 2 |
| $0000A4_H$ | Reserved | Reserved | PWS22 [R/W]<br>-0000000 | PWS12 [R/W]<br>- -000000 | |
| $0000A8_H$ | PWC23 [R/W]<br>- - - - - - XX XXXXXXXX | | PWC13 [R/W]<br>- - - - - - XX XXXXXXXX | | Stepper Motor 3 |
| $0000AC_H$ | Reserved | Reserved | PWS23 [R/W]<br>-0000000 | PWS13 [R/W]<br>- -000000 | |
| $0000B0_H$ | PWC24 [R/W]<br>- - - - - - XX XXXXXXXX | | PWC14 [R/W]<br>- - - - - - XX XXXXXXXX | | Stepper Motor 4 |
| $0000B4_H$ | Reserved | Reserved | PWS24 [R/W]<br>-0000000 | PWS14 [R/W]<br>- -000000 | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $0000B8_H$ | PWC25 [R/W]<br>- - - - - - XX XXXXXXXX | | PWC15 [R/W]<br>- - - - - - XX XXXXXXXX | | Stepper Motor 5 |
| $0000BC_H$ | Reserved | Reserved | PWS25 [R/W]<br>-0000000 | PWS15 [R/W]<br>- -000000 | |
| $0000C0_H$ | Reserved | PWC0 [R/W]<br>-00000-- | Reserved | PWC1 [R/W]<br>-00000-- | Stepper Motor Control<br>0 to 5 |
| $0000C4_H$ | Reserved | PWC2 [R/W]<br>-00000-- | Reserved | PWC3 [R/W]<br>-00000-- | |
| $0000C8_H$ | Reserved | PWC4 [R/W]<br>-00000-- | Reserved | PWC5 [R/W]<br>-00000-- | |
| $0000CC_H$ | Reserved | | | | Reserved |
| 0000D0H | IBCR0 [R/W]<br>00000000 | IBSR0 [R]<br>00000000 | ITBAH0 [R/W]<br>- - - - - - 00 | ITBAL0 [R/W]<br>00000000 | $I^2C$ 0 |
| 0000D4H | ITMKH0 [R/W]<br>00 - - - - 11 | ITMKL0 [R/W]<br>11111111 | ISMK0 [R/W]<br>01111111 | ISBA0 [R/W]<br>- 0000000 | |
| 0000D8H | Reserved | IDAR0 [R/W]<br>00000000 | ICCR0 [R/W]<br>- 0011111 | Reserved | |
| $0000DC_H$ to $000100_H$ | Reserved | | | | Reserved |
| $000104_H$ | GCN11 [R/W]<br>00110010 00010000 | | Reserved | GCN21 [R/W]<br>- - - - 0000 | PPG Control<br>4 to 7 |
| $000108_H$ | GCN12 [R/W]<br>00110010 00010000 | | Reserved | GCN22 [R/W]<br>- - - - 0000 | PPG Control<br>8 to 11 |
| $000110_H$ to $00012C_H$ | Reserved | | | | Reserved |
| $000130_H$ | PTMR04 [R]<br>11111111 11111111 | | PCSR04 [W]<br>XXXXXXXX XXXXXXXX | | PPG 4 |
| $000134_H$ | PDUT04 [W]<br>XXXXXXXX XXXXXXXX | | PCNH04 [R/W]<br>0000000 - | PCNL04 [R/W]<br>000000 - 0 | |
| $000138_H$ | PTMR05 [R]<br>11111111 11111111 | | PCSR05 [W]<br>XXXXXXXX XXXXXXXX | | PPG 5 |
| $00013C_H$ | PDUT05 [W]<br>XXXXXXXX XXXXXXXX | | PCNH05 [R/W]<br>0000000 - | PCNL05 [R/W]<br>000000 - 0 | |
| $000140_H$ | PTMR06 [R]<br>11111111 11111111 | | PCSR06 [W]<br>XXXXXXXX XXXXXXXX | | PPG 6 |
| $000144_H$ | PDUT06 [W]<br>XXXXXXXX XXXXXXXX | | PCNH06 [R/W]<br>0000000 - | PCNL06 [R/W]<br>000000 - 0 | |
| $000148_H$ | PTMR07 [R]<br>11111111 11111111 | | PCSR07 [W]<br>XXXXXXXX XXXXXXXX | | PPG 7 |
| $00014C_H$ | PDUT07 [W]<br>XXXXXXXX XXXXXXXX | | PCNH07 [R/W]<br>0000000 - | PCNL07 [R/W]<br>000000 - 0 | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000150_H$ | PTMR08 [R]<br>11111111 11111111 | | PCSR08 [W]<br>XXXXXXXX XXXXXXXX | | PPG 8 |
| $000154_H$ | PDUT08 [W]<br>XXXXXXXX XXXXXXXX | | PCNH08 [R/W]<br>0000000 - | PCNL08 [R/W]<br>000000 - 0 | |
| $000158_H$ | PTMR09 [R]<br>11111111 11111111 | | PCSR09 [W]<br>XXXXXXXX XXXXXXXX | | PPG 9 |
| $00015C_H$ | PDUT09 [W]<br>XXXXXXXX XXXXXXXX | | PCNH09 [R/W]<br>0000000 - | PCNL09 [R/W]<br>000000 - 0 | |
| $000160_H$ | PTMR10 [R]<br>11111111 11111111 | | PCSR10 [W]<br>XXXXXXXX XXXXXXXX | | PPG 10 |
| $000164_H$ | PDUT10 [W]<br>XXXXXXXX XXXXXXXX | | PCNH10 [R/W]<br>0000000 - | PCNL10 [R/W]<br>000000 - 0 | |
| $000168_H$ | PTMR11 [R]<br>11111111 11111111 | | PCSR11 [W]<br>XXXXXXXX XXXXXXXX | | PPG 11 |
| $00016C_H$ | PDUT11 [W]<br>XXXXXXXX XXXXXXXX | | PCNH11 [R/W]<br>0000000 - | PCNL11 [R/W]<br>000000 - 0 | |
| $000170_H$ | P0TMCSRH<br>[R/W]<br>- 0-000-0 | P0TMCSRL<br>[R/W]<br>- - -00000 | P1TMCSRH<br>[R/W]<br>- 0000000 | P1TMCSRL<br>[R/W]<br>01000000 | Pulse Frequency Modulator |
| $000174_H$ | P0TMRLR [W]<br>XXXXXXXX XXXXXXXX | | P0TMR [R]<br>XXXXXXXX XXXXXXXX | | |
| $000178_H$ | P1TMRLR [W]<br>XXXXXXXX XXXXXXXX | | P1TMR [R]<br>XXXXXXXX XXXXXXXX | | |
| $00017C_H$ | Reserved | | | | Reserved |
| $000180_H$ | Reserved | ICS01 [R/W]<br>00000000 | Reserved | ICS23 [R/W]<br>00000000 | Input Capture 0 to 3 |
| $000184_H$ | IPCP0 [R]<br>XXXXXXXX XXXXXXXX | | IPCP1 [R]<br>XXXXXXXX XXXXXXXX | | |
| $000188_H$ | IPCP2 [R]<br>XXXXXXXX XXXXXXXX | | IPCP3 [R]<br>XXXXXXXX XXXXXXXX | | |
| $00018C_H$ | OCS01 [R/W]<br>- - - 0 - - 00 0000 - - 00 | | OCS23 [R/W]<br>- - - 0 - - 00 0000 - - 00 | | Output Compare 0 to 3 |
| $000190_H$ | OCCP0 [R/W]<br>XXXXXXXX XXXXXXXX | | OCCP1 [R/W]<br>XXXXXXXX XXXXXXXX | | |
| $000194_H$ | OCCP2 [R/W]<br>XXXXXXXX XXXXXXXX | | OCCP3 [R/W]<br>XXXXXXXX XXXXXXXX | | |
| $000198_H$ | SGCRH [R/W]<br>0000 - - 00 | SGCRL [R/W]<br>- - 0 - - 000 | SGFR [R/W, R]<br>XXXXXXXX XXXXXXXX | | Sound Generator |
| $00019C_H$ | SGAR [R/W]<br>00000000 | Reserved | SGTR [R/W]<br>XXXXXXXX | SGDR [R/W]<br>XXXXXXXX | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $0001A0_H$ | ADERH [R/W]<br>00000000 00000000 | | ADERL [R/W]<br>00000000 00000000 | | A/D Converter |
| 0001A4 | ADCS1 [R/W]<br>00000000 | ADCS0 [R/W]<br>00000000 | ADCR1 [R]<br>000000XX | ADCR0 [R]<br>XXXXXXXX | |
| $0001A8_H$ | ADCT1 [R/W]<br>00010000 | ADCT0 [R/W]<br>00101100 | ADSCH [R/W]<br>- - - 00000 | ADECH [R/W]<br>- - - 00000 | |
| $0001AC_H$ | Reserved | ACSR0 [R/W]<br>- 11XXX00 | Reserved | Reserved | Alarm Comparator 0 |
| $0001B0_H$ | TMRLR0 [W]<br>XXXXXXXX XXXXXXX | | TMR0 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 0 |
| $0001B4_H$ | Reserved | | TMCSRH0<br>[R/W]<br>- - - 00000 | TMCSRL0<br>[R/W]<br>0 - 000000 | |
| $0001B8_H$ | TMRLR1 [W]<br>XXXXXXXX XXXXXXXX | | TMR1 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 1 |
| $0001BC_H$ | Reserved | | TMCSRH1<br>[R/W]<br>- - - 00000 | TMCSRL1<br>[R/W]<br>0 - 000000 | |
| $0001C0_H$ | TMRLR2 [W]<br>XXXXXXXX XXXXXXXX | | TMR2 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 2<br>(PPG 4, PPG 5) |
| $0001C4_H$ | Reserved | | TMCSRH2<br>[R/W]<br>- - - 00000 | TMCSRL2<br>[R/W]<br>0 - 000000 | |
| $0001C8_H$ | TMRLR3 [W]<br>XXXXXXXX XXXXXXXX | | TMR3 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 3<br>(PPG 6, PPG 7) |
| $0001CC_H$ | Reserved | | TMCSRH3<br>[R/W]<br>- - - 00000 | TMCSRL3<br>[R/W]<br>0 - 000000 | |
| $0001D0_H$ | TMRLR4 [W]<br>XXXXXXXX XXXXXXXX | | TMR4 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 4<br>(PPG 8, PPG 9) |
| $0001D4_H$ | Reserved | | TMCSRH4<br>[R/W]<br>- - - 00000 | TMCSRL4<br>[R/W]<br>0 - 000000 | |
| $0001D8_H$ | TMRLR5 [W]<br>XXXXXXXX XXXXXXXX | | TMR5 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 5<br>(PPG 10, PPG 11) |
| $0001DC_H$ | Reserved | | TMCSRH5<br>[R/W]<br>- - - 00000 | TMCSRL5<br>[R/W]<br>0 - 000000 | |
| $0001E0_H$ | TMRLR6 [W]<br>XXXXXXXX XXXXXXXX | | TMR6 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 6<br>(PPG 12, PPG 13) |
| $0001E4_H$ | Reserved | | TMCSRH6<br>[R/W]<br>- - - 00000 | TMCSRL6<br>[R/W]<br>0 - 000000 | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $0001E8_H$ | TMRLR7 [W]<br>XXXXXXXX XXXXXXXX | | TMR7 [R]<br>XXXXXXXX XXXXXXXX | | Reload Timer 7<br><br>(PPG 14, PPG 15)<br>(A/D Converter) |
| $0001EC_H$ | Reserved | | TMCSRH7<br>[R/W]<br>- - - 00000 | TMCSRL7<br>[R/W]<br>0 - 000000 | |
| $0001F0_H$ | TCDT0 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS0 [R/W]<br>00000000 | Free Running Timer 0<br><br>(ICU 0, ICU 1) |
| $0001F4_H$ | TCDT1 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS1 [R/W]<br>00000000 | Free Running Timer 1<br><br>(ICU 2, ICU 3) |
| $0001F8_H$ | TCDT2 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS2 [R/W]<br>00000000 | Free Running Timer 2<br><br>(OCU 0, OCU 1) |
| $0001FC_H$ | TCDT3 [R/W]<br>XXXXXXXX XXXXXXXX | | Reserved | TCCS3 [R/W]<br>00000000 | Free Running Timer 3<br><br>(OCU 2, OCU 3) |
| $000200_H$ | DMACA0 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | DMAC |
| $000204_H$ | DMACB0 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000208_H$ | DMACA1 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| $00020C_H$ | DMACB1 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000210_H$ | DMACA2 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| $000214_H$ | DMACB2 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000218_H$ | DMACA3 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| $00021C_H$ | DMACB3 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000220_H$ | DMACA4 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| $000224_H$ | DMACB4 [R/W]<br>00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| $000228_H$ to $00023C_H$ | Reserved | | | | Reserved |
| $000240_H$ | DMACR [R/W]<br>0 - -0 0000 | Reserved | | | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000244_H$ to $0002CC_H$ | Reserved | | | | Reserved |
| $0002D0_H$ | Reserved | ICS045 [R/W] 00000000 | Reserved | ICS67 [R/W] 00000000 | Input Capture 4 to 7 |
| $0002D4_H$ | IPCP4 [R] XXXXXXXX XXXXXXXX | | IPCP5 [R] XXXXXXXX XXXXXXXX | | |
| $0002D8_H$ | IPCP6 [R] XXXXXXXX XXXXXXXX | | IPCP7 [R] XXXXXXXX XXXXXXXX | | |
| $0002DC_H$ to $0002EC_H$ | Reserved | | | | Reserved |
| $0002F0_H$ | TCDT4 [R/W] XXXXXXXX XXXXXXXX | | Reserved | TCCS4 [R/W] 00000000 | Free Running Timer 4 (ICU 4, ICU 5) |
| $0002F4_H$ | TCDT5 [R/W] XXXXXXXX XXXXXXXX | | Reserved | TCCS5 [R/W] 00000000 | Free Running Timer 5 (ICU 6, ICU 7) |
| $0002F8_H$ | TCDT6 [R/W] XXXXXXXX XXXXXXXX | | Reserved | TCCS6 [R/W] 00000000 | Free Running Timer 6 |
| $0002FC_H$ | TCDT7 [R/W] XXXXXXXX XXXXXXXX | | Reserved | TCCS7 [R/W] 00000000 | Free Running Timer 7 |
| $000300_H$ | UDRC1 [W] 00000000 | UDRC0 [W] 00000000 | UDCR1 [R] 00000000 | UDCR0 [R] 00000000 | Up/Down Counter 0 |
| $000304_H$ | UDCCH0 [R/W] 00000000 | UDCCL0 [R/W] 00000000 | Reserved | UDCS0 [R/W] 00000000 | |
| $000308_H$ to $00030C_H$ | Reserved | | | | Reserved |
| $000310_H$ | UDRC3 [W] 00000000 | UDRC2 [W] 00000000 | UDCR3 [R] 00000000 | UDCR2 [R] 00000000 | Up/Down Counter 2 to 3 |
| $000314_H$ | UDCCH2 [R/W] 00000000 | UDCCL2 [R/W] 00000000 | Reserved | UDCS2 [R/W] 00000000 | |
| $000318_H$ | UDCCH3 [R/W] 00000000 | UDCCL3 [R/W] 00000000 | Reserved | UDCS3 [R/W] 00000000 | |
| $00031C_H$ | Reserved | | | | Reserved |
| $000320_H$ | GCN13 [R/W] 00110010 00010000 | | Reserved | GCN23 [R/W] - - - - 0000 | PPG Control 12 to 15 |
| $000324_H$ to $00032C_H$ | Reserved | | | | Reserved |
| $000330_H$ | PTMR12 [R] 11111111 11111111 | | PCSR12 [W] XXXXXXXX XXXXXXXX | | PPG 12 |
| $000334_H$ | PDUT12 [W] XXXXXXXX XXXXXXXX | | PCNH12 [R/W] 0000000 - | PCNL12 [R/W] 000000 - 0 | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000338_H$ | PTMR13 [R]<br>11111111 11111111 | | PCSR13 [W]<br>XXXXXXXX XXXXXXXX | | PPG 13 |
| $00033C_H$ | PDUT13 [W]<br>XXXXXXXX XXXXXXXX | | PCNH13 [R/W]<br>0000000 - | PCNL13 [R/W]<br>000000 - 0 | |
| $000340_H$ | PTMR14 [R]<br>11111111 11111111 | | PCSR14 [W]<br>XXXXXXXX XXXXXXXX | | PPG 14 |
| $000344_H$ | PDUT14 [W]<br>XXXXXXXX XXXXXXXX | | PCNH14 [R/W]<br>0000000 - | PCNL14 [R/W]<br>000000 - 0 | |
| $000348_H$ | PTMR15 [R]<br>11111111 11111111 | | PCSR15 [W]<br>XXXXXXXX XXXXXXXX | | PPG 15 |
| $00034C_H$ | PDUT15 [W]<br>XXXXXXXX XXXXXXXX | | PCNH15 [R/W]<br>0000000 - | PCNL15 [R/W]<br>000000 - 0 | |
| $000350_H$ to $000364_H$ | Reserved | | | | Reserved |
| $000368_H$ | IBCR2 [R/W]<br>00000000 | IBSR2 [R]<br>00000000 | ITBAH2 [R/W]<br>- - - - - - 00 | ITBAL2 [R/W]<br>00000000 | $I^2C$ 2 |
| $00036C_H$ | ITMKH2 [R/W]<br>00 - - - - 11 | ITMKL2 [R/W]<br>11111111 | ISMK2 [R/W]<br>01111111 | ISBA2 [R/W]<br>- 0000000 | |
| $000370_H$ | Reserved | IDAR2 [R/W]<br>00000000 | ICCR2 [R/W]<br>- 0011111 | Reserved | |
| 00374H | IBCR3 [R/W]<br>00000000 | IBSR3 [R]<br>00000000 | ITBAH3 [R/W]<br>- - - - - - 00 | ITBAL3 [R/W]<br>00000000 | $I^2C$ 3 |
| $000378_H$ | ITMKH3 [R/W]<br>00 - - - - 11 | ITMKL3 [R/W]<br>11111111 | ISMK3 [R/W]<br>01111111 | ISBA3 [R/W]<br>- 0000000 | |
| $00037C_H$ | Reserved | IDAR3 [R/W]<br>00000000 | ICCR3 [R/W]<br>- 0011111 | Reserved | |
| $000380_H$ to $00038C_H$ | Reserved | | | | Reserved |
| $000390_H$ | ROMS [R]<br>11111111 00000000 | | Reserved | | ROM Select Register |
| $000394_H$ to $0003EC_H$ | Reserved | | | | Reserved |
| $0003F0_H$ | BSD0 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Bit Search Module |
| $0003F4_H$ | BSD1 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $0003F8_H$ | BSDC [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $0003FC_H$ | BSRR [R]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000400_H$ to $00043C_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000440_H$ | ICR00 [R/W] ---11111 | ICR01 [R/W] ---11111 | ICR02 [R/W] ---11111 | ICR03 [R/W] ---11111 | Interrupt Controller |
| $000444_H$ | ICR04 [R/W] ---11111 | ICR05 [R/W] ---11111 | ICR06 [R/W] ---11111 | ICR07 [R/W] ---11111 | |
| $000448_H$ | ICR08 [R/W] ---11111 | ICR09 [R/W] ---11111 | ICR10 [R/W] ---11111 | ICR11 [R/W] ---11111 | |
| $00044C_H$ | ICR12 [R/W] ---11111 | ICR13 [R/W] ---11111 | ICR14 [R/W] ---11111 | ICR15 [R/W] ---11111 | |
| $000450_H$ | ICR16 [R/W] ---11111 | ICR17 [R/W] ---11111 | ICR18 [R/W] ---11111 | ICR19 [R/W] ---11111 | |
| $000454_H$ | ICR20 [R/W] ---11111 | ICR21 [R/W] ---11111 | ICR22 [R/W] ---11111 | ICR23 [R/W] ---11111 | |
| $000458_H$ | ICR24 [R/W] ---11111 | ICR25 [R/W] ---11111 | ICR26 [R/W] ---11111 | ICR27 [R/W] ---11111 | |
| $00045C_H$ | ICR28 [R/W] ---11111 | ICR29 [R/W] ---11111 | ICR30 [R/W] ---11111 | ICR31 [R/W] ---11111 | |
| $000460_H$ | ICR32 [R/W] ---11111 | ICR33 [R/W] ---11111 | ICR34 [R/W] ---11111 | ICR35 [R/W] ---11111 | |
| $000464_H$ | ICR36 [R/W] ---11111 | ICR37 [R/W] ---11111 | ICR38 [R/W] ---11111 | ICR39 [R/W] ---11111 | |
| $000468_H$ | ICR40 [R/W] ---11111 | ICR41 [R/W] ---11111 | ICR42 [R/W] ---11111 | ICR43 [R/W] ---11111 | |
| $00046C_H$ | ICR44 [R/W] ---11111 | ICR45 [R/W] ---11111 | ICR46 [R/W] ---11111 | ICR47 [R/W] ---11111 | |
| $000470_H$ | ICR48 [R/W] ---11111 | ICR49 [R/W] ---11111 | ICR50 [R/W] ---11111 | ICR51 [R/W] ---11111 | |
| $000474_H$ | ICR52 [R/W] ---11111 | ICR53 [R/W] ---11111 | ICR54 [R/W] ---11111 | ICR55 [R/W] ---11111 | |
| $000478_H$ | ICR56 [R/W] ---11111 | ICR57 [R/W] ---11111 | ICR58 [R/W] ---11111 | ICR59 [R/W] ---11111 | |
| $00047C_H$ | ICR60 [R/W] ---11111 | ICR61 [R/W] ---11111 | ICR62 [R/W] ---11111 | ICR63 [R/W] ---11111 | |
| $000480_H$ | RSRR [R/W] 10000000 | STCR [R/W] 00110011 | TBCR [R/W] 00XXX – 00 | CTBR [W] XXXXXXXX | Clock Controller |
| $000484_H$ | CLKR [R/W] ---- 0000 | WPR [W] XXXXXXXX | DIVR0 [R/W] 00000011 | DIVR1 [R/W] 00000000 | |
| $000488_H$ | CTEST [R/W] XXXX00XX | Reserved | Reserved | Reserved | C-Unit Test (hidden) |
| $00048C_H$ | PLLDIVM [R/W] - - - - 0000 | PLLDIVN [R/W] - - 000000 | PLLDIVG [R/W] - - - - 0000 | PLLMULG [W] 00000000 | PLL Interface |
| $000490_H$ | PLLCTRL [R/W] - - - - 0000 | Reserved | Reserved | Reserved | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000494_H$ | OSCC1 [R/W]<br>- - - - - 010 | OSCS1 [R/W]<br>00001111 | OSCC2 [R/W]<br>- - - - - 010 | OSCS2 [R/W]<br>00001111 | Main/Sub Oscillator Control |
| $000498_H$ | PORTEN [R/W]<br>- - - - - - 00 | Reserved | Reserved | Reserved | Port Input Enable Control |
| $00049C_H$ | Reserved | | | | Reserved |
| $0004A0_H$ | Reserved | WTCER [R/W]<br>- - - - - - 00 | WTCR [R/W]<br>00000000 000 – 00 – 0 | | Real Time Clock (Watch Timer) |
| $0004A4_H$ | Reserved | WTBR [R/W]<br>- - - XXXXX XXXXXXXX XXXXXXXX | | | |
| $0004A8_H$ | WTHR [R/W]<br>- - - 00000 | WTMR [R/W]<br>- - 000000 | WTSR [R/W]<br>- - 000000 | Reserved | |
| $0004AC_H$ | CSVTR [R/W]<br>- - - 00010 | CSVCR [R/W]<br>00011100 | CSCFG [R/W]<br>0X000000 | CMCFG [R/W]<br>00000000 | Clock-Supervisor / Selector / Monitor |
| $0004B0_H$ | CUCR [R/W]<br>- - - - - - - - - - - - 0 - - 00 | | CUTD [R/W]<br>10000000 00000000 | | Calibration of Sub Clock |
| $0004B4_H$ | CUTR1 [R]<br>- - - - - - - - 00000000 | | CUTR2 [R]<br>00000000 00000000 | | |
| $0004B8_H$ | CMPR [R/W]<br>- - 000010 11111101 | | Reserved | CMCR [R/W]<br>- 001 - - 00 | Clock Modulator |
| $0004BC_H$ | CMT1 [R/W]<br>00000000 1 - - - 0000 | | CMT2 [R/W]<br>- - 000000 - - 000000 | | |
| $0004C0_H$ | CANPRE [R/W]<br>0 - - - 0000 | CANCKD [R/W]<br>- - - - - 000[*1] | Reserved | Reserved | CAN Clock Control |
| $0004C4_H$ | LVSEL [R/W]<br>00000111 | LVDET [R/W]<br>0000 0 – 00 | HWWDE [R/W]<br>- - - - - - 00 | HWWD [R/W,W]<br>00011000 | Low Voltage Detection/ Hardware Watchdog |
| $0004C8_H$ | OSCRH [R/W]<br>000 - - 001 | OSCRL [R/W]<br>- - - - - 000 | WPCRH [R/W]<br>00 - - - 000 | WPCRL [R/W]<br>- - - - - - 00 | Main-/Sub-Oscillation Stabilisation Timer |
| $0004CC_H$ | OSCCR [R/W]<br>- - - - - - 00 | Reserved | REGSEL [R/W]<br>- - 000110 | REGCTR [R/W]<br>- - - 0 - - 00 | Main- Oscillation Standby Control Main/Subregulator Control |
| $0004D0_H$ to $0007F8_H$ | Reserved | | | | Reserved |
| $0007FC_H$ | Reserved | MODR [W]<br>XXXXXXXX | Reserved | Reserved | Mode Register |
| $000800_H$ to $000BFC_H$ | Reserved | | | | Reserved |
| $000C00_H$ | TVCTW [W]<br>XXXXXXXX | TVCTR [R]<br>- - XXXXXX | Reserved | IOS [R/W]<br>00000000 | I-Unit Test (hidden) |
| $000C04_H$ to $000CFC_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000D00_H$ | Reserved | Reserved | PDRD02 [R]<br>XXXXXXXX | Reserved | R-bus<br>Port Data<br>Direct Read<br>Register |
| $000D04_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000D08_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000D0C_H$ | Reserved | Reserved | PDRD14 [R]<br>XXXXXXXX | PDRD15 [R]<br>- - - - XXXX | |
| $000D10_H$ | PDRD16 [R]<br>XXXXXXXX | PDRD17 [R]<br>XXXX - - - - | PDRD18 [R]<br>- XXX - XXX | PDRD19 [R]<br>- XXX - XXX | |
| $000D14_H$ | PDRD20 [R]<br>- - - - - XXX | Reserved | PDRD22 [R]<br>- - XX - X - X | PDRD23 [R]<br>- XXXXXXX | |
| $000D18_H$ | PDRD24 [R]<br>XXXXXXXX | PDRD25 [R]<br>XXXXXXXX | PDRD26 [R]<br>XXXXXXXX | PDRD27 [R]<br>XXXXXXXX | |
| $000D1C_H$ | PDRD28 [R]<br>- - XXXXX | PDRD29 [R]<br>XXXXXXXX | Reserved | Reserved | |
| $000D20_H$ to $000D3C_H$ | Reserved | | | | Reserved |
| $000D40_H$ | Reserved | Reserved | DDR02 [R/W]<br>00000000 | Reserved | R-bus<br>Port Direction<br>Register |
| $000D44_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000D48_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000D4C_H$ | Reserved | Reserved | DDR14 [R/W]<br>00000000 | DDR15 [R/W]<br>- - - - 0000 | |
| $000D50_H$ | DDR16 [R/W]<br>00000000 | DDR17 [R/W]<br>0000 - - - - | DDR18 [R/W]<br>- 000 - 000 | DDR19 [R/W]<br>- 000 - 000 | |
| $000D54_H$ | DDR20 [R/W]<br>- - - - - 000 | Reserved | DDR22 [R/W]<br>- - 00 - 0 - 0 | DDR23 [R/W]<br>- 0000000 | |
| $000D58_H$ | DDR24 [R/W]<br>00000000 | DDR25 [R/W]<br>00000000 | DDR26 [R/W]<br>00000000 | DDR27 [R/W]<br>00000000 | |
| $000D5C_H$ | DDR28 [R/W]<br>- - 00000 | DDR29 [R/W]<br>00000000 | Reserved | Reserved | |
| $000D60_H$ to $000D7C_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000D80_H$ | Reserved | Reserved | Reserved | Reserved | R-bus Port Function Register |
| $000D84_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000D88_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000D8C_H$ | Reserved | Reserved | PFR14 [R/W] 00000000 | PFR15 [R/W] - - - - 0000 | |
| $000D90_H$ | PFR16 [R/W] 00000000 | PFR17 [R/W] 0000 - - - - | PFR18 [R/W] - 000 - 000 | PFR19 [R/W] - 000 - 000 | |
| $000D94_H$ | PFR20 [R/W] - - - - - 000 | Reserved | PFR22 [R/W] - - 00 - 0 - 0 | PFR23 [R/W] - 000000 | |
| $000D98_H$ | PFR24 [R/W] 00000000 | PFR25 [R/W] 00000000 | PFR26 [R/W] 00000000 | PFR27 [R/W] 00000000 | |
| $000D9C_H$ | PFR28 [R/w] - - 00000 | PFR29 [R/W] 00000000 | Reserved | Reserved | |
| $000DA0_H$ to $000DBC_H$ | Reserved | | | | Reserved |
| $000DC0_H$ | Reserved | Reserved | Reserved | Reserved | R-bus Extra Port Function Register |
| $000DC4_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000DC8_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000DCC_H$ | Reserved | Reserved | EPFR14 [R/W] 00000000 | EPFR15 [R/W] - - - - 0000 | |
| $000DD0_H$ | EPFR16 [R/W] 0000 - - - - | Reserved | EPFR18 [R/W] - 000 - 000 | EPFR19 [R/W] - 0 - - - 0 - - | |
| $000DD4_H$ | EPFR20 [R/W] - - - - - 000 | Reserved | Reserved | Reserved | |
| $000DD8_H$ | Reserved | Reserved | EPFR26 [R/W] 00000000 | EPFR27 [R/W] 00000000 | |
| $000DDC_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000DE0_H$ to $000DFC_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000E00_H$ | Reserved | Reserved | PODR02 [R/W] 00000000 | Reserved | R-bus Port Output Drive Select Register |
| $000E04_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000E08_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000E0C_H$ | Reserved | Reserved | PODR14 [R/W] 00000000 | PODR15 [R/W] - - - - 0000 | |
| $000E10_H$ | PODR16 [R/W] 00000000 | PODR17 [R/W] 0000 - - - - | PODR18 [R/W] - 000 - 000 | PODR19 [R/W] - 000 - 000 | |
| $000E14_H$ | PODR20 [R/W] - - - - - 000 | Reserved | PODR22 [R/W] - - 00 - 0 - 0 | PODR23 [R/W] - 0000000 | |
| $000E18_H$ | PODR24 [R/W] 00000000 | PODR25 [R/W] 00000000 | PODR26 [R/W] 00000000 | PODR27 [R/W] 00000000 | |
| $000E1C_H$ | PODR28 [R/W] - - 00000 | PODR29 [R/W] 00000000 | Reserved | Reserved | |
| $000E20_H$ to $000E3C_H$ | Reserved | | | | Reserved |
| $000E40_H$ | Reserved | Reserved | PILR02 [R/W] 00000000 | Reserved | R-bus Port Input Level Select Register |
| $000E44_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000E48_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000E4C_H$ | Reserved | Reserved | PILR14 [R/W] 00000000 | PILR15 [R/W] - - - - 0000 | |
| $000E50_H$ | PILR16 [R/W] 00000000 | PILR17 [R/W] 0000 - - - - | PILR18 [R/W] - 000 - 000 | PILR19 [R/W] - 000 - 000 | |
| $000E54_H$ | PILR20 [R/W] - - - - - 000 | Reserved | PILR22 [R/W] - - 00 - 0 - 0 | PILR23 [R/W] - 0000000 | |
| $000E58_H$ | PILR24 [R/W] 00000000 | PILR25 [R/W] 00000000 | PILR26 [R/W] 00000000 | PILR27 [R/W] 00000000 | |
| $000E5C_H$ | PILR28 [R/W] - - 000000 | PILR29 [R/W] 00000000 | Reserved | Reserved | |
| $000E60_H$ to $000E7C_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000E80_H$ | Reserved | Reserved | EPILR02 [R/W] 00000000 | Reserved | R-bus Extra Port Input Level Select Register |
| $000E84_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000E88_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000E8C_H$ | Reserved | Reserved | EPILR14 [R/W] 00000000 | EPILR15 [R/W] - - - - 0000 | |
| $000E90_H$ | EPILR16 [R/W] 00000000 | EPILR17 [R/W] 0000 - - - - | EPILR18 [R/W] - 000 - 000 | EPILR19 [R/W] - 000 - 000 | |
| $000E94_H$ | EPILR20 [R/W] - - - - - 000 | Reserved | EPILR22 [R/W] - - 00 - 0 - 0 | EPILR23 [R/W] - 0000000 | |
| $000E98_H$ | EPILR24 [R/W] 00000000 | EPILR25 [R/W] 00000000 | EPILR26 [R/W] 00000000 | EPILR27 [R/W] 00000000 | |
| $000E9C_H$ | EPILR28 [R/W] - - 00000 | EPILR29 [R/W] 00000000 | Reserved | Reserved | |
| $000EA0_H$ to $000EBC_H$ | Reserved | | | | Reserved |
| $000EC0_H$ | Reserved | Reserved | PPER02 [R/W] 00000000 | Reserved | R-bus Port Pull-Up/Down Enable Register |
| $000EC4_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000EC8_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000ECC_H$ | Reserved | Reserved | PPER14 [R/W] 00000000 | PPER15 [R/W] - - - - 0000 | |
| $000ED0_H$ | PPER16 [R/W] 00000000 | PPER17 [R/W] 0000 - - - - | PPER18 [R/W] - 000 - 000 | PPER19 [R/W] - 000 - 000 | |
| $000ED4_H$ | PPER20 [R/W] - - - - - 000 | Reserved | PPER22 [R/W] - - 00 - 0 - 0 | PPER23 [R/W] - 0000000 | |
| $000ED8_H$ | PPER24 [R/W] 00000000 | PPER25 [R/W] 00000000 | PPER26 [R/W] 00000000 | PPER27 [R/W] 00000000 | |
| $000EDC_H$ | PPER28 [R/W] - - 00000 | PPER29 [R/W] 00000000 | Reserved | Reserved | |
| $000EE0_H$ to $000EFC_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000F00_H$ | Reserved | Reserved | PPCR02 [R/W]<br>11111111 | Reserved | R-bus Port Pull-Up/Down Control Register |
| $000F04_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000F08_H$ | Reserved | Reserved | Reserved | Reserved | |
| $000F0C_H$ | Reserved | Reserved | PPCR14 [R/W]<br>11111111 | PPCR15 [R/W]<br>- - - - 1111 | |
| $000F10_H$ | PPCR16 [R/W]<br>11111111 | PPCR17 [R/W]<br>1111 - - - - | PPCR18 [R/W]<br>- 111 - 111 | PPCR19 [R/W]<br>- 111 - 111 | |
| $000F14_H$ | PPCR20 [R/W]<br>- - - - - 111 | Reserved | PPCR22 [R/W]<br>- - 11 - 1 - 1 | PPCR23 [R/W]<br>-1111111 | |
| $000F18_H$ | PPCR24 [R/W]<br>11111111 | PPCR25 [R/W]<br>11111111 | PPCR26 [R/W]<br>11111111 | PPCR27 [R/W]<br>11111111 | |
| $000F1C_H$ | PPCR28 [R/W]<br>- - 11111 | PPCR29 [R/W]<br>11111111 | Reserved | Reserved | |
| $000F20_H$ to $000F3C_H$ | Reserved | | | | Reserved |
| $001000_H$ | DMASA0 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | DMAC |
| $001004_H$ | DMADA0 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $001008_H$ | DMASA1 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00100C_H$ | DMADA1 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $001010_H$ | DMASA2 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $001014_H$ | DMADA2 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $001018_H$ | DMASA3 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00101C_H$ | DMADA3 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $001020_H$ | DMASA4 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $001024_H$ | DMADA4 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $001028_H$ to $001FFC_H$ | Reserved | | | | Reserved |
| $002000_H$ to $006FFC_H$ | CY91F467Cx Flash-cache size is 8 Kbytes : $004000_H$ to $005FFC_H$<br>CY91F465CA Flash-cache size is 8 Kbytes : $004000_H$ to $005FFC_H$<br>CY91F463CA Flash-cache size is 4 Kbytes : $005000_H$ to $005FFC_H$ | | | | Flash-cache / I-RAM area |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $007000_H$ | FMCS [R/W]<br>01101000 | FMCR [R]<br>- - - 00000 | FCHCR [R/W]<br>- - - - - - 00 10000011 | | Flash Memory/ Flash-cache/ I-RAM Control Register |
| $007004_H$ | FMWT [R/W]<br>11111111 11111111 | | FMWT2 [R]<br>- 001 - - - - | FMPS [R/W]<br>- - - - - 000 | |
| $007008_H$ | FMAC [R]<br>00000000 00000000 00000000 00000000 | | | | |
| $00700C_H$ | FCHA0 [R/W]<br>- - - - - - - - - - - 00000 00000000 00000000 | | | | Flash-cache Non-cacheable area setting Register |
| $007010_H$ | FCHA1 [R/W]<br>- - - - - - - - - - - 00000 00000000 00000000 | | | | |
| $007014_H$ to 007FFCH | Reserved | | | | Reserved |
| 008000H to $00BFFC_H$ | CY91F467Cx Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$<br>CY91F465CA Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$<br>CY91F463CA Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$<br>(instruction access is 1 wait cycle, data access is 1 wait cycle) | | | | Boot ROM area |
| $00C000_H$ | CTRLR0 [R/W]<br>00000000 00000001 | | STATR0 [R/W]<br>00000000 00000000 | | CAN 0 Control Register |
| $00C004_H$ | ERRCNT0 [R]<br>00000000 00000000 | | BTR0 [R/W]<br>00100011 00000001 | | |
| $00C008_H$ | INTR0 [R]<br>00000000 00000000 | | TESTR0 [R/W]<br>00000000 X0000000 | | |
| $00C00C_H$ | BRPE0 [R/W]<br>00000000 00000000 | | Reserved | | |
| $00C010_H$ | IF1CREQ0 [R/W]<br>00000000 00000001 | | IF1CMSK0 [R/W]<br>00000000 00000000 | | CAN 0 IF 1 Register |
| $00C014_H$ | IF1MSK20 [R/W]<br>11111111 11111111 | | IF1MSK10 [R/W]<br>11111111 11111111 | | |
| $00C018_H$ | IF1ARB20 [R/W]<br>00000000 00000000 | | IF1ARB10 [R/W]<br>00000000 00000000 | | |
| $00C01C_H$ | IF1MCTR0 [R/W]<br>00000000 00000000 | | Reserved | | |
| $00C020_H$ | IF1DTA10 [R/W]<br>00000000 00000000 | | IF1DTA20 [R/W]<br>00000000 00000000 | | |
| $00C024_H$ | IF1DTB10 [R/W]<br>00000000 00000000 | | IF1DTB20 [R/W]<br>00000000 00000000 | | |
| $00C028_H$ to $00C02C_H$ | Reserved | | | | |
| $00C030_H$ | IF1DTA20 [R/W]<br>00000000 00000000 | | IF1DTA10 [R/W]<br>00000000 00000000 | | |
| $00C034_H$ | IF1DTB20 [R/W]<br>00000000 00000000 | | IF1DTB10 [R/W]<br>00000000 00000000 | | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $00C038_H$ to $00C03C_H$ | Reserved | | | | |
| $00C040_H$ | IF2CREQ0 [R/W] 00000000 00000001 | | IF2CMSK0 [R/W] 00000000 00000000 | | CAN 0 IF 2 Register |
| $00C044_H$ | IF2MSK20 [R/W] 11111111 11111111 | | IF2MSK10 [R/W] 11111111 11111111 | | |
| $00C048_H$ | IF2ARB20 [R/W] 00000000 00000000 | | IF2ARB10 [R/W] 00000000 00000000 | | |
| $00C04C_H$ | IF2MCTR0 [R/W] 00000000 00000000 | | Reserved | | |
| $00C050_H$ | IF2DTA10 [R/W] 00000000 00000000 | | IF2DTA20 [R/W] 00000000 00000000 | | |
| $00C054_H$ | IF2DTB10 [R/W] 00000000 00000000 | | IF2DTB20 [R/W] 00000000 00000000 | | |
| $00C058_H$ to $00C05C_H$ | Reserved | | | | |
| $00C060_H$ | IF2DTA20 [R/W] 00000000 00000000 | | IF2DTA10 [R/W] 00000000 00000000 | | |
| $00C064_H$ | IF2DTB20 [R/W] 00000000 00000000 | | IF2DTB10 [R/W] 00000000 00000000 | | |
| $00C068_H$ to $00C07C_H$ | Reserved | | | | |
| $00C080_H$ | TREQR20 [R] 00000000 00000000 | | TREQR10 [R] 00000000 00000000 | | CAN 0 Status Flags |
| $00C084_H$ to $00C08C_H$ | Reserved | | | | |
| $00C090_H$ | NEWDT20 [R] 00000000 00000000 | | NEWDT10 [R] 00000000 00000000 | | |
| $00C094_H$ to $00C09C_H$ | Reserved | | | | |
| $00C0A0_H$ | INTPND20 [R] 00000000 00000000 | | INTPND10 [R] 00000000 00000000 | | |
| $00C0A4_H$ to $00C0AC_H$ | Reserved | | | | |
| $00C0B0_H$ | MSGVAL20 [R] 00000000 00000000 | | MSGVAL10 [R] 00000000 00000000 | | |
| $00C0B4_H$ to $00C0FC_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $00C100_H$ | CTRLR1 [R/W]<br>00000000 00000001 | | STATR1 [R/W]<br>00000000 00000000 | | CAN 1<br>Control<br>Register |
| $00C104_H$ | ERRCNT1 [R]<br>00000000 00000000 | | BTR1 [R/W]<br>00100011 00000001 | | |
| $00C108_H$ | INTR1 [R]<br>00000000 00000000 | | TESTR1 [R/W]<br>00000000 X0000000 | | |
| $00C10C_H$ | BRPE1 [R/W]<br>00000000 00000000 | | Reserved | | |
| $00C110_H$ | IF1CREQ1 [R/W]<br>00000000 00000001 | | IF1CMSK1 [R/W]<br>00000000 00000000 | | CAN 1<br>IF 1 Register |
| $00C114_H$ | IF1MSK21 [R/W]<br>11111111 11111111 | | IF1MSK11 [R/W]<br>11111111 11111111 | | |
| $00C118_H$ | IF1ARB21 [R/W]<br>00000000 00000000 | | IF1ARB11 [R/W]<br>00000000 00000000 | | |
| $00C11C_H$ | IF1MCTR1 [R/W]<br>00000000 00000000 | | Reserved | | |
| $00C120_H$ | IF1DTA11 [R/W]<br>00000000 00000000 | | IF1DTA21 [R/W]<br>00000000 00000000 | | |
| $00C124_H$ | IF1DTB11 [R/W]<br>00000000 00000000 | | IF1DTB21 [R/W]<br>00000000 00000000 | | |
| $00C128_H$ to $00C12C_H$ | Reserved | | | | |
| $00C130_H$ | IF1DTA21 [R/W]<br>00000000 00000000 | | IF1DTA11 [R/W]<br>00000000 00000000 | | |
| $00C134_H$ | IF1DTB21 [R/W]<br>00000000 00000000 | | IF1DTB11 [R/W]<br>00000000 00000000 | | |
| $00C138_H$ to $00C13C_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $00C140_H$ | IF2CREQ1 [R/W]<br>00000000 00000001 | | IF2CMSK1 [R/W]<br>00000000 00000000 | | CAN 1<br>IF 2 Register |
| $00C144_H$ | IF2MSK21 [R/W]<br>11111111 11111111 | | IF2MSK11 [R/W]<br>11111111 11111111 | | |
| $00C148_H$ | IF2ARB21 [R/W]<br>00000000 00000000 | | IF2ARB11 [R/W]<br>00000000 00000000 | | |
| $00C14C_H$ | IF2MCTR1 [R/W]<br>00000000 00000000 | | Reserved | | |
| $00C150_H$ | IF2DTA11 [R/W]<br>00000000 00000000 | | IF2DTA21 [R/W]<br>00000000 00000000 | | |
| $00C154_H$ | IF2DTB11 [R/W]<br>00000000 00000000 | | IF2DTB21 [R/W]<br>00000000 00000000 | | |
| $00C158_H$ to $00C15C_H$ | Reserved | | | | |
| $00C160_H$ | IF2DTA21 [R/W]<br>00000000 00000000 | | IF2DTA11 [R/W]<br>00000000 00000000 | | |
| $00C164_H$ | IF2DTB21 [R/W]<br>00000000 00000000 | | IF2DTB11 [R/W]<br>00000000 00000000 | | |
| $00C168_H$ to $00C17C_H$ | Reserved | | | | |
| $00C180_H$ | TREQR21 [R]<br>00000000 00000000 | | TREQR11 [R]<br>00000000 00000000 | | CAN 1<br>Status Flags |
| $00C184_H$ to $00C18C_H$ | Reserved | | | | |
| $00C190_H$ | NEWDT21 [R]<br>00000000 00000000 | | NEWDT11 [R]<br>00000000 00000000 | | |
| $00C194_H$ to $00C19C_H$ | Reserved | | | | |
| $00C1A0_H$ | INTPND21 [R]<br>00000000 00000000 | | INTPND11 [R]<br>00000000 00000000 | | |
| $00C1A4_H$ to $00C1AC_H$ | Reserved | | | | Reserved |
| $00C1B0_H$ | MSGVAL21 [R]<br>00000000 00000000 | | MSGVAL11 [R]<br>00000000 00000000 | | CAN 1<br>Status Flags |
| $00C1B4_H$ to $00C1FC_H$ | Reserved | | | | Reserved |
| $00C200_H$ | CTRLR2 [R/W]<br>00000000 00000001 | | STATR2 [R/W]<br>00000000 00000000 | | CAN 2<br>Control<br>Register |
| $00C204_H$ | ERRCNT2 [R]<br>00000000 00000000 | | BTR2 [R/W]<br>00100011 00000001 | | |
| $00C208_H$ | INTR2 [R]<br>00000000 00000000 | | TESTR2 [R/W]<br>00000000 X0000000 | | |
| $00C20C_H$ | BRPE2 [R/W]<br>00000000 00000000 | | Reserved | | |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $00C210_H$ | IF1CREQ2 [R/W]<br>00000000 00000001 | | IF1CMSK2 [R/W]<br>00000000 00000000 | | CAN 2<br>IF 1 Register |
| $00C214_H$ | IF1MSK22 [R/W]<br>11111111 11111111 | | IF1MSK12 [R/W]<br>11111111 11111111 | | |
| $00C218_H$ | IF1ARB22 [R/W]<br>00000000 00000000 | | IF1ARB12 [R/W]<br>00000000 00000000 | | |
| $00C21C_H$ | IF1MCTR2 [R/W]<br>00000000 00000000 | | Reserved | | |
| $00C220_H$ | IF1DTA12 [R/W]<br>00000000 00000000 | | IF1DTA22 [R/W]<br>00000000 00000000 | | |
| $00C224_H$ | IF1DTB12 [R/W]<br>00000000 00000000 | | IF1DTB22 [R/W]<br>00000000 00000000 | | |
| $00C228_H$ to $00C22C_H$ | Reserved | | | | |
| $00C230_H$ | IF1DTA22 [R/W]<br>00000000 00000000 | | IF1DTA12 [R/W]<br>00000000 00000000 | | |
| $00C234_H$ | IF1DTB22 [R/W]<br>00000000 00000000 | | IF1DTB12 [R/W]<br>00000000 00000000 | | |
| $00C238_H$ to $00C23C_H$ | Reserved | | | | Reserved |
| $00C240_H$ | IF2CREQ2 [R/W]<br>00000000 00000001 | | IF2CMSK2 [R/W]<br>00000000 00000000 | | CAN 2<br>IF 2 Register |
| $00C244_H$ | IF2MSK22 [R/W]<br>11111111 11111111 | | IF2MSK12 [R/W]<br>11111111 11111111 | | |
| $00C248_H$ | IF2ARB22 [R/W]<br>00000000 00000000 | | IF2ARB12 [R/W]<br>00000000 00000000 | | |
| $00C24C_H$ | IF2MCTR2 [R/W]<br>00000000 00000000 | | Reserved | | |
| $00C250_H$ | IF2DTA12 [R/W]<br>00000000 00000000 | | IF2DTA22 [R/W]<br>00000000 00000000 | | |
| $00C254_H$ | IF2DTB12 [R/W]<br>00000000 00000000 | | IF2DTB22 [R/W]<br>00000000 00000000 | | |
| $00C258_H$ to $00C25C_H$ | Reserved | | | | |
| $00C260_H$ | IF2DTA22 [R/W]<br>00000000 00000000 | | IF2DTA12 [R/W]<br>00000000 00000000 | | |
| $00C264_H$ | IF2DTB22 [R/W]<br>00000000 00000000 | | IF2DTB12 [R/W]<br>00000000 00000000 | | |
| $00C268_H$ to $00C27C_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $00C280_H$ | TREQR22 [R]<br>00000000 00000000 | | TREQR12 [R]<br>00000000 00000000 | | CAN 2<br>Status Flags |
| $00C284_H$<br>to $00C28C_H$ | Reserved | | | | |
| $00C290_H$ | NEWDT22 [R]<br>00000000 00000000 | | NEWDT12 [R]<br>00000000 00000000 | | |
| $00C294_H$<br>to $00C29C_H$ | Reserved | | | | |
| $00C2A0_H$ | INTPND22 [R]<br>00000000 00000000 | | INTPND12 [R]<br>00000000 00000000 | | |
| $00C2A4_H$<br>to $00C2AC_H$ | Reserved | | | | |
| $00C2B0_H$ | MSGVAL22 [R]<br>00000000 00000000 | | MSGVAL12 [R]<br>00000000 00000000 | | CAN 2<br>Status Flags |
| $00C2B4_H$<br>to $00EFFC_H$ | Reserved | | | | Reserved |
| $00F000_H$ | BCTRL [R/W]<br>-------- -------- 11111100 00000000 | | | | EDSU / MPU |
| $00F004_H$ | BSTAT [R/W]<br>-------- -----000 00000000 10--0000 | | | | |
| $00F008_H$ | BIAC [R]<br>-------- -------- 00000000 00000000 | | | | |
| $00F00C_H$ | BOAC [R]<br>-------- -------- 00000000 00000000 | | | | |
| $00F010_H$ | BIRQ [R/W]<br>-------- -------- 00000000 00000000 | | | | |
| $00F014_H$<br>to $00F01C_H$ | Reserved | | | | |
| $00F020_H$ | BCR0 [R/W]<br>-------- 00000000 00000000 00000000 | | | | |
| $00F024_H$ | BCR1 [R/W]<br>-------- 00000000 00000000 00000000 | | | | |
| $00F028_H$ | BCR2 [R/W]<br>-------- 00000000 00000000 00000000 | | | | |
| $00F02C_H$ | BCR3 [R/W]<br>-------- 00000000 00000000 00000000 | | | | |
| $00F030_H$<br>to $00F07C_H$ | Reserved | | | | Reserved |

| Address | Register | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $00F080_H$ | BAD0 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | EDSU / MPU |
| $00F084_H$ | BAD1 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F088_H$ | BAD2 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F08C_H$ | BAD3 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F090_H$ | BAD4 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F094_H$ | BAD5 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F098_H$ | BAD6 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F09C_H$ | BAD7 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | EDSU / MPU |
| $00F0A0_H$ | BAD8 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F0A4_H$ | BAD9 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F0A8_H$ | BAD10 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F0AC_H$ | BAD11 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F0B0_H$ | BAD12 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F0B4_H$ | BAD13 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F0B8_H$ | BAD14 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F0BC_H$ | BAD15 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $00F0C0_H$ to $01FFFC_H$ | Reserved | | | | Reserved |
| $020000_H$ to $02FFFC_H$ | CY91F467Cx D-RAM size is 32 Kbytes : $028000_H$ to $02FFFC_H$<br>CY91F465CA D-RAM size is 16 Kbytes : $02C000_H$ to $02FFFC_H$<br>CY91F463CA D-RAM size is 16 Kbytes : $02C000_H$ to $02FFFC_H$<br>(data access is 0 wait cycles) | | | | D-RAM area |
| $030000_H$ to $03FFFC_H$ | CY91F467Cx ID-RAM size is 32 Kbytes : $030000_H$ to $037FFC_H$<br>CY91F465CA ID-RAM size is 16 Kbytes : $030000_H$ to $033FFC_H$<br>CY91F463CA ID-RAM size is 8 Kbytes : $030000_H$ to $031FFC_H$<br>(instruction access is 0 wait cycles, data access is 1 wait cycle) | | | | ID-RAM area |

*1 : depends on the number of available CAN channels

## 12.2 Flash Memory and External Bus Area

| 32bit Read/Write | dat[31:0] | | | | dat[31:0] | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 16bit Read/Write | dat[31:16] | | dat[15:0] | | dat[31:16] | | dat[15:0] | | |
| Address | Register | | | | | | | | Block |
| | + 0 | + 1 | + 2 | + 3 | + 4 | + 5 | + 6 | + 7 | |
| $040000_H$ to $05FFF8_H$ | SA8 (64KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | SA9 (64KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | ROMS0 |
| $060000_H$ to $07FFF8_H$ | SA10 (64KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | SA11 (64KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | ROMS1 |
| $080000_H$ to $09FFF8_H$ | SA12 (64KB, CY91F467Cx, CY91F465CA); Reserved (CY91F463CA) | | | | SA13 (64KB, CY91F467Cx, CY91F465CA); Reserved (CY91F463CA) | | | | ROMS2 |
| $0A0000_H$ to $0BFFF8_H$ | SA14 (64KB, CY91F467Cx, CY91F465CA); Reserved (CY91F463CA) | | | | SA15 (64KB, CY91F467Cx, CY91F465CA); Reserved (CY91F463CA) | | | | ROMS3 |
| $0C0000_H$ to $0DFFF8_H$ | SA16 (64KB) | | | | SA17 (64KB) | | | | ROMS4 |
| $0E0000_H$ to $0FFFF0_H$ | SA18 (64KB) | | | | SA19 (64KB) | | | | ROMS5 |
| $0FFFF8_H$ | FMV [R] 06 00 00 00H | | | | FRV [R] 00 00 BF F8H | | | | |
| $100000_H$ to $11FFF8_H$ | SA20 (64KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | SA21 (64KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | ROMS6 |
| $120000_H$ to $13FFF8_H$ | SA22 (64KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | SA23 (64KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | |
| $140000_H$ to $143FF8_H$ | SA0 (8KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | SA1 (8KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | ROMS7 |
| $144000_H$ to $17FF8_H$ | SA2 (8KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | SA3 (8KB, CY91F467Cx); Reserved (CY91F465CA, CY91F463CA) | | | | |
| $148000_H$ to $14BFF8_H$ | SA4 (8KB) | | | | SA5 (8KB) | | | | |
| $14C000_H$ to $14FFF8_H$ | SA6 (8KB) | | | | SA7 (8KB) | | | | |
| $150000_H$ to $17FFF8_H$ | Reserved | | | | | | | | |

| 32bit Read/Write | dat[31:0] | | | | dat[31:0] | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 16bit Read/Write | dat[31:16] | | dat[15:0] | | dat[31:16] | | dat[15:0] | | |
| Address | Register | | | | | | | | Block |
| | + 0 | + 1 | + 2 | + 3 | + 4 | + 5 | + 6 | + 7 | |
| $180000_H$ to $1BFFF8_H$ | Reserved | | | | | | | | ROMS8 |
| $1C0000_H$ to $1FFFF8_H$ | | | | | | | | | ROMS9 |
| $200000_H$ to $27FFF8_H$ | | | | | | | | | ROMS10 |
| $280000_H$ to $2FFFF8_H$ | | | | | | | | | ROMS11 |
| $300000_H$ to $37FFF8_H$ | | | | | | | | | ROMS12 |
| $380000_H$ to $3FFFF8_H$ | | | | | | | | | ROMS13 |
| $400000_H$ to $47FFF8_H$ | | | | | | | | | ROMS14 |
| $480000_H$ to $4FFFF8_H$ | | | | | | | | | ROMS15 |

Notes: Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read.

On CY91F465CA and CY91F463CA, write access to the flash is only possible in 16-bit mode.

## 13. Interrupt Vector Table

| Interrupt | Interrupt Number | | Interrupt Level *1 | | Interrupt Vector *2 | | DMA Resource Number |
|---|---|---|---|---|---|---|---|
| | Decimal | Hexa-decimal | Setting Register | Register Address | Offset | Default Vector Address | |
| Reset | 0 | 00 | - | - | 0x3FC | 0x000FFFFC | |
| Mode vector | 1 | 01 | - | - | 0x3F8 | 0x000FFFF8 | |
| System reserved | 2 | 02 | - | - | 0x3F4 | 0x000FFFF4 | |
| System reserved | 3 | 03 | - | - | 0x3F0 | 0x000FFFF0 | |
| System reserved | 4 | 04 | - | - | 0x3EC | 0x000FFFEC | |
| CPU supervisor mode (INT #5 instruction) *6 | 5 | 05 | - | - | 0x3E8 | 0x000FFFE8 | |
| Memory Protection exception *6 | 6 | 06 | - | - | 0x3E4 | 0x000FFFE4 | |
| Co-processor fault trap *5 | 7 | 07 | - | - | 0x3E0 | 0x000FFFE0 | |
| Co-processor error trap *5 | 8 | 08 | - | - | 0x3DC | 0x000FFFDC | |
| INTE instruction *5 | 9 | 09 | - | - | 0x3D8 | 0x000FFFD8 | |
| Instruction break exception *5 | 10 | 0A | - | - | 0x3D4 | 0x000FFFD4 | |
| Operand break trap *5 | 11 | 0B | - | - | 0x3D0 | 0x000FFFD0 | |
| Step trace trap *5 | 12 | 0C | - | - | 0x3CC | 0x000FFFCC | |
| NMI interrupt (tool)*5 | 13 | 0D | - | - | 0x3C8 | 0x000FFFC8 | |
| Undefined instruction exception | 14 | 0E | - | - | 0x3C4 | 0x000FFFC4 | |
| NMI request | 15 | 0F | $F_H$ fixed | | 0x3C0 | 0x000FFFC0 | |
| External Interrupt 0 | 16 | 10 | ICR00 | 0x440 | 0x3BC | 0x000FFFBC | 0, 16 |
| External Interrupt 1 | 17 | 11 | | | 0x3B8 | 0x000FFFB8 | 1, 17 |
| External Interrupt 2 | 18 | 12 | ICR01 | 0x441 | 0x3B4 | 0x000FFFB4 | 2, 18 |
| External Interrupt 3 | 19 | 13 | | | 0x3B0 | 0x000FFFB0 | 3, 19 |
| External Interrupt 4 | 20 | 14 | ICR02 | 0x442 | 0x3AC | 0x000FFFAC | 20 |
| External Interrupt 5 | 21 | 15 | | | 0x3A8 | 0x000FFFA8 | 21 |
| External Interrupt 6 | 22 | 16 | ICR03 | 0x443 | 0x3A4 | 0x000FFFA4 | 22 |
| External Interrupt 7 | 23 | 17 | | | 0x3A0 | 0x000FFFA0 | 23 |
| External Interrupt 8 | 24 | 18 | ICR04 | 0x444 | 0x39C | 0x000FFF9C | |
| External Interrupt 9 | 25 | 19 | | | 0x398 | 0x000FFF98 | |
| External Interrupt 10 | 26 | 1A | ICR05 | 0x445 | 0x394 | 0x000FFF94 | |
| External Interrupt 11 | 27 | 1B | | | 0x390 | 0x000FFF90 | |
| External Interrupt 12 | 28 | 1C | ICR06 | 0x446 | 0x38C | 0x000FFF8C | |
| External Interrupt 13 | 29 | 1D | | | 0x388 | 0x000FFF88 | |

| Interrupt | Interrupt Number | | Interrupt Level *1 | | Interrupt Vector *2 | | DMA Resource Number |
|---|---|---|---|---|---|---|---|
| | Decimal | Hexa-decimal | Setting Register | Register Address | Offset | Default Vector Address | |
| External Interrupt 14 | 30 | 1E | ICR07 | 0x447 | 0x384 | 0x000FFF84 | |
| Reserved | 31 | 1F | | | 0x380 | 0x000FFF80 | |
| Reload Timer 0 | 32 | 20 | ICR08 | 0x448 | 0x37C | 0x000FFF7C | 4, 32 |
| Reload Timer 1 | 33 | 21 | | | 0x378 | 0x000FFF78 | 5, 33 |
| Reload Timer 2 | 34 | 22 | ICR09 | 0x449 | 0x374 | 0x000FFF74 | 34 |
| Reload Timer 3 | 35 | 23 | | | 0x370 | 0x000FFF70 | 35 |
| Reload Timer 4 | 36 | 24 | ICR10 | 0x44A | 0x36C | 0x000FFF6C | 36 |
| Reload Timer 5 | 37 | 25 | | | 0x368 | 0x000FFF68 | 37 |
| Reload Timer 6 | 38 | 26 | ICR11 | 0x44B | 0x364 | 0x000FFF64 | 38 |
| Reload Timer 7 | 39 | 27 | | | 0x360 | 0x000FFF60 | 39 |
| Free Run Timer 0 | 40 | 28 | ICR12 | 0x44C | 0x35C | 0x000FFF5C | 40 |
| Free Run Timer 1 | 41 | 29 | | | 0x358 | 0x000FFF58 | 41 |
| Free Run Timer 2 | 42 | 2A | ICR13 | 0x44D | 0x354 | 0x000FFF54 | 42 |
| Free Run Timer 3 | 43 | 2B | | | 0x350 | 0x000FFF50 | 43 |
| Free Run Timer 4 | 44 | 2C | ICR14 | 0x44E | 0x34C | 0x000FFF4C | 44 |
| Free Run Timer 5 | 45 | 2D | | | 0x348 | 0x000FFF48 | 45 |
| Free Run Timer 6 | 46 | 2E | ICR15 | 0x44F | 0x344 | 0x000FFF44 | 46 |
| Free Run Timer 7 | 47 | 2F | | | 0x340 | 0x000FFF40 | 47 |
| CAN 0 | 48 | 30 | ICR16 | 0x450 | 0x33C | 0x000FFF3C | |
| CAN 1 | 49 | 31 | | | 0x338 | 0x000FFF38 | |
| CAN 2 | 50 | 32 | ICR17 | 0x451 | 0x334 | 0x000FFF34 | |
| Reserved | 51 | 33 | | | 0x330 | 0x000FFF30 | |
| Reserved | 52 | 34 | ICR18 | 0x452 | 0x32C | 0x000FFF2C | |
| Reserved | 53 | 35 | | | 0x328 | 0x000FFF28 | |
| Reserved | 54 | 36 | ICR19 | 0x453 | 0x324 | 0x000FFF24 | 6, 48 |
| Reserved | 55 | 37 | | | 0x320 | 0x000FFF20 | 7, 49 |
| Reserved | 56 | 38 | ICR20 | 0x454 | 0x31C | 0x000FFF1C | 8, 50 |
| Reserved | 57 | 39 | | | 0x318 | 0x000FFF18 | 9, 51 |
| USART (LIN) 2 RX | 58 | 3A | ICR21 | 0x455 | 0x314 | 0x000FFF14 | 52 |
| USART (LIN) 2 TX | 59 | 3B | | | 0x310 | 0x000FFF10 | 53 |
| Reserved | 60 | 3C | ICR22 | 0x456 | 0x30C | 0x000FFF0C | 54 |
| Reserved | 61 | 3D | | | 0x308 | 0x000FFF08 | 55 |
| System reserved | 62 | 3E | ICR23 *4 | 0x457 | 0x304 | 0x000FFF04 | |
| Delayed Interrupt | 63 | 3F | | | 0x300 | 0x000FFF00 | |
| System reserved *3 | 64 | 40 | (ICR24) | (0x458) | 0x2FC | 0x000FFEFC | |
| System reserved *3 | 65 | 41 | | | 0x2F8 | 0x000FFEF8 | |

| Interrupt | Interrupt Number | | Interrupt Level *1 | | Interrupt Vector *2 | | DMA Resource Number |
|---|---|---|---|---|---|---|---|
| | Decimal | Hexa-decimal | Setting Register | Register Address | Offset | Default Vector Address | |
| USART (LIN, FIFO) 4 RX | 66 | 42 | ICR25 | 0x459 | 0x2F4 | 0x000FFEF4 | 10, 56 |
| USART (LIN, FIFO) 4 TX | 67 | 43 | | | 0x2F0 | 0x000FFEF0 | 11, 57 |
| USART (LIN, FIFO) 5 RX | 68 | 44 | ICR26 | 0x45A | 0x2EC | 0x000FFEEC | 12, 58 |
| USART (LIN, FIFO) 5 TX | 69 | 45 | | | 0x2E8 | 0x000FFEE8 | 13, 59 |
| USART (LIN, FIFO) 6 RX | 70 | 46 | ICR27 | 0x45B | 0x2E4 | 0x000FFEE4 | 60 |
| USART (LIN, FIFO) 6 TX | 71 | 47 | | | 0x2E0 | 0x000FFEE0 | 61 |
| USART (LIN, FIFO) 7 RX | 72 | 48 | ICR28 | 0x45C | 0x2DC | 0x000FFEDC | 62 |
| USART (LIN, FIFO) 7 TX | 73 | 49 | | | 0x2D8 | 0x000FFED8 | 63 |
| $I^2C$ 0 / $I^2C$ 2 | 74 | 4A | ICR29 | 0x45D | 0x2D4 | 0x000FFED4 | |
| $I^2C$ 3 | 75 | 4B | | | 0x2D0 | 0x000FFED0 | |
| Reserved | 76 | 4C | ICR30 | 0x45E | 0x2CC | 0x000FFECC | 64 |
| Reserved | 77 | 4D | | | 0x2C8 | 0x000FFEC8 | 65 |
| Reserved | 78 | 4E | ICR31 | 0x45F | 0x2C4 | 0x000FFEC4 | 66 |
| Reserved | 79 | 4F | | | 0x2C0 | 0x000FFEC0 | 67 |
| Reserved | 80 | 50 | ICR32 | 0x460 | 0x2BC | 0x000FFEBC | 68 |
| Reserved | 81 | 51 | | | 0x2B8 | 0x000FFEB8 | 69 |
| Reserved | 82 | 52 | ICR33 | 0x461 | 0x2B4 | 0x000FFEB4 | 70 |
| Reserved | 83 | 53 | | | 0x2B0 | 0x000FFEB0 | 71 |
| Reserved | 84 | 54 | ICR34 | 0x462 | 0x2AC | 0x000FFEAC | 72 |
| Reserved | 85 | 55 | | | 0x2A8 | 0x000FFEA8 | 73 |
| Reserved | 86 | 56 | ICR35 | 0x463 | 0x2A4 | 0x000FFEA4 | 74 |
| Reserved | 87 | 57 | | | 0x2A0 | 0x000FFEA0 | 75 |
| Reserved | 88 | 58 | ICR36 | 0x464 | 0x29C | 0x000FFE9C | 76 |
| Reserved | 89 | 59 | | | 0x298 | 0x000FFE98 | 77 |
| Reserved | 90 | 5A | ICR37 | 0x465 | 0x294 | 0x000FFE94 | 78 |
| Reserved | 91 | 5B | | | 0x290 | 0x000FFE90 | 79 |
| Input Capture 0 | 92 | 5C | ICR38 | 0x466 | 0x28C | 0x000FFE8C | 80 |
| Input Capture 1 | 93 | 5D | | | 0x288 | 0x000FFE88 | 81 |
| Input Capture 2 | 94 | 5E | ICR39 | 0x467 | 0x284 | 0x000FFE84 | 82 |
| Input Capture 3 | 95 | 5F | | | 0x280 | 0x000FFE80 | 83 |
| Input Capture 4 | 96 | 60 | ICR40 | 0x468 | 0x27C | 0x000FFE7C | 84 |
| Input Capture 5 | 97 | 61 | | | 0x278 | 0x000FFE78 | 85 |
| Input Capture 6 | 98 | 62 | ICR41 | 0x469 | 0x274 | 0x000FFE74 | 86 |
| Input Capture 7 | 99 | 63 | | | 0x270 | 0x000FFE70 | 87 |
| Output Compare 0 | 100 | 64 | ICR42 | 0x46A | 0x26C | 0x000FFE6C | 88 |
| Output Compare 1 | 101 | 65 | | | 0x268 | 0x000FFE68 | 89 |

| Interrupt | Interrupt Number | | Interrupt Level *1 | | Interrupt Vector *2 | | DMA Resource Number |
|---|---|---|---|---|---|---|---|
| | Decimal | Hexa-decimal | Setting Register | Register Address | Offset | Default Vector Address | |
| Output Compare 2 | 102 | 66 | ICR43 | 0x46B | 0x264 | 0x000FFE64 | 90 |
| Output Compare 3 | 103 | 67 | | | 0x260 | 0x000FFE60 | 91 |
| Reserved | 104 | 68 | ICR44 | 0x46C | 0x25C | 0x000FFE5C | 92 |
| Reserved | 105 | 69 | | | 0x258 | 0x000FFE58 | 93 |
| Reserved | 106 | 6A | ICR45 | 0x46D | 0x254 | 0x000FFE54 | 94 |
| Reserved | 107 | 6B | | | 0x250 | 0x000FFE50 | 95 |
| Sound Generator | 108 | 6C | ICR46 | 0x46E | 0x24C | 0x000FFE4C | |
| Phase Frequ. Modulator | 109 | 6D | | | 0x248 | 0x000FFE48 | |
| System reserved | 110 | 6E | ICR47 *4 | 0x46F | 0x244 | 0x000FFE44 | |
| System reserved | 111 | 6F | | | 0x240 | 0x000FFE40 | |
| Reserved | 112 | 70 | ICR48 | 0x470 | 0x23C | 0x000FFE3C | 15, 96 |
| Reserved | 113 | 71 | | | 0x238 | 0x000FFE38 | 97 |
| Reserved | 114 | 72 | ICR49 | 0x471 | 0x234 | 0x000FFE34 | 98 |
| Reserved | 115 | 73 | | | 0x230 | 0x000FFE30 | 99 |
| Prog. Pulse Gen. 4 | 116 | 74 | ICR50 | 0x472 | 0x22C | 0x000FFE2C | 100 |
| Prog. Pulse Gen. 5 | 117 | 75 | | | 0x228 | 0x000FFE28 | 101 |
| Prog. Pulse Gen. 6 | 118 | 76 | ICR51 | 0x473 | 0x224 | 0x000FFE24 | 102 |
| Prog. Pulse Gen. 7 | 119 | 77 | | | 0x220 | 0x000FFE20 | 103 |
| Prog. Pulse Gen. 8 | 120 | 78 | ICR52 | 0x474 | 0x21C | 0x000FFE1C | 104 |
| Prog. Pulse Gen. 9 | 121 | 79 | | | 0x218 | 0x000FFE18 | 105 |
| Prog. Pulse Gen. 10 | 122 | 7A | ICR53 | 0x475 | 0x214 | 0x000FFE14 | 106 |
| Prog. Pulse Gen. 11 | 123 | 7B | | | 0x210 | 0x000FFE10 | 107 |
| Prog. Pulse Gen. 12 | 124 | 7C | ICR54 | 0x476 | 0x20C | 0x000FFE0C | 108 |
| Prog. Pulse Gen. 13 | 125 | 7D | | | 0x208 | 0x000FFE08 | 109 |
| Prog. Pulse Gen. 14 | 126 | 7E | ICR55 | 0x477 | 0x204 | 0x000FFE04 | 110 |
| Prog. Pulse Gen. 15 | 127 | 7F | | | 0x200 | 0x000FFE00 | 111 |
| Up/Down Counter 0 | 128 | 80 | ICR56 | 0x478 | 0x1FC | 0x000FFDFC | |
| Reserved | 129 | 81 | | | 0x1F8 | 0x000FFDF8 | |
| Up/Down Counter 2 | 130 | 82 | ICR57 | 0x479 | 0x1F4 | 0x000FFDF4 | |
| Up/Down Counter 3 | 131 | 83 | | | 0x1F0 | 0x000FFDF0 | |
| Real Time Clock | 132 | 84 | ICR58 | 0x47A | 0x1EC | 0x000FFDEC | |
| Calibration Unit | 133 | 85 | | | 0x1E8 | 0x000FFDE8 | |
| A/D Converter 0 | 134 | 86 | ICR59 | 0x47B | 0x1E4 | 0x000FFDE4 | 14, 112 |
| Reserved | 135 | 87 | | | 0x1E0 | 0x000FFDE0 | |
| Alarm Comparator 0 | 136 | 88 | ICR60 | 0x47C | 0x1DC | 0x000FFDDC | |
| Reserved | 137 | 89 | | | 0x1D8 | 0x000FFDD8 | |

| Interrupt | Interrupt Number | | Interrupt Level *1 | | Interrupt Vector *2 | | DMA Resource Number |
|---|---|---|---|---|---|---|---|
| | Decimal | Hexa-decimal | Setting Register | Register Address | Offset | Default Vector Address | |
| Low Voltage Detection | 138 | 8A | ICR61 | 0x47D | 0x1D4 | 0x000FFDD4 | |
| Reserved | 139 | 8B | | | 0x1D0 | 0x000FFDD0 | |
| Timebase Overflow | 140 | 8C | ICR62 | 0x47E | 0x1CC | 0x000FFDCC | |
| PLL Clock Gear | 141 | 8D | | | 0x1C8 | 0x000FFDC8 | |
| DMA Controller | 142 | 8E | ICR63 | 0x47F | 0x1C4 | 0x000FFDC4 | |
| Main/Sub OSC stability wait | 143 | 8F | | | 0x1C0 | 0x000FFDC0 | |
| Security vector | 144 | 90 | - | - | 0x1BC | 0x000FFDBC | |
| Used by the INT instruction. | 145 to 255 | 91 to FF | - | - | 0x1B8 to 0x000 | 0x000FFDB8 to 0x000FFC00 | |

Notes:

*1: The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.
*2:The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset. After execution of the internal boot ROM TBR is set to 0x000FFC00.
*3: Used by REALOS
*4: ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0x0C03 : IOS[0])
*5: System reserved
*6: Memory Protection Unit (MPU) support

# 14. Recommended Settings

## 14.1 PLL and Clockgear Settings

Please note that for CY91F460C series the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

**Recommended PLL Divider and Clockgear Settings**

| PLL Input (CLK) [MHz] | Frequency Parameter | | Clockgear Parameter | | PLL Output (X) [MHz] | Core Base Clock [MHz] | Remarks |
|---|---|---|---|---|---|---|---|
| | DIVM | DIVN | DIVG | MULG | MULG | | |
| 4 | 2 | 25 | 16 | 24 | 200 | 100 | |
| 4 | 2 | 24 | 16 | 24 | 192 | 96 | |
| 4 | 2 | 23 | 16 | 24 | 184 | 92 | |
| 4 | 2 | 22 | 16 | 24 | 176 | 88 | |
| 4 | 2 | 21 | 16 | 20 | 168 | 84 | |
| 4 | 2 | 20 | 16 | 20 | 160 | 80 | |
| 4 | 2 | 19 | 16 | 20 | 152 | 76 | |
| 4 | 2 | 18 | 16 | 20 | 144 | 72 | |
| 4 | 2 | 17 | 16 | 16 | 136 | 68 | |
| 4 | 2 | 16 | 16 | 16 | 128 | 64 | |
| 4 | 2 | 15 | 16 | 16 | 120 | 60 | |
| 4 | 2 | 14 | 16 | 16 | 112 | 56 | |
| 4 | 2 | 13 | 16 | 12 | 104 | 52 | |
| 4 | 2 | 12 | 16 | 12 | 96 | 48 | |
| 4 | 2 | 11 | 16 | 12 | 88 | 44 | |
| 4 | 4 | 10 | 16 | 24 | 160 | 40 | |
| 4 | 4 | 9 | 16 | 24 | 144 | 36 | |
| 4 | 4 | 8 | 16 | 24 | 128 | 32 | |
| 4 | 4 | 7 | 16 | 24 | 112 | 28 | |
| 4 | 6 | 6 | 16 | 24 | 144 | 24 | |
| 4 | 8 | 5 | 16 | 28 | 160 | 20 | |
| 4 | 10 | 4 | 16 | 32 | 160 | 16 | |
| 4 | 12 | 3 | 16 | 32 | 144 | 12 | |

## 14.2 Clock Modulator Settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

**Clock Modulator Settings, Frequency Range and Supported Supply Voltage**

| Modulation Degree (k) | Random No (N) | CMPR [hex] | Baseclk [MHz] | Fmin [MHz] | Fmax [MHz] |
|---|---|---|---|---|---|
| 1 | 3 | 026F | 88 | 79.5 | 98.5 |
| 1 | 3 | 026F | 84 | 76.1 | 93.8 |
| 1 | 3 | 026F | 80 | 72.6 | 89.1 |
| 1 | 5 | 02AE | 80 | 68.7 | 95.8 |
| 2 | 3 | 046E | 80 | 68.7 | 95.8 |
| 1 | 3 | 026F | 76 | 69.1 | 84.5 |
| 1 | 5 | 02AE | 76 | 65.3 | 90.8 |
| 1 | 7 | 02ED | 76 | 62 | 98.1 |
| 2 | 3 | 046E | 76 | 65.3 | 90.8 |
| 3 | 3 | 066D | 76 | 62 | 98.1 |
| 1 | 3 | 026F | 72 | 65.5 | 79.9 |
| 1 | 5 | 02AE | 72 | 62 | 85.8 |
| 1 | 7 | 02ED | 72 | 58.8 | 92.7 |
| 2 | 3 | 046E | 72 | 62 | 85.8 |
| 3 | 3 | 066D | 72 | 58.8 | 92.7 |
| 1 | 3 | 026F | 68 | 62 | 75.3 |
| 1 | 5 | 02AE | 68 | 58.7 | 80.9 |
| 1 | 7 | 02ED | 68 | 55.7 | 87.3 |
| 1 | 9 | 032C | 68 | 53 | 95 |
| 2 | 3 | 046E | 68 | 58.7 | 80.9 |
| 2 | 5 | 04AC | 68 | 53 | 95 |
| 3 | 3 | 066D | 68 | 55.7 | 87.3 |
| 4 | 3 | 086C | 68 | 53 | 95 |
| 1 | 3 | 026F | 64 | 58.5 | 70.7 |
| 1 | 5 | 02AE | 64 | 55.3 | 75.9 |
| 1 | 7 | 02ED | 64 | 52.5 | 82 |
| 1 | 9 | 032C | 64 | 49.9 | 89.1 |
| 1 | 11 | 036B | 64 | 47.6 | 97.6 |
| 2 | 3 | 046E | 64 | 55.3 | 75.9 |
| 2 | 5 | 04AC | 64 | 49.9 | 89.1 |
| 3 | 3 | 066D | 64 | 52.5 | 82 |
| 4 | 3 | 086C | 64 | 49.9 | 89.1 |
| 5 | 3 | 0A6B | 64 | 47.6 | 97.6 |

| Modulation Degree (k) | Random No (N) | CMPR [hex] | Baseclk [MHz] | Fmin [MHz] | Fmax [MHz] |
|---|---|---|---|---|---|
| 1 | 3 | 026F | 60 | 54.9 | 66.1 |
| 1 | 5 | 02AE | 60 | 51.9 | 71 |
| 1 | 7 | 02ED | 60 | 49.3 | 76.7 |
| 1 | 9 | 032C | 60 | 46.9 | 83.3 |
| 1 | 11 | 036B | 60 | 44.7 | 91.3 |
| 2 | 3 | 046E | 60 | 51.9 | 71 |
| 2 | 5 | 04AC | 60 | 46.9 | 83.3 |
| 3 | 3 | 066D | 60 | 49.3 | 76.7 |
| 4 | 3 | 086C | 60 | 46.9 | 83.3 |
| 5 | 3 | 0A6B | 60 | 44.7 | 91.3 |
| 1 | 3 | 026F | 56 | 51.4 | 61.6 |
| 1 | 5 | 02AE | 56 | 48.6 | 66.1 |
| 1 | 7 | 02ED | 56 | 46.1 | 71.4 |
| 1 | 9 | 032C | 56 | 43.8 | 77.6 |
| 1 | 11 | 036B | 56 | 41.8 | 84.9 |
| 1 | 13 | 03AA | 56 | 39.9 | 93.8 |
| 2 | 3 | 046E | 56 | 48.6 | 66.1 |
| 2 | 5 | 04AC | 56 | 43.8 | 77.6 |
| 2 | 7 | 04EA | 56 | 39.9 | 93.8 |
| 3 | 3 | 066D | 56 | 46.1 | 71.4 |
| 3 | 5 | 06AA | 56 | 39.9 | 93.8 |
| 4 | 3 | 086C | 56 | 43.8 | 77.6 |
| 5 | 3 | 0A6B | 56 | 41.8 | 84.9 |
| 6 | 3 | 0C6A | 56 | 39.9 | 93.8 |
| 1 | 3 | 026F | 52 | 47.8 | 57 |
| 1 | 5 | 02AE | 52 | 45.2 | 61.2 |
| 1 | 7 | 02ED | 52 | 42.9 | 66.1 |
| 1 | 9 | 032C | 52 | 40.8 | 71.8 |
| 1 | 11 | 036B | 52 | 38.8 | 78.6 |
| 1 | 13 | 03AA | 52 | 37.1 | 86.8 |
| 1 | 15 | 03E9 | 52 | 35.5 | 96.9 |
| 2 | 3 | 046E | 52 | 45.2 | 61.2 |
| 2 | 5 | 04AC | 52 | 40.8 | 71.8 |
| 2 | 7 | 04EA | 52 | 37.1 | 86.8 |
| 3 | 3 | 066D | 52 | 42.9 | 66.1 |
| 3 | 5 | 06AA | 52 | 37.1 | 86.8 |
| 4 | 3 | 086C | 52 | 40.8 | 71.8 |

| Modulation Degree (k) | Random No (N) | CMPR [hex] | Baseclk [MHz] | Fmin [MHz] | Fmax [MHz] |
|---|---|---|---|---|---|
| 5 | 3 | 0A6B | 52 | 38.8 | 78.6 |
| 6 | 3 | 0C6A | 52 | 37.1 | 86.8 |
| 7 | 3 | 0E69 | 52 | 35.5 | 96.9 |
| 1 | 3 | 026F | 48 | 44.2 | 52.5 |
| 1 | 5 | 02AE | 48 | 41.8 | 56.4 |
| 1 | 7 | 02ED | 48 | 39.6 | 60.9 |
| 1 | 9 | 032C | 48 | 37.7 | 66.1 |
| 1 | 11 | 036B | 48 | 35.9 | 72.3 |
| 1 | 13 | 03AA | 48 | 34.3 | 79.9 |
| 1 | 15 | 03E9 | 48 | 32.8 | 89.1 |
| 2 | 3 | 046E | 48 | 41.8 | 56.4 |
| 2 | 5 | 04AC | 48 | 37.7 | 66.1 |
| 2 | 7 | 04EA | 48 | 34.3 | 79.9 |
| 3 | 3 | 066D | 48 | 39.6 | 60.9 |
| 3 | 5 | 06AA | 48 | 34.3 | 79.9 |
| 4 | 3 | 086C | 48 | 37.7 | 66.1 |
| 5 | 3 | 0A6B | 48 | 35.9 | 72.3 |
| 6 | 3 | 0C6A | 48 | 34.3 | 79.9 |
| 7 | 3 | 0E69 | 48 | 32.8 | 89.1 |
| 1 | 3 | 026F | 44 | 40.6 | 48.1 |
| 1 | 5 | 02AE | 44 | 38.4 | 51.6 |
| 1 | 7 | 02ED | 44 | 36.4 | 55.7 |
| 1 | 9 | 032C | 44 | 34.6 | 60.4 |
| 1 | 11 | 036B | 44 | 33 | 66.1 |
| 1 | 13 | 03AA | 44 | 31.5 | 73 |
| 1 | 15 | 03E9 | 44 | 30.1 | 81.4 |
| 2 | 3 | 046E | 44 | 38.4 | 51.6 |
| 2 | 5 | 04AC | 44 | 34.6 | 60.4 |
| 2 | 7 | 04EA | 44 | 31.5 | 73 |
| 2 | 9 | 0528 | 44 | 28.9 | 92.1 |
| 3 | 3 | 066D | 44 | 36.4 | 55.7 |
| 3 | 5 | 06AA | 44 | 31.5 | 73 |
| 4 | 3 | 086C | 44 | 34.6 | 60.4 |
| 4 | 5 | 08A8 | 44 | 28.9 | 92.1 |
| 5 | 3 | 0A6B | 44 | 33 | 66.1 |
| 6 | 3 | 0C6A | 44 | 31.5 | 73 |
| 7 | 3 | 0E69 | 44 | 30.1 | 81.4 |

| Modulation Degree (k) | Random No (N) | CMPR [hex] | Baseclk [MHz] | Fmin [MHz] | Fmax [MHz] |
|---|---|---|---|---|---|
| 8 | 3 | 1068 | 44 | 28.9 | 92.1 |
| 1 | 3 | 026F | 40 | 37 | 43.6 |
| 1 | 5 | 02AE | 40 | 34.9 | 46.8 |
| 1 | 7 | 02ED | 40 | 33.1 | 50.5 |
| 1 | 9 | 032C | 40 | 31.5 | 54.8 |
| 1 | 11 | 036B | 40 | 30 | 59.9 |
| 1 | 13 | 03AA | 40 | 28.7 | 66.1 |
| 1 | 15 | 03E9 | 40 | 27.4 | 73.7 |
| 2 | 3 | 046E | 40 | 34.9 | 46.8 |
| 2 | 5 | 04AC | 40 | 31.5 | 54.8 |
| 2 | 7 | 04EA | 40 | 28.7 | 66.1 |
| 2 | 9 | 0528 | 40 | 26.3 | 83.3 |
| 3 | 3 | 066D | 40 | 33.1 | 50.5 |
| 3 | 5 | 06AA | 40 | 28.7 | 66.1 |
| 3 | 7 | 06E7 | 40 | 25.3 | 95.8 |
| 4 | 3 | 086C | 40 | 31.5 | 54.8 |
| 4 | 5 | 08A8 | 40 | 26.3 | 83.3 |
| 5 | 3 | 0A6B | 40 | 30 | 59.9 |
| 6 | 3 | 0C6A | 40 | 28.7 | 66.1 |
| 7 | 3 | 0E69 | 40 | 27.4 | 73.7 |
| 8 | 3 | 1068 | 40 | 26.3 | 83.3 |
| 9 | 3 | 1267 | 40 | 25.3 | 95.8 |
| 1 | 3 | 026F | 36 | 33.3 | 39.2 |
| 1 | 5 | 02AE | 36 | 31.5 | 42 |
| 1 | 7 | 02ED | 36 | 29.9 | 45.3 |
| 1 | 9 | 032C | 36 | 28.4 | 49.2 |
| 1 | 11 | 036B | 36 | 27.1 | 53.8 |
| 1 | 13 | 03AA | 36 | 25.8 | 59.3 |
| 1 | 15 | 03E9 | 36 | 24.7 | 66.1 |
| 2 | 3 | 046E | 36 | 31.5 | 42 |
| 2 | 5 | 04AC | 36 | 28.4 | 49.2 |
| 2 | 7 | 04EA | 36 | 25.8 | 59.3 |
| 2 | 9 | 0528 | 36 | 23.7 | 74.7 |
| 3 | 3 | 066D | 36 | 29.9 | 45.3 |
| 3 | 5 | 06AA | 36 | 25.8 | 59.3 |
| 3 | 7 | 06E7 | 36 | 22.8 | 85.8 |
| 4 | 3 | 086C | 36 | 28.4 | 49.2 |

| Modulation Degree (k) | Random No (N) | CMPR [hex] | Baseclk [MHz] | Fmin [MHz] | Fmax [MHz] |
|---|---|---|---|---|---|
| 4 | 5 | 08A8 | 36 | 23.7 | 74.7 |
| 5 | 3 | 0A6B | 36 | 27.1 | 53.8 |
| 6 | 3 | 0C6A | 36 | 25.8 | 59.3 |
| 7 | 3 | 0E69 | 36 | 24.7 | 66.1 |
| 8 | 3 | 1068 | 36 | 23.7 | 74.7 |
| 9 | 3 | 1267 | 36 | 22.8 | 85.8 |
| 1 | 3 | 026F | 32 | 29.7 | 34.7 |
| 1 | 5 | 02AE | 32 | 28 | 37.3 |
| 1 | 7 | 02ED | 32 | 26.6 | 40.2 |
| 1 | 9 | 032C | 32 | 25.3 | 43.6 |
| 1 | 11 | 036B | 32 | 24.1 | 47.7 |
| 1 | 13 | 03AA | 32 | 23 | 52.5 |
| 1 | 15 | 03E9 | 32 | 22 | 58.6 |
| 2 | 3 | 046E | 32 | 28 | 37.3 |
| 2 | 5 | 04AC | 32 | 25.3 | 43.6 |
| 2 | 7 | 04EA | 32 | 23 | 52.5 |
| 2 | 9 | 0528 | 32 | 21.1 | 66.1 |
| 2 | 11 | 0566 | 32 | 19.5 | 89.1 |
| 3 | 3 | 066D | 32 | 26.6 | 40.2 |
| 3 | 5 | 06AA | 32 | 23 | 52.5 |
| 3 | 7 | 06E7 | 32 | 20.3 | 75.9 |
| 4 | 3 | 086C | 32 | 25.3 | 43.6 |
| 4 | 5 | 08A8 | 32 | 21.1 | 66.1 |
| 5 | 3 | 0A6B | 32 | 24.1 | 47.7 |
| 5 | 5 | 0AA6 | 32 | 19.5 | 89.1 |
| 6 | 3 | 0C6A | 32 | 23 | 52.5 |
| 7 | 3 | 0E69 | 32 | 22 | 58.6 |
| 8 | 3 | 1068 | 32 | 21.1 | 66.1 |
| 9 | 3 | 1267 | 32 | 20.3 | 75.9 |
| 10 | 3 | 1466 | 32 | 19.5 | 89.1 |

# 15. Electrical Characteristics

## 15.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply slew rate | — | — | 50 | V/ms | |
| Power supply voltage 1*1 | $V_{DD}5R$ | − 0.3 | + 6.0 | V | |
| Power supply voltage 2*1 | $V_{DD}5$ | − 0.3 | + 6.0 | V | |
| Power supply voltage 3*1 | $HV_{DD}5$ | − 0.3 | + 6.0 | V | |
| Relationship of the supply voltages | $HV_{DD}5$ | $V_{DD}5$-0.3 | $V_{DD}5$+0.3 | V | SMC mode |
| | | $V_{SS}5$-0.3 | $V_{DD}5$+0.3 | V | General purpose port mode |
| | $AV_{CC}5$ | $V_{DD}5$-0.3 | $V_{DD}5$+0.3 | V | At least one pin of the Ports 25 to 29 (SMC, ANn) is used as digital input or output. |
| | | $V_{SS}5$-0.3 | $V_{DD}5$+0.3 | V | All pins of the Ports 25 to 29 (SMC, ANn) follow the condition of $V_{IA}$ |
| Analog power supply voltage*1 | $AV_{CC}5$ | − 0.3 | + 6.0 | V | *2 |
| Analog reference power supply voltage*1 | AVRH | − 0.3 | + 6.0 | V | *2 |
| Input voltage 1*1 | $V_{I1}$ | Vss5 − 0.3 | $V_{DD}5$ + 0.3 | V | |
| Input voltage 3*1 | $V_{I3}$ | HVss5 − 0.3 | $HV_{DD}5$ + 0.3 | V | Stepper motor controller |
| Analog pin input voltage*1 | $V_{IA}$ | AVss5 − 0.3 | AVcc5 + 0.3 | V | |
| Output voltage 1*1 | $V_{O1}$ | Vss5 − 0.3 | $V_{DD}5$ + 0.3 | V | |
| Output voltage 3*1 | $V_{O3}$ | HVss5 − 0.3 | $HV_{DD}5$ + 0.3 | V | Stepper motor controller |
| Maximum clamp current | $I_{CLAMP}$ | − 4.0 | + 4.0 | mA | *3 |
| Total maximum clamp current | $\Sigma \lvert I_{CLAMP} \rvert$ | — | 20 | mA | *3 |
| “L” level maximum output current*4 | $I_{OL}$ | — | 10 | mA | |
| | | — | 40 | mA | Stepper motor controller |
| “L” level average output current*5 | $I_{OLAV}$ | — | 8 | mA | |
| | | — | 30 | mA | Stepper motor controller |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| | | — | 360 | mA | Stepper motor controller |
| “L” level total average output current*6 | $\Sigma I_{OLAV}$ | — | 50 | mA | |
| | | — | 230 | mA | Stepper motor controller |
| “H” level maximum output current*4 | $I_{OH}$ | — | − 10 | mA | |
| | | — | − 40 | mA | Stepper motor controller |
| “H” level average output current*5 | $I_{OHAV}$ | — | − 4 | mA | |
| | | — | − 30 | mA | Stepper motor controller |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | − 100 | mA | |
| | | — | − 360 | mA | Stepper motor controller |

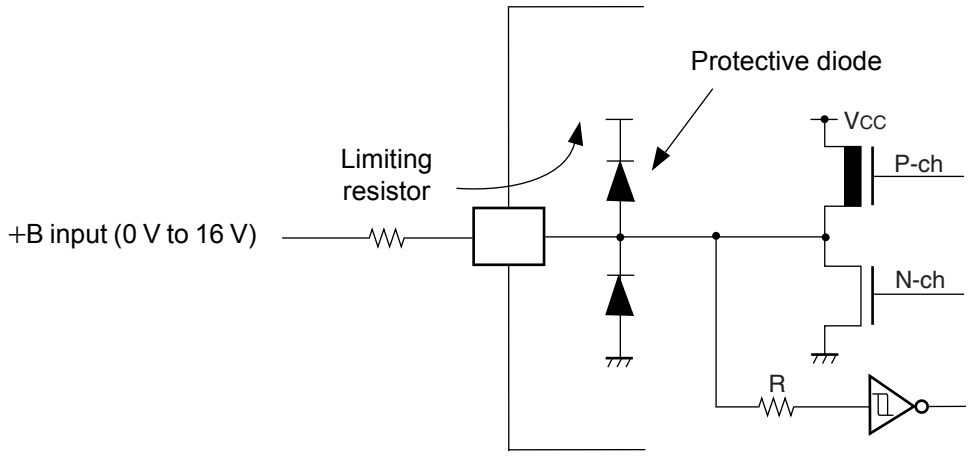
| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| "H" level total average output current*6 | $\Sigma I_{OHAV}$ | — | − 25 | mA | |
| | | — | − 230 | mA | Stepper motor controller |
| Power consumption | $P_D$ | — | 1000 | mW | |
| Operating temperature | $T_A$ | − 40 | + 105 | °C | |
| Storage temperature | Tstg | − 55 | + 150 | °C | |

*1 : The parameter is based on $V_{SS}5 = HV_{SS}5 = AV_{SS}5 = 0.0$ V.

*2 : $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V.

*3 :
- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time , either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit :

**Input/Output Equivalent Circuit**




*4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

*6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

WARNING:Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 15.2 Recommended Operating Conditions

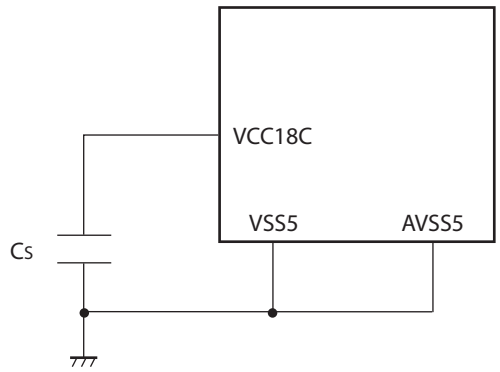
($V_{SS}5 = AV_{SS}5 = 0.0$ V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{DD}5$ | 3.0 | — | 5.5 | V | |
| | $V_{DD}5R$ | 3.0 | — | 5.5 | V | Internal regulator |
| | $HV_{DD}5$ | 4.5 | — | 5.5 | V | Stepper motor controller |
| | | 3.0 | — | 5.5 | V | Stepper motor controller (when all pins are used as general-purpose ports) |
| | $AV_{CC}5$ | 3.0 | — | 5.5 | V | A/D converter |
| Smoothing capacitor at VCC18C pin | $C_S$ | — | 4.7 | — | µF | Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics. |
| Power supply slew rate | — | — | — | 50 | V/ms | |
| Operating temperature | $T_A$ | − 40 | — | + 105 | °C | |
| Stepper motor control slew rate | — | — | 40 | — | ns | Cload = 0 pF |
| Main Oscillation stabilisation time | — | 10 | — | — | ms | |
| Lock-up time PLL (4 MHz ->16 ...100MHz) | — | — | — | 0.6 | ms | |
| ESD Protection (Human body model) | $V_{surge}$ | 2 | — | — | kV | $R_{discharge}$ = 1.5kΩ<br>$C_{discharge}$ = 100pF |
| RC Oscillator | $f_{RC100kHz}$<br>$f_{RC2MHz}$ | 50<br>1 | 100<br>2 | 200<br>4 | kHz<br>MHz | $VDD_{CORE}$≥1.65V |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.



## 15.3 DC Characteristics

Note: In the following tables, "$V_{DD}$" means $HV_{DD}5$ for SMC pins or $V_{DD}5$ for other pins.
In the following tables, "$V_{SS}$" means Hvss5 for ground Pins of the stepper motor and $V_{SS}5$ for the other pins.

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input "H" voltage | $V_{IH}$ | — | Port inputs if CMOS Hysteresis 0.8/0.2 input is selected | $0.8 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | CMOS hysteresis input |
| | | — | Port inputs if CMOS Hysteresis 0.7/0.3 input is selected | $0.7 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V |
| | | | | $0.74 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | 3 V ≤ $V_{DD}$ ≤ 4.5 V |
| | | — | AUTOMOTIVE Hysteresis input is selected | $0.8 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | |
| | | — | Port inputs if TTL input is selected | 2.0 | — | $V_{DD} + 0.3$ | V | |
| | $V_{IHR}$ | INITX | — | $0.8 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | INITX input pin (CMOS Hysteresis) |
| | $V_{IHM}$ | MD_3 to MD_0 | — | $V_{DD} - 0.3$ | — | $V_{DD} + 0.3$ | V | Mode input pins |
| | $V_{IHX0S}$ | X0, X0A | — | 2.5 | — | $V_{DD} + 0.3$ | V | External clock in "Oscillation mode" |
| | $V_{IHX0F}$ | X0 | — | $0.8 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | External clock in "Fast Clock Input mode" |
| Input "L" voltage | $V_{IL}$ | — | Port inputs if CMOS Hysteresis 0.8/0.2 input is selected | $V_{SS} - 0.3$ | — | $0.2 \times V_{DD}$ | V | |
| | | — | Port inputs if CMOS Hysteresis 0.7/0.3 input is selected | $V_{SS} - 0.3$ | — | $0.3 \times V_{DD}$ | V | |
| | | — | Port inputs if AUTOMOTIVE Hysteresis input is selected | $V_{SS} - 0.3$ | — | $0.5 \times V_{DD}$ | V | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V |
| | | | | $V_{SS} - 0.3$ | — | $0.46 \times V_{DD}$ | V | 3 V ≤ $V_{DD}$ ≤ 4.5 V |
| | | — | Port inputs if TTL input is selected | $V_{SS} - 0.3$ | — | 0.8 | V | |
| | $V_{ILR}$ | INITX | — | $V_{SS} - 0.3$ | — | $0.2 \times V_{DD}$ | V | INITX input pin (CMOS Hysteresis) |
| | $V_{ILM}$ | MD_3 to MD_0 | — | $V_{SS} - 0.3$ | — | $V_{SS} + 0.3$ | V | Mode input pins |
| | $V_{ILXDS}$ | X0, X0A | — | $V_{SS} - 0.3$ | — | 0.5 | V | External clock in "Oscillation mode" |

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input “L” voltage | $V_{ILXDF}$ | X0 | — | $V_{SS} - 0.3$ | — | $0.2 \times V_{DD}$ | V | External clock in “Fast Clock Input mode” |
| Output “H” voltage | $V_{OH2}$ | Normal outputs | $4.5V \le V_{DD} \le 5.5V$, $I_{OH} = -2mA$ | $V_{DD} - 0.5$ | — | — | V | Driving strength set to 2 mA |
| | | | $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = -1.6mA$ | | | | | |
| | $V_{OH5}$ | Normal outputs | $4.5V \le V_{DD} \le 5.5V$, $I_{OH} = -5mA$ | $V_{DD} - 0.5$ | — | — | V | Driving strength set to 5 mA |
| | | | $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = -3mA$ | | | | | |
| | $V_{OH3}$ | $I^2C$ outputs | $3.0V \le V_{DD} \le 5.5V$, $I_{OH} = -3mA$ | $V_{DD} - 0.5$ | — | — | V | |
| | $V_{OH30}$ | High current outputs | $4.5V \le V_{DD} \le 5.5V$, $T_A$ = -40°C, $I_{OH}$ = -40mA | $V_{DD} - 0.5$ | — | — | V | Driving strength set to 30mA |
| | | | $4.5V \le V_{DD} \le 5.5V$, $I_{OH}$ = -30mA | | | | | |
| | | | $3.0V \le V_{DD} \le 4.5V$, $I_{OH}$ = -20mA | | | | | |
| Output “L” voltage | $V_{OL2}$ | Normal outputs | $4.5V \le V_{DD} \le 5.5V$, $I_{OH} = +2mA$ | — | — | 0.4 | V | Driving strength set to 2 mA |
| | | | $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = +1.6mA$ | | | | | |
| | $V_{OL5}$ | Normal outputs | $4.5V \le V_{DD} \le 5.5V$, $I_{OH} = +5mA$ | — | — | 0.4 | V | Driving strength set to 5 mA |
| | | | $3.0V \le V_{DD} \le 4.5V$, $I_{OH} = +3mA$ | | | | | |
| | $V_{OL3}$ | $I^2C$ outputs | $3.0V \le V_{DD} \le 5.5V$, $I_{OH} = +3mA$ | — | — | 0.4 | V | |
| | $V_{OL30}$ | High current outputs | $4.5V \le V_{DD} \le 5.5V$, $T_A$ = -40°C, $I_{OH}$ = +40mA | — | — | 0.5 | V | Driving strength set to 30mA |
| | | | $4.5V \le V_{DD} \le 5.5V$, $I_{OH}$ = +30mA | | | | | |
| | | | $3.0V \le V_{DD} \le 4.5V$, $I_{OH}$ = +20mA | | | | | |
| Input leakage current | $I_{IL}$ | Pnn_m *1 | $3.0V \le V_{DD} \le 5.5V$ $V_{SS}5 < V_I < V_{DD}$ $T_A$=25 °C | $-1$ | — | $+1$ | µA | |
| | | | $3.0V \le V_{DD} \le 5.5V$ $V_{SS}5 < V_I < V_{DD}$ $T_A$=105 °C | $-3$ | — | $+3$ | | |

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Analog input leakage current | $I_{AIN}$ | ANn *2 | 3.0V ≤ $V_{DD}$ ≤ 5.5V<br>$T_A$=25 °C | − 1 | — | + 1 | µA | |
| | | | 3.0V ≤ $V_{DD}$ ≤ 5.5V<br>$T_A$=105 °C | − 3 | — | + 3 | µA | |
| Pull-up resistance | $R_{UP}$ | Pnn_m*3 , INITX | 3.0V ≤ $V_{DD}$ ≤ 3.6V | 40 | 100 | 160 | kΩ | |
| | | | 4.5V ≤ $V_{DD}$ ≤ 5.5V | 25 | 50 | 100 | | |
| Pull-down resistance | $R_{DOWN}$ | Pnn_m*4 | 3.0V ≤ $V_{DD}$ ≤ 3.6V | 40 | 100 | 180 | kΩ | |
| | | | 4.5V ≤ $V_{DD}$ ≤ 5.5V | 25 | 50 | 100 | | |
| Input capacitance | $C_{IN}$ | All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}$, AVRH5 | f = 1 MHz | — | 5 | 15 | pF | |
| Power supply current<br><br>CY91-F467Cx | $I_{CC}$ | $V_{DD}5R$ | CY91F467Cx:<br>CLKB: 100 MHz<br>CLKP: 50 MHz<br>CLKT: 50 MHz<br>CLKCAN: 50 MHz | — | 120 | 150 | mA | Code fetch from Flash |
| | $I_{CCH}$ | $V_{DD}5R$ | $T_A$ = + 25 °C | — | 30 | 150 | µA | At stop mode *5 |
| | | | $T_A$ = + 105 °C | — | 400 | 2000 | µA | |
| | | | $T_A$ = + 25 °C | — | 100 | 500 | µA | RTC :<br>4 MHz mode *5 |
| | | | $T_A$ = + 105 °C | — | 500 | 2400 | µA | |
| | | | $T_A$ = + 25 °C | — | 50 | 250 | µA | RTC :<br>100 kHz mode *5<br>32 kHz mode *6 |
| | | | $T_A$ = + 105 °C | — | 450 | 2200 | µA | |
| | $I_{LVE}$ | $V_{DD}5$ | — | — | 70 | 150 | µA | External low voltage detection |
| | $I_{LVI}$ | $V_{DD}5R$ | — | — | 50 | 100 | µA | Internal low voltage detection |
| | $I_{OSC}$ | $V_{DD}5$ | — | — | 250 | 500 | µA | Main clock (4 MHz) |
| | | | — | — | 20 | 40 | µA | Sub clock (32 kHz) |

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current<br><br>CY91-F465CA | $I_{CC}$ | $V_{DD}5R$ | CY91F465CA:<br>CLKB: 100 MHz<br>CLKP: 50 MHz<br>CLKT: 50 MHz<br>CLKCAN: 50 MHz | — | 110 | 140 | mA | Code fetch from Flash |
| | $I_{CCH}$ | $V_{DD}5R$ | $T_A$ = + 25 °C | — | 30 | 150 | µA | At stop mode *5 |
| | | | $T_A$ = + 105 °C | — | 300 | 2000 | µA | |
| | | | $T_A$ = + 25 °C | — | 100 | 500 | µA | RTC :<br>4 MHz mode *5 |
| | | | $T_A$ = + 105 °C | — | 500 | 2400 | µA | |
| | | | $T_A$ = + 25 °C | — | 50 | 250 | µA | RTC :<br>100 kHz mode *5<br>32 kHz mode *6 |
| | | | $T_A$ = + 105 °C | — | 400 | 2200 | µA | |
| | $I_{LVE}$ | $V_{DD}5$ | — | — | 70 | 150 | µA | External low voltage detection |
| | $I_{LVI}$ | $V_{DD}5R$ | — | — | 50 | 100 | µA | Internal low voltage detection |
| | $I_{OSC}$ | $V_{DD}5$ | — | — | 250 | 500 | µA | Main clock (4 MHz) |
| | | | — | — | 20 | 40 | µA | Sub clock (32 kHz) |
| Power supply current<br><br>CY91-F463CA (target data) | $I_{CC}$ | $V_{DD}5R$ | CY91F463CA:<br>CLKB: 100 MHz<br>CLKP: 50 MHz<br>CLKT: 50 MHz<br>CLKCAN: 50 MHz | — | 100 | 130 | mA | Code fetch from Flash |
| | $I_{CCH}$ | $V_{DD}5R$ | $T_A$ = + 25 °C | — | 30 | 150 | µA | At stop mode *5 |
| | | | $T_A$ = + 105 °C | — | 300 | 2000 | µA | |
| | | | $T_A$ = + 25 °C | — | 100 | 500 | µA | RTC :<br>4 MHz mode *5 |
| | | | $T_A$ = + 105 °C | — | 500 | 2400 | µA | |
| | | | $T_A$ = + 25 °C | — | 50 | 250 | µA | RTC :<br>100 kHz mode *5<br>32 kHz mode *6 |
| | | | $T_A$ = + 105 °C | — | 400 | 2200 | µA | |
| | $I_{LVE}$ | $V_{DD}5$ | — | — | 70 | 150 | µA | External low voltage detection |
| | $I_{LVI}$ | $V_{DD}5R$ | — | — | 50 | 100 | µA | Internal low voltage detection |
| | $I_{OSC}$ | $V_{DD}5$ | — | — | 250 | 500 | µA | Main clock (4 MHz) |
| | | | — | — | 20 | 40 | µA | Sub clock (32 kHz) |

1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.
3. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.

4. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
5. Main regulator OFF, sub regulator set to 1.2 V, Low voltage detection disabled.
6. Main regulator OFF, sub regulator set 1.2 V, Low voltage detection disabled, RC oscillator enabled.
   Additional current consumption of Sub oscillator $I_{OSC}$ has to be taken into account.

### 15.4 A/D Converter Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | − 3 | — | + 3 | LSB | |
| Nonlinearity error | — | — | − 2.5 | — | + 2.5 | LSB | |
| Differential nonlinearity error | — | — | − 1.9 | — | + 1.9 | LSB | |
| Zero reading voltage | $V_{OT}$ | ANn | AVRL − 1.5 LSB | AVRL + 0.5 LSB | AVRL + 2.5 LSB | V | |
| Full scale reading voltage | $V_{FST}$ | ANn | AVRH − 3.5 LSB | AVRH − 1.5 LSB | AVRH + 0.5 LSB | V | |
| Compare time | $T_{comp}$ | — | 0.6 | — | 16,500 | µs | 4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V |
| | | | 2.0 | — | — | µs | 3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V |
| Sampling time | $T_{samp}$ | — | 0.4 | — | — | µs | 4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, $R_{EXT}$ < 2 kΩ |
| | | | 1.0 | — | — | µs | 3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, $R_{EXT}$ < 1 kΩ |
| Conversion time | $T_{conv}$ | — | 1.0 | — | — | µs | 4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V |
| | | | 3.0 | — | — | µs | 3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V |
| Input capacitance | $C_{IN}$ | ANn | — | — | 11 | pF | |
| Input resistance | $R_{IN}$ | ANn | — | — | 2.6 | kΩ | 4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V |
| | | | — | — | 12.1 | kΩ | 3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V |
| Analog input leakage current | $I_{AIN}$ | ANn | − 1 | — | + 1 | µA | $T_A$ = + 25 °C |
| | | | − 3 | — | + 3 | µA | $T_A$ = + 105 °C |
| Analog input voltage range | $V_{AIN}$ | ANn | AVRL | — | AVRH | V | |
| Offset between input channels | — | ANn | — | — | 4 | LSB | |

*(Continued)*

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

*(Continued)*

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Reference voltage range | AVRH | AVRH5 | 0.75 × $AV_{CC}5$ | — | $AV_{CC}5$ | V | |
| | AVRL | $AV_{SS}5$ | $AV_{SS}5$ | — | $AV_{CC}5$ × 0.25 | V | |
| Power supply current per ADC macro *3 | $I_A$ | $AV_{CC}5$ | — | 2.5 | 5 | mA | A/D Converter active |
| | $I_{AH}$ | $AV_{CC}5$ | — | — | 5 | µA | A/D Converter not operated *1 |
| Reference voltage current per ADC macro *3 | $I_R$ | AVRH5 | — | 0.7 | 1 | mA | A/D Converter active |
| | $I_{RH}$ | AVRH5 | — | — | 5 | µA | A/D Converter not operated *2 |

*1 : Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*2 : Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*3 : The current consumption per ADC macro is given here. On devices having more then one A/D converter, the current values have to be multiplied by the number of macros.

Sampling Time Calculation
$T_{samp} = (2.6\ kOhm + R_{EXT}) \cdot 11pF \cdot 7$; for $4.5V \leq AV_{CC}5 \leq 5.5V$
$T_{samp} = (12.1\ kOhm + R_{EXT}) \cdot 11pF \cdot 7$; for $3.0V \leq AV_{CC}5 \leq 4.5V$

Conversion Time Calculation
$T_{conv} = T_{samp} + T_{comp}$

### Definition of A/D Converter Terms

■ Resolution

Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error

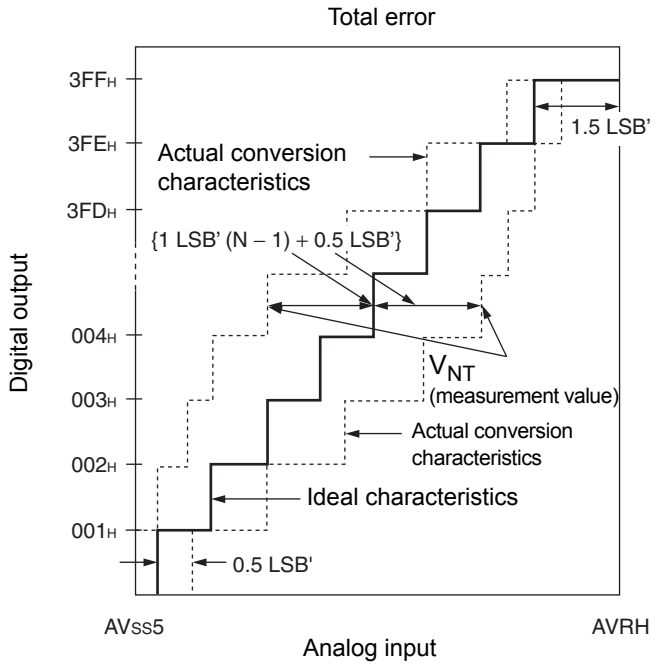
Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).

■ Differential nonlinearity error

Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

■ Total error

This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



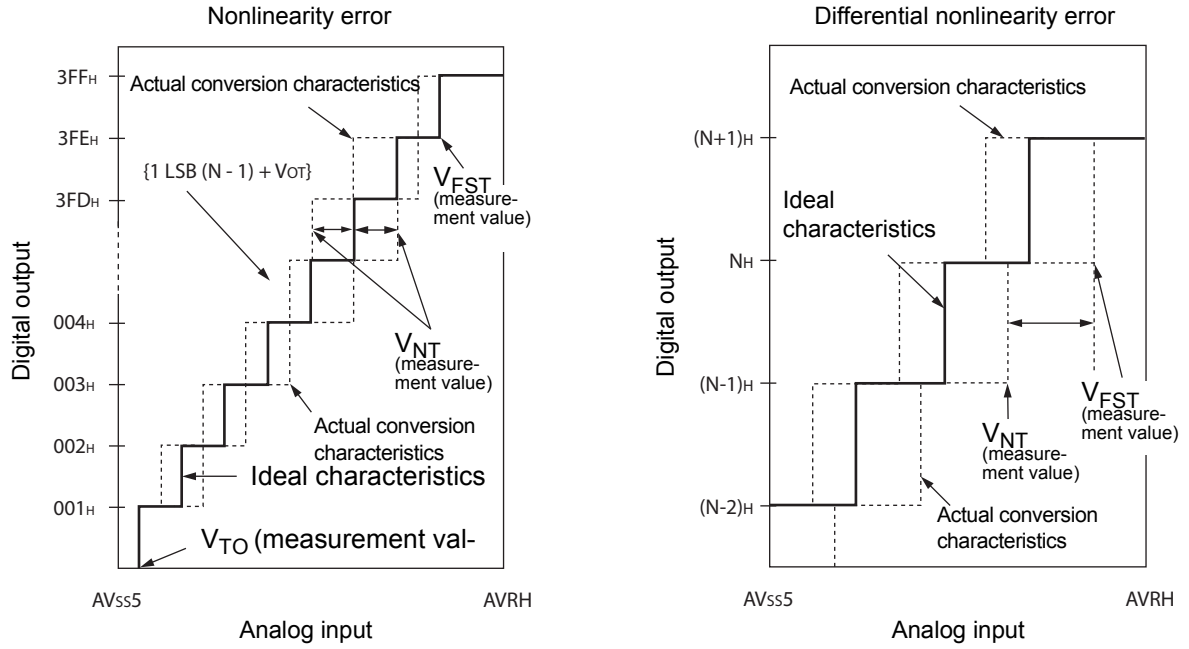

$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}5}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \cdot (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
$V_{OT}'$ (ideal value) = $AV_{SS}5 + 0.5$ LSB' [V]
$V_{FST}'$ (ideal value) = AVRH − 1.5 LSB' [V]
$V_{NT}$ : Voltage at which the digital output changes from $(N + 1)_H$ to $N_H$

*(Continued)*

*(Continued)*




$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \cdot (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value
$V_{OT}$ : Voltage at which the digital output changes from $000_H$ to $001_H$.
$V_{FST}$ : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

### 15.5 Alarm Comparator Characteristics

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Power supply current | $I_{A5ALMF}$ | $AV_{CC}5$ | — | 25 | 40 | µA | Alarm comparator enabled in fast mode (per channel) *1 |
| | $I_{A5ALMS}$ | | — | 7 | 10 | µA | Alarm comparator enabled in normal mode (per channel) *1 |
| | $I_{A5ALMH}$ | | — | — | 5 | µA | Alarm comparator disabled |
| ALARM pin input current | $I_{ALIN}$ | ALARM_n | − 1 | — | + 1 | µA | $T_A$=25 °C |
| | | | − 3 | — | + 3 | µA | $T_A$=105 °C |
| ALARM pin input voltage range | $V_{ALIN}$ | | 0 | — | $AV_{CC}5$ | V | |
| Alarm upper limit voltage | $V_{IAH}$ | | $AV_{CC}5 \times 0.78 - 3\%$ | $AV_{CC}5 \times 0.78$ | $AV_{CC}5 \times 0.78 + 3\%$ | V | |
| Alarm lower limit voltage | $V_{IAL}$ | | $AV_{CC}5 \times 0.36 - 5\%$ | $AV_{CC}5 \times 0.36$ | $AV_{CC}5 \times 0.36 + 5\%$ | V | |
| Alarm hysteresis voltage | $V_{IAHYS}$ | | 50 | — | 250 | mV | |
| Alarm input resistance | $R_{IN}$ | | 5 | — | — | MΩ | |
| Comparion time | $t_{COMPF}$ | | — | 0.1 | 0.2 | µA | Alarm comparator enabled in fast mode *1 |
| | $t_{COMPS}$ | | — | 1 | 2 | µA | Alarm comparator enabled in normal mode *1 |

Note: *1 : The fast Alarm Comparator mode is enabled by setting ACSR.MD=1
Setting ACSR.MD=0 sets the normal mode.

## 15.6 FLASH Memory Program/Erase Characteristics

### *15.6.1 CY91F463CA, CY91F465CA*

($T_A$ = 25°C, Vcc = 5.0V)

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 0.9 | 3.6 | s | Erasure programming time not included |
| Chip erase time | - | n*0.9 | n*3.6 | s | n is the number of Flash sector of the device |
| Word (16-bit width) programming time | - | 23 | 370 | µs | System overhead time not included |
| Programme/Erase cycle | 10 000 | - | - | cycle | |
| Flash data retention time | 20 | - | - | year | *1 |

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

### *15.6.2 CY91F467Cx*

($T_A$ = 25°C, Vcc = 5.0V)

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 0.5 | 2.0 | s | Erasure programming time not included |
| Chip erase time | - | n*0.5 | n*2.0 | s | n is the number of Flash sector of the device |
| Word (16-bit or 32-bit width) programming time | - | 6 | 100 | µs | System overhead time not included |
| Programme/Erase cycle | 10 000 | - | - | cycle | |
| Flash data retention time | 20 | - | - | year | *1 |

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

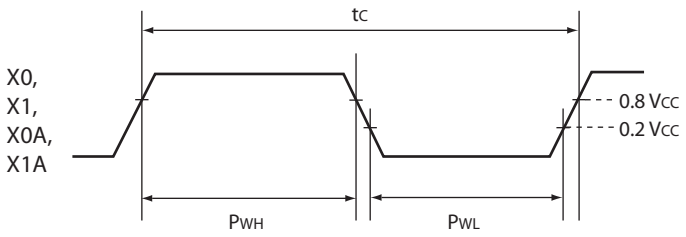
## 15.7 AC Characteristics

### *15.7.1 Clock Timing*

($V_{DD}5 = 3.0$ V to 5.5 V, $Vss5 = AVss5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

| Parameter | Symbol | Pin name | Value | | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_C$ | X0<br>X1 | 3.5 | 4 | 16 | MHz | Opposite phase external supply or crystal |
| | | X0A<br>X1A | 32 | 32.768 | 100 | kHz | |

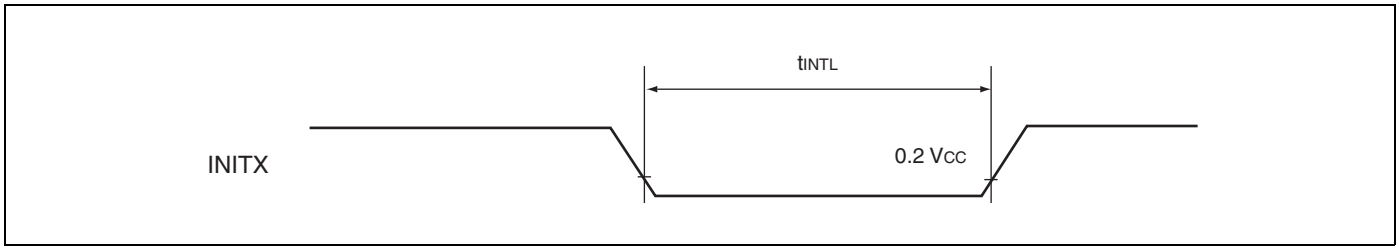
**Clock Timing Condition**



*15.7.2 Reset Input Ratings*

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| INITX input time (at power-on) | $t_{INTL}$ | INITX | — | 10 | — | ms |
| INITX input time (other than the above) | | | | 20 | — | µs |



*15.7.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V*

- Conditions during AC measurements
- All AC tests were measured under the following conditions:
- - $IO_{drive}$ = 5 mA
- - $V_{DD}5$ = 3.0 V to 5.5 V, $I_{load}$ = 3 mA
- - $V_{SS}5$ = 0 V
- - $T_a$ = -40°C to +105°C
- - $C_l$ = 50 pF (load capacity value of pins when testing)
- - VOL = 0.2 x $V_{DD}5$
- - VOH = 0.8 x $V_{DD}5$
- - EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

| Parameter | Symbol | Pin Name | Condition | $V_{DD}5 = 3.0$ V to 4.5 V | | $V_{DD}5 = 4.5$ V to 5.5 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYCI}$ | SCKn | Internal clock operation (master mode) | 4 $t_{CLKP}$ | — | 4 $t_{CLKP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCKn SOTn | | − 30 | 30 | − 20 | 20 | ns |
| SOT → SCK ↓ delay time | $t_{OVSHI}$ | SCKn SOTn | | m × $t_{CLKP}$ − 30* | — | m × $t_{CLKP}$ − 20* | — | ns |
| Valid SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCKn SINn | | $t_{CLKP}$ + 55 | — | $t_{CLKP}$ + 45 | — | ns |
| SCK ↑ → valid SIN hold time | $t_{SHIXI}$ | SCKn SINn | | 0 | — | 0 | — | ns |
| Serial clock “H” pulse width | $t_{SHSLE}$ | SCKn | External clock operation (slave mode) | $t_{CLKP}$ + 10 | — | $t_{CLKP}$ + 10 | — | ns |
| Serial clock “L” pulse width | $t_{SLSHE}$ | SCKn | | $t_{CLKP}$ + 10 | — | $t_{CLKP}$ + 10 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCKn SOTn | | — | 2 $t_{CLKP}$ + 55 | — | 2 $t_{CLKP}$ + 45 | ns |
| Valid SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCKn SINn | | 10 | — | 10 | — | ns |
| SCK ↑ → valid SIN hold time | $t_{SHIXE}$ | SCKn SINn | | $t_{CLKP}$ + 10 | — | $t_{CLKP}$ + 10 | — | ns |
| SCK rising time | $t_{FE}$ | SCKn | | — | 20 | — | 20 | ns |
| SCK falling time | $t_{RE}$ | SCKn | | — | 20 | — | 20 | ns |

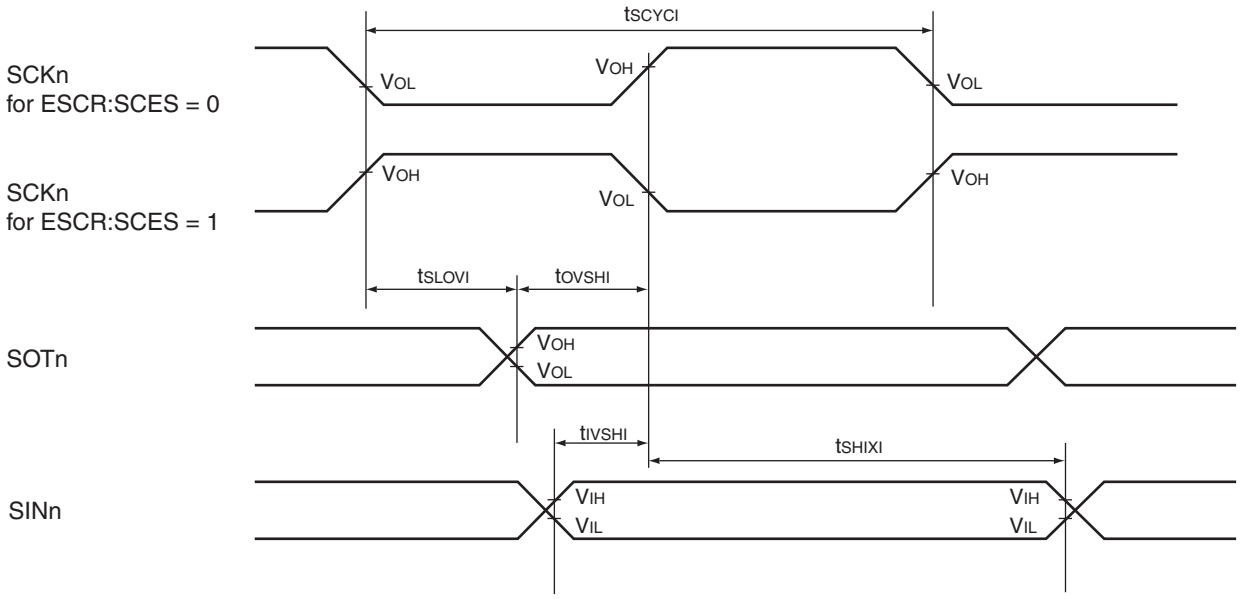
* : Parameter m depends on $t_{SCYCI}$ and can be calculated as :

- if $t_{SCYCI} = 2*k*t_{CLKP}$, then m = k, where k is an integer > 2
- if $t_{SCYCI} = (2*k + 1)*t_{CLKP}$, then m = k + 1, where k is an integer > 1

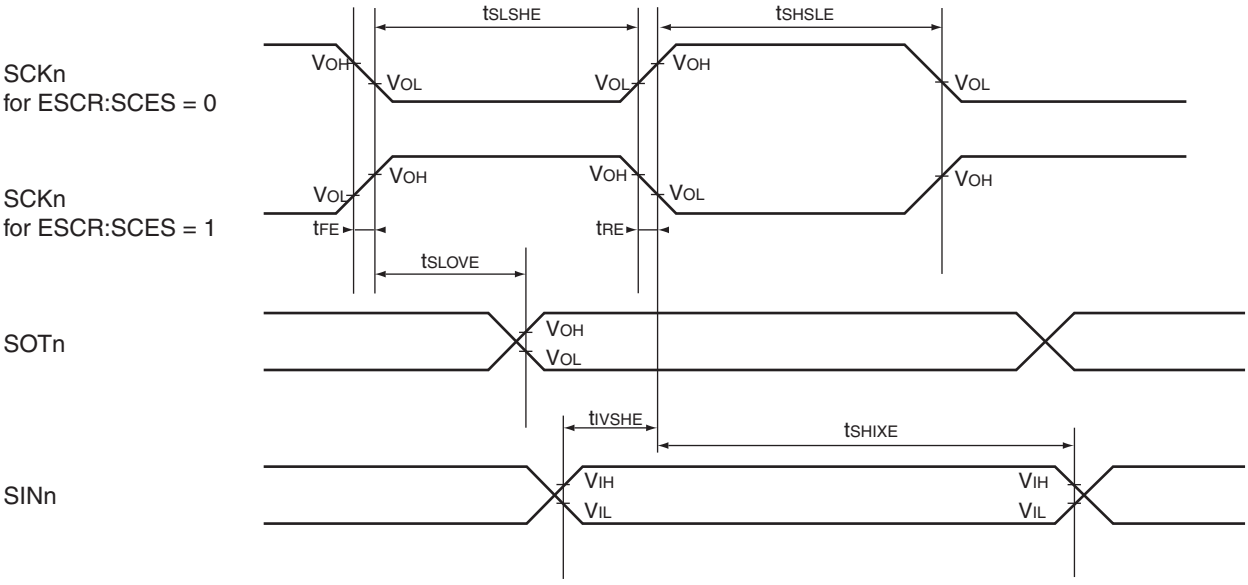
Notes :

- The above values are AC characteristics for CLK synchronous mode.
- $t_{CLKP}$ is the cycle time of the peripheral clock.

### Internal Clock Mode (Master Mode)




### External Clock Mode (Slave Mode)



### 15.7.4 $I^2C$ AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - $IO_{drive}$ = 3 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, $I_{load}$ = 3 mA ($V_{DD}$ = 4.5 V to 5.5 V for CY91F467Cx)
  - $V_{SS}5$ = 0 V
  - Ta = −40 °C to +105 °C
  - $C_l$ = 50 pF
  - VOL = 0.3 × $V_{DD}5$
  - VOH = 0.7 × $V_{DD}5$
  - EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

Fast mode:

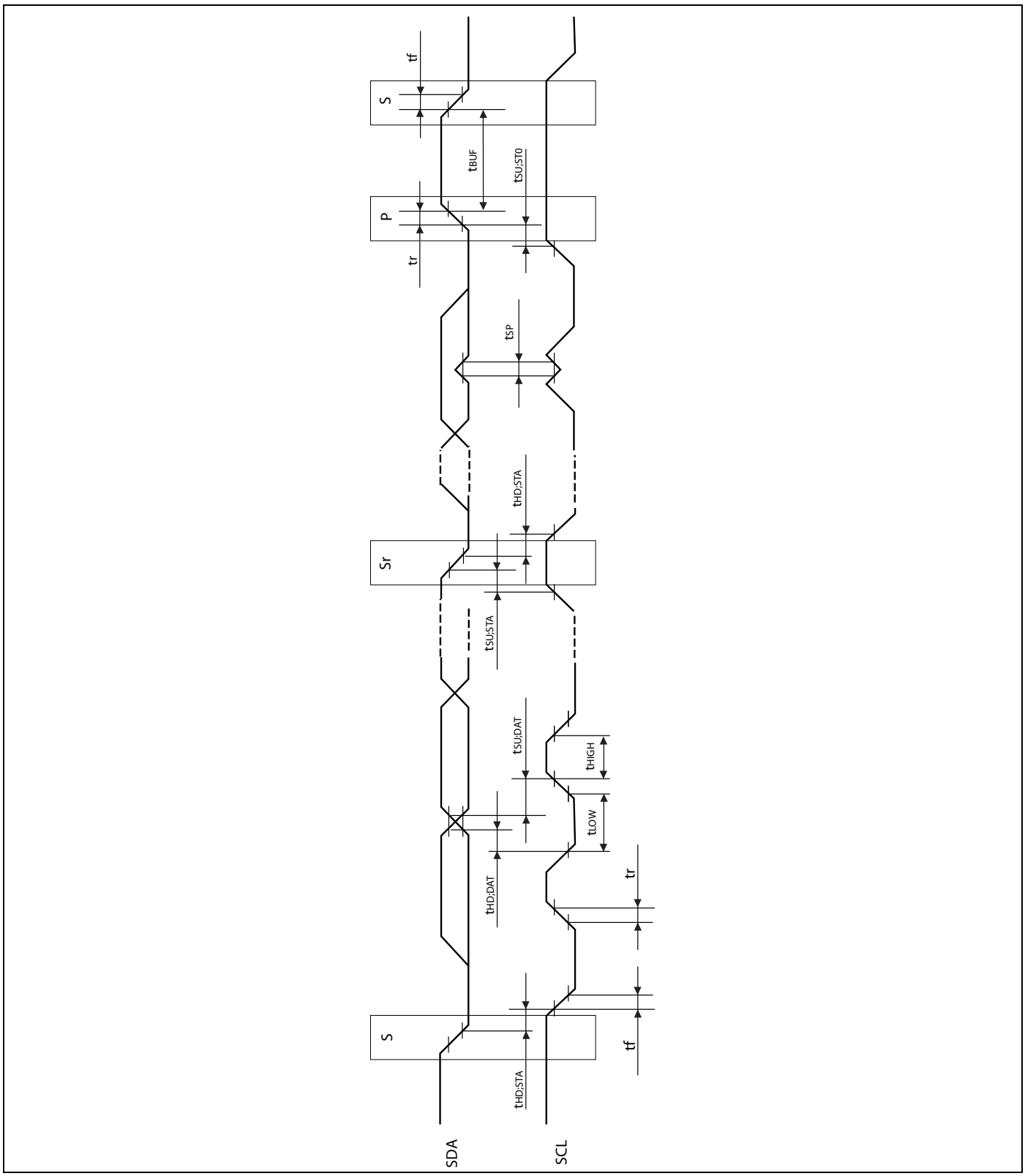
($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, $T_A$ = −40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Value | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| SCL clock frequency | $f_{SCL}$ | SCLn | 0 | 400 | kHz | |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD;STA}$ | SCLn, SDAn | 0.6 | — | µs | |
| LOW period of the SCL clock | $t_{LOW}$ | SCLn | 1.3 | — | µs | |
| HIGH period of the SCL clock | $t_{HIGH}$ | SCLn | 0.6 | — | µs | |
| Setup time for a repeated START condition | $t_{SU;STA}$ | SCLn, SDAn | 0.6 | — | µs | |
| Data hold time for $I^2C$-bus devices | $t_{HD;DAT}$ | SCLn, SDAn | 0 | 0.9 | µs | |
| Data setup time | $t_{SU;DAT}$ | SCLn SDAn | 100 | — | ns | |
| Rise time of both SDA and SCL signals | $t_r$ | SCLn, SDAn | 20 + 0.1Cb | 300 | ns | *1 |
| Fall time of both SDA and SCL signals | $t_f$ | SCLn, SDAn | 20 + 0.1Cb | 300 | ns | *1 |
| Setup time for STOP condition | $t_{SU;STO}$ | SCLn, SDAn | 0.6 | — | µs | |
| Bus free time between a STOP and START condition | $t_{BUF}$ | SCLn, SDAn | 1.3 | — | µs | |
| Capacitive load for each bus line | $C_b$ | SCLn, SDAn | — | 400 | pF | |
| Pulse width of spike suppressed by input filter | $t_{SP}$ | SCLn, SDAn | 0 | (1.1.5) × $t_{CLKP}$ | ns | *2 |

*1: On CY91F467Cx only guaranteed for 4.5 V < $V_{DD}5$ < 5.5 V.

*2: The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between $I^2C$ signals (SDA, SCL) and peripheral clock.

Note: $t_{CLKP}$ is the cycle time of the peripheral clock.

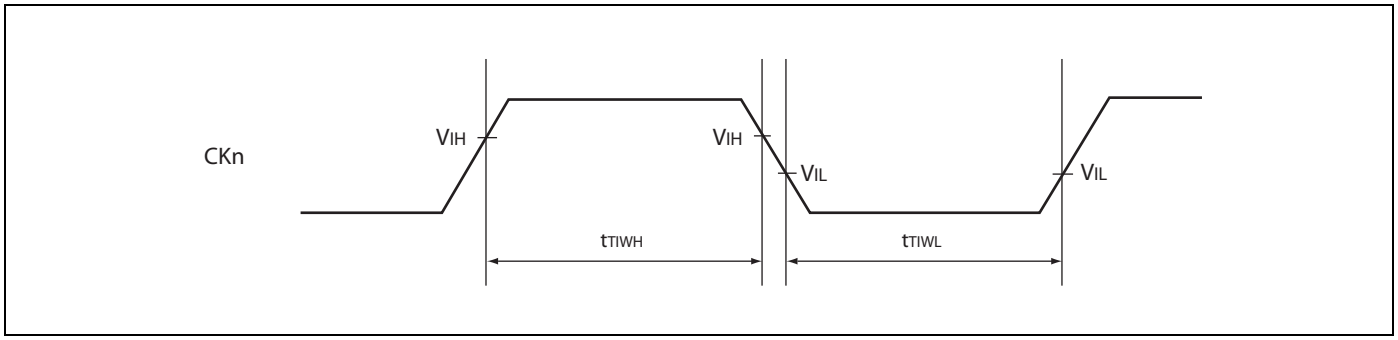

tf
S
tBUF
tSU;STO
P
tr
tSP
tHD;STA
Sr
tSU;STA
tSU;DAT
tHIGH
tLOW
tHD;DAT
tr
tf
S
tHD;STA
SDA
SCL

### 15.7.5 Free-run Timer Clock

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | CKn | — | $4t_{CLKP}$ | — | ns |

Note : $t_{CLKP}$ is the cycle time of the peripheral clock.

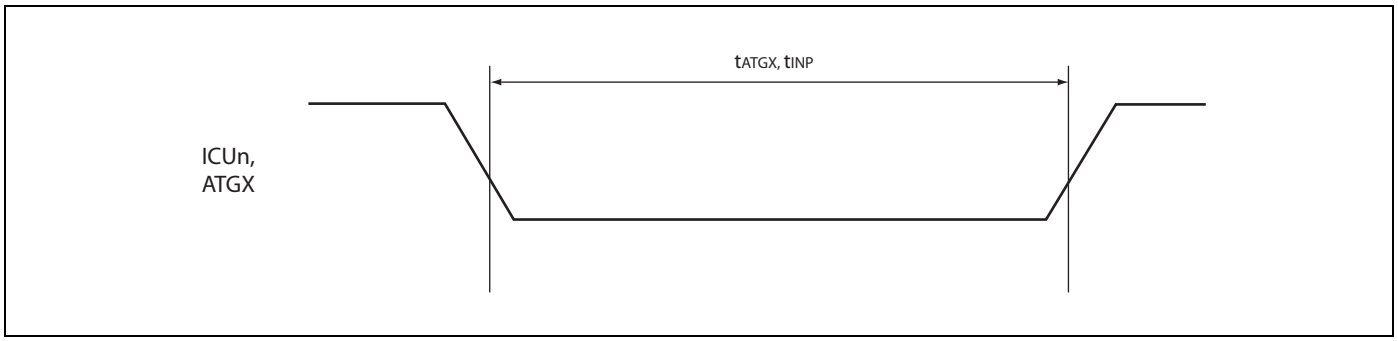



### 15.7.6 Trigger Input Timing

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input capture input trigger | $t_{INP}$ | ICUn | — | $5t_{CLKP}$ | — | ns |
| A/D converter trigger | $t_{ATGX}$ | ATGX | — | $5t_{CLKP}$ | — | ns |

Note : $t_{CLKP}$ is the cycle time of the peripheral clock.

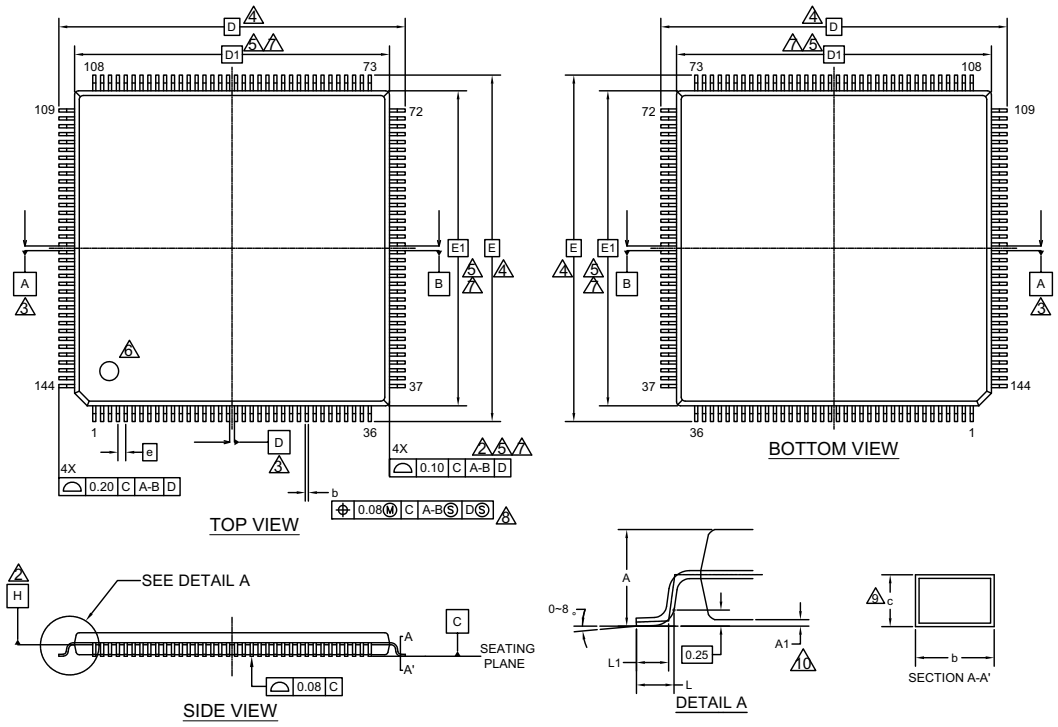


## 16. Ordering Information

| Part Number | Package | Remarks |
|---|---|---|
| CY91F467CBPMCR-GS-UJE2 | 144-pin plastic LQFP (LQS144) | |
| CY91F465CAPMC-GS-UJE2 | | |

## 17. Package Dimension

| Package Type | Package Code |
|---|---|
| LQFP 144-pin | LQS144 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 22.00 BSC | | |
| D1 | 20.00 BSC | | |
| e | 0.50 BSC | | |
| E | 22.00 BSC | | |
| E1 | 20.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV*A

002-13015 *A

## 18. Revision History

| Version | Date | Remark |
|---|---|---|
| 2.0 | 2008-04-16 | Initial Version |
| 2.1 | 2008-08-15 | Handling devices: Section Notes on PS Register changed for better understanding;<br>Interrupt Vector Table: corrected the footnotes<br>FLASH: Added note about the flash operation mode switching;<br>added section "Poweron Sequence in parallel programming mode";<br>FLASH Security: Corrected sector assignments FSV1,FSV2<br>Absolute maximum ratings: Removed the note that analog input/output pins cannot accept +B signal input.<br>DC Characteristics: Updated PullUp/Down resistors and the footnotes, splitted $I_{LV}$ into external and internal LV detection<br>AD Converter characteristics updated (complete section);<br>Ordering information updated;<br>Company name updated |
| 2.2 | 2008-11-24 | Flash: Added MB91F463CA to all sections<br>Memory maps: Removed external bus areas (no ext. bus available)<br>IO-Map: Added/corrected MB91F463CA<br>Ordering Information: Added MB91F463CA |

## 19. Major Changes

**Spansion Publication Number: DS07-16610-2E**

| Page | Section | Change Results |
|---|---|---|
| 2 | Features<br>2. Internal peripheral resources | Deleted following description:<br>Fly-by transfer support (between external I/O and memory) |
| 29 | Embedded Program /<br>Data Memory (Flash) | Corrected the Note:<br>The operation mode of the flash memory → The operation mode of the MCU |
| 49 | I/O Map | Added Reload Timer 0 and 1 on address $0001B0_H$ to $0001BC_H$ |
| 89, 90 | Electrical Characteristics<br>3. DC characteristics | Corrected the Remarks column of Parameter: Power supply current<br>RTC: 100 kHz mode*5 →<br>RTC: 100 kHz mode*5, 32 kHz mode*6 |
| 91 | | Added Footnote 6: |
| 99 | Electrical Characteristics<br>7.2. Reset input ratings | Corrected the spec value of INITX input time (at power-on)<br>Min: 8 ms → 10 ms |

Note: Please see “Document History” about later revised information.

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>Rev.*B</td><td colspan="2"></td></tr>
<tr><td>-</td><td colspan="2">Marketing Part Numbers changed from an MB prefix to a CY prefix for all of these products.</td></tr>
<tr><td>P2</td><td>Features</td><td>Deleted following description:<br>Note:MB91F463CA is under development.</td></tr>
<tr><td>P6</td><td>2. Pin Assignment</td><td>Added the following package code.<br>(LQS144)</td></tr>
<tr><td>P101</td><td>16. Ordering Information</td><td>Revised Marketing Part Numbers as follows:<br><br>Before)
<table>
<tr><th>Part number</th><th>Package</th><th>Remarks</th></tr>
<tr><td>MB91F467CAPMC-GSE2</td><td rowspan="4">144-pin plastic LQFP<br>(FPT-144P-M08)</td><td>not recommended</td></tr>
<tr><td>MB91F467CBPMC-GSE2</td><td>Lead-free package</td></tr>
<tr><td>MB91F465CAPMC-GSE2</td><td>Lead-free package</td></tr>
<tr><td>MB91F463CAPMC-GSE2</td><td>Lead-free package</td></tr>
</table>
After)
<table>
<tr><th>Part number</th><th>Package</th><th>Remarks</th></tr>
<tr><td>CY91F467CBPMCR-GS-UJE2</td><td rowspan="2">144-pin plastic LQFP<br>(LQS144)</td><td></td></tr>
<tr><td>CY91F465CAPMC-GS-UJE2</td><td></td></tr>
</table></td></tr>
<tr><td>P101,<br>P102</td><td>16. Ordering Information<br>17. Package Dimension</td><td>Package description modified to JEDEC description.<br>FPT-144P-M08 → LQS144</td></tr>
</table>

## Document History

| Document Title: CY91460C Series FR60 32-bit Microcontroller<br>Document Number: 002-04609 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submis-sion Date** | **Description of Change** |
| ** | — | TORS | 04/28/2010 | Migrated to Cypress and assigned document number 002-04609.<br>No change to document contents or format. |
| *A | 5200971 | TORS | 04/12/2016 | Updated to Cypress format. |
| *B | 5966511 | MIYH | 11/20/2017 | Revised the following items:<br>Marketing Part Numbers changed from an MB prefix to a CY prefix for all of these products.<br>Pin Assignment<br>Ordering Information<br>Package Dimension<br>For details, please see 19. Major Changes. |

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