ANALOG DEVICES

EVAL-ADAU1466Z User Guide

UG-1135

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Evaluating the ADAU1466 SigmaDSP Audio Processor

FEATURES

4 analog inputs
8 analog outputs
Stereo S/PDIF input and output
Self boot EEPROM memory

EVALUATION KIT CONTENTS

EVAL-ADAU1466Z evaluation board
EVAL-ADUSB2EBZ (USBi) communications adapter
USB cable with Mini-B plug
6 V ac to dc power supply

HARDWARE REQUIRED

PC running Windows XP, Windows Vista, or Windows 7
Analog, stereo audio source with an output cable terminated with a 3.5 mm (1/8 inch) plug (for analog input)
Headphones, desktop speakers, or audio input with a cable terminated with a 3.5 mm (1/8 inch) plug (for analog output)
S/PDIF audio source and receiver, each with optical cables terminated with TOSLINK connectors (for digital input/output)

SOFTWARE REQUIRED

SigmaStudio software, available for download from the SigmaStudio product page

DOCUMENTS NEEDED

ADAU1466 data sheet
AD1938 data sheet
AN-1006 Application Note

GENERAL DESCRIPTION

This user guide details the design, setup, and operation of the EVAL-ADAU1466Z evaluation board. This device is suitable for evaluation of, and software development for, the ADAU1466 and ADAU1462 SigmaDSP processors. Note that the ADAU1466 and the ADAU1462 are functionally identical, except that the ADAU1466 has more program and data memory than the ADAU1462. When using this evaluation board to evaluate the ADAU1462, in the Setting Up Communications in SigmaStudio section, select the ADAU1462 block rather than the ADAU1466 as shown in Figure 15. Performing this action informs the compiler to limit the amount of memory allocated to match the ADAU1462. All other procedures and instructions in this user guide are identical for the ADAU1462 and ADAU1466.

This evaluation board provides access to the digital serial audio ports of the ADAU1466, as well as some of its general-purpose input/outputs (GPIOs). An analog input and output is provided by the AD1938 codec that is included in the evaluation kit. The ADAU1466 core is programmed using Analog Devices, Inc., SigmaStudio® software, which interfaces to the evaluation board via a USB interface (USBi). The on-board EEPROM can be programmed for self boot mode. The evaluation board is powered by a 6 V dc supply, which is regulated to the voltages required on the board. The printed circuit board (PCB) is a 4-layer design, with a ground plane and a power plane on the inner layers. The evaluation board includes connectors for external analog inputs and outputs, and optical Sony/Philips Digital Interface (S/PDIF) interfaces. The master clock is provided by the integrated oscillator circuit and the on-board 12.288 MHz passive crystal.

For full details, see the ADAU1466 and AD1938 data sheets, which must be used in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

8/2017—Revision 0: Initial Version

EVAL-ADAU1466Z EVALUATION BOARD PHOTOGRAPH

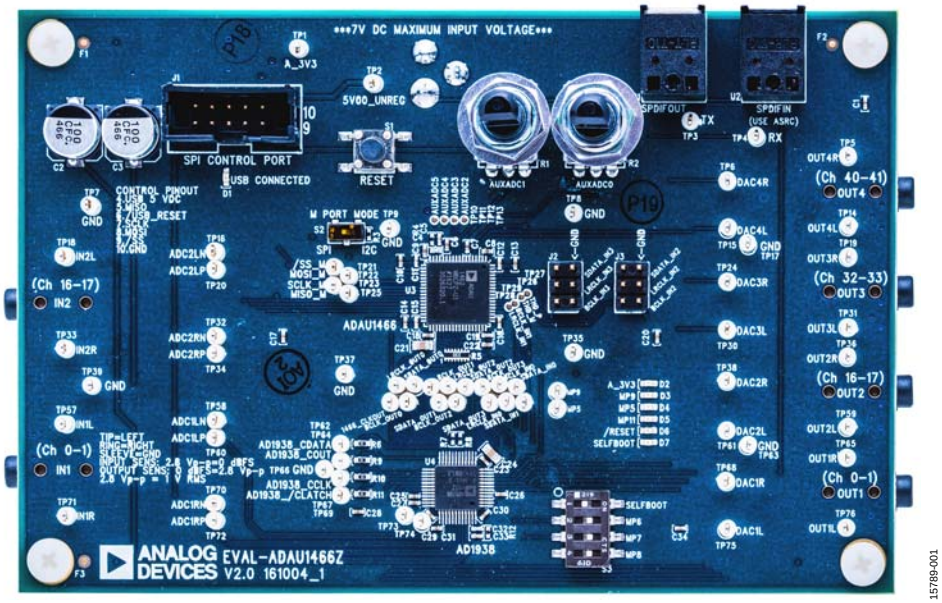

Figure 1.

SETTING UP THE EVALUATION BOARD

Using the EVAL-ADAU1466Z evaluation board requires a PC running Windows® XP or later with a USB interface and an internet connection. The PC communicates with the evaluation board using the included USBi interface. The software tool chain used with the ADAU1466 is SigmaStudio, a fully GUI-based programming environment. No DSP programming is required. A full version of SigmaStudio, which includes a library of DSP building blocks and the required USBi drivers, is available for download from the SigmaStudio software page on the Analog Devices website at www.analog.com/SigmaStudio.

INSTALLING THE SigmaStudio SOFTWARE

To download the latest version of SigmaStudio, take the following steps:

1. Go to the SigmaStudio software page on the Analog Devices website and select the latest version of the SigmaStudio software from the **Downloads and Related Software** section.
2. Determine whether the software must be installed on a 32-bit or 64-bit version of Windows, and locate the latest release version of SigmaStudio as appropriate.
3. Download the installer for and execute the executable. Follow the prompts, and accept the license agreement to install the software.

INSTALLING THE USBi (EVAL-ADUSB2EBZ) DRIVERS

SigmaStudio must be installed to use the USB interface (USBi). After the SigmaStudio installation is complete, take the following steps:

1. Connect the USBi to an available USB 2.0 port using the USB cable included in the evaluation board kit. (The USBi does not function properly with a USB 3.0 port.)
2. Install the driver software (see the Using Windows XP section or the Using Windows 7 or Windows Vista section for more information).

Using Windows XP

After connecting the USBi to the USB 2.0 port, Windows recognizes the device (see Figure 2) and prompts you to install the drivers. To install these drivers, take the following steps:

*Figure 2. **Found New Hardware** Notification*

1. From the **Found New Hardware Wizard** window, select the **Install from a list or specific location (Advanced)** option and click **Next >** (see Figure 3).

*Figure 3. **Found New Hardware Wizard**—Installation*

2. Click **Search for the best driver in these locations**, select **Include this location in the search**, and click **Browse** to find the USB drivers subdirectory within the SigmaStudio directory (see Figure 4).

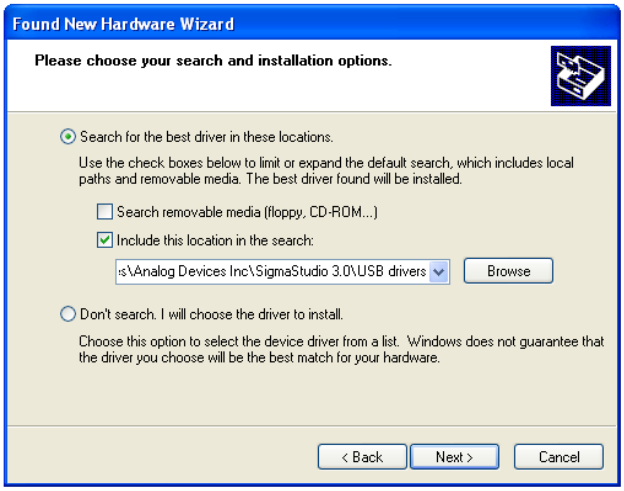

*Figure 4. **Found New Hardware Wizard**—Search and Installation Options*

3. When the warning about Windows logo testing appears, click **Continue Anyway** (see Figure 5).

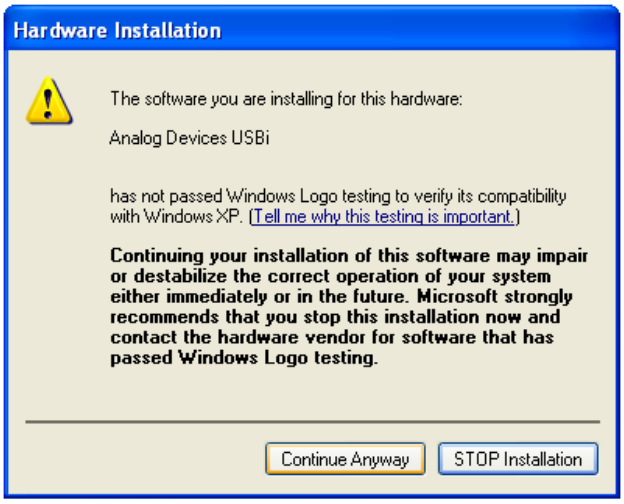

*Figure 5. **Hardware Installation**—Windows Logo Testing Warning*

The USBi drivers are now installed. Leave the USBi connected to the PC.

Using Windows 7 or Windows Vista

After connecting the USBi to the USB 2.0 port, Windows 7 or Windows Vista recognizes the device and installs the drivers automatically (see Figure 6). After the installation is complete, leave the USBi connected to the PC.

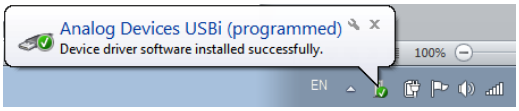

Figure 6. USBi Driver Installed Correctly

Confirming Proper Installation of the USBi Drivers

To confirm that the USBi drivers have been installed properly, take the following steps:

1. With the USBi still connected to the USB 2.0 port of the computer, check that both the yellow I²C LED and the red power indicator LED are illuminated (see Figure 7).
2. In the Windows **Device Manager**, under the **Universal Serial Bus controllers** section,(see Figure 8), check that **Analog Devices USBi (programmed)** is displayed.

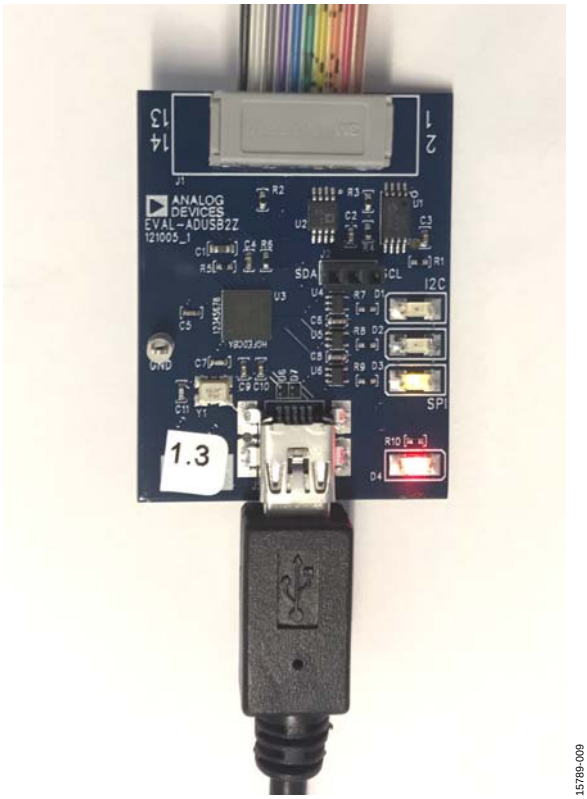

Figure 7. State of USBi Status LEDs After Driver Installation

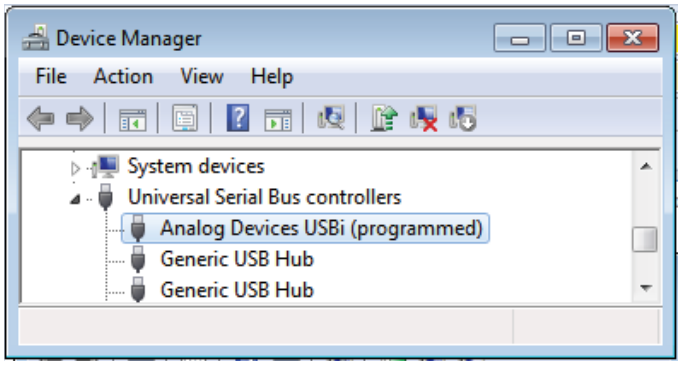

Figure 8. Confirming Driver Installation Using the Device Manager

DISABLING THE SELF BOOT SWITCH

When setting up the EVAL-ADAU1466Z evaluation board, ensure that the first switch of the four-position DIP switches, S3, is in the off position, which is away from the printed label on the evaluation board.

The default position of this switch is the off (disabled) position, which prevents the ADAU1466 from executing a self boot operation at power-up. When the switch is in the on position, the LED D7 is illuminated, and a self boot operation is executed, causing the ADAU1466 to attempt to load code from an EEPROM when it powers up or comes out of reset.

POWERING UP THE EVALUATION BOARD

To power up the evaluation board, take the following steps:

1. Connect the included power supply to the wall outlet (100 V to 240 V, ac 50 Hz to 60 Hz).
2. Connect the female plug of the power supply to the J4 male connector on the EVAL-ADAU1466Z, as shown in Figure 9.

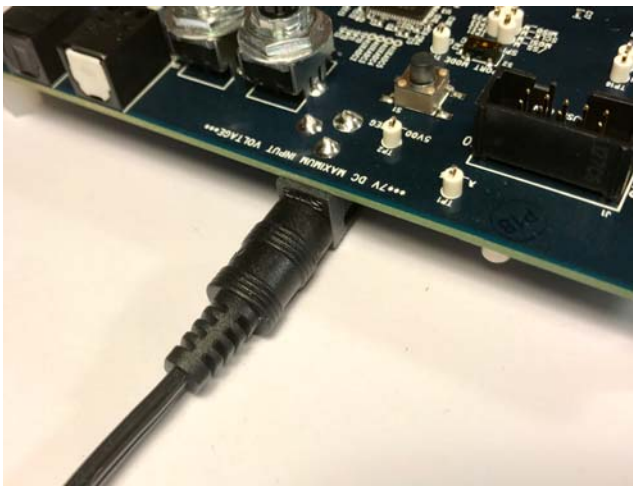

Figure 9. Connecting the Power Supply

3. After the power supply is connected, the D2 status LED (A_3V3) illuminates.
4. Connect the ribbon cable of the USBi to the control port of the EVAL-ADAU1466Z (see Figure 10). The USBi must already be connected to the USB 2.0 port of the computer.

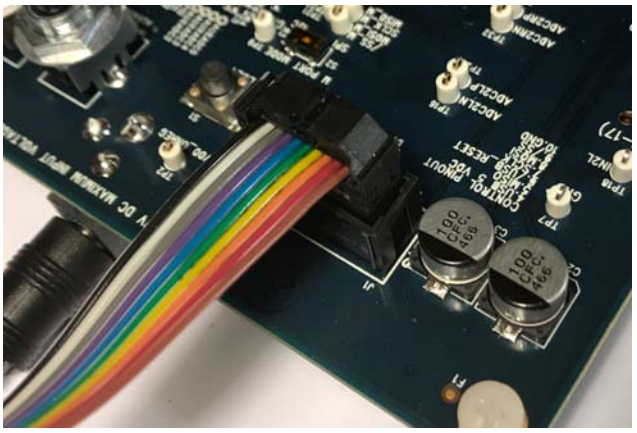

Figure 10. Connecting the USBi to the Serial Peripheral Interface (SPI) Control Port Header

CONNECTING THE AUDIO CABLES

To connect the audio cables to the evaluation board, take the following steps:

1. Connect a stereo audio source to J9 (IN1) with a standard 3.5 mm (1/8 inch) stereo tip, ring, sleeve (TRS) audio cable. The audio signals must be single-ended and line level, with a maximum voltage of 2.8 V p-p. The tip of the plug is the left channel of audio, the ring is the right channel of audio, and the sleeve is the common or ground.
2. Connect headphones or powered speakers to J10 (OUT1).

Figure 11 shows the input source connection. Figure 12 shows the output connection. Figure 13 shows the location of the connectors on the board.

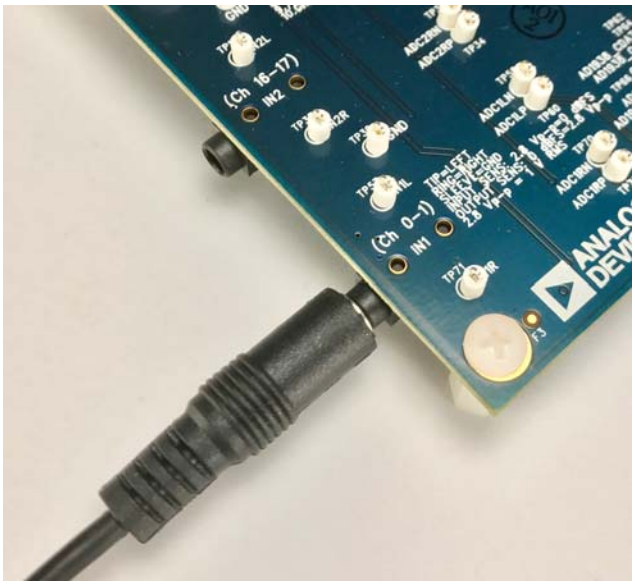

Figure 11. Analog Stereo Input Source Connection

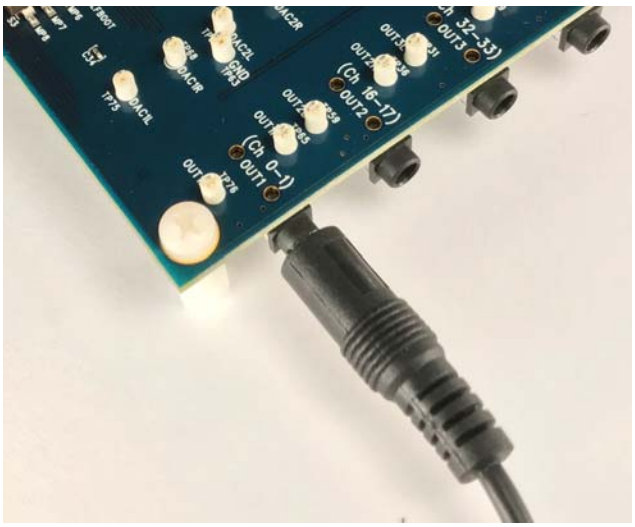

Figure 12. Analog Stereo Output Connection

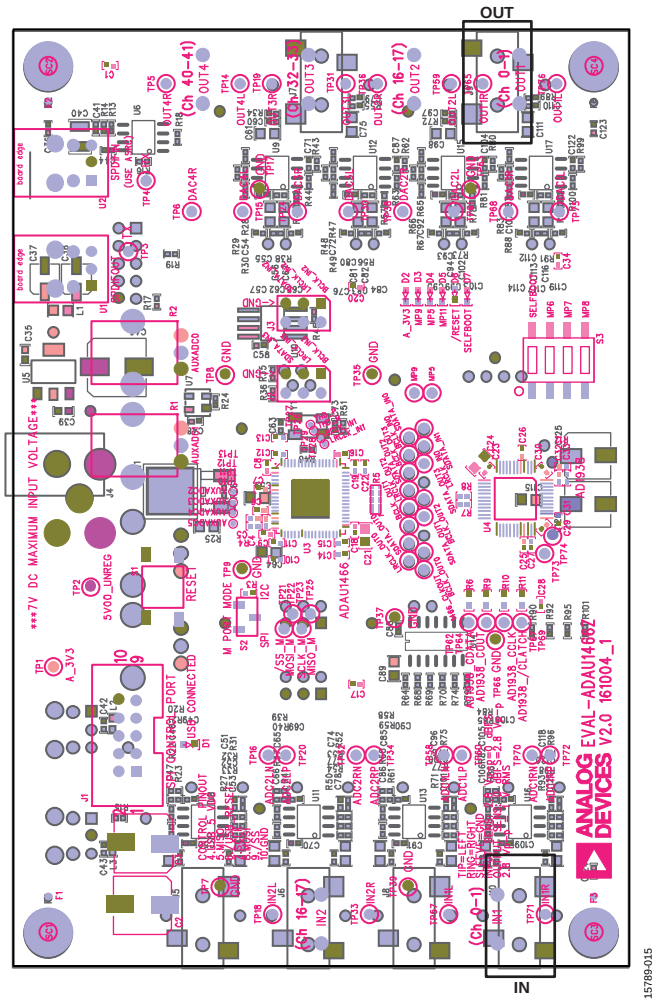

Figure 13. Location of Stereo Output OUT1 (J10) and Stereo Input IN1 (J9), Rotated 90°

SETTING UP COMMUNICATIONS IN SigmaStudio

To set up communications in SigmaStudio, take the following steps:

1. Start the SigmaStudio software by double clicking the shortcut on the desktop or by finding and executing the executable file in Windows Explorer.
2. To create a new project, select **New Project** from the **File** menu or by pressing CTRL + N. (The default view of the new project is the **Hardware Configuration** tab.)
3. In the **Hardware Configuration** tab, add the appropriate components to the project space by clicking and dragging them from the **Tree ToolBox** on the left of the window to the empty white space located on the right of the window.
   a. Click **USBi** to add a USBi component from the **Communication Channels** subsection of the toolbox (see Figure 14).

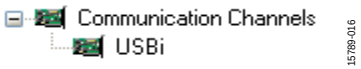

Figure 14. Adding the USBi Communication Channel

   b. Add an **ADAU1466** component from the **Processors (ICs / DSPs)** subsection of the toolbox (see Figure 15).

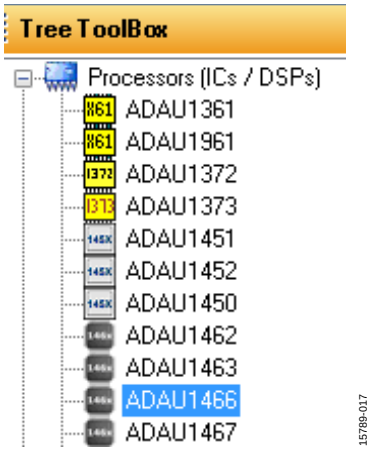

Figure 15. Adding an ADAU1466

4. Ensure that SigmaStudio can detect the USBi on the USB port of the PC as follows:
   a. When SigmaStudio detects the USBi, the background of the **USB** label is green in the **USB Interface** box (see Figure 16).

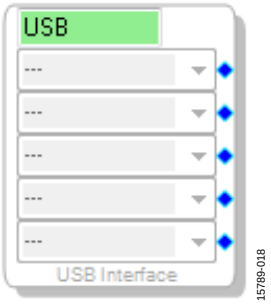

Figure 16. USBi Detected by SigmaStudio

   b. When SigmaStudio cannot detect the USBi on the USB port of the PC, the background of the **USB** label is red (see Figure 17). This error can occur when the USBi is not connected or when the drivers have been installed incorrectly.

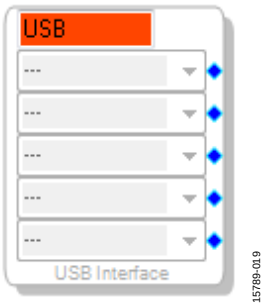

Figure 17. USBi Not Detected by SigmaStudio

   c. To connect the USBi block (USB interface) to the target integrated circuit (IC) block, the ADAU1466, click and drag a line, representing a wire, between the blue pin of the USBi and the green pin of the IC (see Figure 18). This connection allows the USBi to communicate with the ADAU1466. The corresponding dropdown box of the USBi automatically fills with the default mode and channel for that IC. In the case of the ADAU1466, the default communications mode is SPI, the default slave select line is 1, and the default address is 0.

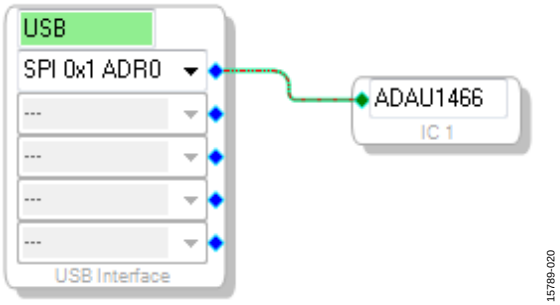

*Figure 18. Connecting the USBi to an ADAU1466 in the **Hardware Configuration** Tab*

CREATING A BASIC SIGNAL FLOW

To create a signal processing flow, take the following steps:

1. Click the **Schematic** tab near the top of the window (see Figure 19).

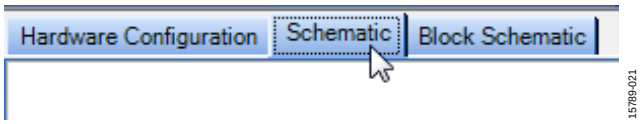

*Figure 19. **Schematic** Tab*

2. To add the appropriate elements to the project space, click and drag the elements from the **Tree ToolBox** on the left of the window to the empty white space located on the right of the window. The toolbox contains all of the algorithms that can run in SigmaDSP.
   a. To add an **Input** block, from the **(IC1) ADAU1466** > **IO** > **Input** > **sdata 0-15** folder, click **Input** (see Figure 20) and drag it into the project space to the right of the toolbox (see Figure 21). By default, Channel 0 and Channel 1 are selected. This configuration matches the analog audio source hardware connections shown in Figure 11 and Figure 12; therefore, no modifications are needed.

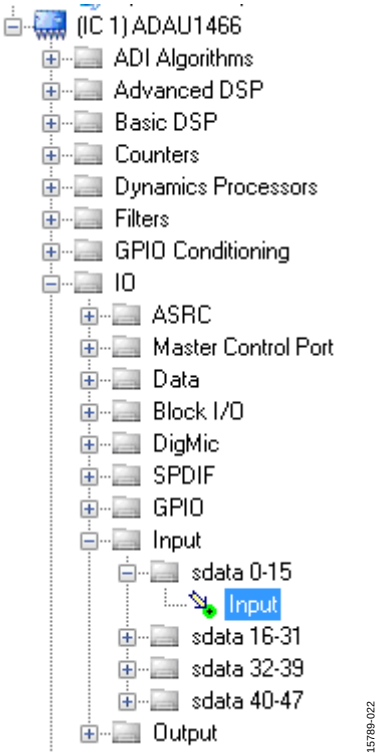

Figure 20. Input Block Selection

Figure 21. Input Block

   b. Add two **Output** blocks as follows, ensuring that these blocks are assigned to Channel 0 and Channel 1:
      i. From the **(IC1) ADAU1466** > **IO** > **Output** folder, click **Output** (see Figure 22) and drag it into the project space to the right of the toolbox.

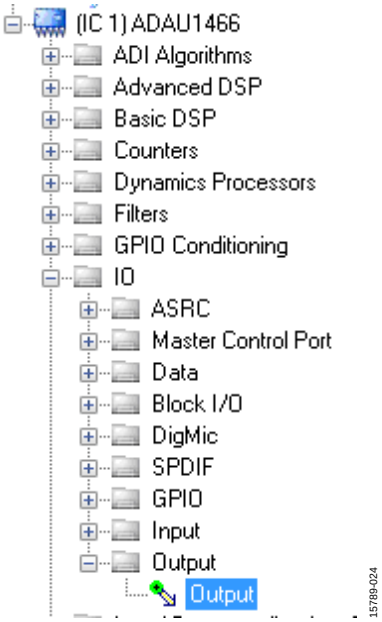

Figure 22. Output Block Selection

      ii. Repeat the previous step to add another output (see Figure 23).

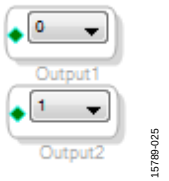

Figure 23. Output Blocks

3. To connect each input channel to its corresponding output channel, click and drag a line, representing a wire, between the blue pin of the input channel and the green pin of the output channel (see Figure 24). Input Channel 0 connects to Output Channel 0 and Input Channel 1 connects to Output Channel 1.

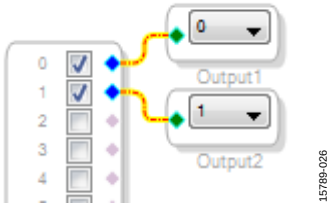

Figure 24. Connected Signal Flow with Stereo Input and Stereo Output

The default register settings in SigmaStudio are configured to match the hardware of the EVAL-ADAU1466Z, including the signal routing between the ADAU1466 and the AD1938 codec.

When these steps are complete, the basic signal flow is complete, and the stereo analog input source passes directly through the SigmaDSP and connects to the stereo analog output.

Add Volume Control

1. To add a volume control block, from the **Volume Controls** > **Adjustable Gain** > **Clickless HW Slew** folder, click **Single Volume** and drag it into the project space to the right of the toolbox.

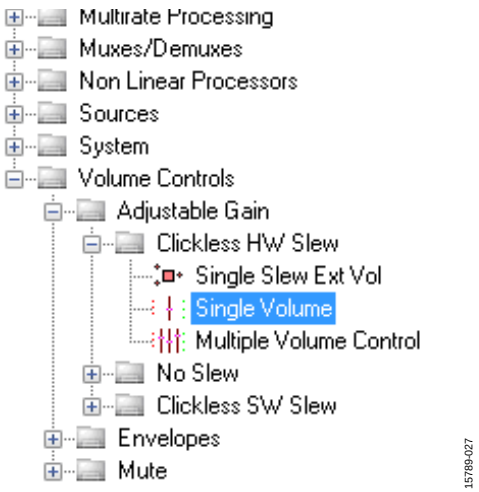

Figure 25. Single Volume Block Selection

2. By default, the volume control block has one input and one output. In other words, it is a single channel. To add another channel, right-click in the empty white space of the **Single-Volume** block, and then from the dropdown menu that appears, select **Grow Algorithm** > **1. Gain (HW Slew)** > **1** (see Figure 26).
3. To delete the existing yellow connection wires (that is, the connections added in Step 3 of the Creating a Basic Signal Flow section), click the connection wires + Delete.

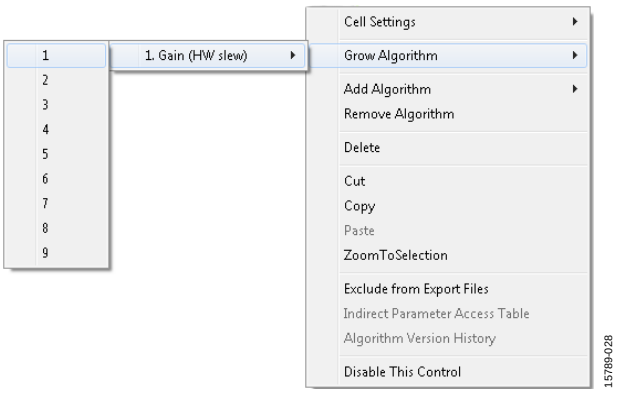

Figure 26. Growing the Volume Control to Two Channels

4. Connect the blocks as shown in Figure 27.

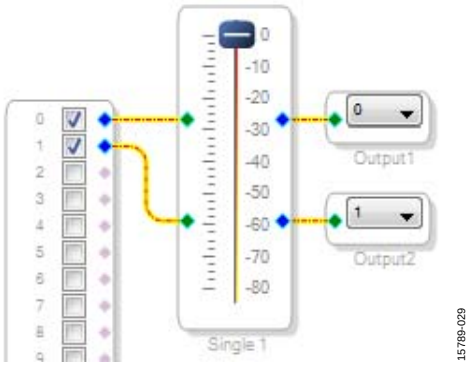

Figure 27. Completed Signal Flow with Volume Control

The schematic is ready to be compiled and downloaded to the evaluation board.

DOWNLOADING THE PROGRAM TO THE DSP

To compile and download the code to the DSP, take the following steps, click the **Link/Compile/Download** button in the main toolbar of SigmaStudio (see Figure 28). Alternatively, press F7.

*Figure 28. **Link/Compile/Download** Button*

After the code has been downloaded to the DSP, the following occurs:

- If the compiler completed compiling the project, the compiled data downloads from SigmaStudio via the USBi to the ADAU1466, and the SigmaDSP starts running.
- The status bar turns from blue to green and the mode displayed changes from **Design Mode** to **Active: Downloaded** in the lower right corner of the window (see Figure 29 and Figure 30). Until this point, SigmaStudio is in design mode, as denoted by the blue bar at the bottom of the screen and the words **Design Mode** displayed in the lower right corner of the SigmaStudio window (see Figure 29).

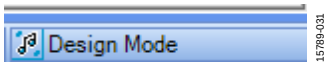

Figure 29. Design Mode and Blue Status Bar

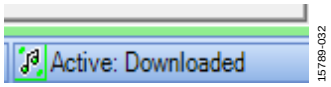

Figure 30. Active Downloaded Mode and Green Status Bar

- The signal flow runs on the evaluation board and the audio passes from the analog input to the analog output. To change the volume in real time, click and drag the volume control slider in the **Schematic** tab.
- If the **Output** window is open at the time of compilation, a compiler output log displays, as shown in Figure 31. The **Output** window can be opened or closed by using the keyboard shortcut CTRL + 4. The **Output** window shows the compiler output log only if it was open when the **Link/Compile/Download** button was clicked.

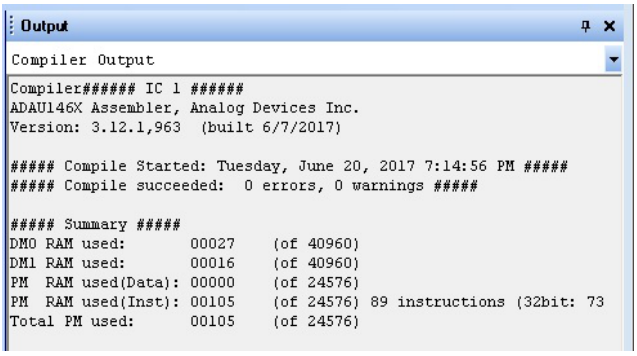

Figure 31. Compiler Output Window

ADDING S/PDIF INPUT AND OUTPUT TO THE PROJECT

The EVAL-ADAU1466Z evaluation board has two optical S/PDIF interfaces. One interface is an input that converts the optical signal to an electrical signal, which is sent to the ADAU1466 S/PDIF receiver (the SPDIFIN pin). The other interface is an optical output that takes the electrical output from the ADAU1466 S/PDIF transmitter (the SPDIFOUT pin) and converts it to an optical signal.

Figure 32 shows the locations of the optical input connector and the optical output connector. The connectors are located on the underside of the PCB.

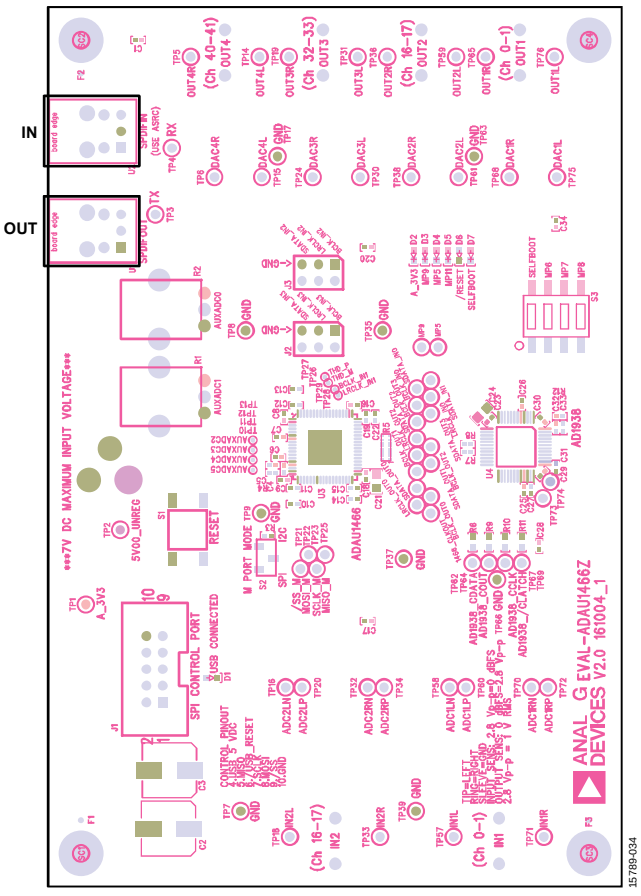

Figure 32. Location of S/PDIF Optical Input (J5) and Output (J6), Rotated 90°

To add an S/PDIF input and output to the project in SigmaStudio, take the following steps:

1. Connect an S/PDIF source to the EVAL-ADAU1466Z evaluation board by using a standard TOSLINK® optical cable and connecting it to the S/PDIF receiver connector, U2 (see Figure 33).

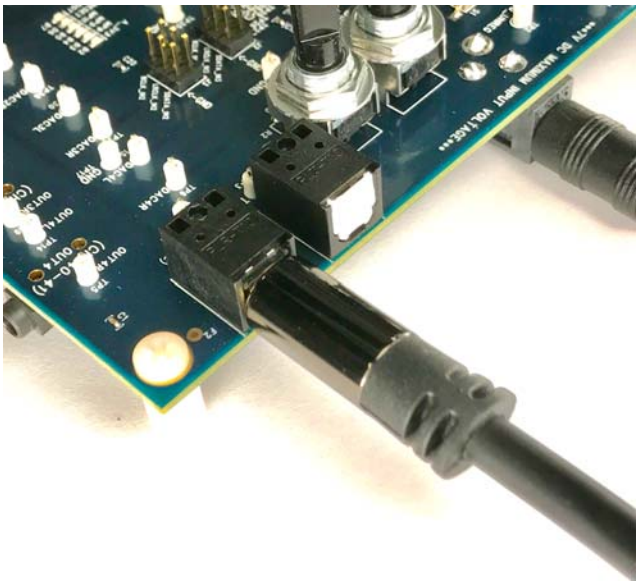

Figure 33. Photograph of the Optical S/PDIF Input Connection

2. Configure the S/PDIF input and output by modifying the ADAU1466 registers as follows:
   a. Click the **Hardware Configuration** tab, then click the **IC 1 – ADAU146x Register Controls** tab at the bottom of the window (see Figure 34).

*Figure 34. **IC 1 - ADAU146x Register Controls** Tab*

   b. Click the **SPDIF** tab (see Figure 36). There are several register control tabs listed across the top of the window. To access the **SPDIF** tab, click the right arrow to scroll (see Figure 35).

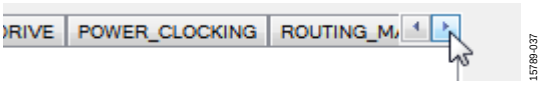

Figure 35. Using the Register Tab Scroll Button

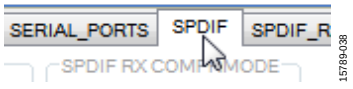

*Figure 36. Selecting the **SPDIF** Tab*

   c. Enable the SPDIF_RESTART register by clicking **Do not restart the audio once a re-lock has occurred** in the **SPDIF RESTART** box. When this button is clicked, the text displayed on the button changes to **Restarts the audio once a re-lock has occurred** and the button color changes from red to green (see Figure 37).

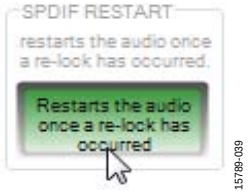

Figure 37. Activating the SPDIF_RESTART Register

   d. To activate the S/PDIF interface, click **Disabled** in the **SPDIF TX EN** box. When this button is clicked, the text displayed on the button changes to **Enabled** and the button color changes from red to green (see Figure 38).

Figure 38. Activating the SPDIF_TX_EN Register

3. Click the **ROUTING_MATRIX** tab (see Figure 39) to allow the configuration of the routing matrix.

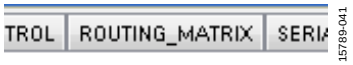

Figure 39. Selecting the ROUTING_MATRIX Tab

4. To configure the S/PDIF receiver signal routing, click the first asynchronous sample rate converter, **ASRC 0** (see Figure 40) and configure ASRC 0 using the dropdown menus until it matches Figure 41. This configuration routes the S/PDIF receiver signal through an ASRC before it is accessed in the DSP core. Routing the signal in this way is necessary because the clock recovered from the S/PDIF source is not synchronous to the ADAU1466.

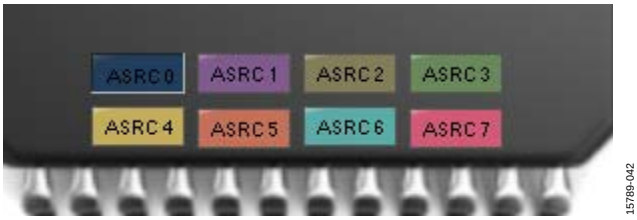

Figure 40. ASRC 0 Control Button

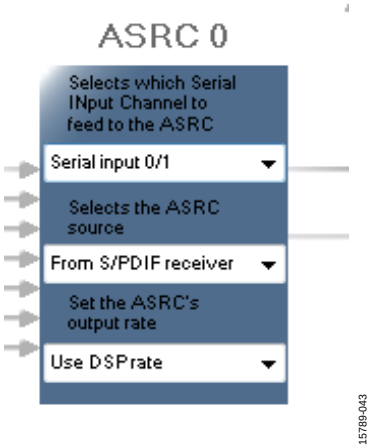

Figure 41. Configuring the ASRC 0 Routing Matrix Registers

5. Configure the S/PDIF transmitter (Tx) signal routing as follows:
   a. Click the **S/PDIF TX** box (see Figure 42).

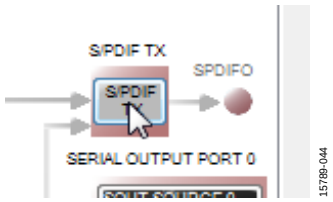

Figure 42. Configuring the S/PDIF Transmitter Routing Matrix Register

   b. From the dropdown menu that appears, select **From DSP** to choose the signal coming from the DSP core (see Figure 43).

Figure 43. Routing the DSP Core Outputs to the S/PDIF Transmitter

   c. Close the dialog box shown in Figure 43.
   d. Confirm that the setting has taken effect by verifying that the color of the **S/PDIF TX** box has changed from gray to black (see Figure 44). If the color of the box changes to black, the DSP core has been routed to the S/PDIF transmitter; therefore, the output of ASRC 0 can be used in the DSP program.

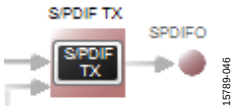

Figure 44. Confirming that the DSP Core Outputs are Routed to the S/PDIF Transmitter

6. Click the **Schematic** tab at the top of the window to return to the schematic design view.
7. Add an S/PDIF input to the project as follows:
   a. From the **IO** > **ASRC** > **From ASRC** folder, click **Asrc Input** (see Figure 45) and drag it into the project space to the right of the toolbox (see Figure 46).

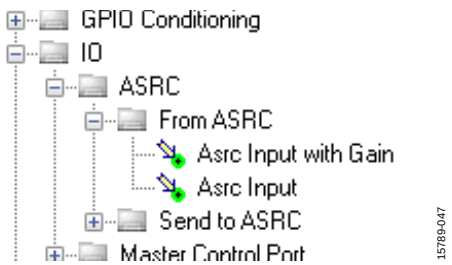

Figure 45. ASRC Input Block Selection

Figure 46. ASRC Input Block

Because the left and right signals of the S/PDIF receiver are passing through the ASRC 0, the input to the DSP program is the **Asrc Input** block in SigmaStudio. This naming convention is such that all blocks in SigmaStudio are named from the perspective of the DSP core. Therefore, the **Asrc Input** block in SigmaStudio represents the input to the DSP from the ASRC outputs. The inputs to the ASRCs themselves are defined in the register window (see Figure 41).

By default, Channel 0 and Channel 1 are active when their corresponding checkboxes are selected. Because the ASRC 0 outputs correspond to Channel 0 and Channel 1, this default configuration can be used (see Figure 46). For reference, a mapping of the ASRC outputs to the corresponding channels on the **Asrc Input** block in the DSP schematic is provided in Table 1.

Table 1. ASRC Output to SigmaStudio Input Channel Mapping

ASRC Output	Corresponding Channels on ASRC Input Block in SigmaStudio
ASRC 0	Channel 0 and Channel 1
ASRC 1	Channel 2 and Channel 3
ASRC 2	Channel 4 and Channel 5
ASRC 3	Channel 6 and Channel 7
ASRC 4	Channel 8 and Channel 9
ASRC 5	Channel 10 and Channel 11
ASRC 6	Channel 12 and Channel 13
ASRC 7	Channel 14 and Channel 15

8. Add two S/PDIF outputs to the project as follows:
   a. From the **IO** > **SPDIF** > **Output** folder, click **Spdif Output** (see Figure 47) and drag it into the project space to the right of the toolbox.

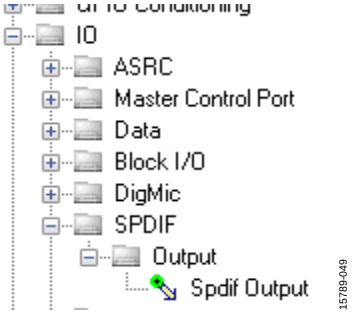

Figure 47. S/PDIF Output Block Selection

   b. Repeat the previous step to add another **Spdif Output** block.
9. Connect the signals from the **Asrc Input** block to the **Spdif Output** blocks so that the resulting signal flow resembles Figure 48.
10. Click the **Link/Compile/Download** button (see Figure 28) or press F7. The signal flow then compiles and downloads to the hardware.
11. Confirm proper operation by checking that any signal input to the S/PDIF optical receiver is copied and output on the S/PDIF optical transmitter.

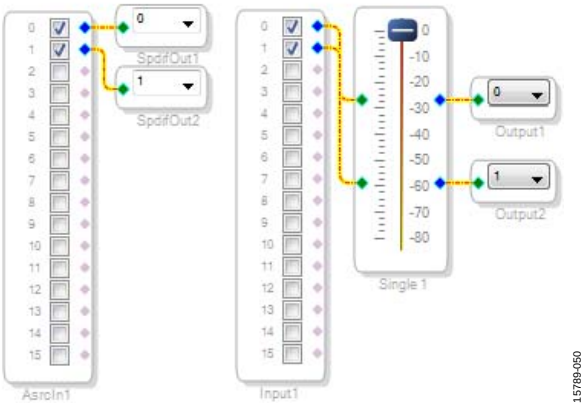

Figure 48. Signal Flow Including S/PDIF Input (via the ASRC) and S/PDIF Output

Add a Filter

To add a filter, take the following steps:

1. Add a **Medium-Size Eq** block to the project space as follows:
   a. From the **Filters** > **Second Order** > **Double Precision** folder, click **Medium-Size Eq** (see Figure 49) and drag it into the project space to the right of the toolbox.

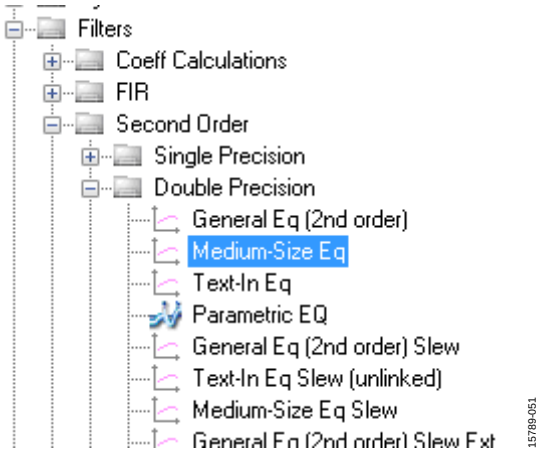

*Figure 49. **Medium-Size Eq** Block Selection*

By default, the block has one input and one output (single-channel). To add another channel, right click in the empty white space of the **Medium-Size Eq** block, then select **Grow Algorithm** > **1. Multi-Channel – Double Precision: Grow Channels** > **1** from the dropdown menu that appears (see Figure 50).

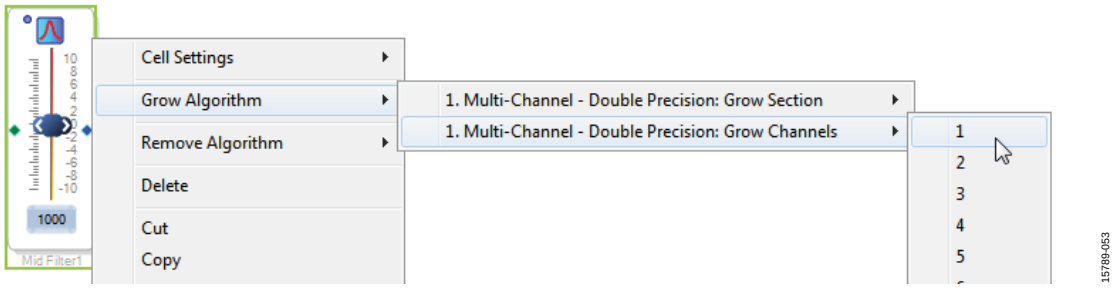

Figure 50. Adding a Channel to the Filter

2. Connect the filter in series between the **Asrc Input** block and the **Spdif Output** blocks so that the filter can be applied to the signals passing through the DSP. The completed signal flow resembles Figure 51.

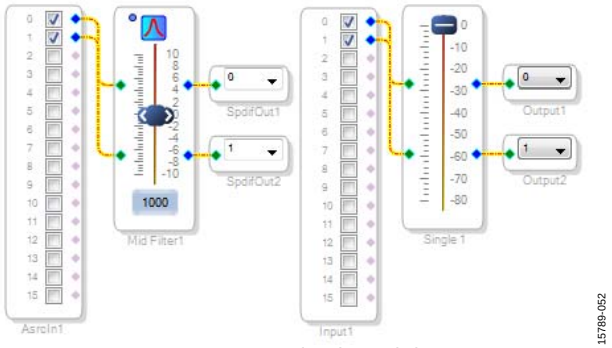

Figure 51. Completed Signal Flow

3. Click the **Link/Compile/Download** button (see Figure 28) or press F7 to compile the signal flow and download it to the hardware. The audio signal passes from the S/PDIF receiver through the ASRCs into the DSP and the EQ filter, and then out on the S/PDIF transmitter. To change the settings of the EQ filter, click the blue icon at top of the block. To change the filter gain in real time while the project is running, drag the control slider in SigmaStudio.

CONTROLLING VOLUME WITH A POTENTIOMETER

The 10-bit auxiliary ADC on the ADAU1466 can eliminate the need for a microcontroller in many applications by using analog control signals as user interface devices. As an example, the EVAL-ADAU1466Z includes two 10 kΩ linear potentiometers connected to Channel AUXADC0 and Channel AUXADC1. These can be used as an inexpensive, versatile, and physical way to control parameters such gain, filter corner frequency, slew rate, and compression level. The following example demonstrates how a potentiometer can be configured as a stereo volume control.

1. Create a new project in SigmaStudio, and use the **Hardware Configuration** tab to use an ADAU1466 as describe above in the Setting Up Communications in SigmaStudio section.
2. Add an input and two output blocks as described in the Creating a Basic Signal Flow section.
3. Add an **Auxiliary ADC Input** block to the project space as follows:
   a. From the **IO** > **GPIO** > **Input** folder, click **Auxiliary ADC Input** (see Figure 52) and drag it into the project space to the right of the toolbox.

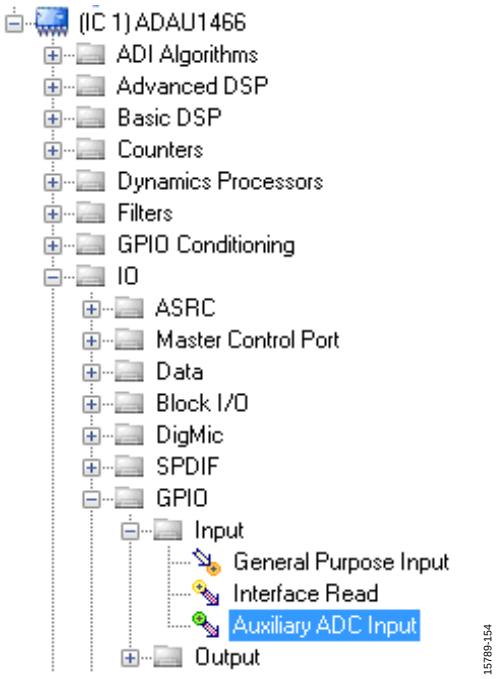

Figure 52. Auxiliary ADC Input Block Selection

4. Add an **Arithmetic Shift** block to the project space as follows:
   a. From the **Basic DSP** > **Arithmetic Operations** folder, click **Arithmetic Shift** (see Figure 53) and drag it into the project space to the right of the toolbox.

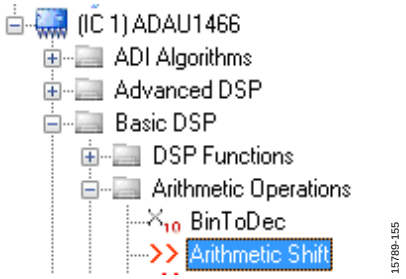

*Figure 53. **Arithmetic Shift** Block Selection*

   b. The arithmetic shift block performs a bitwise right shift or left shift. Click the blue button to select the direction. Ensure the block is performing a left shift. The block appears as shown in Figure 58.
   c. To set the number of bits by which the input are shifted to 14, click and type in the yellow text box. The block appears as shown in Figure 58.

5. Add two **DSP Readback** blocks to the project and set their numeric format as follows:
   a. From the **Basic DSP** > **DSP Function** folder, click **DSP Readback** (see Figure 54) and drag it into the project space to the right of the toolbox.

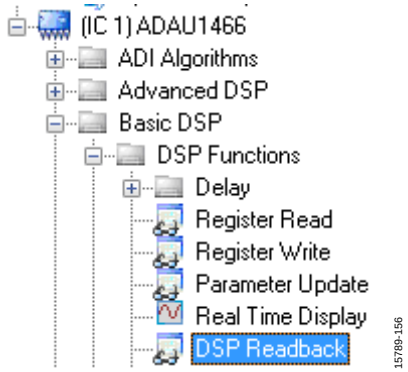

Figure 54. DSP Readback Block Selection

   b. Repeat the previous step to add another **DSP Readback** block.
   c. The **DSP Readback** block uses the USBi interface to read the value of a signal from the memory of the DSP core as the algorithm is executing. The block passes the signal through from its input to its output unchanged.
      i. Press the **Read** button to fetch the instantaneous value of the signal passing through the block. It is also possible to set the block to poll the value repeatedly. This feature is useful for debugging, but it increases the amount of processing, USB communication, and screen refreshes performed by SigmaStudio substantially. Avoid setting a large number of **DSP Readback** blocks to read continuously because this action can cause the PC to run slowly. Note that this action does not affect the real-time processing on the SigmaDSP core.
      ii. On each of the two **DSP Readback** blocks, click on the blue dot to the left of the **Read** button to read both blocks continuously (see Figure 55).

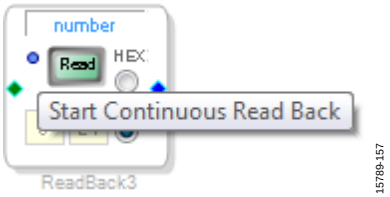

Figure 55. Activating Continuous Read Back

      iii. For one of the DSP readback blocks, change the numeric format used to decode and display of the value of the signal to 32.0 by typing 32 in the left format box then pressing the **TAB** key. SigmaDSP uses a numeric format of 8.24 for audio signals.

6. Add an **Single Slew Ext Volume** block to the project space as follows:
   a. From the **Volume Controls** > **Adjustable Gain** > **Clickless HW Slew** folder, click **Single Slew Ext Vol** (see Figure 56) and drag it into the project space to the right of the toolbox.

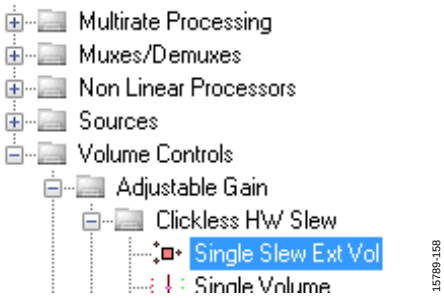

*Figure 56. **Single Slew Ext Vol** Block Selection*

   b. By default, the **Single Slew Ext Vol** block has one audio signal input. To add another channel, right click in the empty white space of the **Single Slew Ext Vol** block, and select **1 > 1. Gain (HW slew) > Grow Algorithm** from the dropdown menu that appears (see Figure 57).

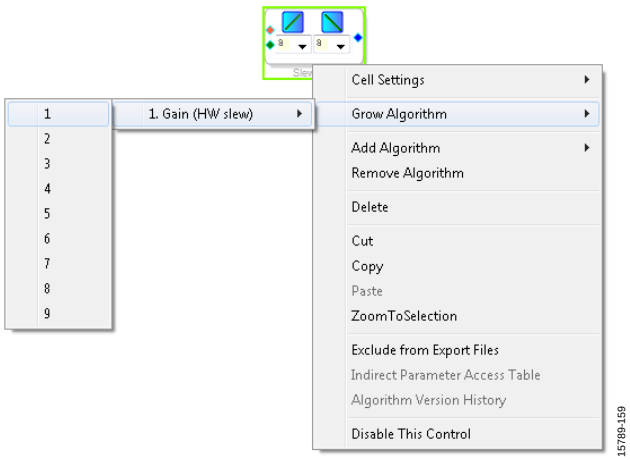

*Figure 57. Growing the **Single Slew Ext Vol** Block to Two Channels*

7. Wire the blocks together as shown in Figure 58. Note that the position of blocks in the diagram does not matter.
8. Click the **Link/Compile/Download** button (see Figure 28) or press F7 to compile the signal flow and download it to the hardware. The audio signal passes from the S/PDIF receiver through the ASRCs into the DSP and the EQ filter, and then out on the S/PDIF transmitter. To change the settings of the EQ filter, click the blue icon at top of the block. Drag the control slider in SigmaStudio to change the filter gain in real-time while the project is running.

The schematic (see Figure 58) shows audio from input Channel 0 and Channel 1 connected to the input of a volume control block. The volume is controlled by the value of the AUXADC1 channel, which is controlled by the left potentiometer, R1.

The output of the auxiliary ADC on the ADAU1466 is a 10-bit integer value in a 32-bit register. The first **DSP Readback** block, before the left shift, displays the output of the ADC in 32.0 format, which can be interpreted as 32 integer bits and 0 fractional bits. When the potentiometer is turned fully counter clockwise, this block reads back the minimum ADC output value of 0. When the potentiometer is turned fully clockwise, this block reads back the maximum ADC output value of 1023 (within the range of the component tolerance).

The native audio format of the ADAU1466 is 8.24. In this example, the volume control multiplies the input signal by a fractional value ranging from 0 (silence) to 1 (unity gain). Therefore, the control signal from the ADC must be left shifted 14 bits to scale the maximum value appropriately.

The second **DSP Readback** block, after the left shift, displays the output of the ADC in 8.24 format, which may be interpreted as 8 integer bits and 24 fractional bits. When the potentiometer is turned fully counter clockwise, this block reads back the minimum ADC output value of 0. When the potentiometer is turned fully clockwise, this block reads back the maximum ADC output value of 1 (within the range of the component tolerance).

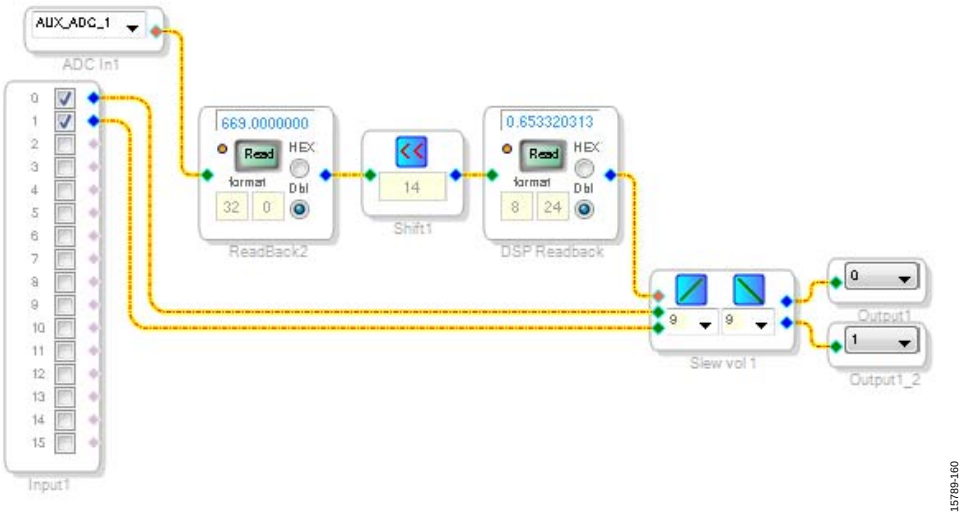

Figure 58. Completed Signal Flow with DSP Read Back

USING THE EVALUATION BOARD

POWER SUPPLY

Power is supplied to the evaluation board using a dc power supply with a female positive center plug. The plug has a 2.1 mm inner diameter, a 5.5 mm outer diameter, and a 9.5 mm length (see Figure 59). The output must range between 5 V and 7 V and must be able to source at least 1.5 A of current. Connect the power supply to Connector J4. The unregulated supply powers the operational amplifiers used in the active audio filters for the analog audio inputs and outputs. An on-board linear regulator (U5) generates the 3.3 V dc supply required for the ADAU1466 and AD1938, as well as other supporting ICs. When the power supply is connected properly, LED D2 (A_3V3) illuminates.

Figure 59. DC Power Supply Plug and Cable

INPUTS AND OUTPUTS

The EVAL-ADAU1466Z provides access to the serial ports, S/PDIF interfaces, multipurpose pins, and auxiliary analog-to-digital converters (ADCs) of the ADAU1466.

AD1938 Codec

Two of the four serial input ports are connected to the ADCs of the AD1938, and all four of the serial output ports are connected to the digital-to-analog converters (DACs) of the AD1938, for a total of four channels of analog audio input and eight channels of analog audio output.

The AD1938 is hardwired in standalone mode, and its serial ports are configured as clock slaves. Therefore, the corresponding serial ports on the ADAU1466 must be set as clock masters. By default, all serial ports on the ADAU1466 are set as clock masters when a new project is created in SigmaStudio.

Standalone mode eliminates the need and ability of the user to configure the registers of the AD1938 via its SPI port. This mode fixes the sample rate of the AD1938 at 44.1 kHz or 48 kHz. It is not possible to change this setting. Even though the ADAU1466 is flexible and can run at any sample rate up to 192 kHz, the analog audio inputs and outputs on the EVAL-ADAU1466Z can be distorted or silent if a sample rate other than 44.1 kHz or 48 kHz is used for the ADAU1466 serial ports.

Stereo Line Inputs

Two stereo input jacks allow four, single-ended, line level, analog input signals. The AD1938 ADC inputs are configured such that the full scale is 2.8 V p-p, which is ~1 V rms for a sine wave. Any signal that exceeds 2.8 V p-p at the audio jack is clipped, which creates distortion. The signals are fed to active low-pass filters and converted to differential pairs before reaching the ADCs of the AD1938. The filters are designed for a system sample rate of 44.1 kHz or 48 kHz.

The stereo input jacks accept standard stereo TRS 3.5 mm (1/8 inch) mini plugs (tip connected to left, ring connected to right, sleeve connected to ground) with two channels of audio (see Figure 60).

Figure 60. Standard Stereo TRS 1/8 Inch Mini Audio Plug and Cable

The signals pass through the AD1938 ADCs and then are sent to the ADAU1466 serial input ports in I²S format. The mapping of input signals to input channels in SigmaDSP and SigmaStudio is shown in Table 2.

Table 2. Mapping of Stereo Analog Input Signals to SigmaStudio Channels

Input Jack	Plug Contact	AD1938 ADC Pins	ADAU1466 Serial Input Pins	Input Channel in SigmaStudio
J9	Left (tip)	ADC1LN, ADC1LP	SDATA_IN0	0
J9	Right (ring)	ADC1RN, ADC1RP	SDATA_IN0	1
J7	Left (tip)	ADC2LN, ADC2LP	SDATA_IN1	16
J7	Right (ring)	ADC2RN, ADC2RP	SDATA_IN1	17

Stereo Line Outputs

Four stereo output jacks allow eight line level analog output signals. The AD1938 DAC outputs are configured such that a full-scale signal is 2.8 V p-p at the jack, which is approximately 1 V rms for a sine wave. The signals output from the DACs are fed to active low-pass filters and then ac-coupled before reaching the output jacks. The filters are designed for a system sample rate of 44.1 kHz or 48 kHz.

The output filters are designed to drive high impedance loads, for instance, loads from active speakers. Some low impedance loads, for example, loads from headphones, can also be driven by these outputs. However, very low impedance loads, for example, loads from passive speakers, cannot be driven by these outputs.

The stereo output jacks accept standard stereo TRS 1/8 inch mini plugs (tip connected to left, ring connected to right, sleeve connected to ground) with two channels of audio (see Figure 60).

The signals pass from the ADAU1466 serial outputs in I²S format to the AD1938 DACs, where they are converted to analog signals and sent through the output filters to the output jacks. The mapping among the SigmaStudio output channels, output serial ports, and output jacks is shown in Table 3.

S/PDIF Optical Transmitter and Receiver

The ADAU1466 S/PDIF interfaces are connected directly to optical transmitter and receiver connectors, which convert the electrical signals to and from optical signals, respectively. The connectors accept standard TOSLINK connectors and optical fiber cables (see Figure 61).

Figure 61. TOSLINK Connector and Optical Fiber Cable for S/PDIF Input and Output

The ADAU1466 S/PDIF receiver accepts signals with sample rates between 18 kHz and 192 kHz. Because the incoming signal is asynchronous to the system sample rate, an ASRC must be used to convert the sample rate of the incoming signal. Optionally, the SigmaDSP core can be configured to start processing audio samples based on the sample rate of the incoming S/PDIF receiver signal, meaning that no ASRC is required. However, using an ASRC is strongly recommended for performance and reliability reasons.

The ADAU1466 S/PDIF transmitter typically transmits signals from the DSP core, meaning that the sample rate of the audio coming out of the S/PDIF transmitter on the EVAL-ADAU1466Z is typically 44.1 kHz or 48 kHz. Optionally, the S/PDIF transmitter can be configured in a pass through mode, where it simply transmits a copy of the signal directly from the receiver.

Both the S/PDIF receiver and transmitter carry two channels of uncompressed audio.

Serial Audio Interface

Two of the four ADAU1466 serial input ports are connected to the AD1938. Because the AD1938 is in standalone mode, the device always drives the SDATA_IN0 and SDATA_IN1 pins of the ADAU1466. As a result, external data signals cannot be input to SDATA_IN0 or SDATA_IN1.

However, the remaining two serial input ports (SDATA_IN2 and SDATA_IN3, along with their corresponding clock pins, BCLK_IN2, LRCLK_IN2/MP12, BCLK_IN3, and LRCLK_IN3/MP13), are accessible directly via the J2 and J3 headers (see Figure 62).

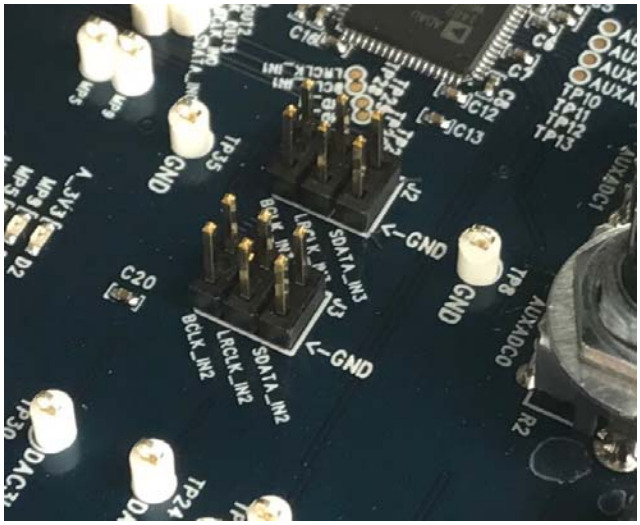

Figure 62. Serial Input Port 2 and Serial Input Port 3 Signal Access Headers

Table 3. Mapping of SigmaStudio Channels to Output Jacks

Output Jack	Plug Contact	AD1938 DAC Pin	ADAU1466 Serial Output Pin	Output Channel in SigmaStudio
J10	Left (tip)	OL1	SDATA_OUT0	0
J10	Right (ring)	OR1	SDATA_OUT0	1
J8	Left (tip)	OL2	SDATA_OUT1	16
J8	Right (ring)	OR2	SDATA_OUT1	17
J6	Left (tip)	OL3	SDATA_OUT2	32
J6	Right (ring)	OR3	SDATA_OUT2	33
J5	Left (tip)	OL4	SDATA_OUT3	40
J5	Right (ring)	OR4	SDATA_OUT3	41

Standard headers with 0.1 inch (2.54 mm) spacing, provide connections from external sources. The J2 and J3 headers each comprise two columns and three rows of pins. There is one signal column and one ground column. Always connect at least one ground wire between the header and the external signal source to maintain proper signal integrity. A standard ribbon cable provides signal integrity over longer distances because signal wires are separated by ground wires (see Figure 63).

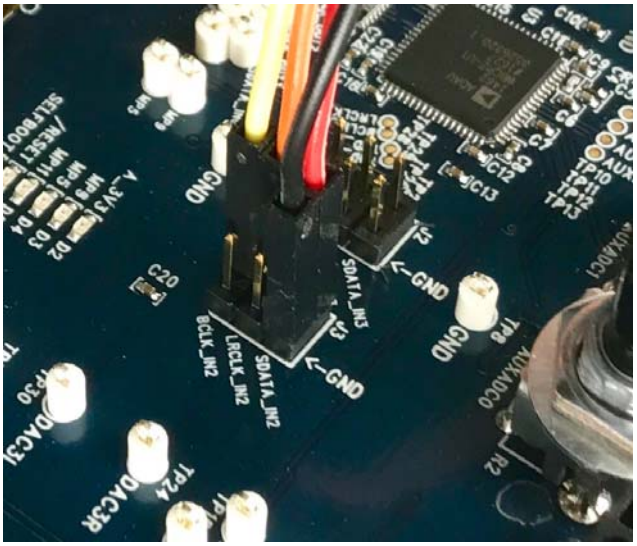

Figure 63. Connecting External I²S Signals to Serial Input Port 2

The signals passing between the ADAU1466 serial output ports and the AD1938 DAC are also accessible via the test points that are situated between the two ICs. Signals can be tapped from these test points and connected to external digital audio sinks, if desired (see Figure 64). When connecting these signals to external devices, connect at least one ground signal to maintain signal integrity.

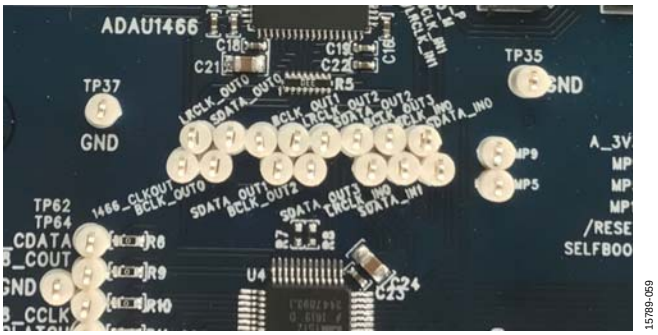

Figure 64. Test Points for Monitoring Digital Audio Signals

MULTIPURPOSE (MP) PINS

The multipurpose pins on the ADAU1466 can be used for general-purpose inputs or outputs when configured as such using the ADAU1466 control registers. Of the 14 multipurpose pins, three are connected to switches that pull them low or tie them high, three are on test points and connected to high impedance inputs to LED drivers, and two are available headers. The remaining six pins are used for other functionality and are, therefore, unavailable for use as multipurpose pins.

The signal from the LRCLK_OUT1/MP5 pin is fed to an inverter that drives LED D4. The signal from the LRCLK_OUT3/MP9 pin is fed to an inverter that drives LED D3. The signal from the LRCLK_IN1/MP11 pin is fed to an inverter that drives LED D5.

The five multipurpose pins available for use as general-purpose inputs or outputs, along with their access points on the evaluation board, are described in Table 4.

Table 4. Multipurpose Pins and Hardware Access Points

MP Pin	Connection	Access Point
LRCLK_OUT1/MP5	Input to inverter (LED D4)	TP56
LRCLK_OUT3/MP9	Input to inverter (LED D3)	TP48
LRCLK_IN1/MP11	Input to inverter (LED D5)	TP29
LRCLK_IN2/MP12	Pin multiplexed with LRCLK_IN2	Header J3, Pin 4
LRCLK_IN3/MP13	Pin multiplexed with LRCLK_IN3	Header J2, Pin 4

To configure the operation of the multipurpose pins, navigate to the **MULTIPURPOSE** tab in the **Hardware Configuration** tab in SigmaStudio (see Figure 65).

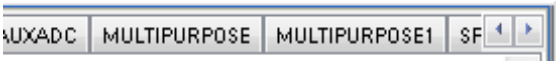

Figure 65. Multipurpose Pin Configuration in SigmaStudio

AUXILIARY ADC PINS

The ADAU1466 has a 10 bit, successive approximation register (SAR) ADC multiplexed across six input channels. Channel AUXADC0 and Channel AUXADC1 are connected to linear Potentiometer R1 and Potentiometer R2. Channel AUXADC2 to Channel AUXADC5 are accessible on test points next to the ADAU1466. Inputs to the ADCs between 0 V and 3.3 V can be connected to these pads and then used in the SigmaStudio signal flow (see Figure 66).

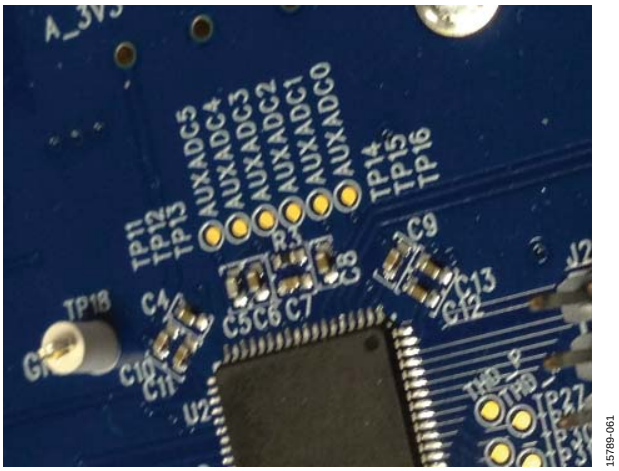

Figure 66. Potentiometers and Copper Pads for Inputting Signals to the Auxiliary ADC

COMMUNICATIONS HEADER

The communications header is a 10-pin header designed to work with the EVAL-ADUSB2EBZ or USBi. The SPI signals are wired from the communications header to the corresponding SPI slave port pins on the ADAU1466. The I^2C pins are not used in this design. A reset line is also included, which allows the user to reset the devices on the board via a command in SigmaStudio. When the USBi is connected and powered and the computer recognizes the USBi on its USB 2.0 port, LED D1 illuminates (see Figure 10).

SELF BOOT

A 1 Mb, 20 MHz, SPI, serial EEPROM memory is included on the EVAL-ADAU1466Z evaluation board. The ADAU1466 is capable of booting and executing a program without help from an external microcontroller. This feature allows any project developed within SigmaStudio to execute when the ADAU1466 powers up or on a rising edge of the $\overline{\text{RESET}}$ pin. Position 1 of Switch S3 switch, the top position of the DIP switch (see Figure 67), sets the state of the SELFBOOT pin of the ADAU1466, which determines whether a self boot operation occurs.

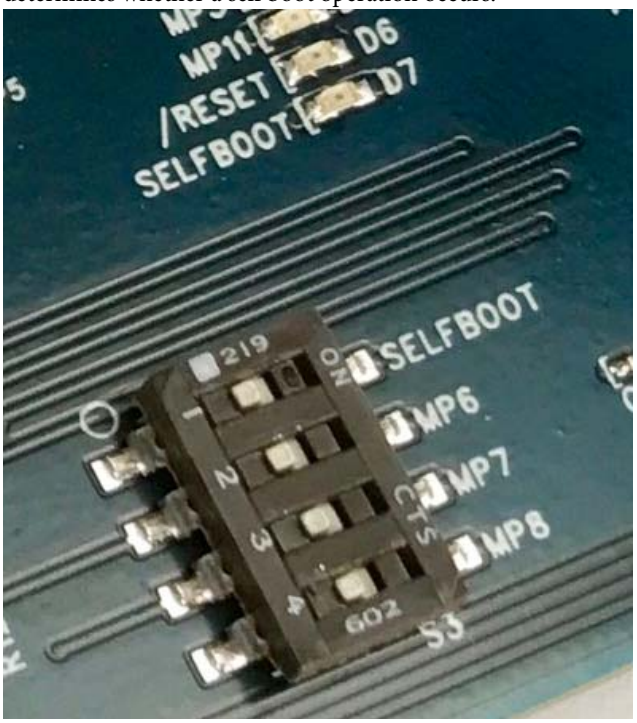

Figure 67. Self Boot EEPROM and Slide Switch

To use the self boot functionality, take the following steps:

1. Add an **E2Prom** block to the project space of the **Hardware Configuration** tab. From the **Processors (ICs / DSPs)** folder, click **E2Prom** (see Figure 68) and drag it into the project space to the right of the toolbox.

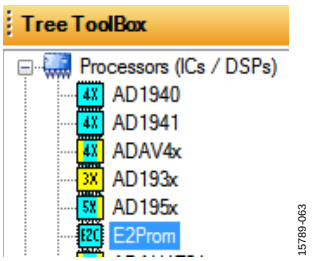

Figure 68. E2Prom IC Selection in SigmaStudio

2. Connect the green input pin of the **E2Prom** IC to one of the available blue output pins of the **USB Interface** block.
3. Set the communication mode to **SPI 0x1 ADR0** (see Figure 69). (There is no physical connection between the USBi connector and the EEPROM on the EVAL-ADAU1466Z. SigmaStudio writes a small program to the ADAU1466, which then writes the self boot data from the master SPI port to the EEPROM.)

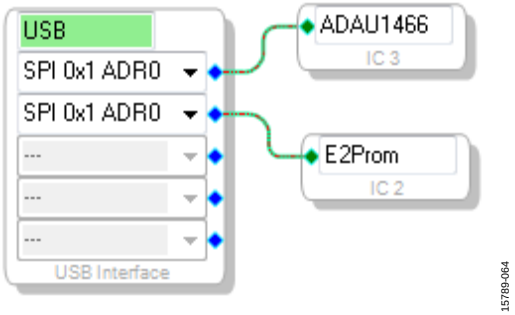

Figure 69. E2Prom Setup in Hardware Configuration Tab

4. Before downloading the self boot data to the EEPROM, click the **Link-Compile-Download** button (see Figure 28) or press F7 to compile the SigmaStudio project file.
5. When writing to the EEPROM, set the self boot switch (Position 1 of Switch S3) to the disabled position.
6. Right click the empty white space in the **ADAU1466 IC** block in the **Hardware Configuration** tab of SigmaStudio. From the menu that appears, select **Self-boot Memory**, then **Write Latest Compilation through DSP** (see Figure 70).

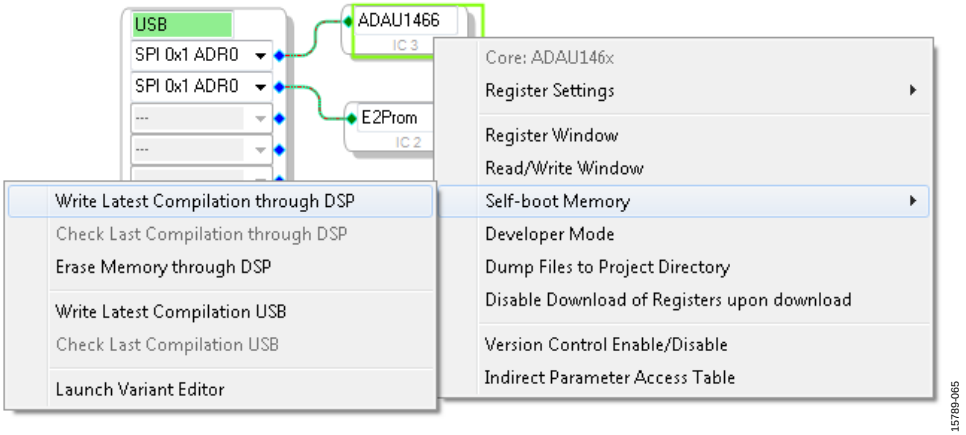

Figure 70. Writing to the EEPROM Through the ADAU1466 Master SPI Port

7. An **EEPROM Properties** dialog box appears. Enter the appropriate values into the text fields as shown in Figure 71, then click **OK**.

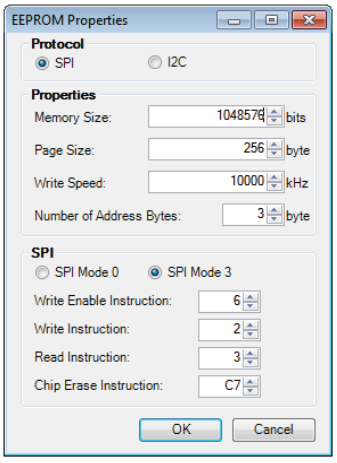

Figure 71. EEPROM Properties Window and Required Settings

8. A warning dialog box appears to remind the user that executing an external memory write erases and overwrites any data currently stored on the EEPROM (see Figure 73). Click **OK** to proceed.

9. SigmaStudio begins the EEPROM write operation. This operation can take several minutes to complete (see Figure 72). When the status window disappears, the operation is complete.

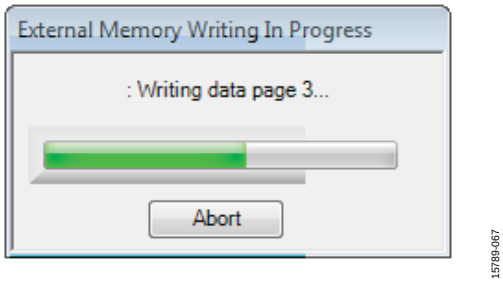

Figure 72. External Memory Write Operation Status Window

To execute a self boot operation, take the following steps:

1. Set the self boot switch (S2) to enabled.
2. Press and release the RESET push-button (S1).

A self boot operation is then performed, and the ADAU1466 runs a program.

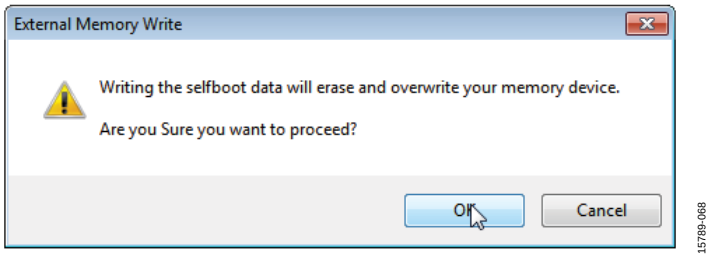

Figure 73. External Memory Erase and Overwrite Warning Window

RESET

To manually reset the ADAU1466 and AD1938, press and release the RESET push-button, S1 (see Figure 74). A reset generator circuit toggles the reset pins on the ADAU1466 and AD1938 to perform a full hardware reset of both devices.

Figure 74. Manual Reset Push-Button

To generate a reset in software, right click in the empty white border of the **USB Interface** block in the **Hardware Configuration** tab, and then choose **Device Enable/Disable** from the menu that appears (see Figure 75). Performing this action once sets the system reset signal to logic low.

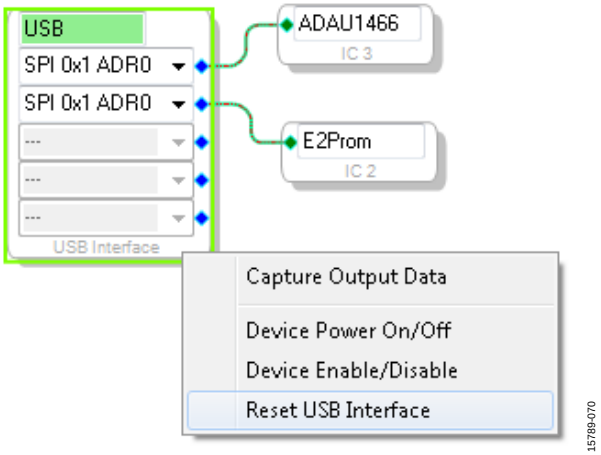

Figure 75. Toggling the Reset Signal in SigmaStudio

STATUS LEDS

Six status LEDs provide information about the state of the EVAL-ADAU1466Z evaluation board (see Figure 76). For additional information pertaining to the status LEDs, see Table 6.

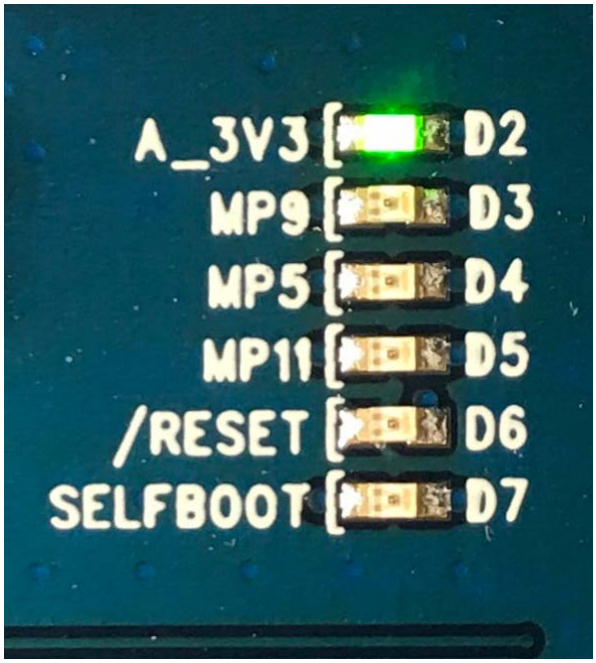

Figure 76. Status LEDs

HARDWARE DESCRIPTION

ICs

Table 5. IC Descriptions

Reference	Functional Name	Description
U1	Everlight PLT133/T8 optical transmitter	S/PDIF optical (TOSLINK) output.
U2	Everlight PLT133/T10W optical receiver	S/PDIF optical (TOSLINK) input.
U3	ADAU1466 SigmaDSP audio processor	Acts as an audio hub for all audio inputs and outputs in the system and performs digital signal processing on those input and output signals.
U4	AD1938 audio codec	Converts analog audio inputs to digital data for the ADAU1466 processor and takes digital data back from the ADAU1466 to convert to analog audio outputs signals.
U5	ADP3338AKCZ3.3RL or ADP3338AKCZ3.3RL7 LDO voltage regulator	Accepts the unregulated dc supply voltage between 5 V and 7 V that is provided on Connector J4 and regulates the supply voltage down to 3.3 V.
U7	ADM811TARTZ reset supervisor	Generates a master reset signal for the ADAU1466 and the AD1938 if the RESET push-button (S1) is pressed or if SigmaStudio sends a reset command via the USBi.
U10	Microchip 25AA1024 serial EEPROM	Stores data, allowing the ADAU1466 to perform a self boot operation.
U6, U8, U9, U11, U12, U13, U15, U17	ADA4841-2 dual, low power, low noise, and low distortion rail-to-rail output amplifier	Implements the analog audio filtering required for the stereo line inputs and outputs.
U14	74ACT04SC hexadecimal inverter	Buffers logic signals and drives status LEDs.

STATUS LEDs

Table 6. LED Descriptions

Reference	Functional Name	Description
D1	USB connected	Illuminates when the USBi is recognized by Windows after the USBi is connected to Control Port J1 and the USB 2.0 port of the computer.
D2	3.3 V supply status LED	Illuminates when the output of the ADP3338AKCZ3.3RL or ADP3338AKCZ3.3RL7 LDO voltage regulator has reached a level sufficient to exceed the V_{IH} logic high input level of the 74ACT04SC inverter. (When this LED is illuminated, it does not guarantee that the LDO output is 3.3 V. It only shows that the LDO output is about 2 V or greater. To perform more detailed measurements of the LDO output level, check the voltage on the A_3V3 test point, TP1.)
D3	MP9 general-purpose LED	Illuminates when the status of the ADAU1466 LRCLK_OUT3/MP9 pin is set to logic high by the ADAU1466.
D4	MP5 general-purpose LED	Illuminates when the status of the ADAU1466 LRCLK_OUT1/MP5 pin is set to logic high by the ADAU1466.
D5	MP11 general-purpose LED	Illuminates when the status of the ADAU1466 LRCLK_IN1/MP11 pin is set to logic high by the ADAU1466.
D6	Master reset status LED	Illuminates when the master reset signal being generated by the ADM811TARTZ reset supervisor IC is logic low, which puts the ADAU1466 and AD1938 into hardware reset. LED D3 does not illuminate when the master reset signal is logic high and the ADAU1466 and AD1938 are out of reset.
D7	Self boot status LED	Illuminates when the self boot switch (Position 1 of Switch S3) is set to the on position, signifying that a self boot operation is to be executed on the rising edge of the ADAU1466 $\overline{\text{RESET}}$ signal or when ADAU1466 is powered up. LED D2 does not illuminate when the self boot slide switch (S2) is set to the disabled, which signifies that no self boot operation is to occur.

SWITCH AND PUSH-BUTTON

Table 7. Switch and Push-Button Descriptions

Reference	Functional Name	Description
S1	Reset push-button	When this switch is pressed and released, a reset signal is generated, which causes the ADM811TARTZ reset supervisor to generate a master reset signal for the ADAU1466 and AD1938.
S2	Master port mode switch	This switch selects whether the master port operated in SPI mode or I^2C mode.
S3	Self boot, MP6, MP7, and MP8 switches	When in the on position, Position 1 of Switch S3 asserts the SELFBOOT pin of the ADAU1466. When in the on position, Position 2 of Switch S3, Position 3 of Switch S3, and Position 4 of Switch S3 tie the MP6, MP7, and MP8 pins high, respectively. When in the off position, these switches pull the MP6, MP7, and MP8 pins low.

EVALUATION BOARD SCHEMATICS AND ARTWORK

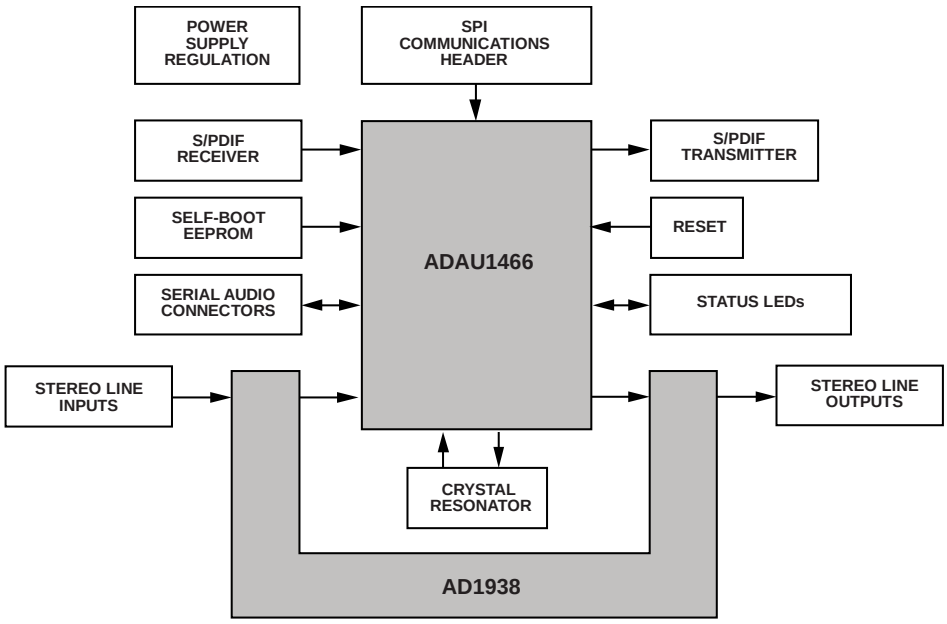

Figure 77. Functional Block Diagram

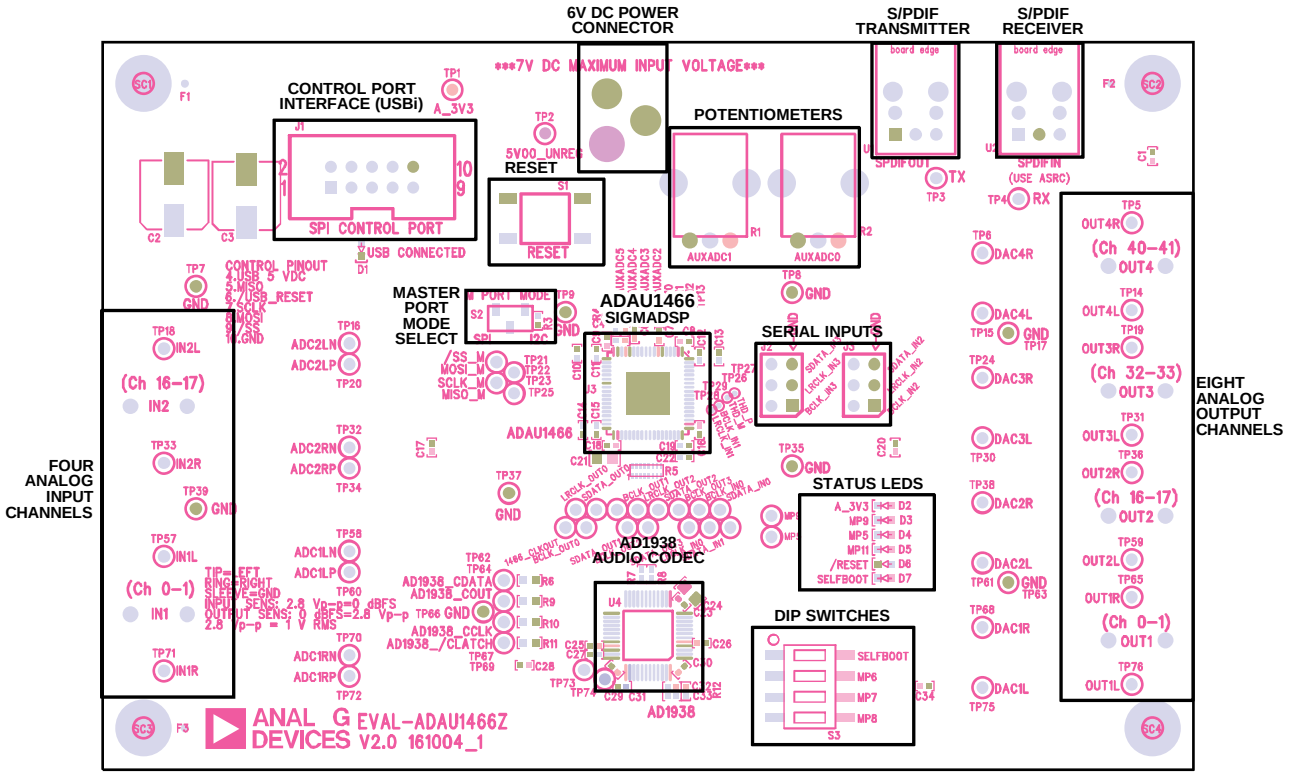

Figure 78. Evaluation Board Layout Block Diagram

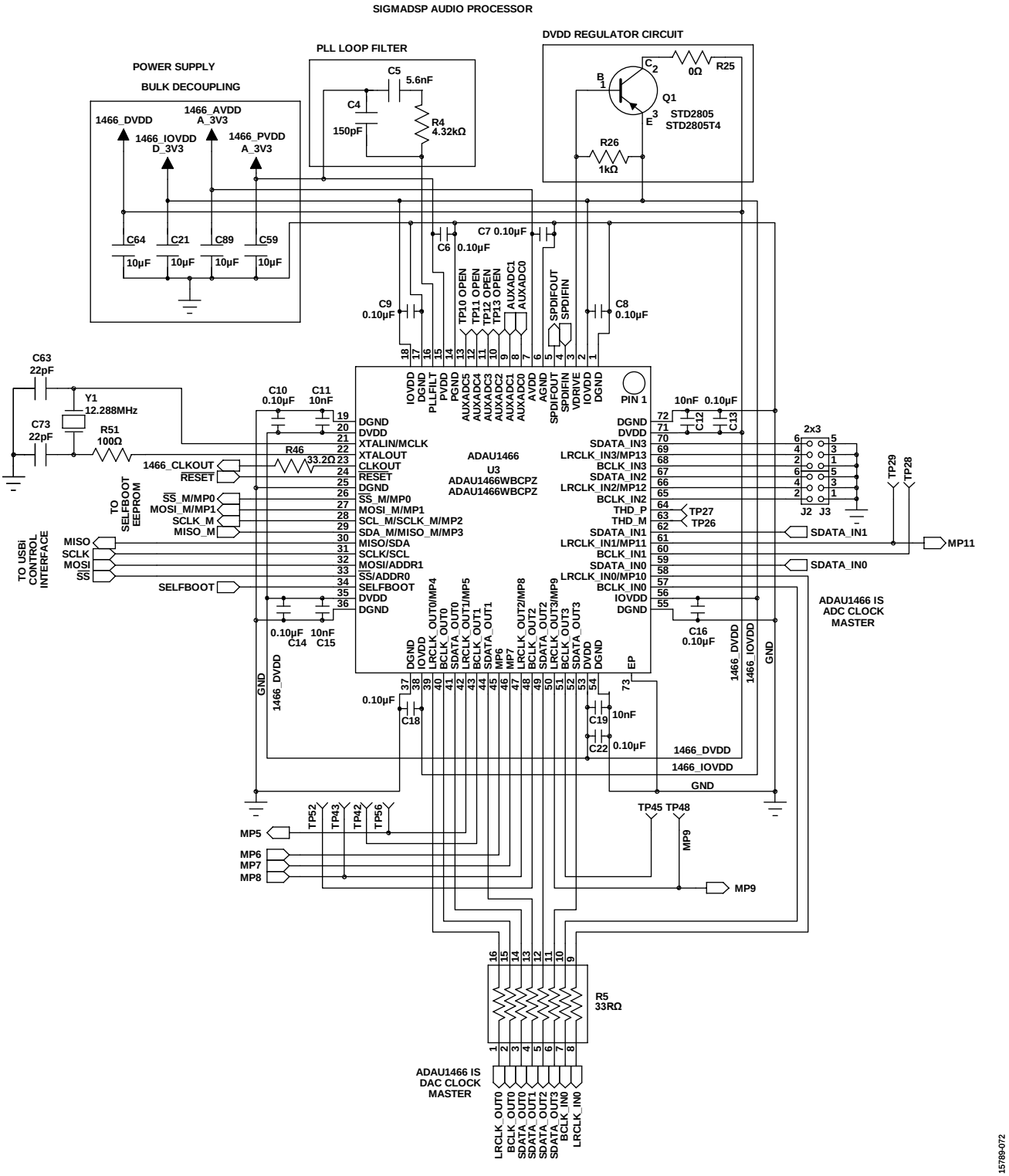

Figure 79. SigmaDSP Audio Processor Schematic

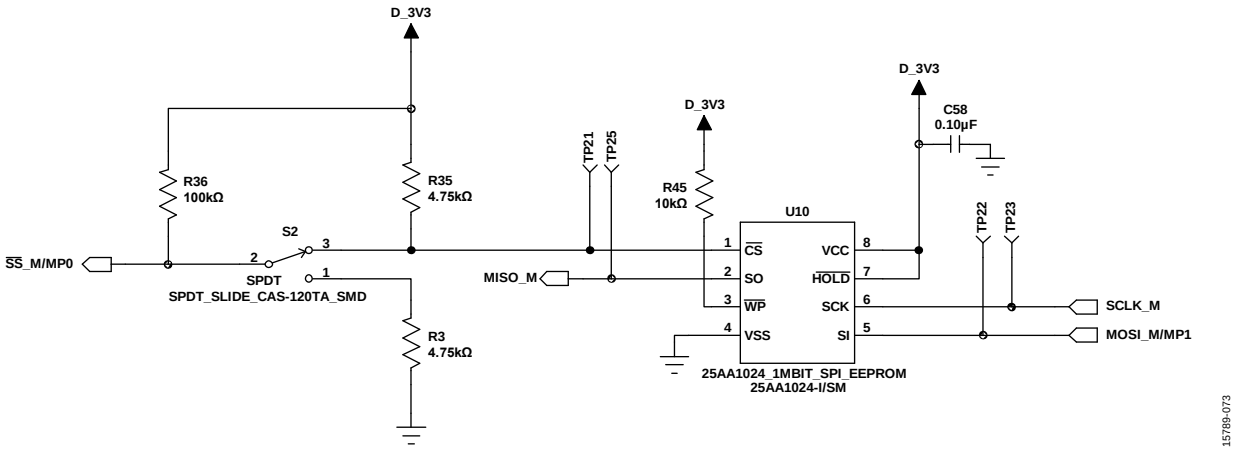

Figure 80. Self Boot Circuit Schematic

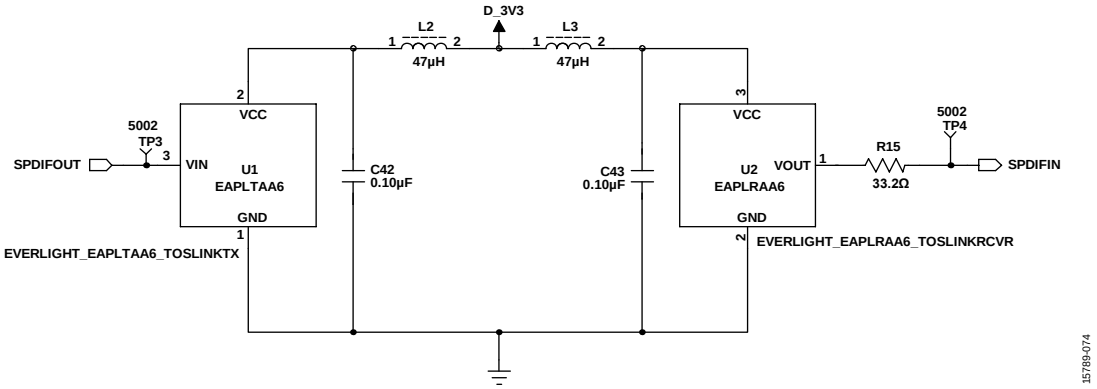

Figure 81. S/PDIF Optical Interfaces Schematic

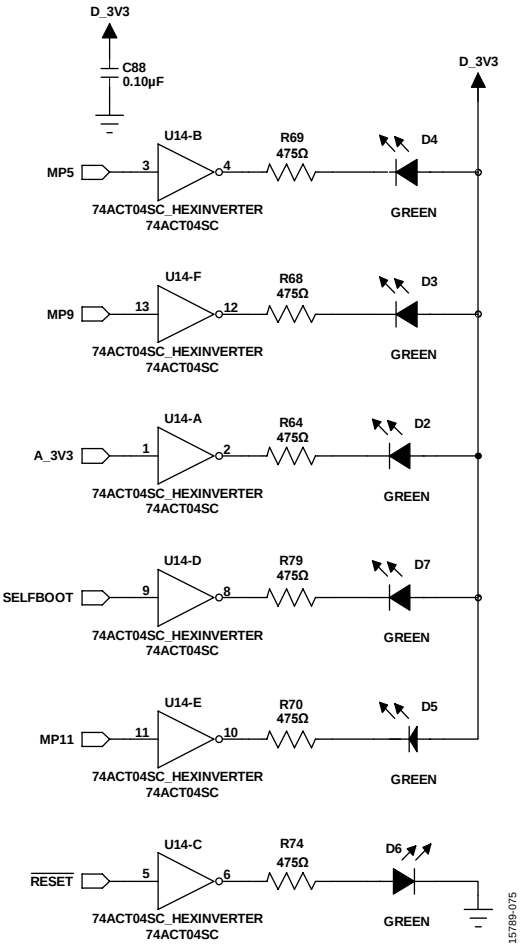

Figure 82. Status LEDs Schematic

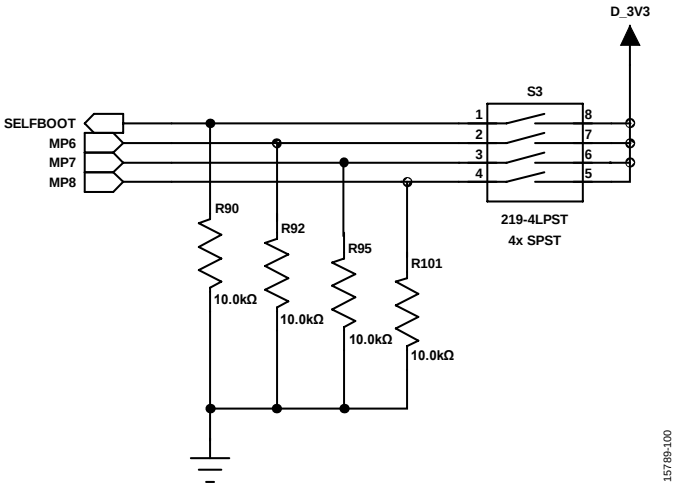

Figure 83. DIP Switch Schematic

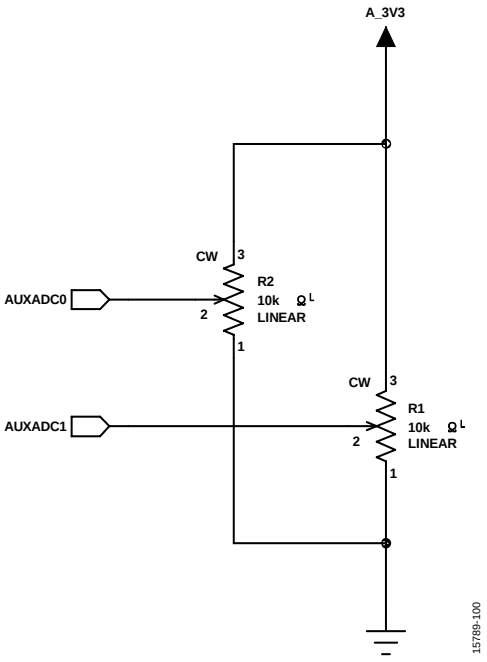

Figure 84. AUXADC Potentiometer Schematic

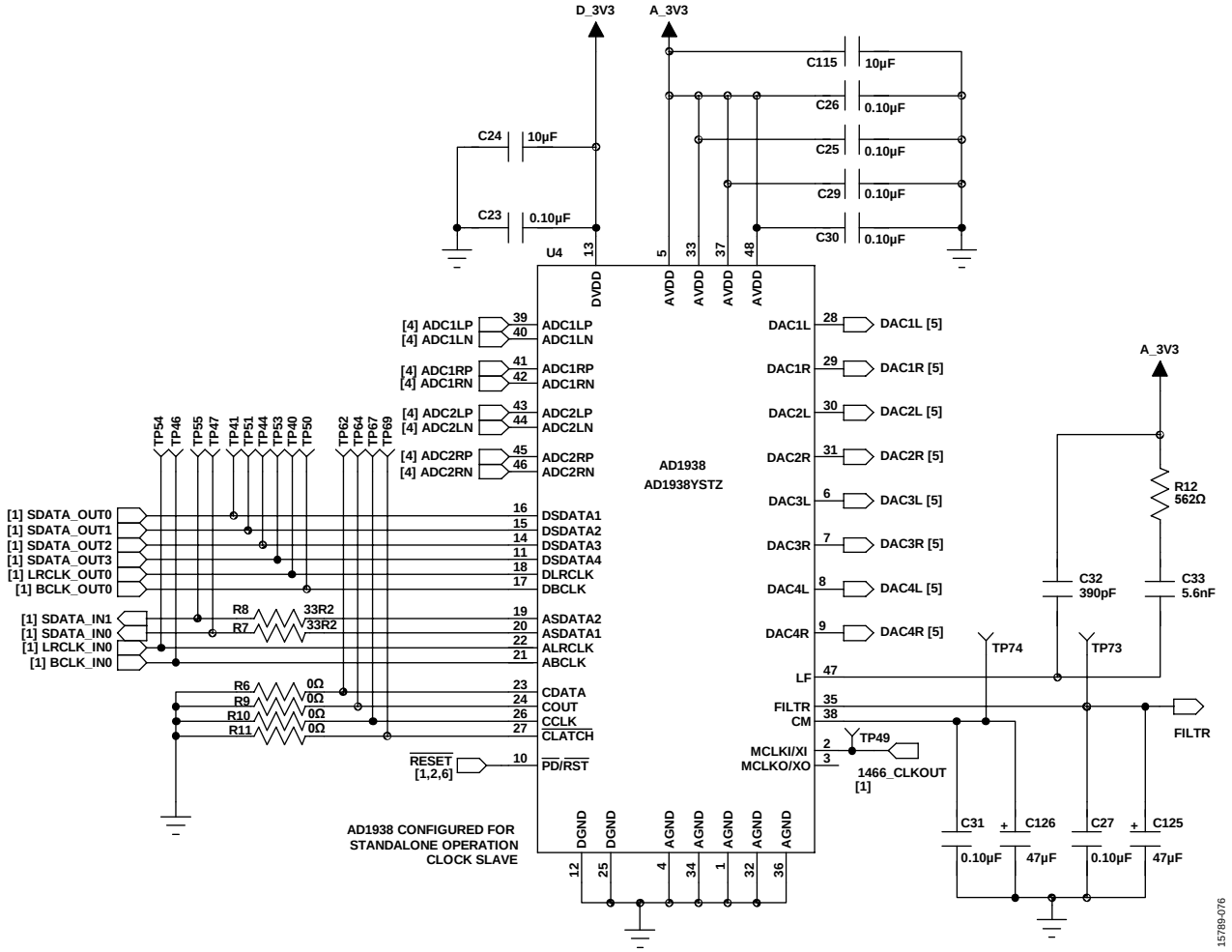

Figure 85. AD1938 Audio Codec Schematic

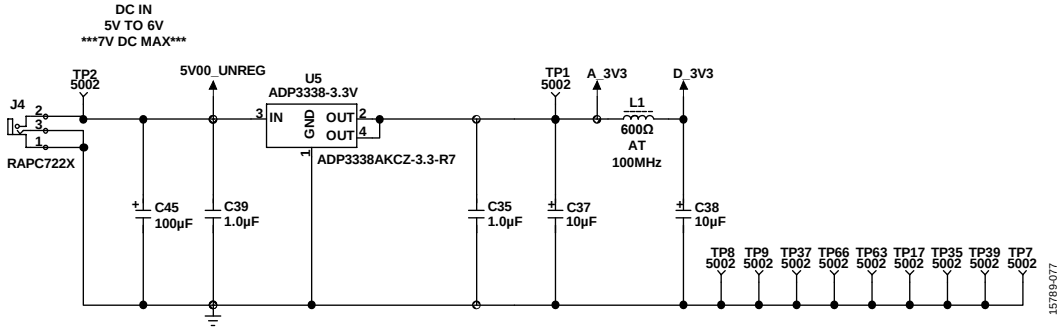

Figure 86. Power Supply Schematic

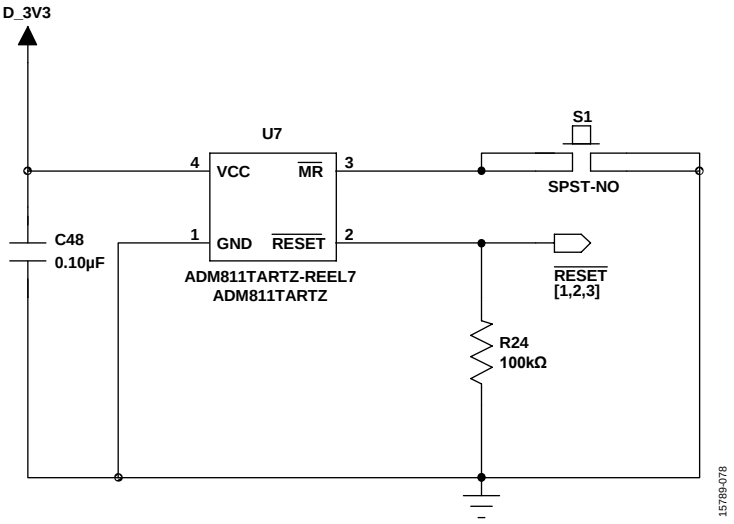

Figure 87. Reset Generator Circuit Schematic

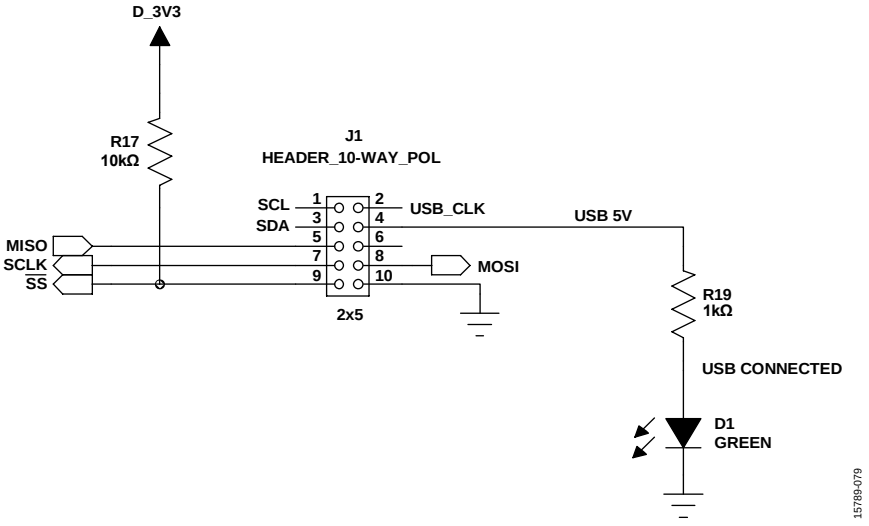

Figure 88. SPI Communication Interface Header Schematic

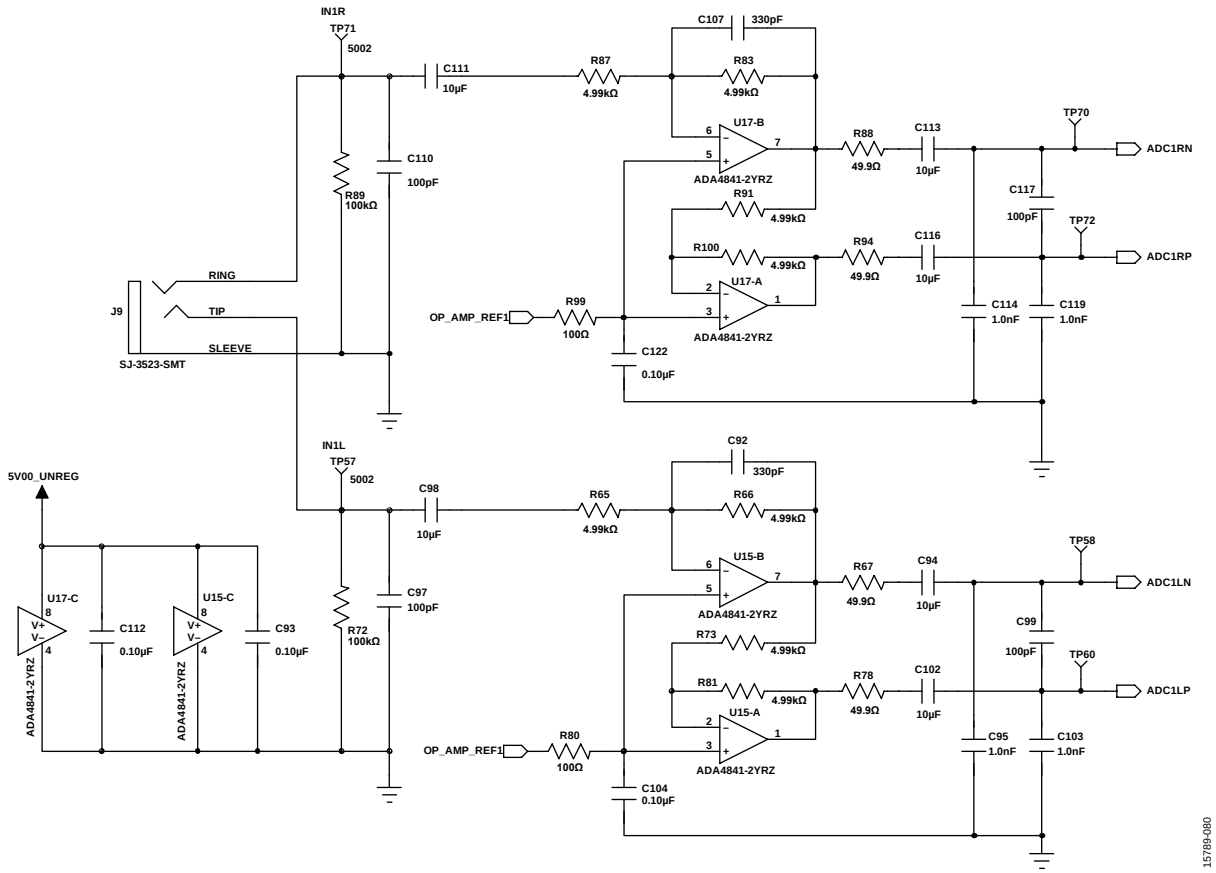

Figure 89. Analog Input Channel 0 and Channel 1 Schematic

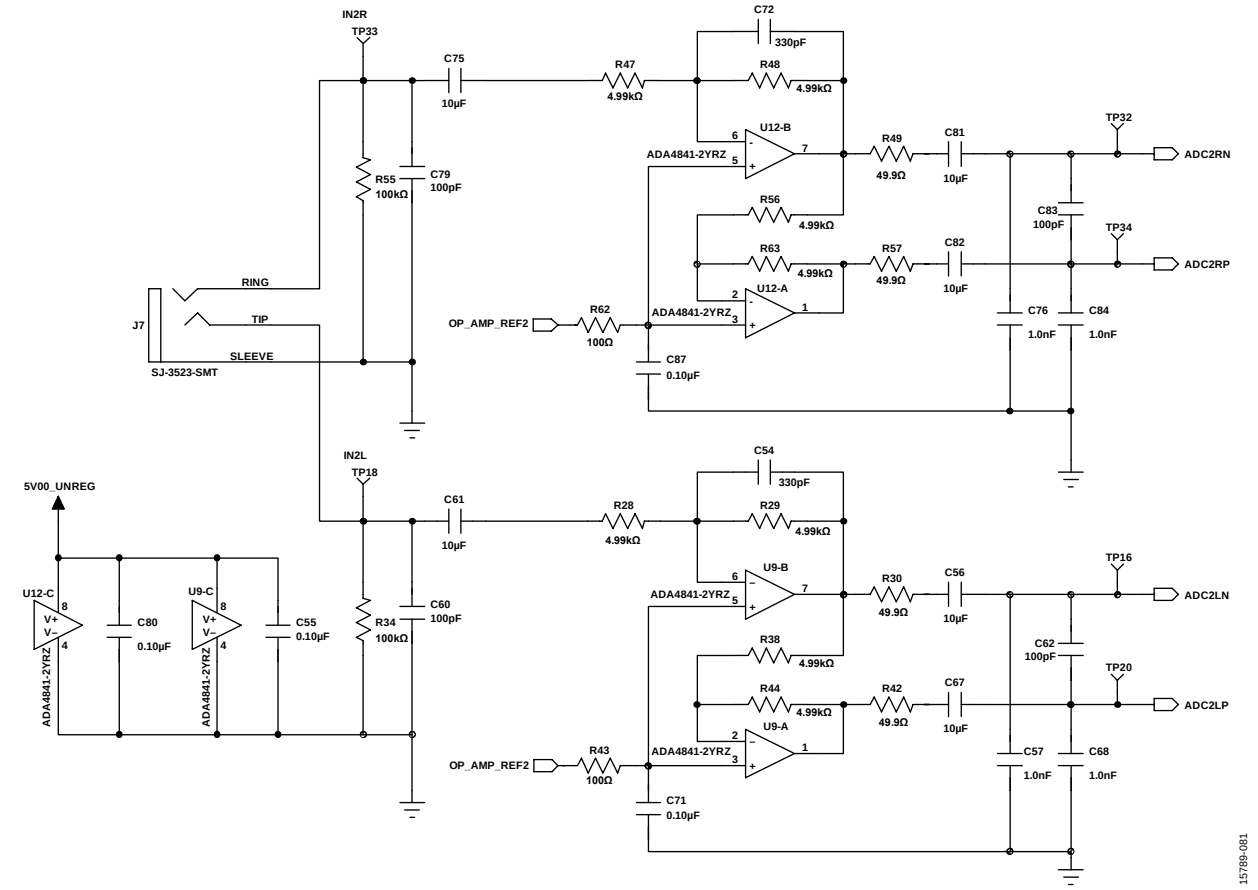

Figure 90. Analog Input Channel 16 and Channel 17 Schematic

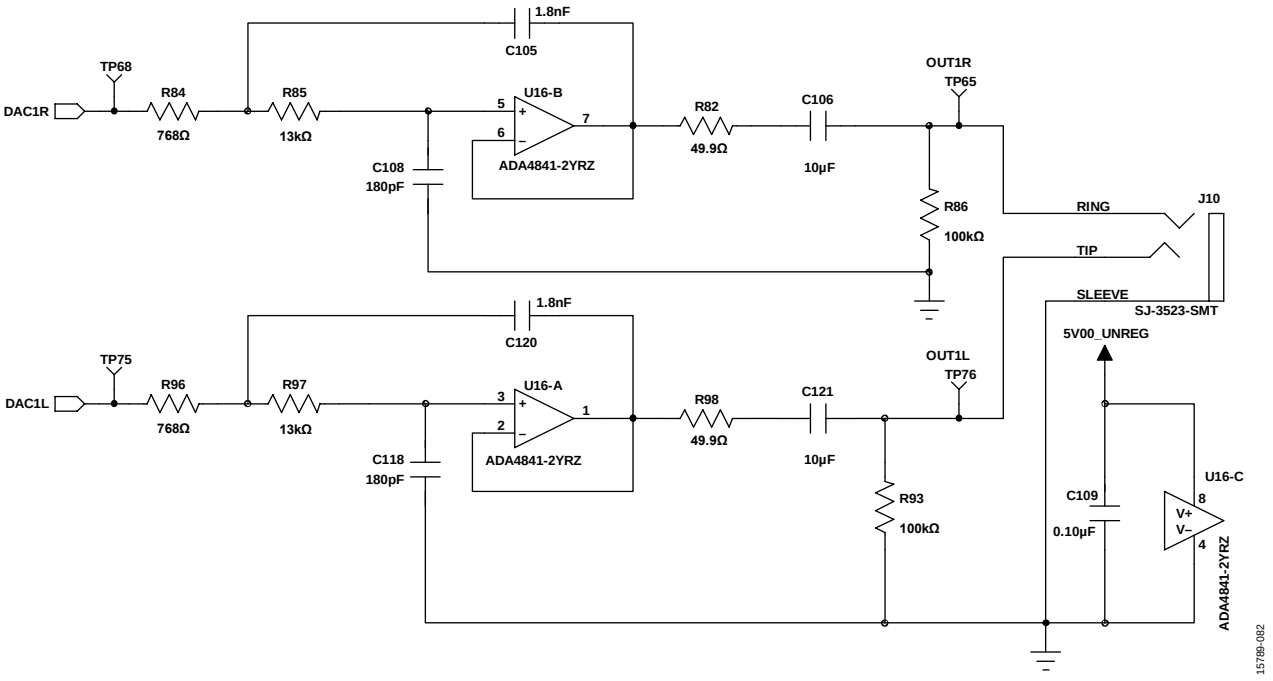

Figure 91. Analog Output Channel 0 and Channel 1 Schematic

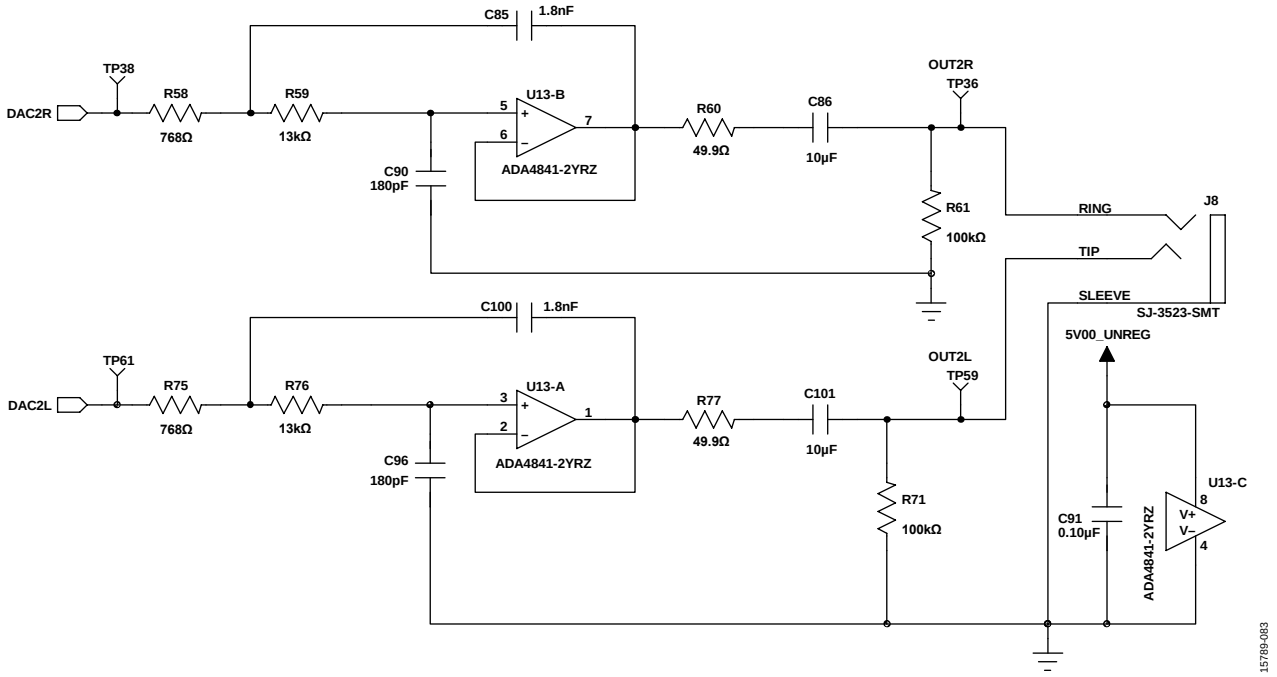

Figure 92. Analog Output Channel 16 and Channel 17 Schematic

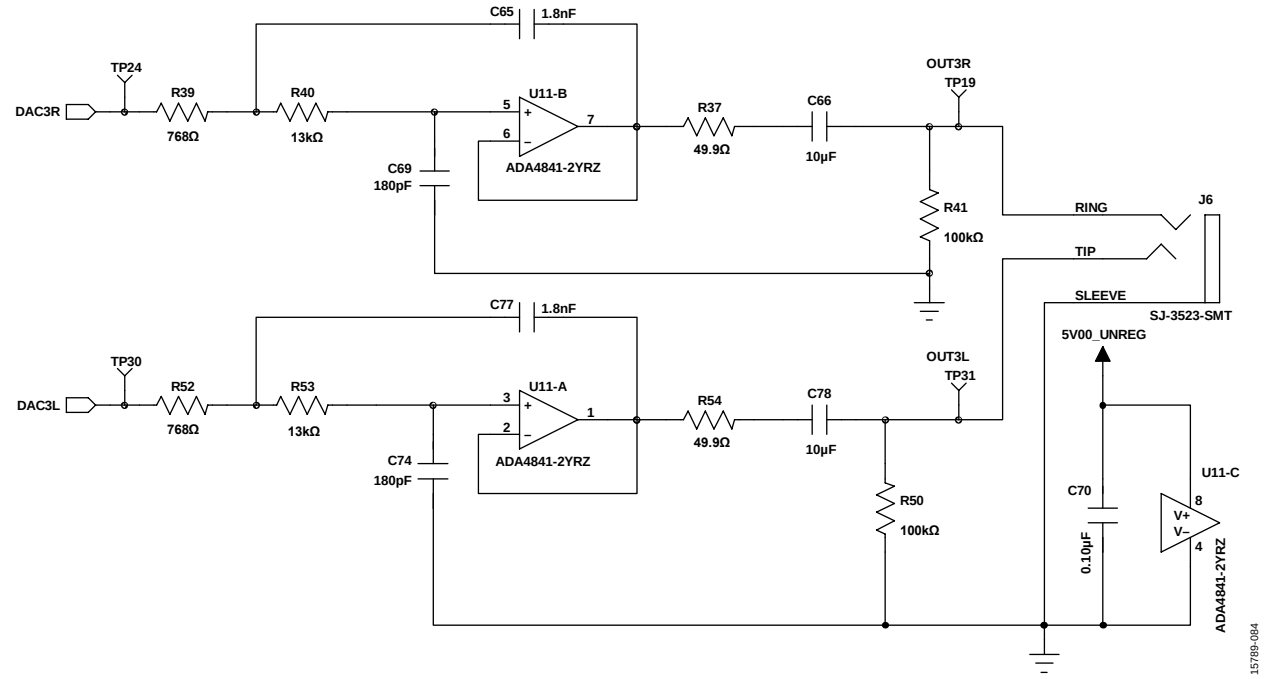

Figure 93. Analog Output Channel 32 and Channel 33 Schematic

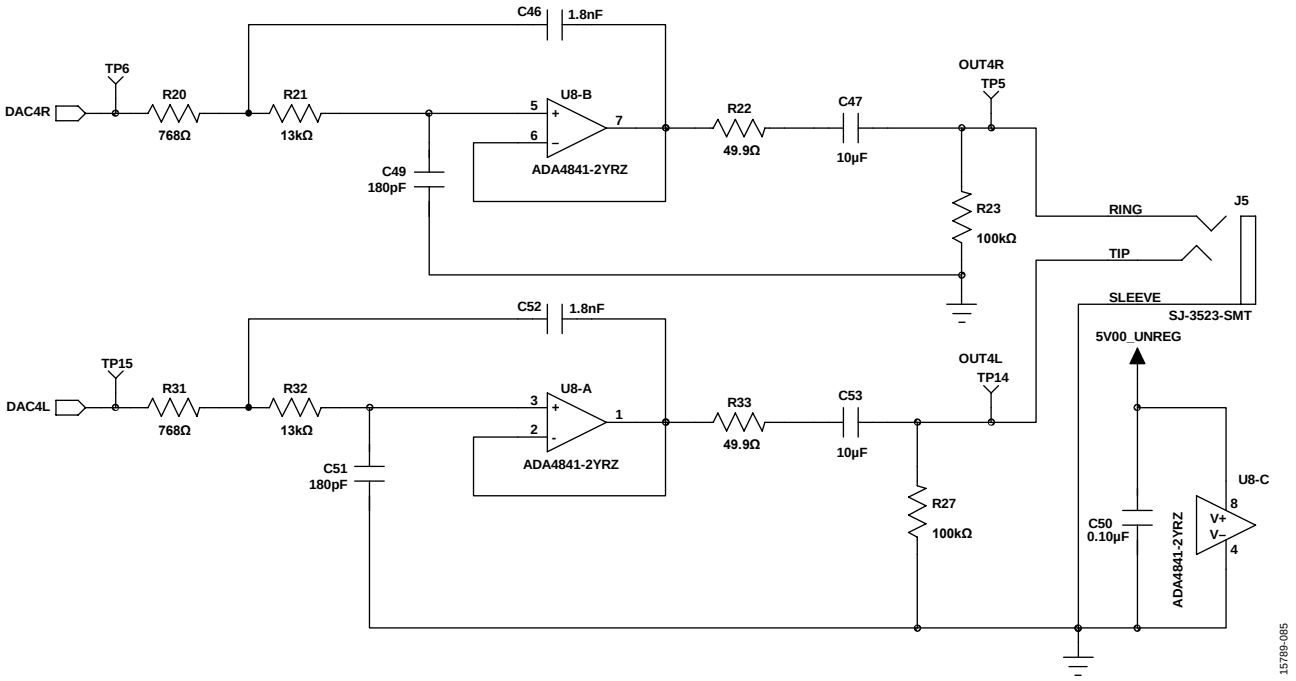

Figure 94. Analog Output Channel 40 and Channel 41 Schematic

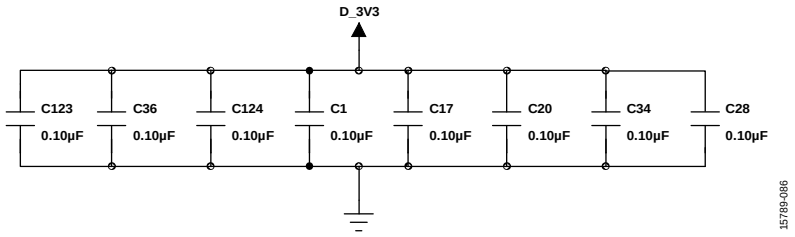

Figure 95. Plane Decoupling Capacitors Schematic

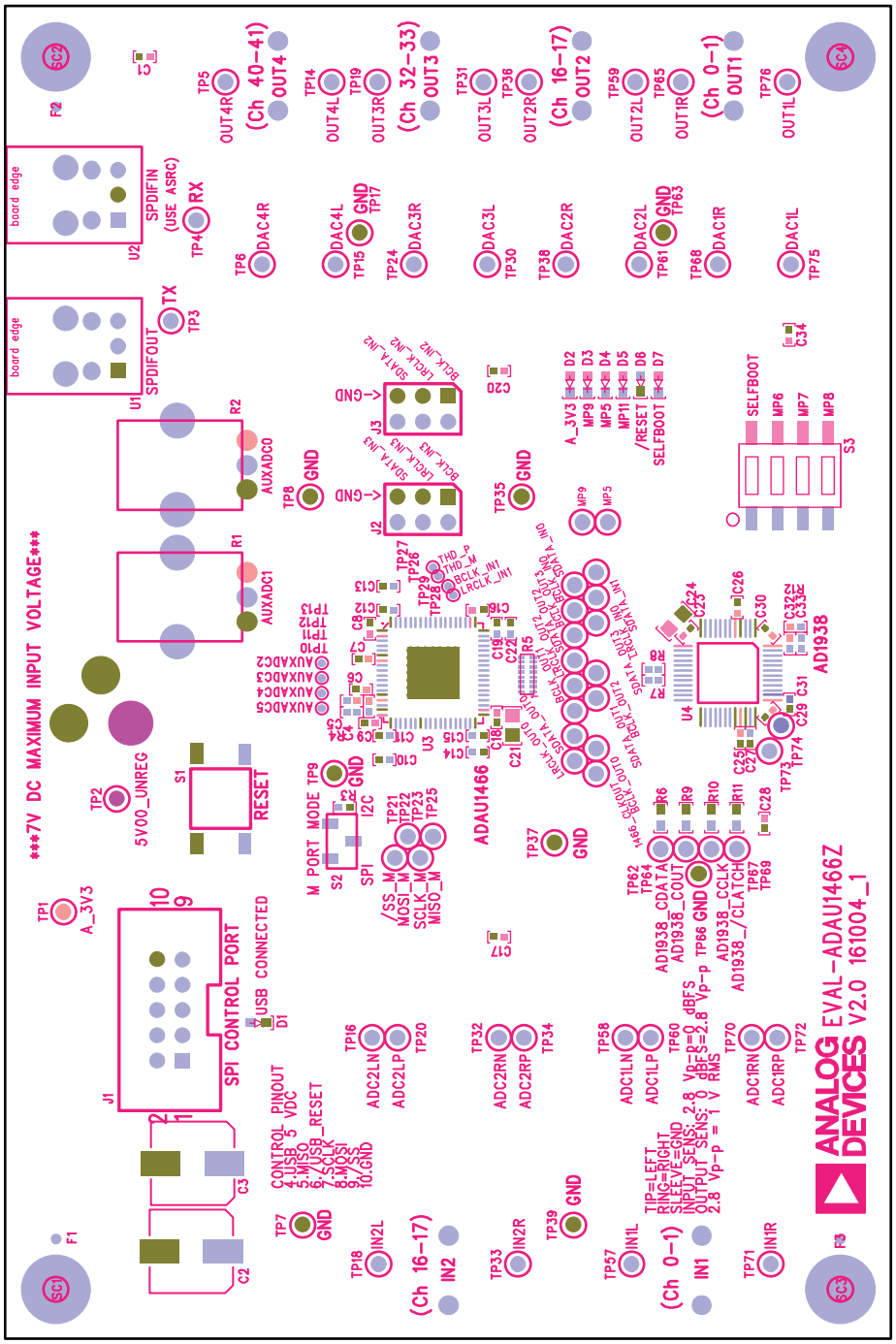

Figure 96. EVAL-ADAU1466Z Layout, Top Assembly

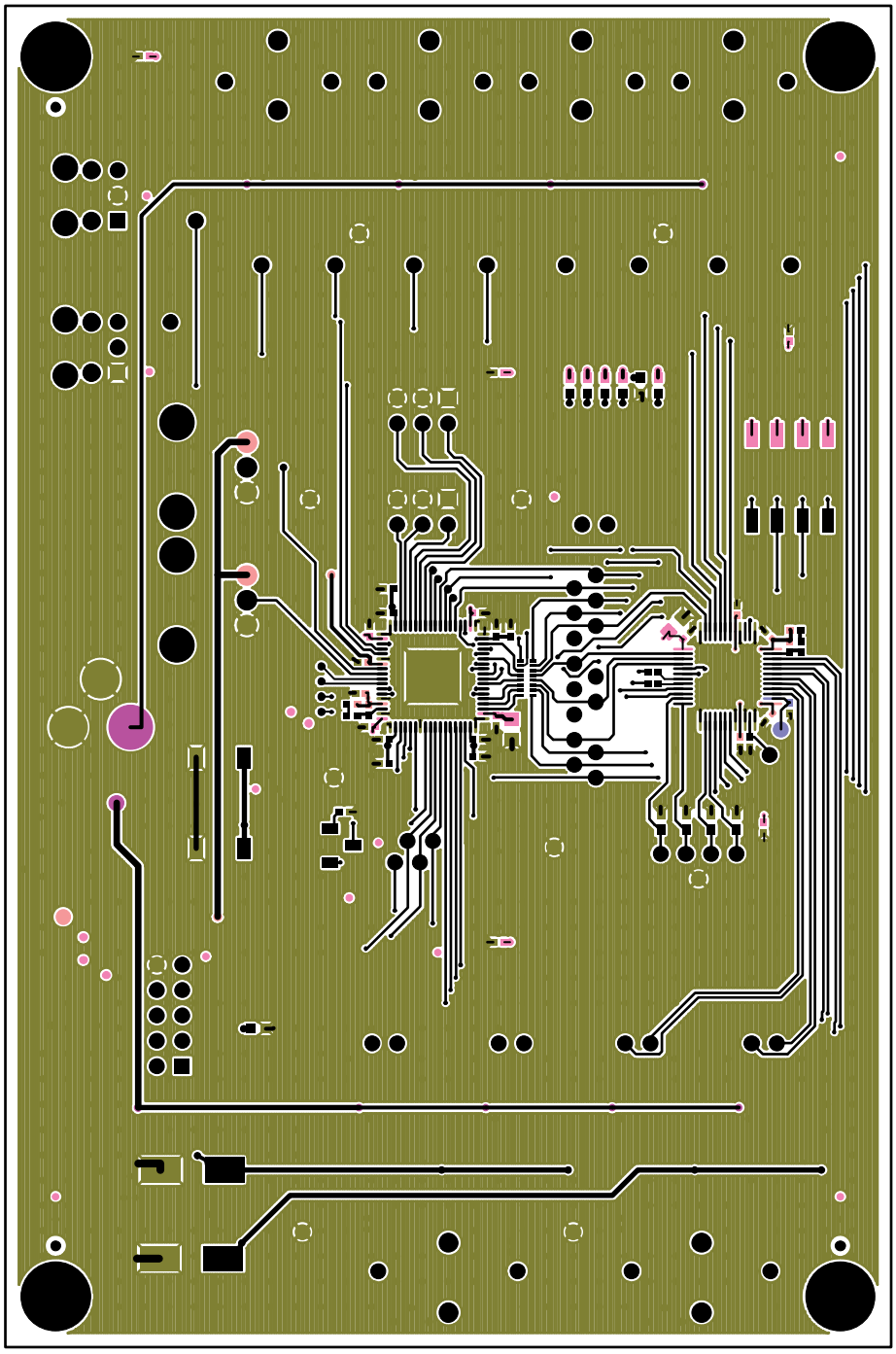

Figure 97. EVAL-ADAU1466Z Layout, Top Copper

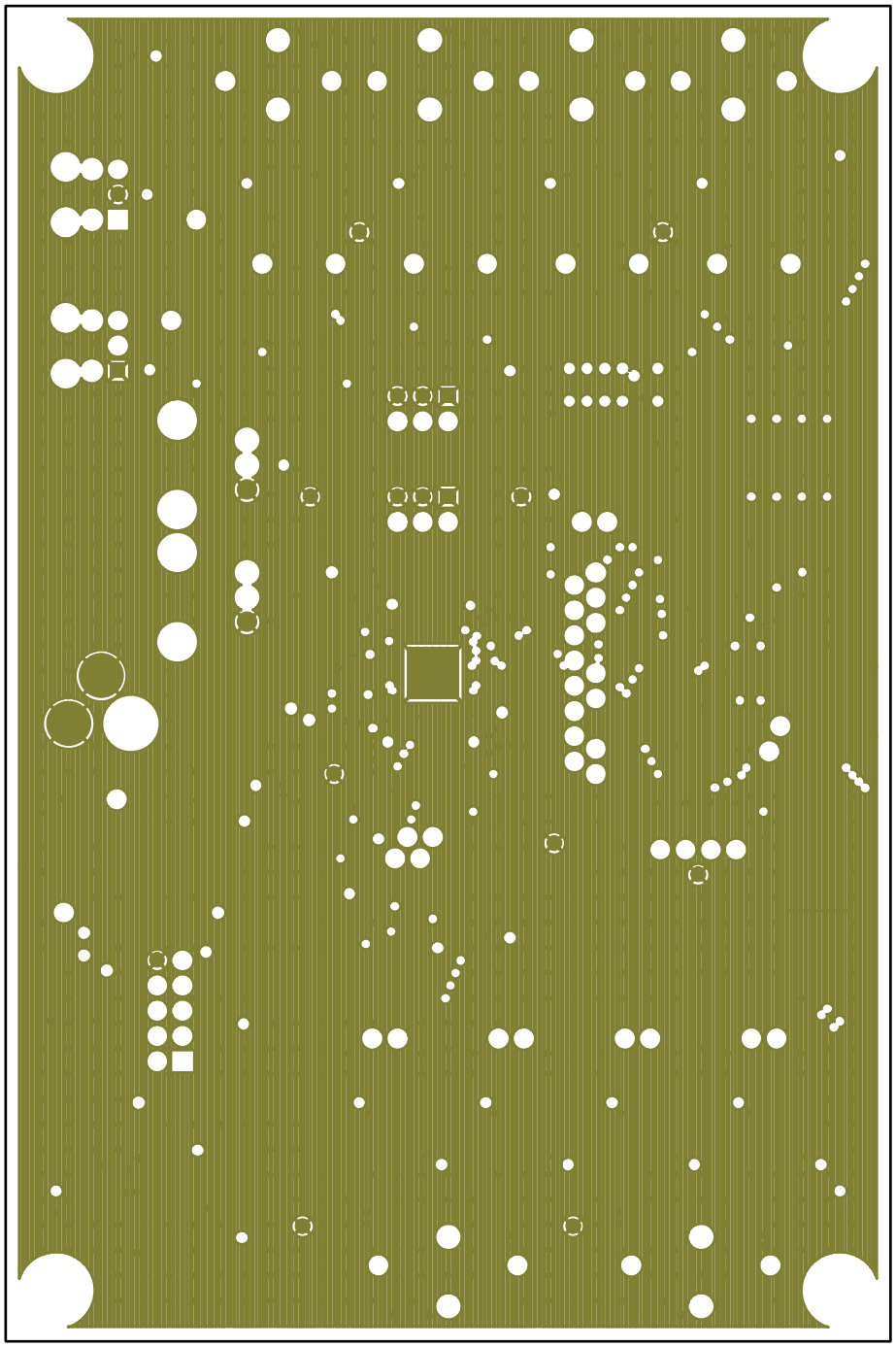

Figure 98. EVAL-ADAU1466Z Layout, Ground Plane

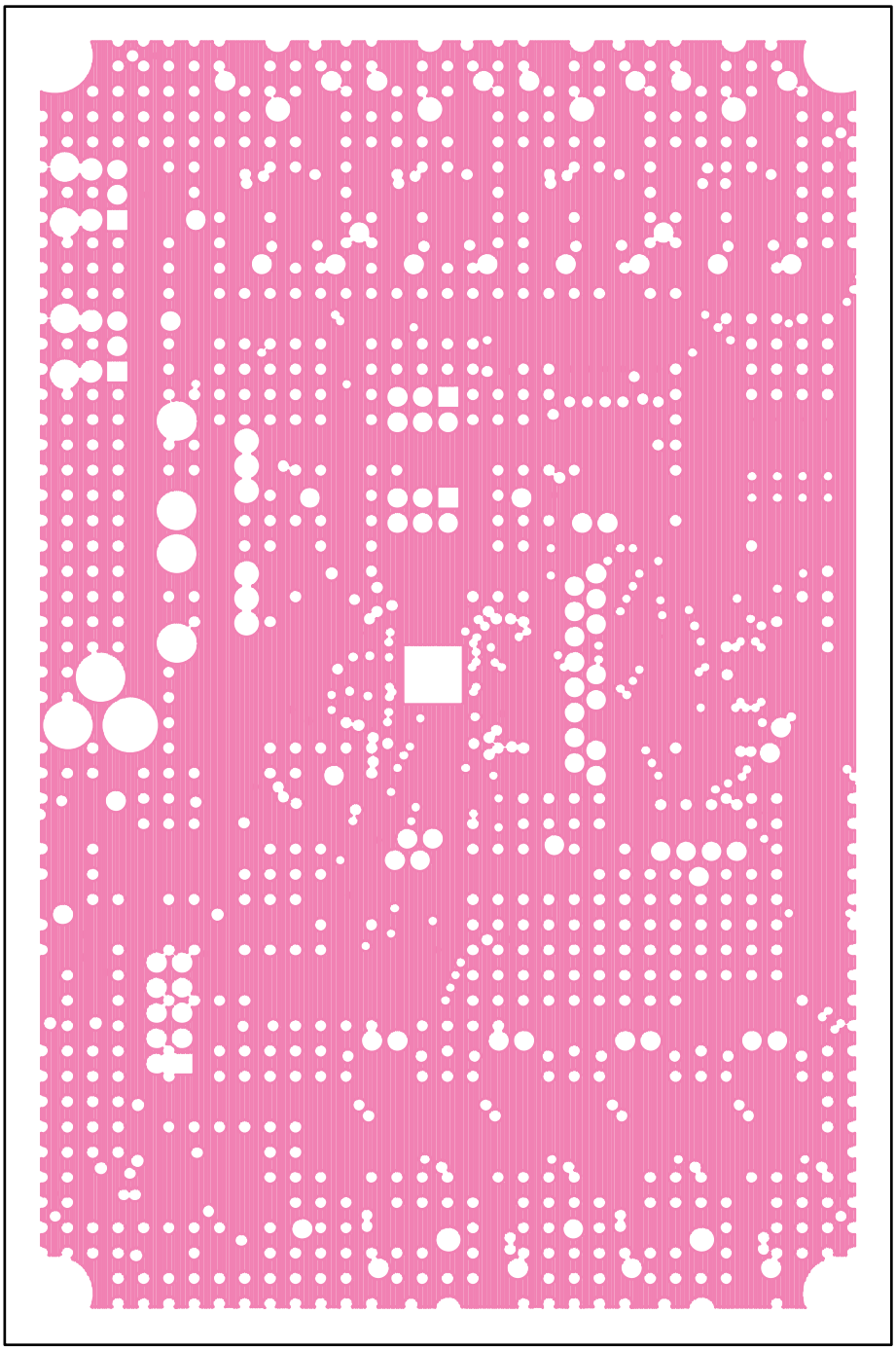

Figure 99. EVAL-ADAU1466Z Layout, Power Plane

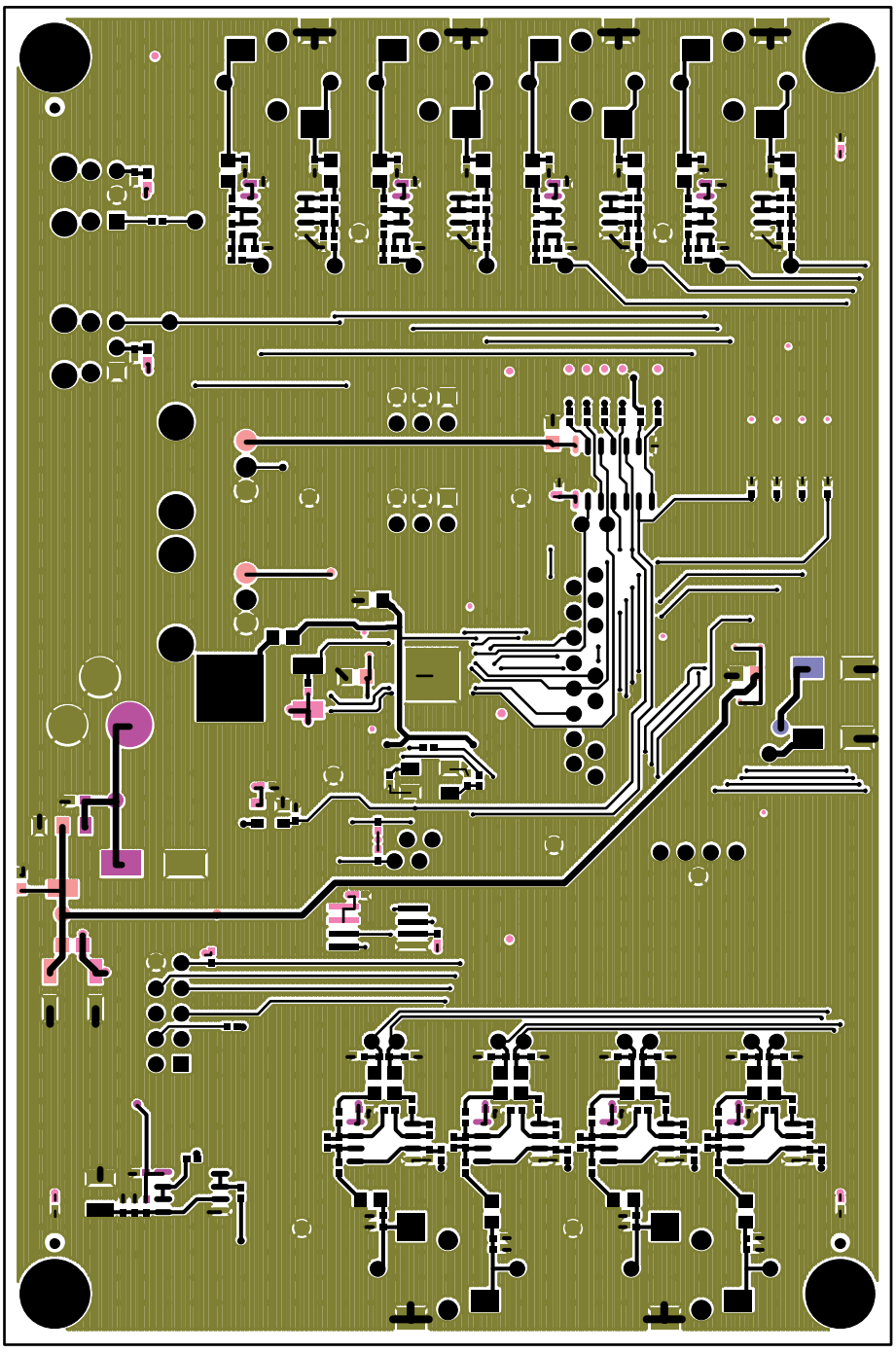

Figure 100. EVAL-ADAU1466Z Layout, Bottom Copper

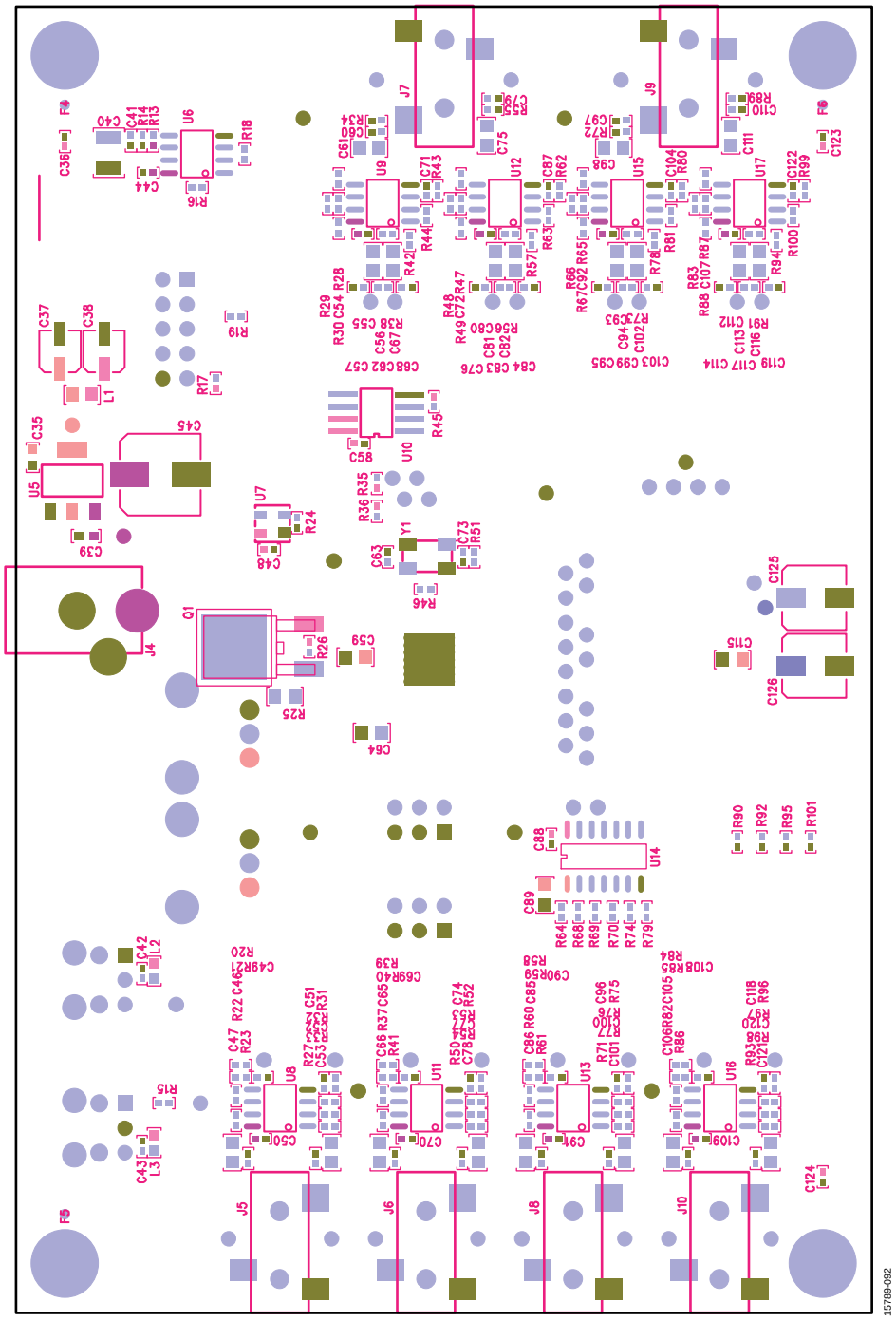

Figure 101. EVAL-ADAU1466Z Layout, Bottom Assembly (Viewed from Below)

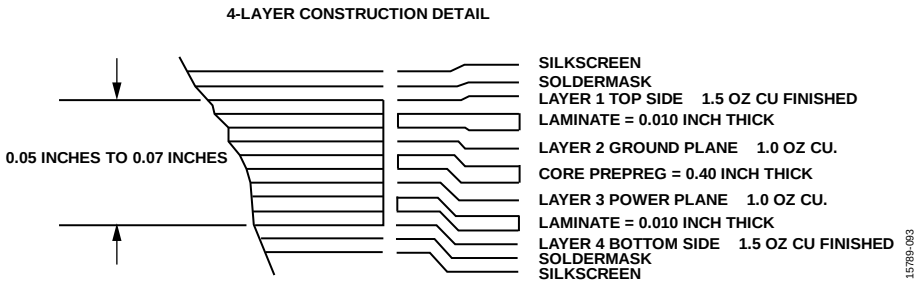

Figure 102. Cross Section of PCB Stack Up

ORDERING INFORMATION

BILL OF MATERIALS

Table 8.

Qty.	Designator	Description	Part Number	Manufacturer
42	C1, C6 to C10, C13, C14, C16 to C18, C20, C22, C23, C25 to C31, C34, C36, C42, C43, C48, C50, C55, C58, C70, C71, C80, C87, C88, C91, C93, C104, C109, C112, C122 to C124	Multilayer ceramic capacitor, 0.10 µF, 16 V, X7R, 0402	GRM155R71C104KA88D	Murata
4	C11, C12, C15, C19	Multilayer ceramic capacitor, 10 nF, 25 V, X7R, 0402	GRM155R71E103JA01J	Murata
2	C125, C126	Aluminum electrolytic capacitor, 47 µF, 105°C, SMD_D	EEE-FC1C470P	Panasonic
26	C21, C24, C47, C53, C56, C59, C61, C64, C66, C67, C75, C78, C81, C82, C86, C89, C94, C98, C101, C102, C106, C111, C113, C115, C116, C121	Multilayer ceramic capacitor, 10 µF, 10 V, X7R, 0805	GRM21BR71A106KE51L	Murata
3	C2, C3, C45	Aluminum, electrolytic capacitor, 100 µF, 105°C, SMD_E	EEE-FC1C101P	Panasonic
1	C32	Multilayer ceramic capacitor, 390 pF, 50 V, NP0, 0402	GRM1555C1H391JA01D	Murata
2	C35, C39	Multilayer ceramic capacitor, 1.0 µF, 16 V, X7R, 0603	GRM188R71C105KA12D	Murata
2	C37, C38	Aluminum electrolytic capacitor, 10 µF, 105°C, SMD_B	EEE-FC1C100R	Panasonic
1	C4	Multilayer ceramic capacitor, 150 pF, 50 V, NP0, 0402	GRM1555C1H151JA01D	Murata
1	C40	Multilayer ceramic capacitor, 10 µF, 25 V, X7R, 1210	GCM32ER71E106KA57L	Murata
2	C41, C44	Multilayer ceramic capacitor, 0.10 µF, 35 V, X7R, 0402	CGA2B3X7R1V104K050BB	TDK Corp
8	C46, C52, C65, C77, C85, C100, C105, C120	Multilayer ceramic capacitor, 1.8 nF, 25 V, NP0, 0402	C0402C182J3GACTU	Kemet
8	C49, C51, C69, C74, C90, C96, C108, C118	Multilayer ceramic capacitor, 180 pF, 50 V, NP0, 0402	GRM1555C1H181GA01D	Murata
2	C5, C33	Multilayer ceramic capacitor, 5.6 nF 25 V, NP0, 0402	GRM155R71E562KA01D	Murata
4	C54, C72, C92, C107	Multilayer ceramic capacitor, 330 pF, 50 V, NP0, 0402	GRM1555C1H331JA01D	Murata
8	C57, C68, C76, C84, C95, C103, C114, C119	Multilayer ceramic capacitor, 1.0 nF, 50 V, NP0, 0402	GRM1555C1H102JA01D	Murata
8	C60, C62, C79, C83, C97, C99, C110, C117	Multilayer ceramic capacitor, 100 pF, 50 V, NP0, 0402	GRM1555C1H101JZ01D	Murata
2	C63, C73	Multilayer ceramic capacitor, 22 pF, 50 V, NP0, 0402	GRM1555C1H220JZ01D	Murata
7	D1 to D7	LED, green, 571 nm, 2 V, 3 mcd, 0603	LTST-C191KGKT	Lite-On
1	J1	Header, 2 × 5, 0.1 inch, shrouded, polarized	N2510-6002RB	3M
2	J2, J3	Header, 2 × 3, 0.1 inch, unshrouded	PBC06DAAN, or cut PBC36DAAN	3M
1	J4	Jack, power connector, 2.0 mm ID, 5.5 mm, outside diameter, through hole, right angle	RAPC722X	Switchcraft
6	J5 to J10	Jack, 3.5 mm headphone, stereo, right angle, SMD	SJ-3523-SMT	CUI Inc.
1	L1	Chip ferrite bead, 600 Ω, at100 MHz, 500 mA, 0805	HZ0805E601R-10	Steward
2	L2, L3	Chip inductor, 47 µH, 140 mA, 3.25 Ω, 0603	CBMF1608T470K	Taiyo Yuden
1	Q1	Transistor, BJT, PNP, 60 V, 5 A, TO-252AA	STD2805T4	STMicroelectronics
1	R12	Chip resistor, 562 Ω, 1%, 63 mW, thick film, 0402	RMCF0402FT562R	Stackpole

Qty.	Designator	Description	Part Number	Manufacturer
2	R1, R2	Potentiometer, 10 kΩ, linear taper, 9 mm, vertical	EVU-F2MFL3B14	Panasonic
4	R13, R14, R19, R26	Chip resistor, 1 kΩ, 1%, 63 mW, thick film, 0402	RC0402FR-071KL	Yageo
18	R16, R18, R22, R30, R33, R37, R42, R49, R54, R57, R60, R67, R77, R78, R82, R88, R94, R98	Chip resistor, 49.9 Ω, 1%, 63 mW, thick film, 0402	RC0402FR-0749R9L	Yageo
6	R17, R45, R90, R92, R95, R101	Chip resistor, 10 kΩ, 1%, 100 mW, thick film, 0402	ERJ-2RKF1002X	Panasonic
8	R20, R31, R39, R52, R58, R75, R84, R96	Chip resistor, 768 Ω, 1%, 63mW, thick film, 0402	RC0402FR-07768RL	Yageo
8	R21, R32, R40, R53, R59, R76, R85, R97	Chip resistor, 13kΩ, 1%, 63 mW, thick film, 0402	RC0402FR-0713KL	Yageo
14	R23, R24, R27, R34, R36, R41, R50, R55, R61, R71, R72, R86, R89, R93	Chip resistor, 100 kΩ, 1%, 100 mW, thick film, 0402	ERJ-2RKF1003X	Panasonic
1	R25	Jumper, 0 Ω, 125 mW, 0805	ERJ-6GEY0R00V	Panasonic
16	R28, R29, R38, R44, R47, R48, R56, R63, R65, R66, R73, R81, R83, R87, R91, R100	Chip resistor, 4.99 Ω, 1%, 63 mW, thick film, 0402	RMCF0402FT4K99	Stackpole
2	R3, R35	Chip resistor, 4.75 kΩ, 1%, 63 mW, thick film, 0402	RC0402FR-074K75L	Yageo
1	R4	Chip resistor, 4.32 kΩ, 1%, 100 mW, thick film, 0402	ERJ-2RKF4321X	Panasonic
5	R43, R51, R62, R80, R99	Chip resistor, 100 Ω, 1%, 100 mW, thick film, 0402	ERJ-2RKF1000X	Panasonic
1	R5	Resistor network, eight-resistor, isolated, 33 Ω, 5%, 63 mW, 1506	741X163330JP	CTS
4	R6, R9 to R11	Resistor, 0 Ω, 125 mW, 0603	ERJ-3GEY0R00V	Panasonic
6	R64, R68 to R70, R74, R79	Chip resistor, 475 Ω, 1%, 63 mW, thick film, 0402	RMCF0402FT475R	Stackpole
4	R7, R8, R15, R46	Chip resistor, 33.2 Ω, 1%, 63 mW, thick film, 0402	RMCF0402FT33R2	Stackpole
1	S1	Switch, top actuated, tactile, SPST normally open, 6 mm gull wing	FSM6JSMA	Tyco/Alcoswitch
1	S2	Switch, SPDT slide, SMD J HOOK	CAS-120TA	Copal Electronics
1	S3	Switch, four-section, SPST, SMD	219-4LPST	CTS Corp
68	TP1 to TP9, TP14 to TP25, TP30 to TP76	Test point, white, 0.1 inch OD	5002	Keystone Electronics
1	U1	Optical transmitter, 16 Mbps	PLT133/T10W	Everlight
1	U10	EEPROM, 128k × 8, 1.8 V to 5.5 V, SOIJ-8	25AA1024-I/SM	Microchip
1	U14	Inverter, 6-channel, SOIC-14	74ACT04SC	Fairchild Semi
1	U2	Optical receiver, 16 Mbps	PLR135/T10	Everlight
1	U3	SigmaDSP processor, 300 MHz	ADAU1466WBCPZ	Analog Devices
1	U4	Codec, four-ADC, eight-DAC, 192 kHz, 24-bit	AD1938YSTZ	Analog Devices
1	U5	Voltage regulator, high accuracy, low dropout, 3.3 V dc	ADP3338AKCZ-3.3-R7	Analog Devices
9	U6, U8, U9, U11 to U13, U15 to U17	Op amp, dual, low power, low noise, low distortion, rail-to-rail, 8-lead SOIC	ADA4841-2YRZ	Analog Devices
1	U7	Supervisor reset generator, 3.08 V, logic low output, 4-lead SOT-143	ADM811TARTZ-REEL7	Analog Devices
1	Y1	Crystal, 12.288 MHz, 18 pF, SMD-4	ABM3B-12.288MHZ-10-1-U-T	Abracon Corp

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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