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Evaluating the ADGS1414D SPI, 1.5 Ω R_{ON}, ±15 V/±5 V/+12 V, High Density Octal SPST Switch

FEATURES

- SPI with error detection
  - Includes CRC, invalid read and write address, and SCLK count error detection
- Analog supply voltages
  - Dual-supply: ±4.5 V to ±16.5 V
  - Single-supply: 5 V to 20 V
- PC control in conjunction with the evaluation software
- EVAL-SDP-CB1Z (SDP-B) system demonstration platform

PACKAGE CONTENTS

EV-ADGS1414DSDZ

DOCUMENTS NEEDED

ADGS1414D data sheet

EQUIPMENT NEEDED

- EVAL-SDP-CB1Z (SDP-B) controller board
- DC voltage source
  - ±16.5 V (dual supply)
  - 20 V (single supply)
- Optional 3.3 V digital logic supply
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

SOFTWARE NEEDED

ACE software with EV-ADGS1414DSDZ plugin

GENERAL DESCRIPTION

The EV-ADGS1414DSDZ is the evaluation board for the ADGS1414D. The ADGS1414D is an *i*CMOS®, octal SPST switch controlled by a serial peripheral interface (SPI). The SPI has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read and write address detection, and SCLK count error detection. The ADGS1414D also supports burst mode, which decreases the time between SPI commands.

Figure 1 shows the EV-ADGS1414DSDZ in a typical evaluation setup. The EV-ADGS1414DSDZ is controlled by the system demonstration platform (SDP) EVAL-SDP-CB1Z (SDP-B), which connects to a PC via a USB port. The ADGS1414D is on the center of the evaluation board, and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device, and a fourth terminal provides users with a defined digital logic supply voltage, if required. Alternatively, the digital logic supply voltage can be supplied from the SDP-B. The EVAL-SDP-CB1Z (SDP-B) controller board is available to order on the Analog Devices, Inc., website.

For full details on the ADGS1414D, see the ADGS1414D data sheet, which must be consulted in conjunction with this user guide when using this evaluation board.

EVALUATION BOARD PHOTOGRAPH

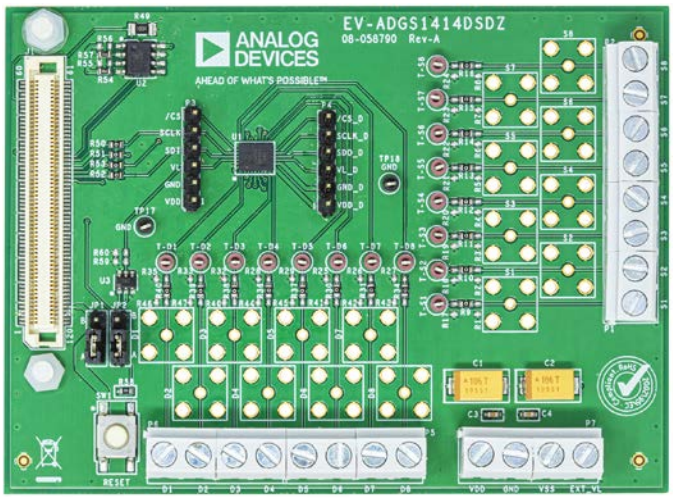

Figure 1.

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REVISION HISTORY

6/2020—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The P7 connector provides access to the supply pins of the ADGS1414D. VDD, GND, and VSS on P7 link to the appropriate pins on the ADGS1414D. For dual-supply voltages, the EV-ADGS1414DSDZ can be powered from ±4.5 V to ±16.5 V. For single-supply voltages, the GND and VSS terminals must be connected together and can power the EV-ADGS1414DSDZ with 5 V to 20 V. Additionally, 3.3 V is supplied to the $\overline{\text{RESET}}/V_L$ pins of the ADGS1414D by the SDP-B controller board when the JP1 link is in Position B. When controlling the ADGS1414D by a method other than the SDP-B controller board, supply between 2.7 V and 5.5 V to the $\overline{\text{RESET}}/V_L$ pins of the ADGS1414D via the EXT_VL screw terminal input on P7. Ensure JP1 is in Position A.

INPUT SIGNALS

The P1, P2, P5, and P6 screw connectors connect to both the source and drain pins of the ADGS1414D. Additional Subminiature Version B (SMB) connector pads are available if extra connections are required.

Each trace on the source and drain side of the EV-ADGS1414DSDZ includes two sets of 0603 pads that can place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor and the 0603 pads create a simple RC filter.

LINK OPTIONS

Ensure that the link options provided on the EV-ADGS1414DSDZ are set for the required operating conditions before using the evaluation board. Table 1 details the positions of the links to control the evaluation board via the SDP-B controller board using a PC and external power supplies. The functions of these link options are detailed in Table 2.

When using the SDP-B controller board in conjunction with the EV-ADGS1414DSDZ, place JP1 in Position B to avoid damage to the SDP-B.

Table 1. Link Options for SDP-B Control (Default)

Link Number	Option
JP1	B
JP2	B

ROUTE THROUGH PINS FOR DAISY CHAINS

The P3 and P4 headers allow access to the route through pins of the ADGS1414D. Use the P3 and P4 headers to daisy-chain multiple EV-ADGS1414DSDZ devices together. To daisy-chain the EV-ADGS1414DSDZ devices, connect /CS_D, SCLK_D, and SDO_D on P4 of one EV-ADGS1414DSDZ to /CS, SCLK, and SDI on P3 of the next EV-ADGS1414DSDZ. VL, GND, and VDD can also be shared between these evaluation boards via the P3 and P4 headers. However, because VSS is only accessible from P7, connect VSS in each daisy-chained EV-ADGS1414DSDZ.

Table 2. Link Functions

Link Number	Function
JP1	The JP1 link selects the source of the V_L voltage supplied to the ADGS1414D. Position A selects EXT_VL from P7. Position B selects 3.3 V from the SDP-B controller board.
JP2	The JP2 link selects how a hardware reset is performed. Position A indicates the SW1 push-button can perform a hardware reset. Position B indicates the SDP-B controller board can perform a hardware reset.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EV-ADGS1414DSDZ uses the Analog Devices Analysis, Control, Evaluation (ACE) software. ACE is a desktop software application that allows users to evaluate and control multiple evaluation systems.

The ACE installer installs the necessary SDP drivers and .NET Framework 4 by default. Install ACE before connecting the SDP-B controller board. The full instructions on how to install and use the ACE software can be found on the Analog Devices website at www.analog.com/ace.

After ACE is installed, the EV-ADGS1414DSDZ plugin appears when opening the application.

INITIAL SET UP

To set up the EV-ADGS1414DSDZ, complete the following steps:

1. Connect the EV-ADGS1414DSDZ to the SDP-B controller board via the 120-pin connector.
2. Connect the SDP-B controller board to the computer using the USB cable provided with the SDP-B.
3. Power the EV-ADGS1414DSDZ as described in the Power Supplies section.
4. Run the ACE application. The EV-ADGS1414DSDZ plugin appears in the **Attached Hardware** section of the **Start** tab.
5. Double click the **ADGS1414D Board** evaluation board plugin to open the **ADGS1414D** chip view, as shown in Figure 2.

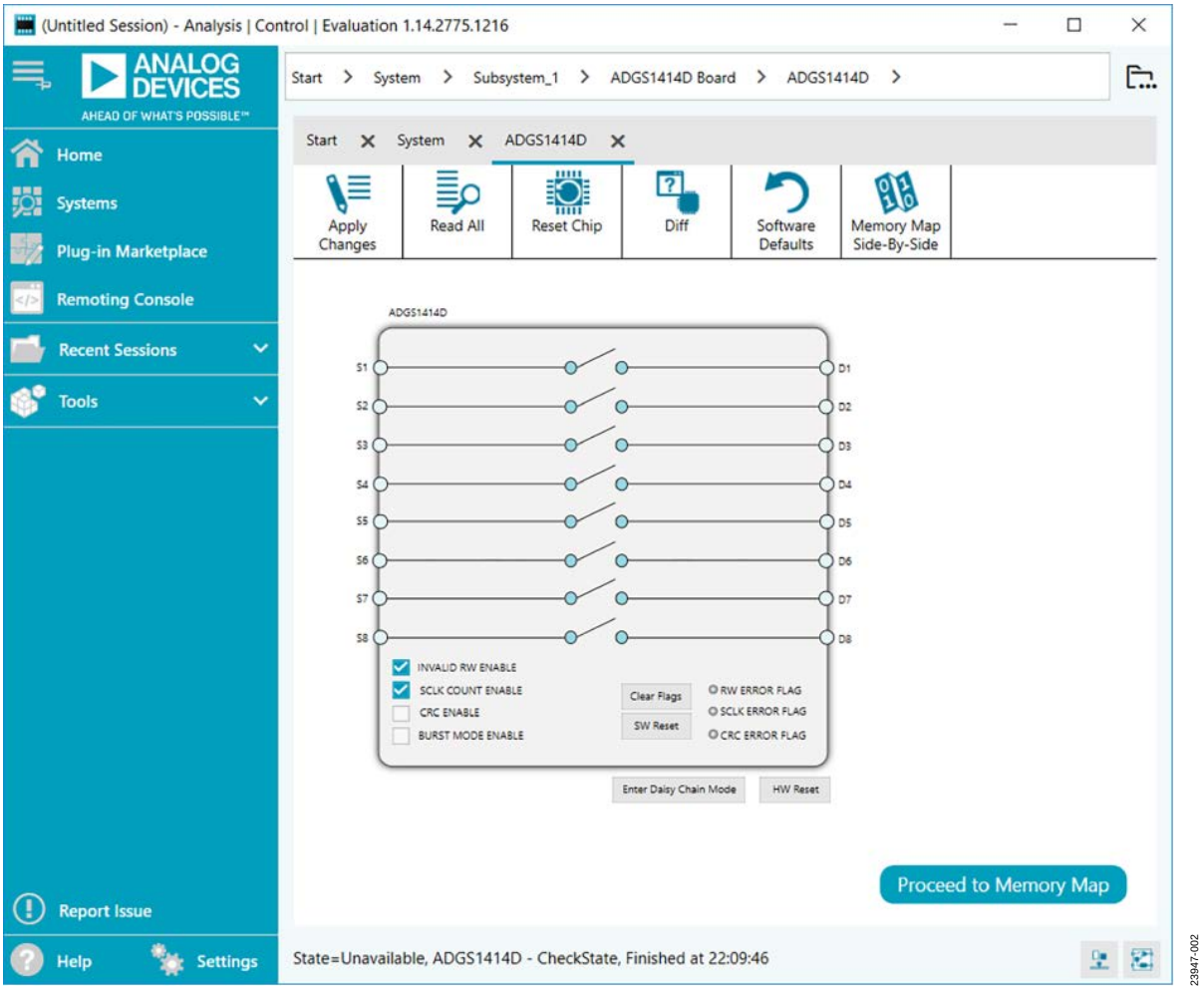

Figure 2. Chip View for the ADGS1414D

BLOCK DIAGRAM AND DESCRIPTION

The **ADGS1414D** chip view is similar to the functional block diagram shown in the ADGS1414D data sheet. Therefore, it is simple to correlate the functions on the EV-ADGS1414DSDZ with the descriptions in the data sheet. See the ADGS1414D data sheet for a full description of each block, register, and setting.

Some of the blocks and their functions are described in this section as they pertain to the EV-ADGS1414DSDZ. Figure 3 shows the full screen block diagram (with labels), and Table 3 describes the functionality of each labeled block.

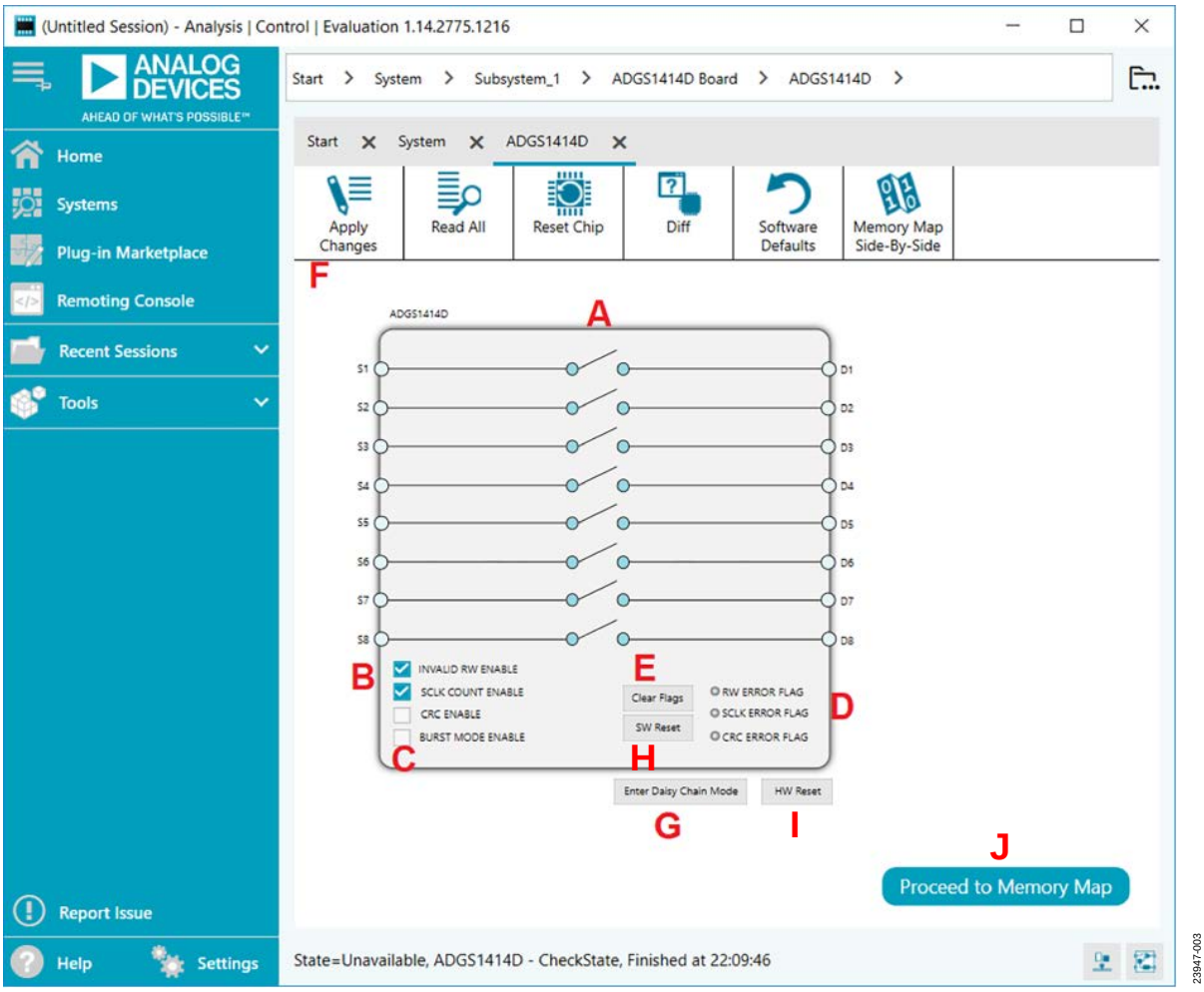

Figure 3. Chip View for the ADGS1414D with Labeled Block Diagram

Table 3. Block Diagram Functions

Label	Function
A	The eight switches configure SW1 to SW8 as open or closed. Click the switch to configure it.
B	**INVALID RW ENABLE**, **SCLK COUNT ENABLE**, and **CRC ENABLE**. Select or clear these check boxes to enable or disable the error detection features on the SPI.
C	**BURST MODE ENABLE**. Select or clear this check box to enable or disable burst mode.
D	**RW ERROR FLAG**, **SCLK ERROR FLAG**, and **CRC ERROR FLAG**. These indicators illuminate red if flags assert in the error flags register.
E	**Clear Flags**. Click this button to clear the error flags register.
F	**Apply Changes**. Click this button to apply all modified values to the devices.
G	**Enter Daisy Chain Mode**. Click this button to put all evaluation boards that are connected in a daisy-chain configuration into daisy-chain mode.
H	**SW Reset**. Click this button to perform a software reset on the ADGS1414D.
I	**HW Reset**. Click this button to perform a hardware reset on the ADGS1414D. JP2 must be set to Position B.
J	**Proceed to Memory Map**. Click this button to access the **ADGS1414D Memory Map** view.

DAISY-CHAIN MODE

It is possible to daisy-chain multiple ADGS1414D devices together. Daisy-chain mode enables the configuration of multiple devices with a minimal amount of digital lines. The route of digital signals and supplies through the ADGS1414D allows an increase in channel density when using the device in daisy-chain mode. Integrated passive components eliminate the need for external passive components.

Click **Enter Daisy Chain Mode** to open the **Daisy Chain Mode** view, as shown in Figure 4. Select the number of boards that are connected in the daisy chain from the **Number of Devices in Daisy Chain** dropdown box. Select the check boxes of the switches that are to be turned on. Click **Apply Changes** to write these values to the devices in the daisy chain. To exit daisy-chain mode, perform a hardware reset. To perform a hardware reset, click the **HW Reset** button in the **Daisy Chain Mode** view (JP2 must be set to Position B), or press the physical hardware reset button on the EV-ADGS1414DSDZ.

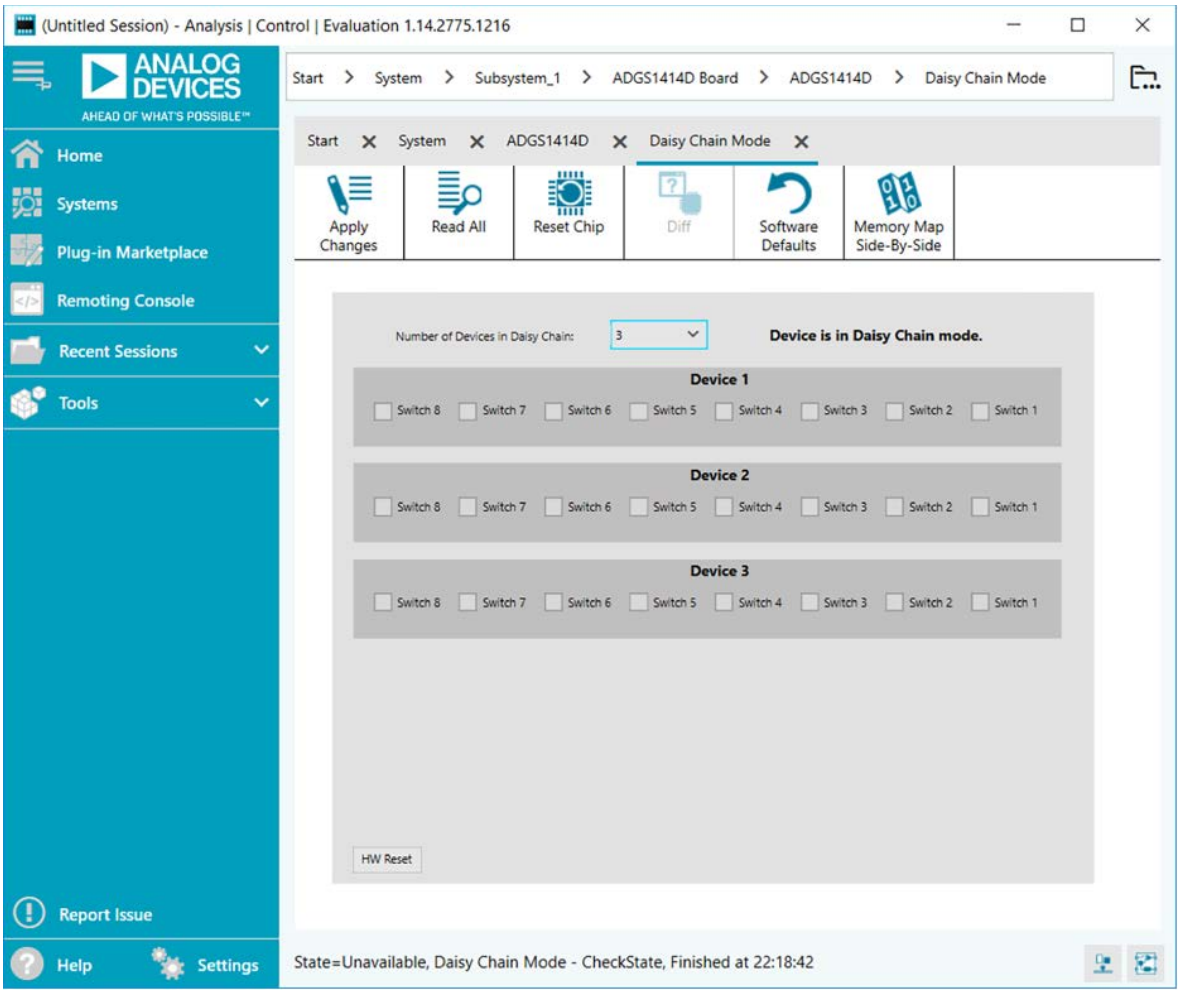

*Figure 4. **Daisy Chain Mode** View*

MEMORY MAP

All registers are fully accessible from the **ADGS1414D Memory Map** view. To access the **ADGS1414D Memory Map** view, click **Proceed to Memory Map**. The **ADGS1414D Memory Map** view allows registers to be edited at a bit level (see Figure 5 and Figure 6). The shaded bits are read only bits and cannot be accessed in ACE. All other bits are toggled. The bold bits or registers are modified values that have not been transferred to the evaluation board. Click **Apply Changes** to transfer the data to the EV-ADGS1414DSDZ.

All changes made in the **ADGS1414D Memory Map** view correspond to the block diagram. For example, if the internal register bit is enabled, the bit displays as enabled on the block diagram

*Figure 5. **ADGS1414D Memory Map** View*

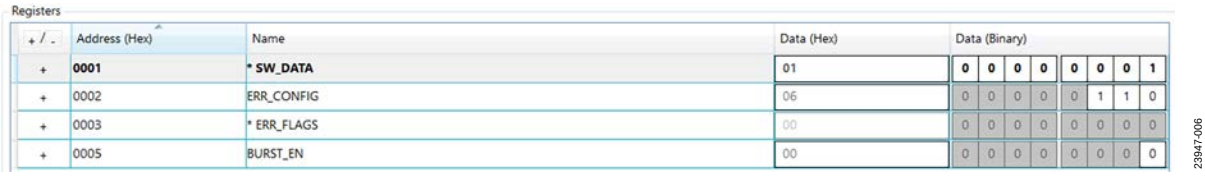

*Figure 6. **ADGS1414D Memory Map** View with Unapplied Changes in the SW_DATA Register*

EVALUATION BOARD SCHEMATICS AND ARTWORK

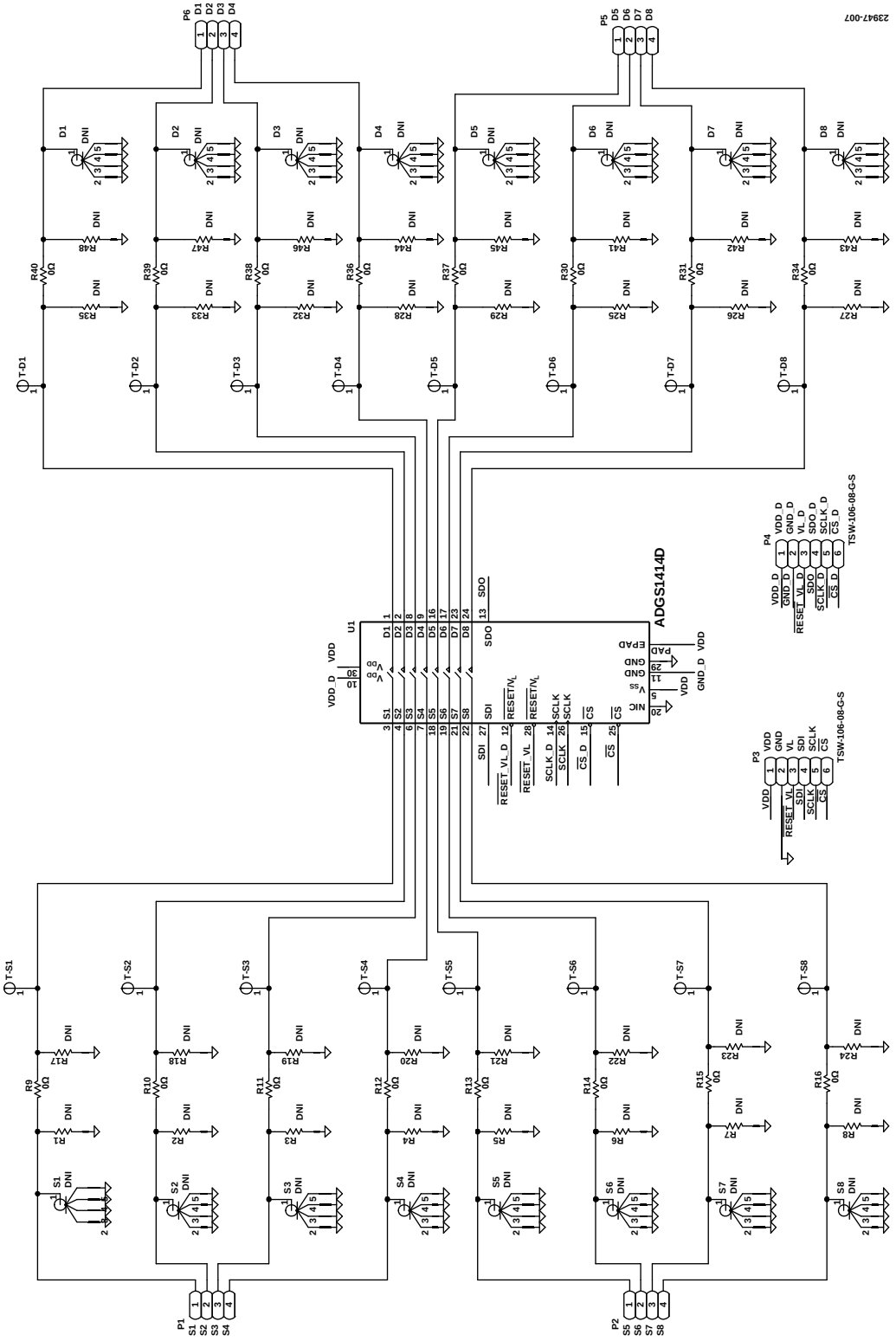

Figure 7. EV-ADGS1414DSDZ Schematic 1

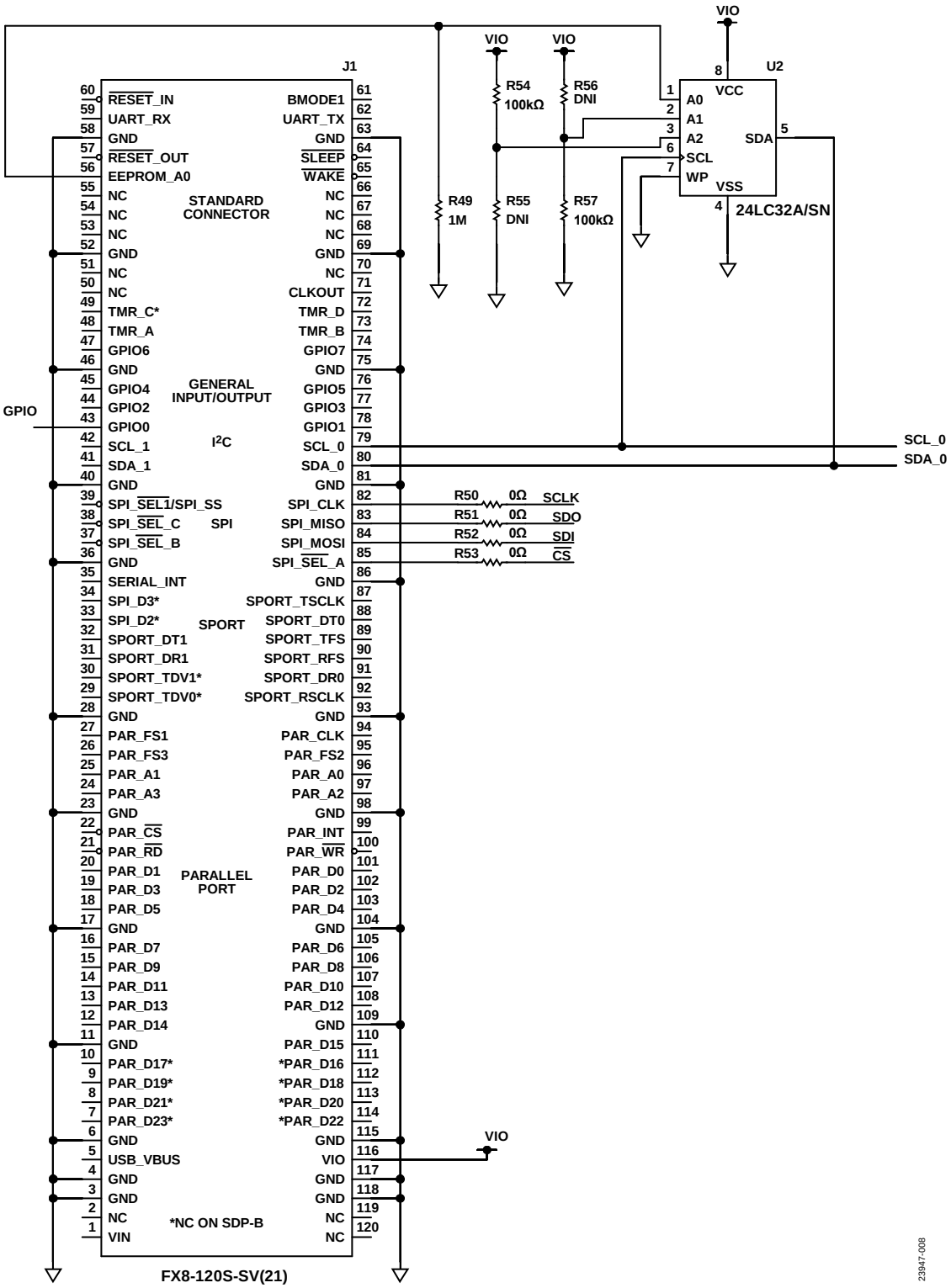

Figure 8. EV-ADGS1414DSDZ Schematic 2

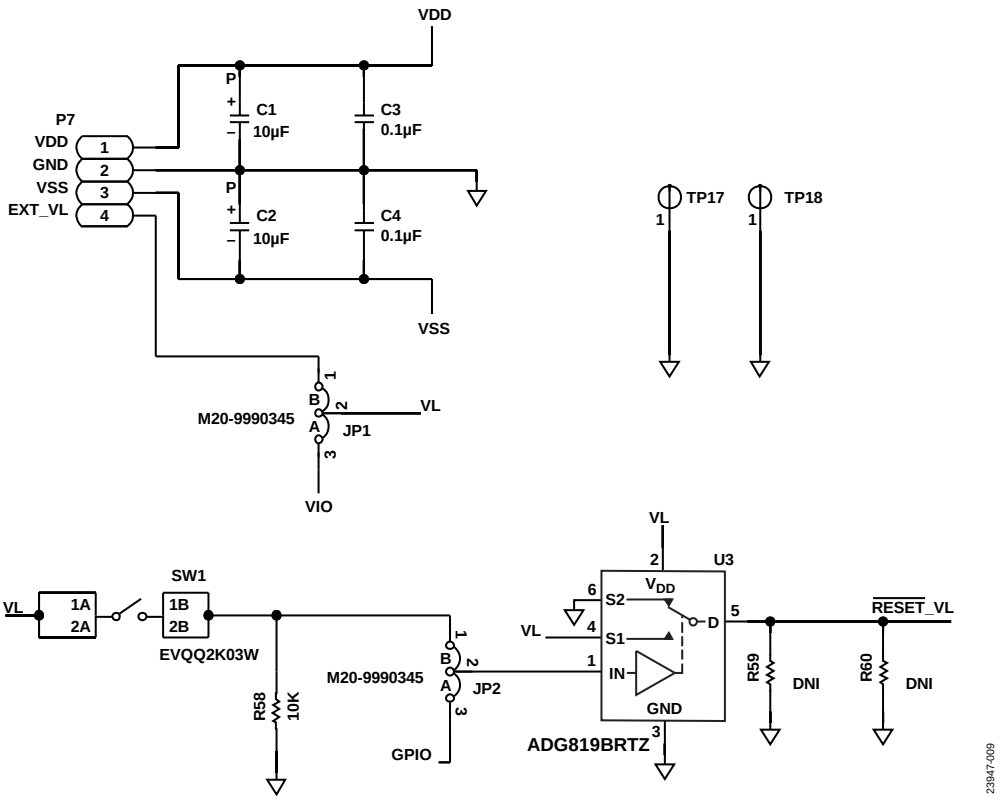

Figure 9. EV-ADGS1414DSDZ Schematic 3

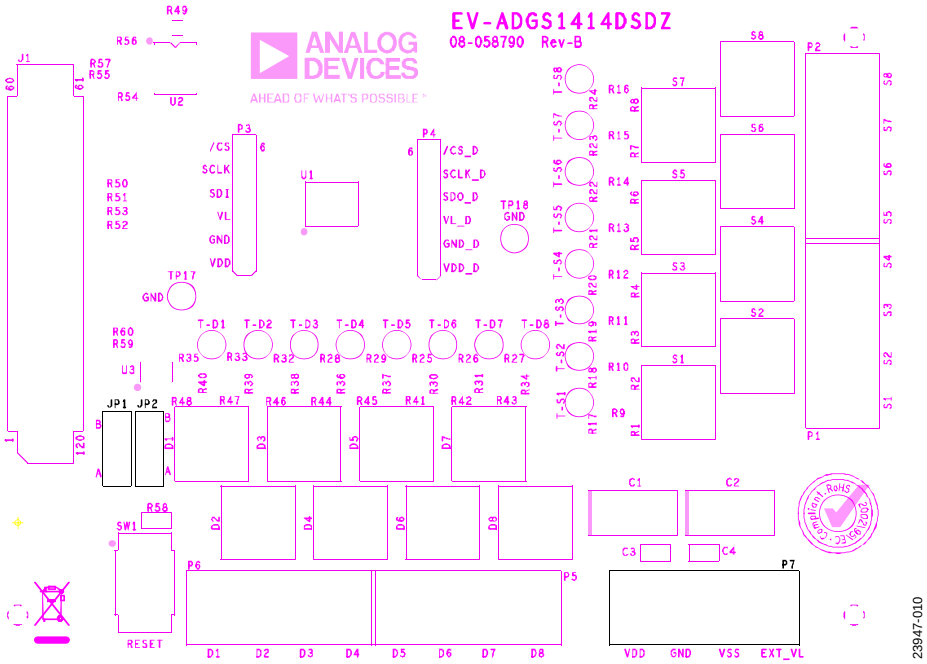

Figure 10. EV-ADGS1414DSDZ Silkscreen

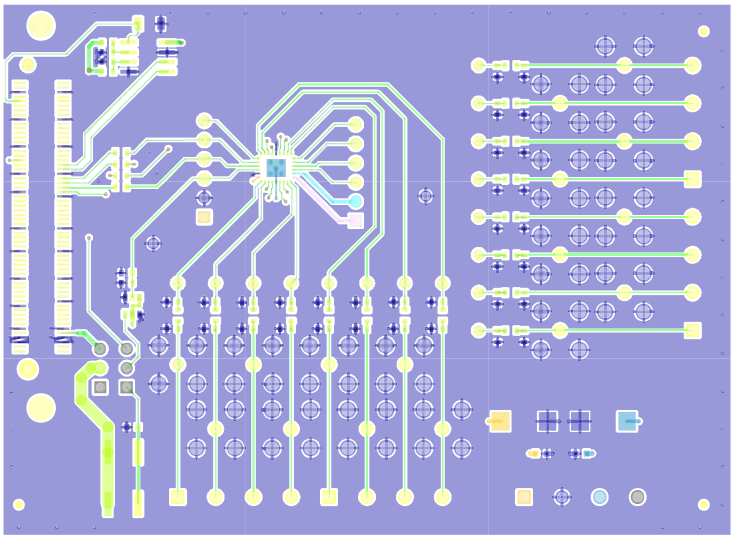

Figure 11. EV-ADGS1414DSDZ Top Layer

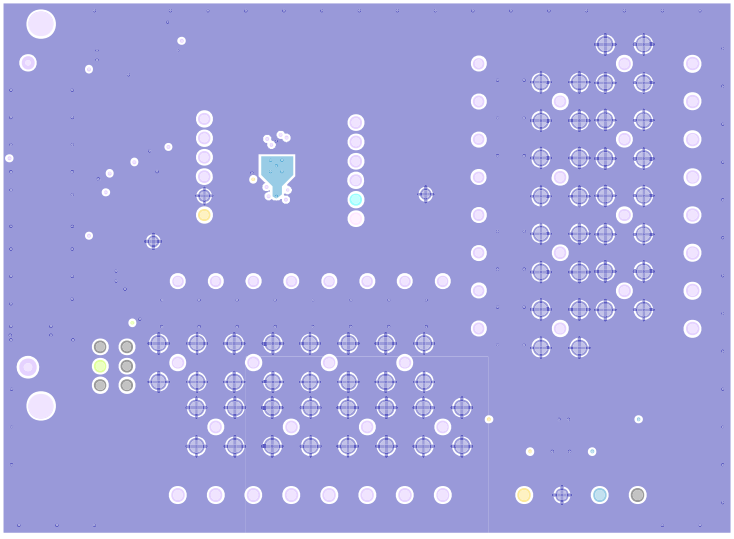

Figure 12. EV-ADGS1414DSDZ Layer 2

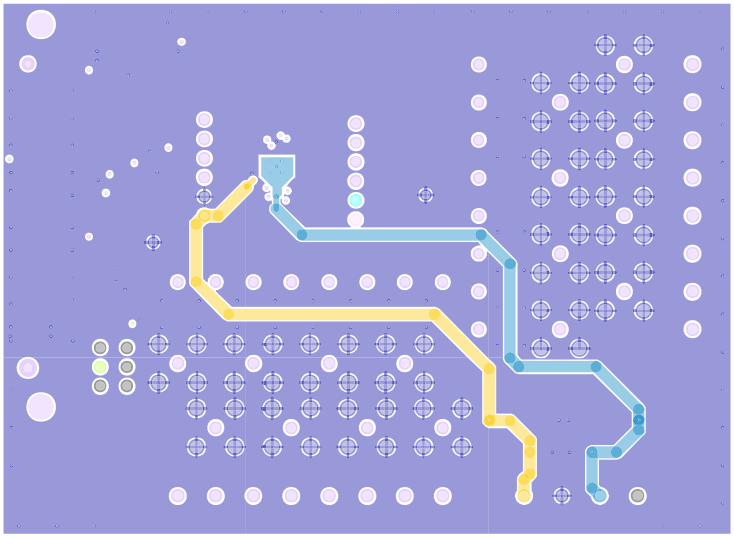

Figure 13. EV-ADGS1414DSDZ Layer 3

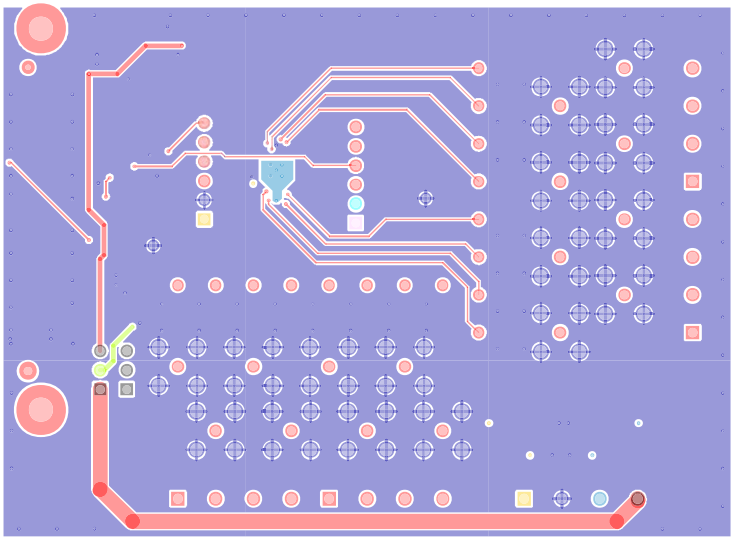

Figure 14. EV-ADGS1414DSDZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Reference Designator	Description
C1, C2	50 V tantalum capacitor, 10 µF, D size
C3, C4	50 V, X7R, multilayer ceramic capacitor, 0.1 µF, 0603
D1 to D8	Not placed
S1 to S8	Not placed
T-D1 to T-D8, T-S1 to T-S8	Red test point
TP17, TP18	Black test point
P1, P2, P5 to P7	4-pin terminal block, 5 mm pitch
P3 ,P4	Through hole, header, 4 × 2, 2.54 mm
J1	120-way connector, 0.6 mm pitch
JP1, JP2	3-pin single inline (SIL) header and shorting link
R1 to R8, R17 to R29, R32, R33, R35, R41 to R48, R55, R56, R59, R60	Not placed
R9 to R16, R30, R31, R34, R36 to R40, R50 to R53	Resistor, 0 Ω, 0603, 1%
R58	Resistor, 10 kΩ, 0.063 W, 1%, 0603
R49	Resistor, 1 MΩ, 0.25 W, 1%, 1206
R54, R57	Resistor, 100 kΩ, 0.063 W, 1%, 0603
SW1	Surface-mount device (SMD) push-button switch
U1	ADGS1414D, SPI controlled, octal SPST switch
U2	32 kΩ, I²C serial electronically erasable programmable read only memory (EEPROM)
U3	ADG819, 1.8 V to 5.5 V, 2:1 multiplexer and SPDT switch

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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