ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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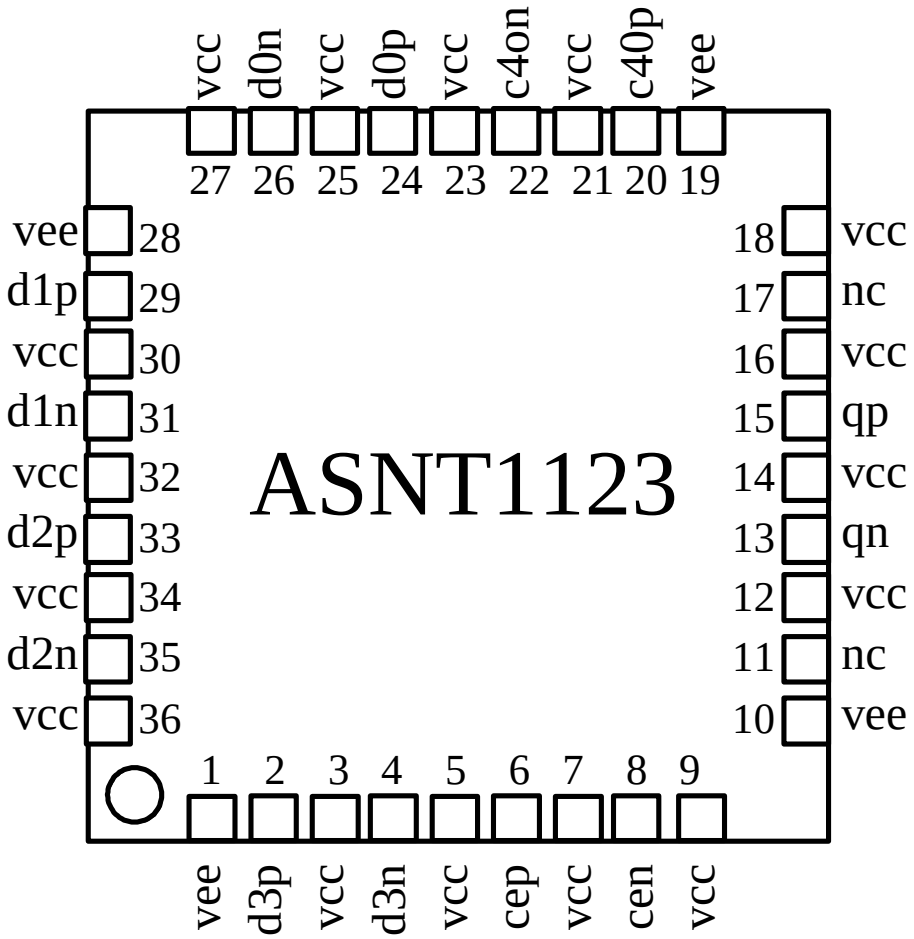
ASNT1123-PQP
DC-32*Gbps* Broadband Digital DDR 4:1 Multiplexer

- High speed broadband 4:1 Multiplexer (MUX)
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for high speed proof-of-concept prototyping
- Differential CML I/O data and clock buffers
- Half-rate clock input (DDR mode)
- Quarter-rate clock output
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.15*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Standard 36-pin QFN package with a thermal pad



DESCRIPTION

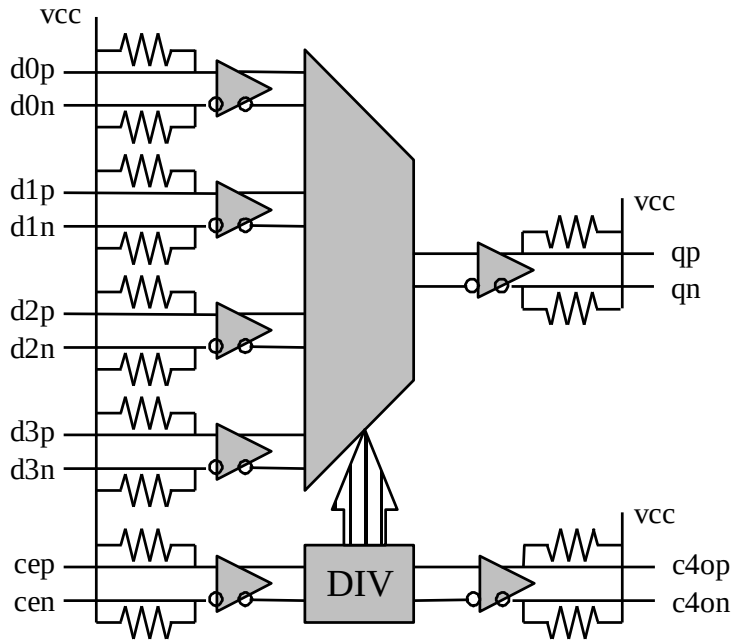


Fig. 1. Functional Block Diagram

The ASNT1123-PQP SiGe IC is a low power and high-speed digital 4 to 1 serializer-multiplexer (MUX) that functions seamlessly over data rates (f_{bit}) ranging from DC to its maximum frequency.

The main function of the part shown in Fig. 1 is to multiplex 4 parallel differential CML data signals d0p/d0n, d1p/d1n, d2p/d2n, d3p/d3n running at a bit rate of $f_{bit}/4$ into a high speed serial bit stream qp/qn running at a bit rate of f_{bit}. Differential or single-ended half-rate clock cep/cen (DDR mode) must be provided by an external source for the part to function properly.

The serialized data words qp/qn and the clock divided-by-4 signal c4op/c4on are transmitted through CML output interfaces. The clock and data outputs are phase-matched to each other resulting in very little relative skew over the operating temperature range of the device.

The input data streams should be phase-aligned to the output c4 clock as shown in Fig. 2 and Table 1.

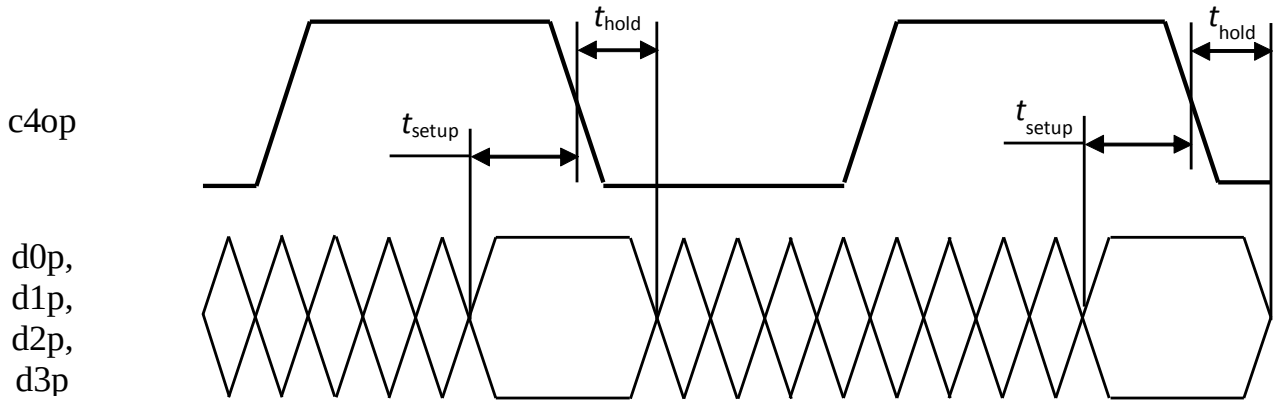


Fig. 2. Input Data Alignment to Output c4 Clock

Table 1. Input Data to Output c4 Clock Phase Requirements

Maximum required t_{setup}, *ps*	Maximum required t_{hold}, *ps*
25	-16

The output data is then delayed in relation to the input half-rate clock as shown in Fig. 3 and Table 2.

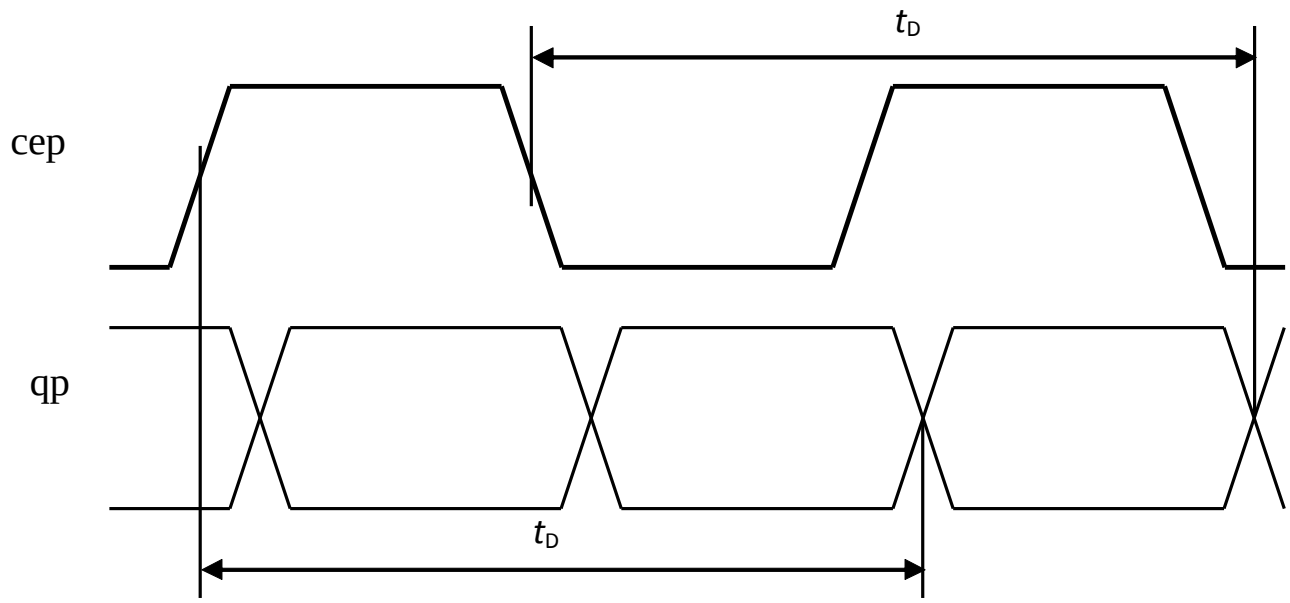


Fig. 3. Output Data to Input Clock Delay

Table 2. Output Data to Input Clock Delay Values (DDR Mode)

Minimum t_D, *ps*	Maximum t_D, *ps*
60	118

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.3	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
Low-Speed I/Os			
d0p	24	CML input	Differential quarter-rate data inputs with internal SE 50*Ohm* termination to vcc
d0n	26		
d1p	29	CML input	Differential quarter-rate data inputs with internal SE 50*Ohm* termination to vcc
d1n	31		
d2p	33	CML input	Differential quarter-rate data inputs with internal SE 50*Ohm* termination to vcc
d2n	35		
d3p	2	CML input	Differential quarter-rate data inputs with internal SE 50*Ohm* termination to vcc
d3n	4		
c4op	20	CML output	Differential quater-rate clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
c4on	22		
High-Speed I/Os			
cep	6	CML input	Differential half-rate clock input signals with internal 50*Ohm* termination to vcc
cen	8		
qp	15	CML output	Differential full-rate data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
qn	13		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	3, 5, 7, 9, 12, 14, 16, 18, 21, 23, 25, 27, 30, 32, 34, 36
vee	Negative power supply (0*V* or -3.3*V*)	1, 10, 19, 28
n/c	Not connected pins	11, 17

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		347		*mA*	
Power consumption		1.15		*W*	
Junction temperature	-40	25	125	*°C*	
LS Input Data (d0p/d0n, d1p/d1n, d2p/d2n, d3p/d3n)					
Data Rate	DC		8	*Gb/s*	
Swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cep/cen)					
Frequency	DC		16	*GHz*	
Swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty Cycle	40	50	60	*%*	
HS Output Data (qp/qn)					
Data Rate	DC		32	*Gb/s*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Output Jitter		2		*ps*	Peak-to-peak at 32*Gb/s*
LS Output Clock (c4op/c4on)					
Frequency	DC		4	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Duty Cycle		50		*%*	
Output Jitter			1	*ps*	Peak-to-peak at 4*GHz*

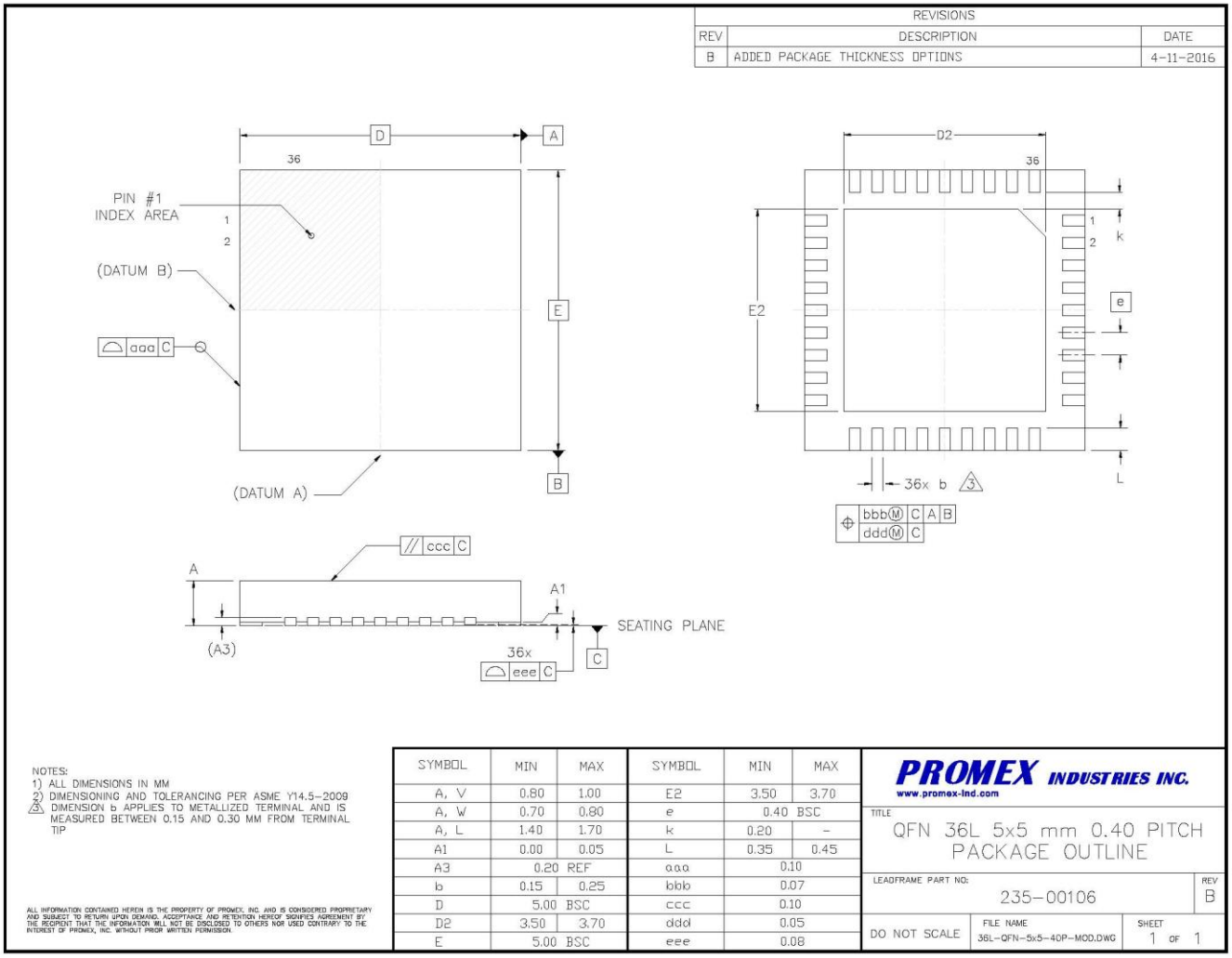
PACKAGE INFORMATION

The chip is packaged in a standard 36-pin QFN package shown Fig. 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part’s identification label is ASNT1123-PQP. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package’s manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous

substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.



SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	3.50	3.70
A, W	0.70	0.80	e	0.40 BSC	
A, L	1.40	1.70	k	0.20	–
A1	0.00	0.05	L	0.35	0.45
A3	0.20 REF		aaa	0.10	
b	0.15	0.25	bbb	0.07	
D	5.00 BSC		ccc	0.10	
D2	3.50	3.70	ddd	0.05	
E	5.00 BSC		eee	0.08	

Fig. 4. QFN 36-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.0.1	02-2021	First release