

# AFE7900 4T6R RF Sampling AFE with 12 GSPS DACs and 3 GSPS ADCs

## 1 Features

- [Request full data sheet](#)
- Quad RF sampling 12-GSPS transmit DACs
- Quad RF sampling 3-GSPS receive ADCs
- Dual RF sampling 3-GSPS feedback (auxiliary RX) ADCs
- Maximum RF signal bandwidth:
  - 4TX or 2FB: 1200 MHz or 2TX: 2400 MHz
  - RX): 1200 MHz (no FB), 600 MHz (with FB)
- RF frequency range:
  - TX: 5MHz - 7.4GHz
  - RX/FB: 5MHz -7.4GHz
- Digital step attenuators (DSA):
  - TX: 40 dB range, 0.125-dB steps
  - RX or FB: 25 dB range, 0.5-dB steps
- Single or dual-band DUC or DDCs for TX and RX
- 16x NCOs per TX or RX and FB
- Optional Internal PLL or VCO for DAC or ADC clocks or external clock at DAC or ADC sample rate
- Sysref Alignment Detector
- SerDes data interface:
  - JESD204B and JESD204C compatible
  - 8 SerDes transceivers up to 29.5 Gbps
  - Subclass 1 multi-device synchronization
- Package: 17-mm × 17-mm FCBGA, 0.8-mm pitch

## 2 Applications

- [Radar](#)
- [Seeker front end](#)
- [Defense radio](#)
- Tactical communications infrastructure
- [Wireless communications test](#)

## 3 Description

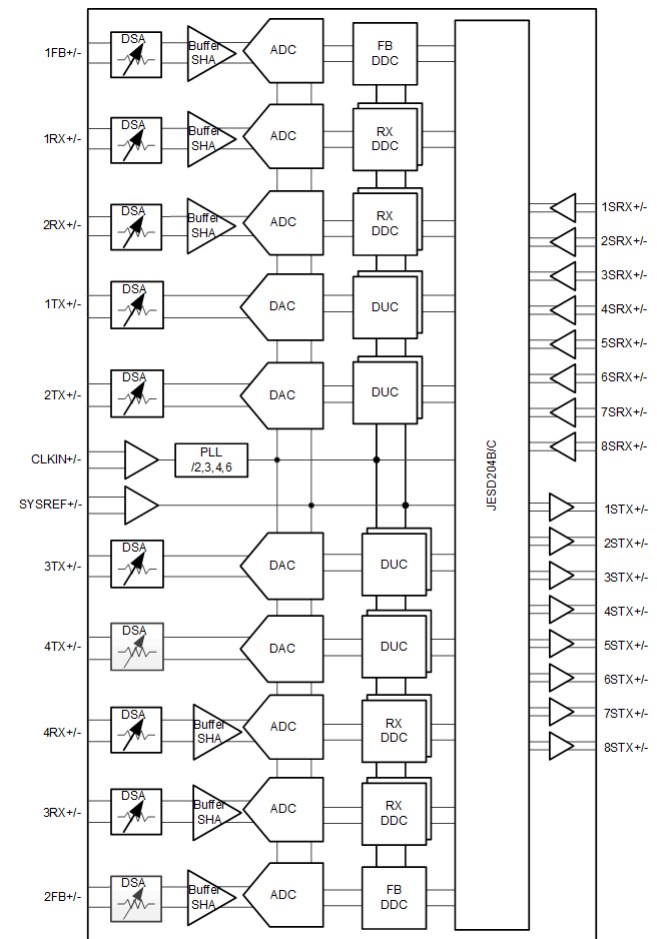
The AFE7900 is a high performance, wide bandwidth multi-channel transceiver, integrating four RF sampling transmitter chains, four RF sampling receiver chains and two RF sampling feedback chains (six RF sampling ADCs total). With operation up to 7.4 GHz, this device enables direct RF sampling in the L, S and C-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

The TX signal paths support interpolation and digital up conversion options that deliver up to 1200 MHz of signal bandwidth for four TX or 2400 MHz for two TX. The output of the DUCs drives a 12-GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2nd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40-dB range and 1-dB analog and 0.125-dB digital steps.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE
AFE7900	FC-BGA	17.00 mm × 17.00 mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.



Functional Block Diagram



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## 4 Description (continued)

Each receiver chain includes a 25-dB range DSA (Digital Step Attenuator), followed by a 3-GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of data bandwidth up to 1200 MHz for four RX without FB paths or 600 MHz with two FB paths (1200 MHz BW each).

The device contains a SYSREF timing detector to allow optimization of the SYSREF input timing relative to the device clock.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (February 2021) to Revision A (August 2021)</b>	<b>Page</b>
• Added <i>Feature</i> to Request the full data sheet.....	<a href="#">1</a>
• Added the <a href="#">Specification</a> tables to the data sheet.....	<a href="#">4</a>
• Added the <a href="#">Typical Characteristics</a> section to the data sheet.....	<a href="#">32</a>

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## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	-0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	-0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVC0, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	-0.5	2.1	V
Pin Voltage Range	{1/2/3/4}RXIN+/-	-0.5	VDDR1P8+0.3	V
	1FBIN+/-, 2FB+/-	-0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	-0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	-0.3	1.4	V
	{1:8}SRX+/-	-0.3	1.4	V
	{1:8}STX+/-	-0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	-0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	-0.3	VDDCLK1P8 + 0.3	V
SRDAMUX1, SRDAMUX2	-0.3	VDDA1P8+0.3	V	
Peak Input Current	any input		20	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	150	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.



### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T <sub>A</sub>	Ambient temperature	-40		85	°C
T <sub>J</sub>	Operating Junction Temperature			110 <sup>(1)</sup>	°C
	Maximum Operating Junction Temperature	125			°C

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		AFE7900	UNIT
		ABJ (FC-BGA)	
		400 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	16.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.42	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	4.85	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.12	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	4.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Transmitter Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{DAC} = 11796.48\text{MSPS}$  below 6GHz and  $f_{DAC} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC <sub>RES</sub>	DAC resolution			14		bits
f <sub>RFout</sub>	RF output frequency range	f <sub>DAC</sub> = 12 GSPS, 1 <sup>st</sup> Nyquist	5		6000	MHz
		f <sub>DAC</sub> = 9 GSPS, 1 <sup>st</sup> Nyquist	5		4500	
		f <sub>DAC</sub> = 9 GSPS, 2 <sup>nd</sup> Nyquist	4500		7400	
		f <sub>DAC</sub> = 6 GSPS, 1 <sup>st</sup> Nyquist	5		3000	
		f <sub>DAC</sub> = 6 GSPS, 2 <sup>nd</sup> Nyquist	3000		6000	
P <sub>max_FS</sub>	Max Full Scale Output Power, max gain 1 tone, at device pins	f <sub>out</sub> = 10 MHz, f <sub>DAC</sub> = 6GSPS, -0.1dBFS		6.5		dBm
		f <sub>out</sub> = 30 MHz, f <sub>DAC</sub> = 6GSPS, -0.1dBFS		6.5		dBm
		f <sub>out</sub> = 400 MHz, f <sub>DAC</sub> = 6GSPS, -0.1dBFS		5.6		dBm
		f <sub>out</sub> = 850 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS		4.3		dBm
		f <sub>out</sub> = 1800 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS		3.2		dBm
		f <sub>out</sub> = 2600 MHz, f <sub>DAC</sub> = 8847.36 MSPS, -0.5dBFS		2.3		dBm
		f <sub>out</sub> = 3500 MHz, -0.5dBFS		2.9		dBm
		f <sub>out</sub> = 4900 MHz, -0.5dBFS		-0.6		dBm
		f <sub>out</sub> = 3500 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS, straight mode		-2.3		dBm
		f <sub>out</sub> = 4900 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS, straight mode		-3.4		dBm
		f <sub>out</sub> = 4900 MHz, f <sub>DAC</sub> = 8847.36 MSPS, -0.5dBFS, straight mode		-3.9		dBm
R <sub>TERM</sub>	Output termination resistor	Default setting		100		Ω
ATT <sub>range</sub>	DSA Attenuation range			40		dB
ATT <sub>step</sub>	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL) (2)	0 < Atten < 40dB, after calibration		±0.1		dB
		0 < Atten < 40dB, before calibration			±0.2	
ATT <sub>step</sub>	DSA Gain Steps Phase accuracy, any 8dB range(2)	f <sub>out</sub> = 30MHz		±1		deg
		f <sub>out</sub> = 400MHz		±1		deg
		f <sub>out</sub> = 850MHz		±1		deg
		f <sub>out</sub> = 1800MHz		±1		deg
		f <sub>out</sub> = 2600MHz		±1		deg
		f <sub>out</sub> = 3500MHz		±1		
		f <sub>out</sub> = 4900MHz		±1		deg
G <sub>flat</sub>	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F <sub>out</sub> < 4.9G		1.2		

### 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  below 6GHz and  $f_{\text{DAC}} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion	$f_{\text{DAC}} = 6 \text{ GSPS}$ , $f_{\text{out}} = 5 \text{ MHz}$ $\pm 1 \text{ MHz}$ , -7dBFS each tone		-48		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}$ , $f_{\text{out}} = 30 \text{ MHz}$ $\pm 1 \text{ MHz}$ , -7dBFS each tone		-47		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}$ , $f_{\text{out}} = 400 \text{ MHz}$ $\pm 2 \text{ MHz}$ , -7dBFS each tone		-51		dBc
		$f_{\text{out}} = 850 \text{ MHz} \pm 10 \text{ MHz}$ , -7dBFS each tone		-61		dBc
		$f_{\text{out}} = 1800 \text{ MHz} \pm 10 \text{ MHz}$ , -7dBFS each tone		-62		dBc
		$f_{\text{out}} = 2600 \text{ MHz} \pm 10 \text{ MHz}$ , -7dBFS each tone		-64		dBc
		$f_{\text{out}} = 3500 \text{ MHz} \pm 10 \text{ MHz}$ , -7dBFS each tone		-63		dBc
		$f_{\text{out}} = 4900 \text{ MHz} \pm 10 \text{ MHz}$ , -7dBFS each tone		-64		dBc
		$f_{\text{out}} = 5 \text{ MHz} \pm 1 \text{ MHz}$ , -13dBFS each tone		-72		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}$ , $f_{\text{out}} = 30 \text{ MHz}$ $\pm 1 \text{ MHz}$ , -13dBFS each tone		-71		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}$ , $f_{\text{out}} = 400 \text{ MHz}$ $\pm 2 \text{ MHz}$ , -13dBFS each tone		-72		dBc
		$f_{\text{out}} = 850 \text{ MHz} \pm 10 \text{ MHz}$ , -13dBFS each tone		-73		dBc
		$f_{\text{out}} = 1800 \text{ MHz} \pm 10 \text{ MHz}$ , -13dBFS each tone		-75		dBc
		$f_{\text{out}} = 2600 \text{ MHz} \pm 10 \text{ MHz}$ , -13dBFS each tone		-79		dBc
		$f_{\text{out}} = 3500 \text{ MHz} \pm 10 \text{ MHz}$ , -13dBFS each tone		-77		dBc
$f_{\text{out}} = 4900 \text{ MHz} \pm 10 \text{ MHz}$ , -13dBFS each tone		-77		dBc		
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 30 \text{ MHz}$ , $f_{\text{DAC}} = 6000 \text{ MSPS}$ , interleave mode, 20Gbps SerDes rate		45		dBc
		$f_{\text{out}} = 400 \text{ MHz}$ , $f_{\text{DAC}} = 6000 \text{ MSPS}$ , interleave mode, 20Gbps SerDes rate		48		dBc
		$f_{\text{out}} = 850 \text{ MHz}$ , $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		62		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$ , $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		56		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$ , $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		39		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$ , $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		42		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$ , $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		60		dBc

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  below 6GHz and  $f_{\text{DAC}} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_s/2 - f_{\text{OUT}}$	Interleaving Image	$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode		-47		dBc
		$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode		-43		dBc
		$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode		-43		dBc
HD2	2 <sup>nd</sup> Harmonic Distortion (within Nyquist zone)	$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 5\text{MHz}$		-72		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 30\text{MHz}$		-75		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 100\text{MHz}$		-73		dBc
		$f_{\text{out}} = 400\text{MHz}$		-46		dBc
		$f_{\text{out}} = 850\text{MHz}$		-65		dBc
		$f_{\text{out}} = 1800\text{MHz}$		-68		dBc
		$f_{\text{out}} = 2600\text{MHz}$		-47		dBc
		$f_{\text{out}} = 3500\text{MHz}$		-59		dBc
		$f_{\text{out}} = 4900\text{MHz}$		-48		dBc
		$f_{\text{out}} = 850\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-74		dBc
		$f_{\text{out}} = 1800\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-67		dBc
		$f_{\text{out}} = 2600\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-58		dBc
		$f_{\text{out}} = 3500\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-69		dBc
$f_{\text{out}} = 4900\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-59		dBc		
HD3	3 <sup>rd</sup> Harmonic Distortion (within Nyquist zone)	$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 5\text{MHz}$		-46		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 30\text{MHz}$		-48		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 100\text{MHz}$		-49		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 400\text{MHz}$		-49		dBc
		$f_{\text{out}} = 850\text{MHz}$		-56		dBc
		$f_{\text{out}} = 1800\text{MHz}$		-58		dBc
		$f_{\text{out}} = 2600\text{MHz}$		-60		dBc
		$f_{\text{out}} = 3500\text{MHz}$		-63		dBc
		$f_{\text{out}} = 4900\text{MHz}$		-66		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 5\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-83		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 30\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-83		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 100\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{DAC}} = 6\text{GSPS}$ , $f_{\text{out}} = 400\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 850\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 1800\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 2600\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 3500\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 4900\text{MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-88		dBc

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  below 6GHz and  $f_{\text{DAC}} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD <sub>n</sub> , n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 5 \text{ MHz}$		-58		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 30 \text{ MHz}$		-60		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 100 \text{ MHz}$		-61		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 400 \text{ MHz}$		-50		dBc
		$f_{\text{out}} = 850 \text{ MHz}$		-85		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-90		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-84		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-86		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-87		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 5 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-92		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 30 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-94		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 400 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-85		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-89		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-92		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-88		dBc
$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-89		dBc		
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 400 \text{ MHz}$		87		dBc
		$f_{\text{out}} = 850 \text{ MHz}, f_{\text{DAC}} = 11796.48 \text{ MSPS}$		84		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, f_{\text{DAC}} = 11796.48 \text{ MSPS}$		78		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, f_{\text{DAC}} = 11796.48 \text{ MSPS}$		80		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, f_{\text{DAC}} = 11796.48 \text{ MSPS}$		81		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, f_{\text{DAC}} = 11796.48 \text{ MSPS}$		74		dBc
$f_s/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}, f_{\text{OUT}} = f_{\text{DAC}}/4\text{-}50\text{MHz}$		-95		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}, f_{\text{OUT}} = f_{\text{DAC}}/4\text{-}50\text{MHz}$		-88		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}, f_{\text{OUT}} = f_{\text{DAC}}/4\text{-}50\text{MHz}$		-76		dBFS
$f_s/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}, f_{\text{OUT}} = f_{\text{DAC}}/2\text{-}50\text{MHz}$		-52		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}, f_{\text{OUT}} = f_{\text{DAC}}/2\text{-}50\text{MHz}$		-45		dBFS
		$f_{\text{DAC}} = 11796.48 \text{ MSPS}, f_{\text{OUT}} = f_{\text{DAC}}/2\text{-}50\text{MHz}$		-49		dBFS

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  below 6GHz and  $f_{\text{DAC}} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$3*f_S/4$	Fixed Spur	2nd Nyquist, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $f_{\text{OUT}}=3*f_{\text{DAC}}/4-50\text{MHz}$		-82		dBFS
		2nd Nyquist, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , $f_{\text{OUT}}=3*f_{\text{DAC}}/4-50\text{MHz}$		-75		dBFS
		2nd Nyquist, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , $f_{\text{OUT}}=3*f_{\text{DAC}}/4-50\text{MHz}$		-49		dBFS
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-70		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-66		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-62		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-51		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 1.8425\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-71		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-66		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-61		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-50		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-72		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-66		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-60		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-49		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-71		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-65		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-58		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-47		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-69		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-64		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-58		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-47		dBc

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  below 6GHz and  $f_{\text{DAC}} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 2.6$ GHz	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-65		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-59		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-53		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-41		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 3.5$ GHz	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-63		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-56		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-49		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-38		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 4.9$ GHz	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-63		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-56		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-51		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-41		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85$ GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.16		%
		$F_{\text{out}} = 1.8425$ GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.21		%
		$F_{\text{out}} = 2.6$ GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.24		%
		$F_{\text{out}} = 3.5$ GHz, $P_{\text{OUT}} = -13\text{dBFS}$		0.27		%
		$F_{\text{out}} = 4.9$ GHz, $P_{\text{OUT}} = -13\text{dBFS}$		0.38		%
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 5$ MHz	Atten=0dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-148		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-143		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-139		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-129		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 30$ MHz	Atten=0dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-154		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-146		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-142		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-132		dBFS/Hz

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  below 6GHz and  $f_{\text{DAC}} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 100\text{ MHz}$	Atten=0dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-158		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-150		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-146		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-136		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 400\text{ MHz}$	Atten=0dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-160		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-153		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-150		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 6000\text{MSPS}$ , 20Gbps SerDes rate, Pout=-12dBFS		-139		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-158.8		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-152.7		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-148.7		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-137.9		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-157.9		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-151.3		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-145.6		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-134.8		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-158.3		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-151.6		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-144.9		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-134.0		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-158.2		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-150.9		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-144.4		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-133.4		dBFS/ Hz



## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  below 6GHz and  $f_{\text{DAC}} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-154.6		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-147.0		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-140.7		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$ , Pout=-13dBFS		-129.9		dBFS/ Hz
S22	Output Return Loss, +/- fc * 10%	with matching		-12		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT <sup>(1)</sup>	$f_{\text{out}} = 10\text{ MHz}$ , $f_{\text{DAC}} = 6000\text{MSPS}$ , straight mode <sup>(3)</sup>		-96		dB
		$f_{\text{out}} = 30\text{ MHz}$ , $f_{\text{DAC}} = 6000\text{MSPS}$ , straight mode <sup>(3)</sup>		-97		dB
		$f_{\text{out}} = 100\text{ MHz}$ , $f_{\text{DAC}} = 6000\text{MSPS}$ , straight mode <sup>(3)</sup>		-102		dB
		$f_{\text{out}} = 400\text{ MHz}$ , $f_{\text{DAC}} = 6000\text{MSPS}$ , straight mode <sup>(4)</sup>		-85		dB
		$f_{\text{out}} = 900\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-80		dB
		$f_{\text{out}} = 1850\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-77		dB
		$f_{\text{out}} = 2600\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-64		dB
		$f_{\text{out}} = 3500\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-61		dB
		$f_{\text{out}} = 4900\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-60		dB
Isolation	Far Channel: 1/2TXOUT to 3/4TXOUT	$f_{\text{out}} = 10\text{ MHz}$ , $f_{\text{DAC}} = 6000\text{MSPS}$ , straight mode <sup>(3)</sup>		-104		dB
		$f_{\text{out}} = 30\text{ MHz}$ , $f_{\text{DAC}} = 6000\text{MSPS}$ , straight mode <sup>(3)</sup>		-100		dB
		$f_{\text{out}} = 100\text{ MHz}$ , $f_{\text{DAC}} = 6000\text{MSPS}$ , straight mode <sup>(3)</sup>		-105		dB
		$f_{\text{out}} = 400\text{ MHz}$ , $f_{\text{DAC}} = 6000\text{MSPS}$ , straight mode <sup>(4)</sup>		-97		dB
		$f_{\text{out}} = 900\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-90		dB
		$f_{\text{out}} = 1850\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-91		dB
		$f_{\text{out}} = 2600\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-93		dB
		$f_{\text{out}} = 3500\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-94		dB
		$f_{\text{out}} = 4900\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-83.2		dB

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  below 6GHz and  $f_{\text{DAC}} = 9000\text{MSPS}$  above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN <sub>TXADD</sub>	Additive Phase Noise External Clock Mode <sup>(5)</sup>	$f_{\text{out}} = 3.7\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{Hz}$		-97		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{kHz}$		-106		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{kHz}$		-117		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{kHz}$		-128		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{MHz}$		-138		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{MHz}$		-144		dBc/Hz

- (1) Measured with differential 100 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
- (2) After DSA calibration procedure
- (3) measured with 1 $\mu\text{H}$  DC feed inductor
- (4) measured with 0.39 $\mu\text{H}$  DC feed inductor
- (5) Input clock phase noise subtracted.

## 6.6 RF ADC Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$  below 6GHz and  $f_{\text{ADC}} = 3000\text{MSPS}$  above 6GHz; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC <sub>RES</sub>	ADC resolution			14		bits
F <sub>RFIn</sub>	RF input frequency range		5		7400	MHz
P <sub>FS_CW,min</sub>	Min Full scale input power, at device pins (1)	$f_{\text{IN}} = 5\text{ MHz}$ , DSA=0dB, $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-0.4		dBm
		$f_{\text{IN}} = 30\text{ MHz}$ , DSA=0dB, $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		-2.2		dBm
		$f_{\text{IN}} = 410\text{ MHz}$ , DSA=0dB, $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 12		-2.5		dBm
		$f_{\text{IN}} = 830\text{ MHz}$ , DSA=0dB		-2.9		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$ , DSA=0dB		-2.8		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$ , DSA=0dB		-1.8		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$ , DSA=0dB		-0.4		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$ , DSA=0dB		0.1		dBm
P <sub>FS_CW,MAX</sub>	MAX Full scale input power - reliability limited, at device pins	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		19.7		dBm
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		17.8		dBm
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		17.6		dBm
		$f_{\text{IN}} = 830\text{ MHz}$		16.7		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$		17.0		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$		18		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$		18.5		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$		19.3		dBm
R <sub>TERM</sub>	Input reference impedance			100.0		$\Omega$
ATT <sub>range</sub>	DSA Attenuation range			25.0		dB
ATT <sub>step</sub>	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), $F_{\text{in}}=3610\text{MHz}$ , after calibration		0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	$F_{\text{in}}=3610\text{MHz}$ , after calibration		0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	$F_{\text{in}}=4910\text{MHz}$ , after calibration		1.8		deg
G <sub>flat</sub>	Gain flatness	Measured Over 80MHz BW		0.2		dB
		Measured Over 200MHz BW		0.5		dB
		Measured Over 400MHz BW		1.1		dB

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$  below 6GHz and  $f_{\text{ADC}} = 3000\text{MSPS}$  above 6GHz; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Density <sup>(3)</sup> (small signal = -30dBFS)	$f_{\text{IN}} = 5\text{ MHz}$ , DSA = 3dB, $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-147.1		dBFS/Hz
		$f_{\text{IN}} = 30\text{ MHz}$ , DSA = 3dB, $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		-150.7		dBFS/Hz
		$f_{\text{IN}} = 410\text{ MHz}$ , DSA = 3dB, $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		-155.4		dBFS/Hz
		$f_{\text{IN}} = 830\text{ MHz}$ , DSA = 3dB		-156.2		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$ , DSA = 3dB		-156.0		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$ , DSA = 3dB		-155.4		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$ , DSA = 3dB		-155.1		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$ , DSA = 3dB		-155.1		dBFS/Hz
		$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48, 3<=Atten<=22		-147.8		dBFS/Hz
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24, 3<=Atten<=22		-151.5		dBFS/Hz
		$f_{\text{IN}} = 410\text{ MHz}$ , 3<=Atten<=22, $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		-156.6		dBFS/Hz
		$f_{\text{IN}} = 830\text{ MHz}$ , 3<=Atten<=22		-156.0		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$ , 3<=Atten<=25		-155.8		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$ , 3<=Atten<=25		-155.7		dBFS/Hz
$f_{\text{IN}} = 3610\text{ MHz}$ , 3<=Atten<=25		-155.4		dBFS/Hz		
$f_{\text{IN}} = 4910\text{ MHz}$ , 3<=Atten<=25		-155.8		dBFS/Hz		
NF <sub>min</sub>	Noise Figure min DSA Atten=0 - 3dB	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		29.4		dB
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		24.5		dB
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		19.3		dB
		$f_{\text{IN}} = 830\text{ MHz}$		19.1		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		19.0		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		20.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		22.8		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		22.4		dB

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$  below 6GHz and  $f_{\text{ADC}} = 3000\text{MSPS}$  above 6GHz; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure <sup>(4)</sup> DSA Atten=4dB	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		30.6		dB
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		25.1		dB
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		20.1		dB
		$f_{\text{IN}} = 830\text{ MHz}$		20.0		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		20.6		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		21.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		23.5		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		22.3		dB
NF <sub>max</sub>	Noise Figure DSA Atten=20dB	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		45.9		dB
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		40.2		dB
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		35.0		dB
		$f_{\text{IN}} = 830\text{ MHz}$		34.7		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		35.2		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		36.0		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		37.3		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		37.6		dB
IMD3	3 <sup>rd</sup> order intermodulation 2 tones at at $f_{\text{IN}} \pm 10\text{MHz}$ -7dBFS each tone	$f_{\text{IN}} = 30 \pm 1\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		-82		dBc
		$f_{\text{IN}} = 400\text{MHz}$ and $405\text{MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		-75		dBc
		$f_{\text{IN}} = 840\text{ MHz}$		-82		dBc
		$f_{\text{IN}} = 1770\text{ MHz}$		-84		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-74		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-77		dBc
		$f_{\text{IN}} = 4920\text{ MHz}$		-76		dBc

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$  below 6GHz and  $f_{\text{ADC}} = 3000\text{MSPS}$  above 6GHz; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		78		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		100		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		94		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		81		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		79		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}^{(2)}$	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-84		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , Bypass Mode (TI only test mode)		-91		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , Bypass Mode (TI only test mode)		-90		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-87		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-84		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-78		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , Bypass Mode (TI only test mode)		-96		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , Bypass Mode (TI only test mode)		-94		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-80		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-85		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-75		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-94		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		-94		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		-94		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-81		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-82		dBFS

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$  below 6GHz and  $f_{\text{ADC}} = 3000\text{MSPS}$  above 6GHz; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious Free Dynamic Range $A_{\text{IN}} = -13\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		101		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		105		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		95		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		89		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		89		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		87		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		90		dBFS
HD2	2nd Harmonic Distortion <sup>(2)</sup> $A_{\text{IN}} = -13\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-104		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , Bypass Mode (TI only test mode)		-91		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , Bypass Mode (TI only test mode)		-104		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$ , with board trim		-79		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$ , with board trim		-102		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$ , with board trim		-100		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$ , with board trim		-101		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$ , with board trim		-99		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-103		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , Bypass Mode (TI only test mode)		-84		dBFS
		$f_{\text{IN}} = 381\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , Bypass Mode (TI only test mode)		-91		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-98		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-97		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-94		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -13\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-104		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		-105		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24		-95		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-89		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-89		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-90		dBFS

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$  below 6GHz and  $f_{\text{ADC}} = 3000\text{MSPS}$  above 6GHz; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 3dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RX-RX/FB Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN 1FBIN to 1RXIN 2FBIN to 3RXIN	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-98		dB
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		-98		dB
		$f_{\text{IN}} = 400\text{ MHz}$		-88		dB
		$f_{\text{IN}} = 830\text{ MHz}$		-77		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		-71		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		-74		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		-77		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		-65		dB
TX-FB Isolation	Near Channel: 1TXOUT to 1FBIN 3TXOUT to 2FBIN	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-92		dB
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		-93		dB
		$f_{\text{IN}} = 400\text{ MHz}$		-92		dB
		$f_{\text{IN}} = 830\text{ MHz}$		-84		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		-88		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		-86		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		-82		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		-81		dB
TX-RX Isolation	Far Channel: 1TXOUT to 1RXIN 3TXOUT to 2RXIN	$f_{\text{IN}} = 5\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48		-105		dB
		$f_{\text{IN}} = 30\text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24		-101		dB
		$f_{\text{IN}} = 400\text{ MHz}$		-99		dB
		$f_{\text{IN}} = 830\text{ MHz}$		-86		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		-87		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		-84		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		-82		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		-82		dB

- (1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) After HD2 trim on specific printed circuit board.
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB



## 6.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f<sub>DAC</sub> = f<sub>VCO</sub>, f<sub>OUT</sub> = f<sub>DAC</sub>/4, normalized to f<sub>VCO</sub>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>VCO1</sub>	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f <sub>VCO2</sub>	VCO2 min frequency				8.848	GHz
	VCO2 max frequency		9.216			GHz
f <sub>VCO3</sub>	VCO3 min frequency				9.8304	GHz
	VCO3 max frequency		10.24			GHz
f <sub>VCO4</sub>	VCO4 min frequency				11.7965	GHz
	VCO4 max frequency		12.288			GHz
DIV <sub>DAC</sub>	DAC sample rate divider			1, 2 or 3		
DIV <sub>FBADC</sub>	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
DIV <sub>RXADC</sub>	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN <sub>VCO</sub>	Closed Loop Phase Noise F <sub>PLL</sub> = 11.79848 GHz F <sub>REF</sub> =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		-141		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> =8.84736 GHz F <sub>REF</sub> =491.52MHz	600kHz		-114		dBc/Hz
		800kHz		-118		dBc/Hz
		1MHz		-120		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-135		dBc/Hz
		50MHz		-142		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> = 9.8403 GHz F <sub>REF</sub> =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-134		dBc/Hz
		50MHz		-140		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> = 7.86432GHz F <sub>REF</sub> =491.52MHz	600kHz		-116		dBc/Hz
		800kHz		-119		dBc/Hz
		1MHz		-122		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-136		dBc/Hz
		50MHz		-143		dBc/Hz
F <sub>rms</sub>	Clock PLL integrated phase error <sup>(1)</sup>	f <sub>PLL</sub> =11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f <sub>PLL</sub> =8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f <sub>PLL</sub> =9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f <sub>PFD</sub>	PFD frequency		100		500	MHz
PN <sub>pll_flat</sub>	Normalized PLL flat Noise	f <sub>VCO</sub> = 11796.48MHz		-226.5		dBc/Hz
F <sub>REF</sub>	Input Clock frequency		0.1		12	GHz
V <sub>SS</sub>	Input Clock level		0.6		1.8	Vppdiff

## 6.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; Reference clock input frequency 491.52MHz (unless otherwise noted),  $f_{\text{DAC}} = f_{\text{VCO}}$ ,  $f_{\text{OUT}} = f_{\text{DAC}}/4$ , normalized to  $f_{\text{VCO}}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance <sup>(2)</sup>	Parallel resistance		100		$\Omega$
		Parallel capacitance		0.5		pF

- (1) Single Sideband, not including the reference clock contribution  
(2) Refer to S11 data available from TI for impedance vs frequency

## 6.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CML SerDes Inputs [8:1]SRX+/-</b>						
V <sub>SRDIFF</sub>	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V <sub>SRCOM</sub>	SerDes Input Common Mode			400		mV
Z <sub>SRdiff</sub>	SerDes Internal Differential Termination <sup>(1)</sup>			100		Ω
F <sub>SerDes</sub>	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance <sup>(2)</sup>	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
<b>CML SerDes Outputs [8:1]STX+/-</b>						
V <sub>STDIFF</sub>	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V <sub>STCOM</sub>	SerDes Output Common Mode		0.4	0.45	0.55	V
Z <sub>STdiff</sub>	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
<b>CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1</b>						
V <sub>IH</sub>	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V <sub>IL</sub>	Low-Level Input Voltage				0.4×VDD1 P8GPIO	V
I <sub>IH</sub>	High-Level Input Current		-250		250	mA
I <sub>IL</sub>	Low-Level Input Current		-250		250	mA
C <sub>L</sub>	CMOS input capacitance			2		pF
V <sub>OH</sub>	High-Level Input Voltage		VDD1P8G PIO-0.2			V
V <sub>OL</sub>	Low-Level Input Voltage				0.2	V
<b>Differential Inputs: SYSREF+/- Mode A</b>						
F <sub>SYSREFMAX</sub>	SYSREF Input Frequency Maximum			40		MHz
V <sub>SWINGSRMAX</sub>	SYSREF Input Swing Maximum			1.8		Vppdiff <sup>(3)</sup>
V <sub>SWINGSRMIN</sub>	SYSREF Input Swing Minimum	f <sub>REF</sub> < 500MHz		0.3		Vppdiff <sup>(3)</sup>
V <sub>SWINGSRMIN</sub>	SYSREF Input Swing Minimum	f <sub>REF</sub> > 500MHz		0.6		Vppdiff <sup>(3)</sup>
V <sub>COMSRMAX</sub>	SYSREF Input Common Mode Voltage Maximum			0.8		V
V <sub>COMSRMIN</sub>	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z <sub>T</sub>	Input termination	differential		100 <sup>(1)</sup>		Ω
C <sub>L</sub>	Input capacitance	Each pin to GND		0.5		pF
<b>LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-</b>						
V <sub>ICOM</sub>	Input Common Voltage			1.2		V
V <sub>ID</sub>	Differential Input Voltage swing			450		Vppdiff <sup>(3)</sup>
Z <sub>T</sub>	Input termination	differential		100		Ω
<b>LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-</b>						
V <sub>OCOM</sub>	Output Common Voltage			1.2		V
V <sub>OD</sub>	Differential Output Voltage swing			500		Vppdiff <sup>(3)</sup>

## 6.8 Digital Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_T$	Internal Termination			100		$\Omega$

- (1) SYSREF termination is programmable between 100 $\Omega$ , 150 $\Omega$  and 300 $\Omega$
- (2) Loss tolerance is bump to bump from STX to SRX
- (3)  $V_{ppdiff}$  is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

## 6.9 Power Supply Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; TX Input Rate = 737.28MSPS,  $f_{DAC} = 8847.36\text{MSPS}$  interleave mode;  $f_{ADC} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T2F - FDD FB 100% on, no RX TX/FB Rate: 491.52 Msps Single Band: 12x Int, FB 6x Dec $f_{DAC} = 5898.24$ SPS $f_{ADC} = 2949.12\text{MSPS}$ $f_{TX} = 1.85$ GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1		948.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDPA1P8			533.7		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			77.3		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			299.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			804.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			49.1		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			2041.3		mA
$P_{diss}$	Power Dissipation			6027.1		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 2: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 12x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{DAC} = 8847.36\text{MSPS}$ $f_{ADC} = 2949.12\text{MSPS}$ $f_{OUT}=f_{IN} = 1.9, 2.6$ GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		820.4	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDPA1P8			735.2		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			74.4		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			289.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			822.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			45.6		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			2263.8		mA
$P_{diss}$	Power Dissipation			6359.2		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R2F - FDD FB 100% on TX Dual Band: 12x Int, FB 6x Dec RX Dual Band: RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{DAC} = 11796.48$ MSPS $f_{ADC} = 2949.12$ MSPS $f_{TX} = 1.85 + 2.15$ GHz $f_{RX} = 1.75 + 1.88$ GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1			1668.6	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDPA1P8			965.1		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			77.6		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			893.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			879.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			50.7		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			3826.9		mA
$P_{diss}$	Power Dissipation			10513.0		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 737.28MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4T4R2F - FDD FB 100% on 7.5 GSPS DAC, 2.5 GSPS ADC Single Band: 15x Int, FB 5x Dec Dual Band: RX 20x TX/FB Rate 491.52 MspS RX Rate 122.88 MspS $f_{\text{DAC}} = 7372.8\text{MSPS}$ $f_{\text{ADC}} = 2457.6\text{MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-16-16-1	1611.5			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		694.5			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		72.8			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX		768.5			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		940.5			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		45.5			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		3000.5			mA
$P_{\text{diss}}$	Power Dissipation		9087.4			mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 5: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 MspS RX Rate 491.52 MspS $f_{\text{DAC}} = 11796.48\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 3.5\text{GHz}$ $f_{\text{RX}} = 3.5\text{GHz}$ 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1	821.8		
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8	808.5				mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0	77.4				mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	289.5				mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC	682.0				mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF	49.0				mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9	2123.3				mA
$P_{\text{diss}}$	Power Dissipation	6209.3				mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 8: same configuration as mode 7, Sleep Mode. SLEEP pin is pull high.		20.3		
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		292.8			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		12.6			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX		4.6			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		54.3			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		15.3			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		313.1			mA
$P_{\text{diss}}$	Power Dissipation		956.8			mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; TX Input Rate = 737.28MSPS,  $f_{DAC} = 8847.36\text{MSPS}$  interleave mode;  $f_{ADC} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 9: 4T4R2F - FDD FB 100% on TX Single Band: 24x Int, FB 12x Dec RX Single Band: RX 24x TX/FB Rate 245.76 Msps RX Rate 122.88 Msps $f_{DAC} = 5898.24\text{ MSPS}$ $f_{ADC} = 2949.12\text{ MSPS}$ $f_{TX} = 0.85\text{ GHz}$ $f_{RX} = 0.8\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-8-8-1		1593.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			840.6		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			77.3		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			905.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			817.7		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			52.1		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			2405.2		mA
$P_{diss}$	Power Dissipation			8814.3		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 10: 4T4R2F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msps RX Rate 245.76 Msps $f_{DAC} = 8847.36\text{ MSPS}$ $f_{ADC} = 2949.12\text{ MSPS}$ $f_{TX} = 1.85\text{ GHz}$ $f_{RX} = 1.75\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 8-8-2-1, FB: 4-4-2-1, RX: 4-8-4-1		1626.2	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			976.4		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			74.6		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			902.7		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1111.9		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			48.0		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			3578.9		mA
$P_{diss}$	Power Dissipation			10515.0		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11a: TDD 4T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{DAC} = 11796.48\text{ MSPS}$ , interleave mode, $f_{ADC} = 2949.12\text{ MSPS}$ $f_{TX} = f_{RX} = 3.7\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1			797	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			817		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			73.2		mA
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			179		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			906		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			70.5		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			2483		mA
$P_{diss}$	Power Dissipation			6754		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 737.28MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ , interleave mode, $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 3.7\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		726		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			876		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			72.8		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			583		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			270		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			71.6		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		2130		mA	
$P_{\text{diss}}$	Power Dissipation		6124		mW	



## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 737.28MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11c: TDD 4T4R1FB average TX/FB: 75%, RX 25% Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}}$ = 11796.48 MSPS, interleave mode, $f_{\text{ADC}}$ = 2949.12 MSPS $f_{\text{TX}} = f_{\text{RX}} = 3.7\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		779		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			832		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			73.1		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			280		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			747		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			70.8		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			2395		mA
$P_{\text{diss}}$	Power Dissipation			6596		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 11d: FDD 4T4R Single Band: 8x Int, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}}$ = 11796.48 MSPS, interleave mode, $f_{\text{ADC}}$ = 2949.12 MSPS $f_{\text{TX}} = f_{\text{RX}} = 3.7\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		1236	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			915		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			73.2		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			583		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			923		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			72		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			3097		mA
$P_{\text{diss}}$	Power Dissipation			8798		mW

## 6.10 Timing Requirements

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
<b>Timing: SYSREF+/-</b>					
$t_{\text{s}}(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{\text{h}}(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
<b>Timing: Serial ports</b>					
$t_{\text{s}}(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK		15		ns
$t_{\text{h}}(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK <sup>(1)</sup>		$5 + t_{\text{sCLK}}$		ns
$t_{\text{s}}(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{\text{h}}(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{\text{s}}(\text{SCLK\_W})$	Minimum SCLK period: registers write		25		ns
$t_{\text{s}}(\text{SCLK\_R})$	Minimum SCLK period: registers read		50		ns
$t_{\text{d}}(\text{data\_out})$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
$t_{\text{RESET}}$	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\ need to be held one more extra clock cycle with the last SCLK edge

## 6.11 Switching Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

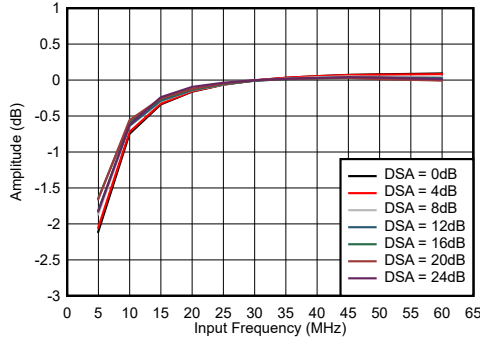
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TX Channel Latency</b>						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
$t_{\text{JESD TX}}$	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles <sup>(1)</sup>
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
<b>RX Channel Latency</b>						
	SerDes Transmitter Analog Delay			3.6		ns
$t_{\text{JESD RX}}$	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles <sup>(1)</sup>
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)		118		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
<b>FB Channel Latency</b>						
	SerDes Transmitter Analog Delay			3.6		ns
$t_{\text{JESD FB}}$	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles <sup>(1)</sup>
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface clock rate, e.g. 1GSPS = 1ns.

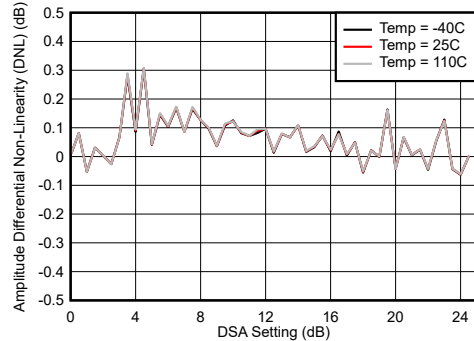
## 6.12 Typical Characteristics

### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz

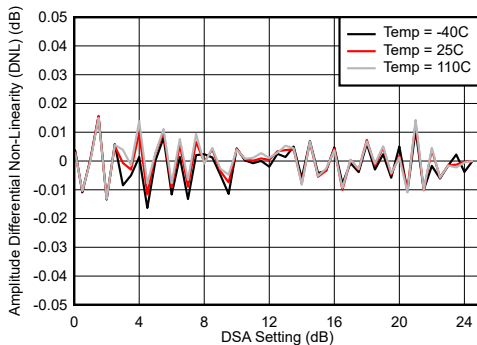
Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{REF} = 500\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{REF} = 500\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB.



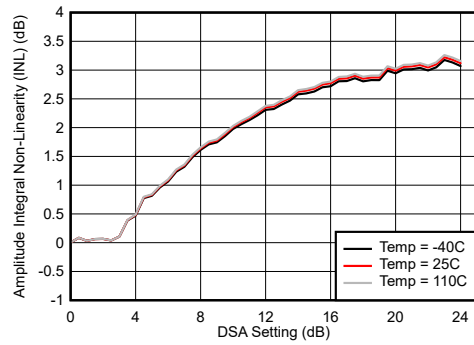
Normalized to 30 MHz  
**Figure 6-1. RX In-Band Gain Flatness,  $f_{IN} = 30\text{ MHz}$**



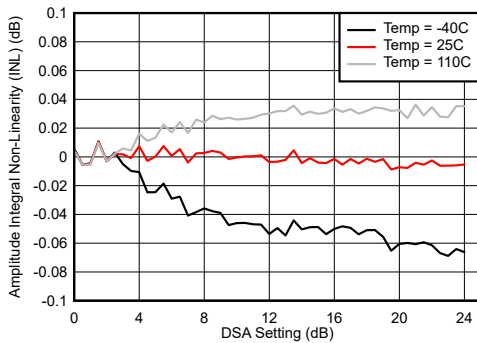
Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$   
**Figure 6-2. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz**



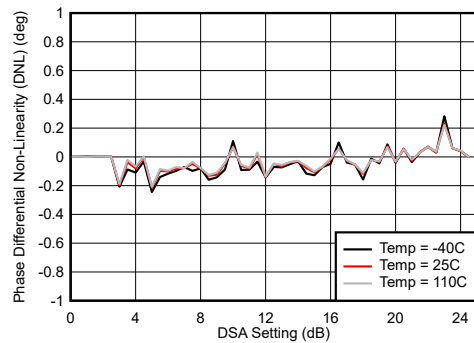
Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$   
**Figure 6-3. RX Calibrated Differential Amplitude Error vs DSA Setting at 30 MHz**



Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$   
**Figure 6-4. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 30 MHz**



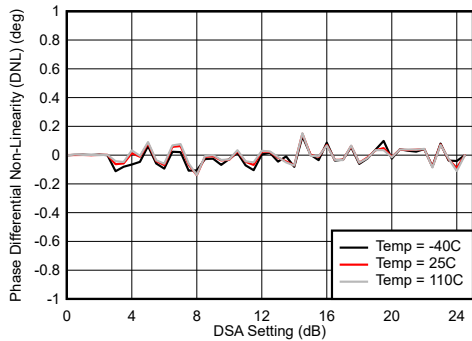
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$   
**Figure 6-5. RX Calibrated Integrated Amplitude Error vs DSA Setting at 30 MHz**



Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$   
**Figure 6-6. RX Uncalibrated Differential Phase Error vs DSA Setting at 30 MHz**

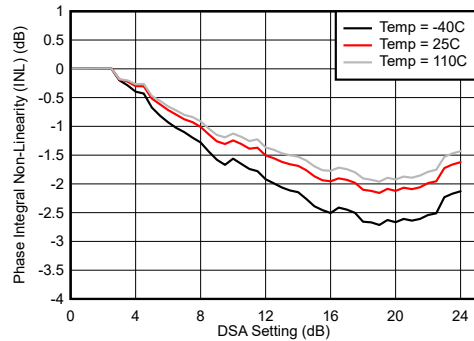
### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{REF} = 500\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{REF} = 500\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB.



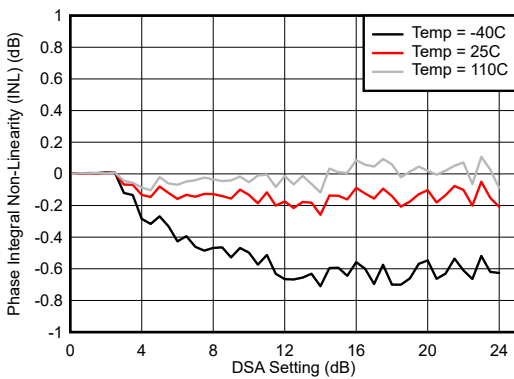
$$\text{Differential Phase Error} = \text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$$

**Figure 6-7. RX Calibrated Differential Phase Error vs DSA Setting at 30 MHz**



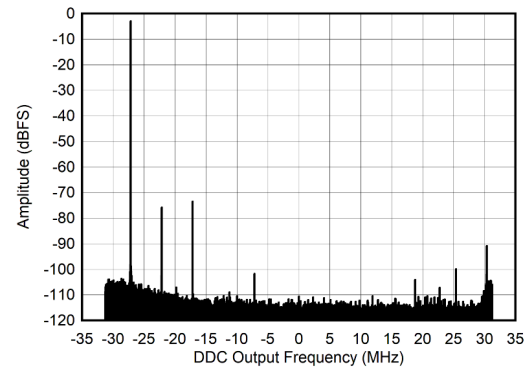
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 6-8. RX Uncalibrated Integrated Phase Error vs DSA Setting at 30 MHz**



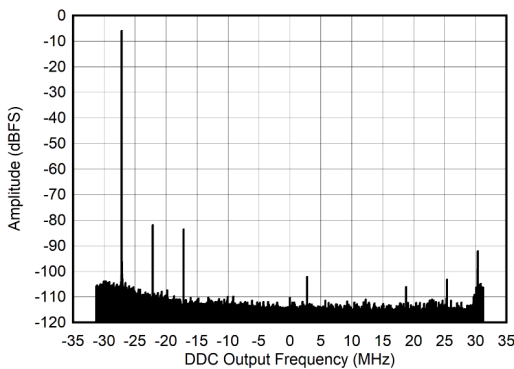
With 0.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-9. RX Calibrated Integrated Phase Error vs DSA Setting at 30 MHz**



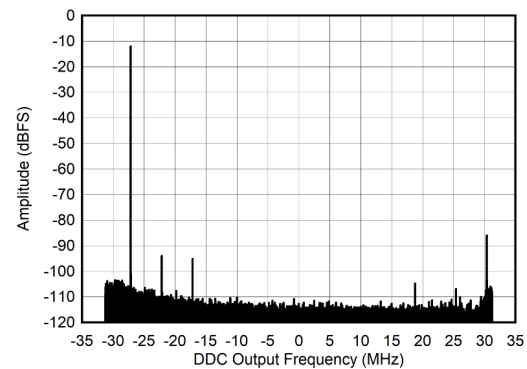
$A_{IN} = -3\text{ dBFS}$ ,  $f_{ADC} = 1500\text{ MSPS}$ ,  $f_{NCO} = 32.13\text{ MHz}$ ,  
Decimate by 24x

**Figure 6-10. RX Output FFT at 5 MHz**



$A_{IN} = -6\text{ dBFS}$ ,  $f_{ADC} = 1500\text{ MSPS}$ ,  $f_{NCO} = 32.$ , Decimate by 24x

**Figure 6-11. RX Output FFT at 5 MHz**

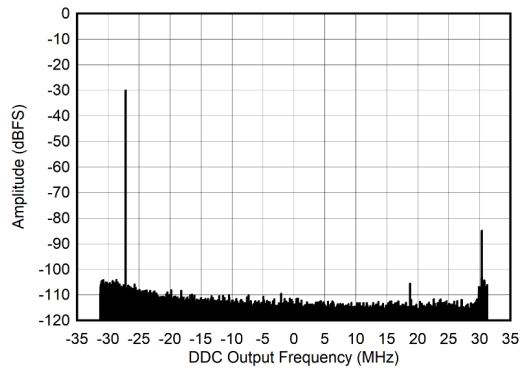


$A_{IN} = -12\text{ dBFS}$ ,  $f_{ADC} = 1500\text{ MSPS}$ ,  $f_{NCO} = 32.13\text{ MHz}$ ,  
Decimate by 24x

**Figure 6-12. RX Output FFT at 5 MHz**

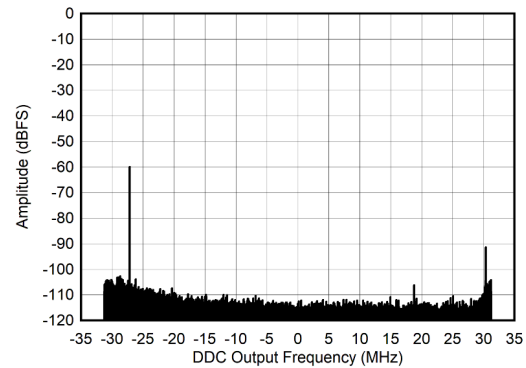
### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 3 dB.



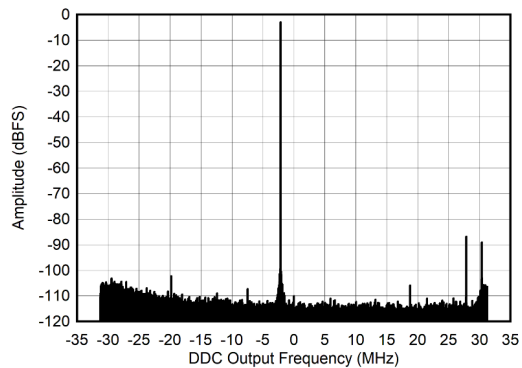
$A_{\text{IN}} = -30$  dBFS,  $f_{\text{ADC}} = 1500$  MSPS,  $f_{\text{NCO}} = 32.13$  MHz,  
Decimate by 24x

**Figure 6-13. RX Output FFT at 5 MHz**



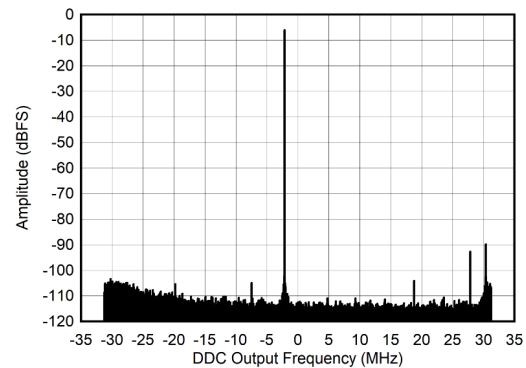
$A_{\text{IN}} = -60$  dBFS,  $f_{\text{ADC}} = 1500$  MSPS,  $f_{\text{NCO}} = 32.13$  MHz,  
Decimate by 24x

**Figure 6-14. RX Output FFT at 5 MHz**



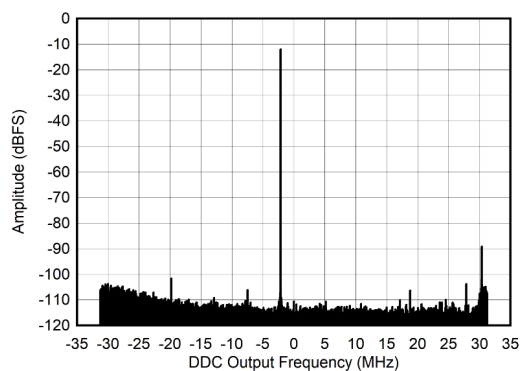
$A_{\text{IN}} = -3$  dBFS,  $f_{\text{ADC}} = 1500$  MSPS,  $f_{\text{NCO}} = 32.13$  MHz,  
Decimate by 24x

**Figure 6-15. RX Output FFT at 30 MHz**



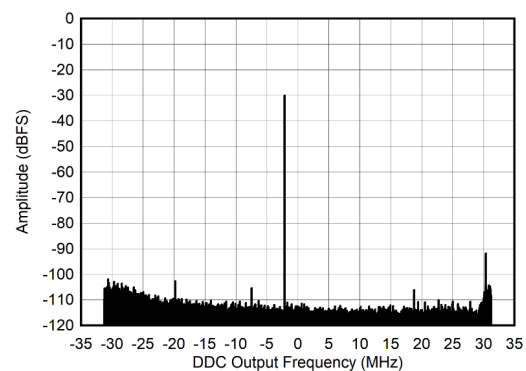
$A_{\text{IN}} = -6$  dBFS,  $f_{\text{ADC}} = 1500$  MSPS,  $f_{\text{NCO}} = 32.13$  MHz,  
Decimate by 24x

**Figure 6-16. RX Output FFT at 30 MHz**



$A_{\text{IN}} = -12$  dBFS,  $f_{\text{ADC}} = 1500$  MSPS,  $f_{\text{NCO}} = 32.13$  MHz,  
Decimate by 24x

**Figure 6-17. RX Output FFT at 30 MHz**

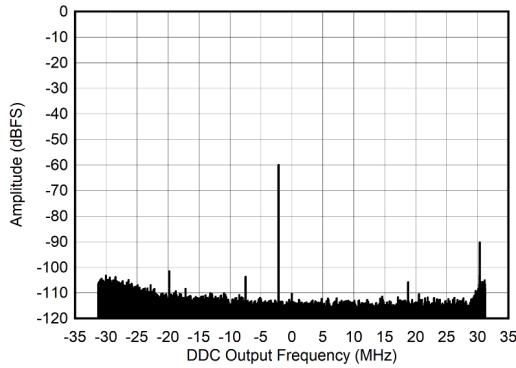


$A_{\text{IN}} = -30$  dBFS,  $f_{\text{ADC}} = 1500$  MSPS,  $f_{\text{NCO}} = 32.13$  MHz,  
Decimate by 24x

**Figure 6-18. RX Output FFT at 30 MHz**

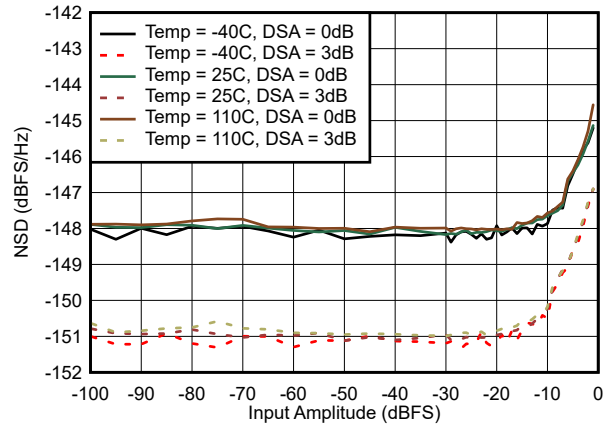
### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{REF} = 500$  MHz,  $A_{IN} = -3$  dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{REF} = 500$  MHz,  $A_{IN} = -3$  dBFS, DSA setting = 3 dB.



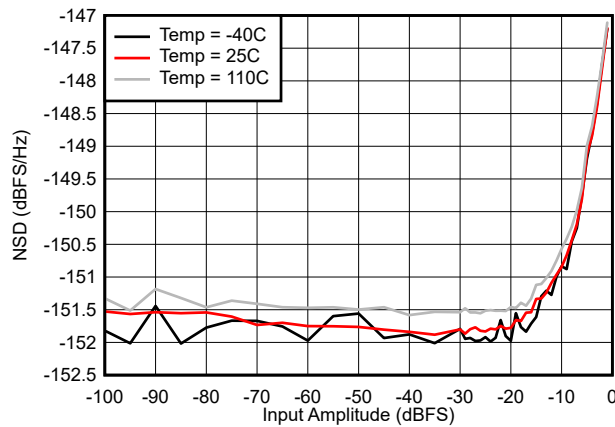
$A_{IN} = -60$  dBFS,  $f_{ADC} = 1500$  MSPS,  $f_{NCO} = 32.13$  MHz, Decimate by 24x

Figure 6-19. RX Output FFT at 30 MHz



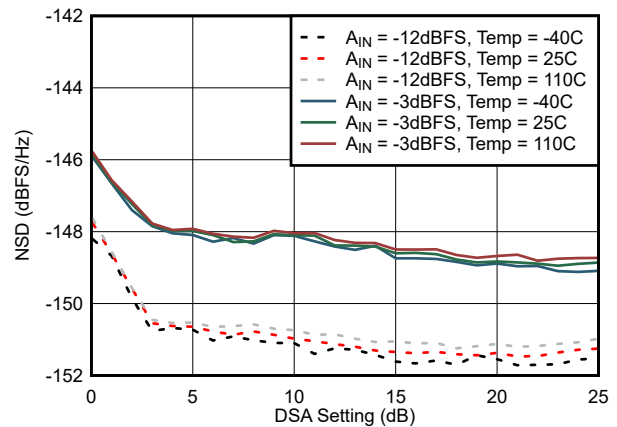
$f_{ADC} = 1500$  MSPS,  $f_{NCO} = 32.13$  MHz, Decimate by 24x

Figure 6-20. NSD vs Input Amplitude at 30 MHz with DSA = 0 and 3dB



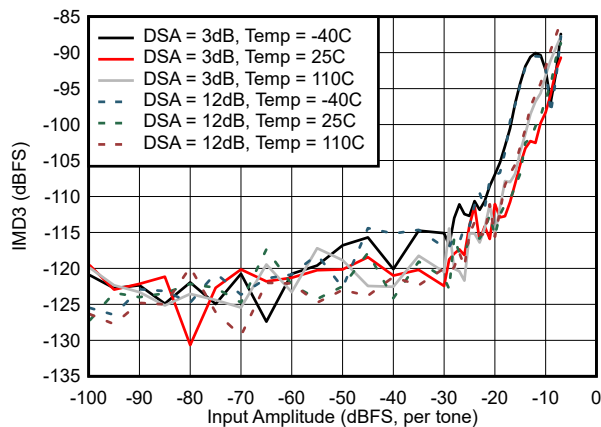
$f_{ADC} = 1500$  MSPS,  $f_{NCO} = 32.13$  MHz, Decimate by 24x

Figure 6-21. NSD vs Input Amplitude at 30 MHz with DSA = 12



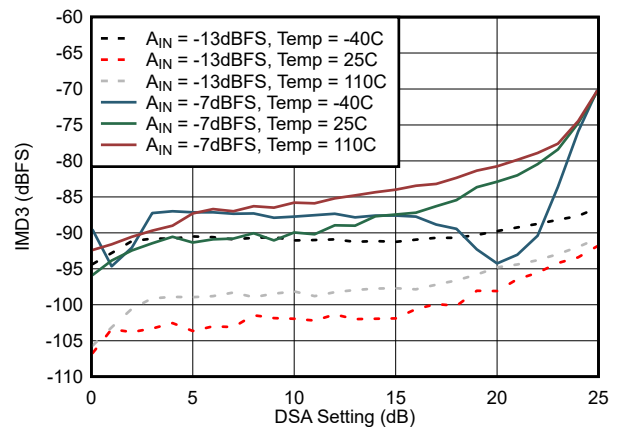
$f_{ADC} = 1500$  MSPS,  $f_{NCO} = 32.13$  MHz, Decimate by 24x

Figure 6-22. NSD vs DSA Attenuation at 30 MHz



$f_{ADC} = 1500$  MSPS,  $f_{NCO} = 32.13$  MHz, Decimate by 24x

Figure 6-23. IMD3 vs Input Amplitude at 30 MHz

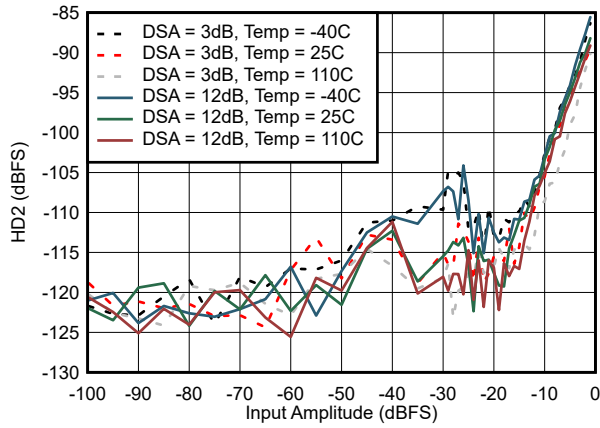


$f_{ADC} = 1500$  MSPS,  $f_{NCO} = 32.13$  MHz, Decimate by 24x

Figure 6-24. IMD3 vs DSA Setting at 30 MHz

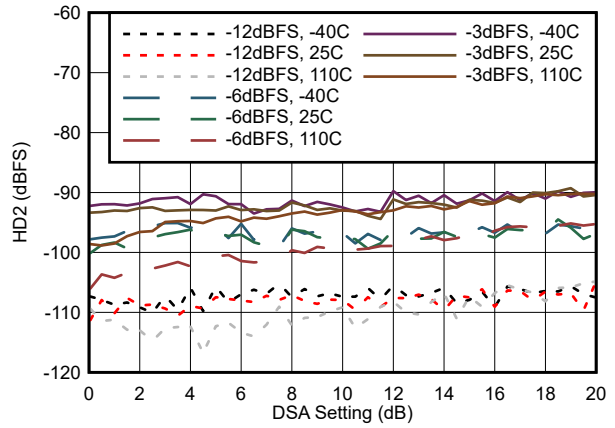
### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{REF} = 500\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{REF} = 500\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB.



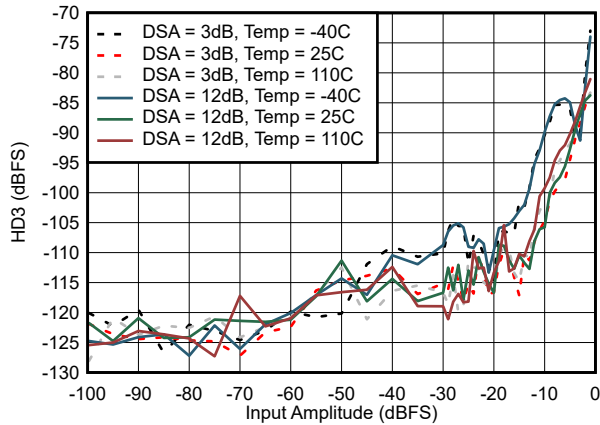
$f_{ADC} = 1500\text{ MSPS}$ ,  $f_{NCO} = 32.13\text{ MHz}$ , Decimate by 24x

Figure 6-25. HD2 vs Input Amplitude at 30 MHz



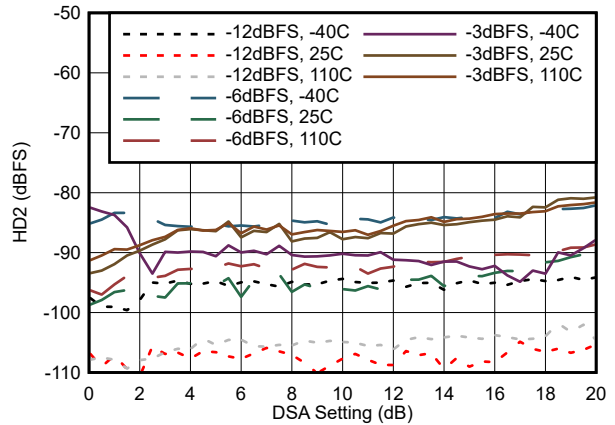
$f_{ADC} = 1500\text{ MSPS}$ ,  $f_{NCO} = 32.$ , Decimate by 24x

Figure 6-26. HD2 vs DSA Setting at 30 MHz



$f_{ADC} = 1500\text{ MSPS}$ ,  $f_{NCO} = 32.13\text{ MHz}$ , Decimate by 24x

Figure 6-27. HD3 vs Input Amplitude at 30 MHz



$f_{ADC} = 1500\text{ MSPS}$ ,  $f_{NCO} = 32.13\text{ MHz}$ , Decimate by 24x

Figure 6-28. HD3 vs DSA Setting at 30 MHz



### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 3 dB.

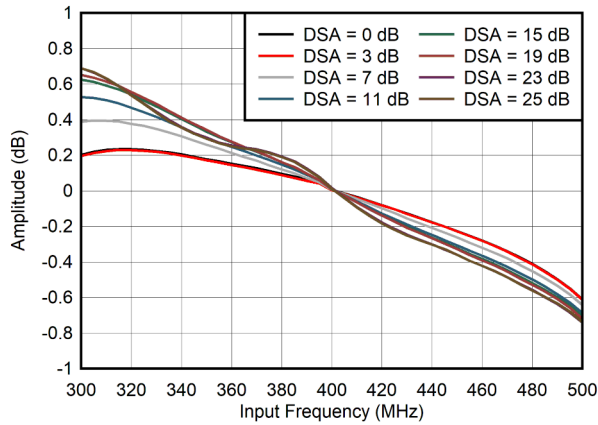
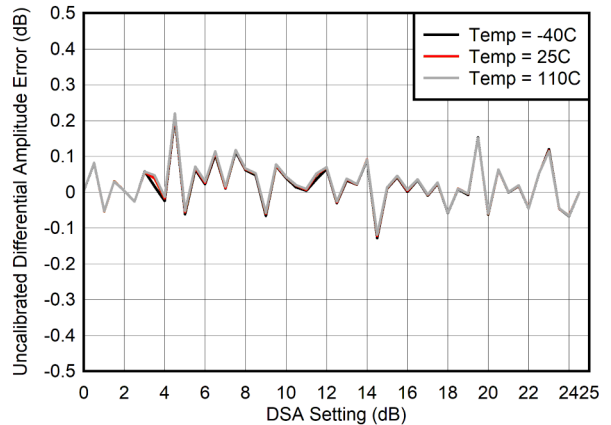
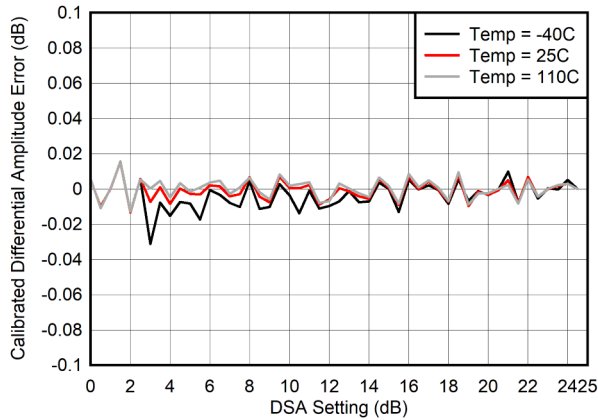


Figure 6-29. RX In-Band Gain Flatness,  $f_{\text{IN}} = 400$  MHz



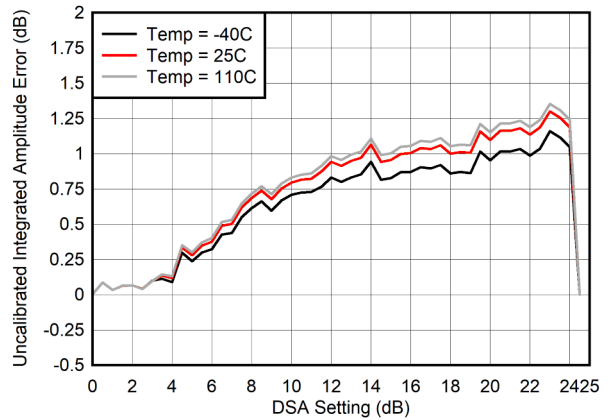
$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting} + 1)$$

Figure 6-30. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting} + 1)$$

Figure 6-31. RX Calibrated Differential Amplitude Error vs DSA Setting at 400 MHz



$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

Figure 6-32. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 400 MHz

### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{REF} = 500\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{REF} = 500\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 3 dB.

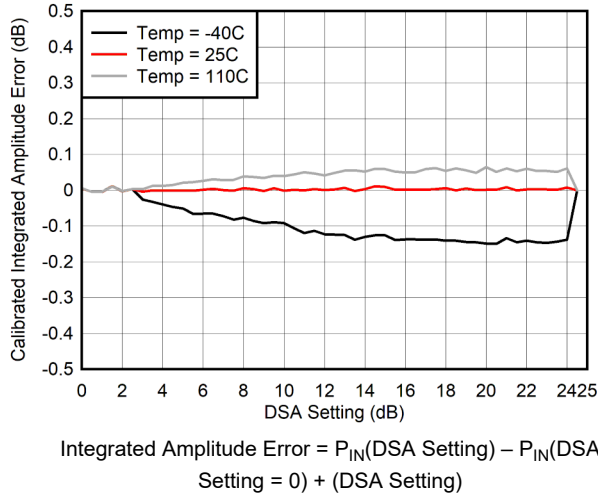


Figure 6-33. RX Calibrated Integrated Amplitude Error vs DSA Setting at 400 MHz

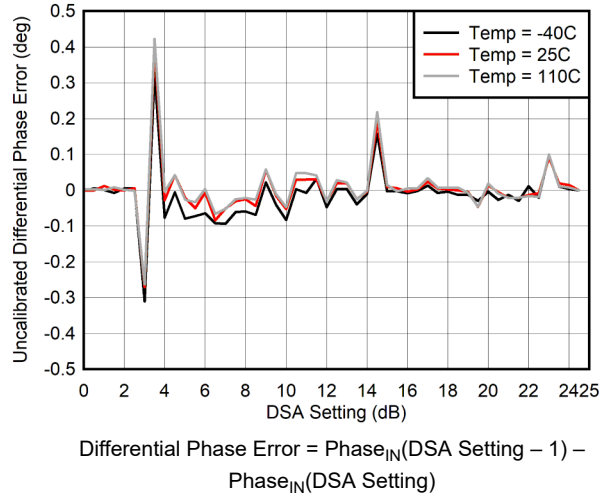


Figure 6-34. RX Uncalibrated Differential Phase Error vs DSA Setting at 400 MHz

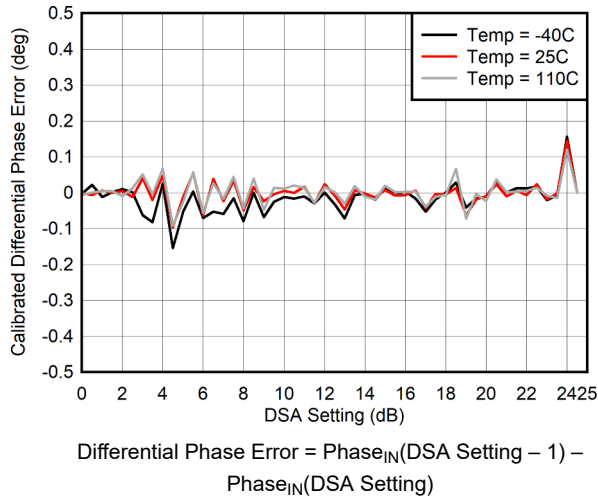


Figure 6-35. RX Calibrated Differential Phase Error vs DSA Setting at 400 MHz

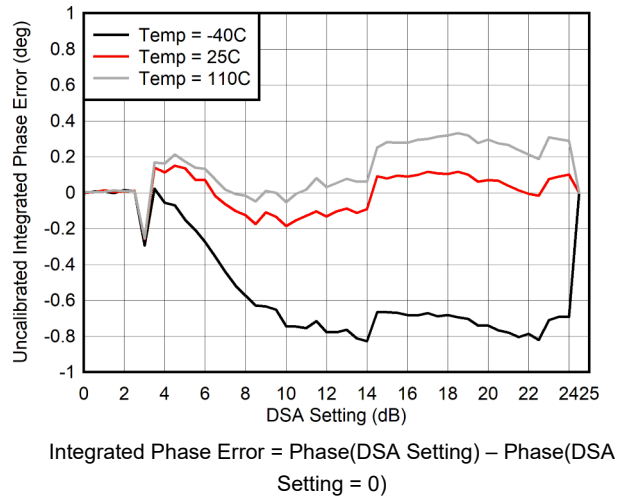
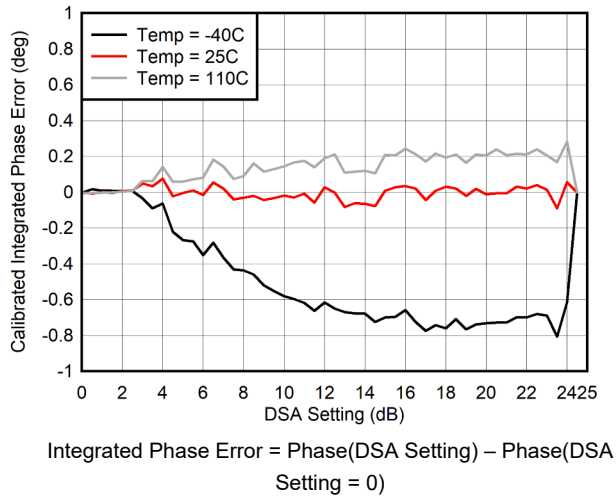


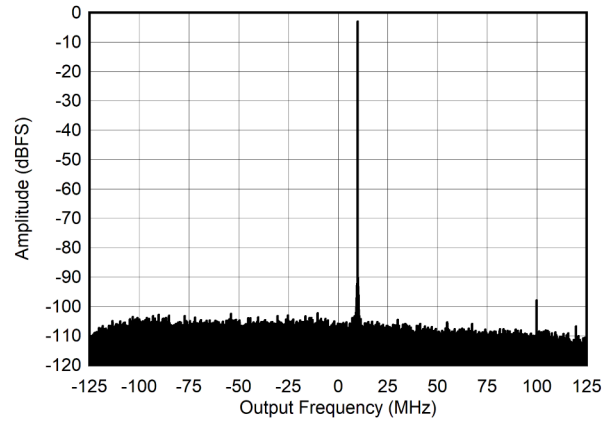
Figure 6-36. RX Uncalibrated Integrated Phase Error vs DSA Setting at 400 MHz

### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 3 dB.

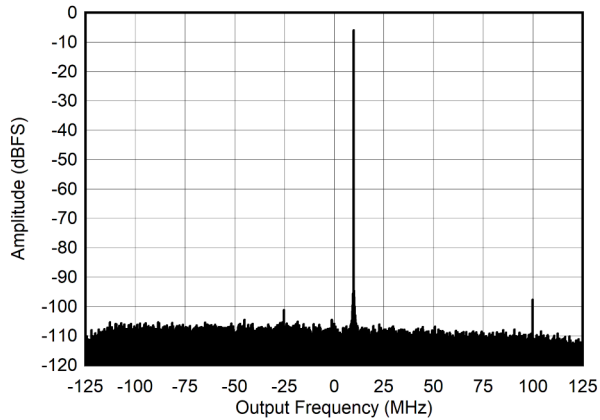


**Figure 6-37. RX Calibrated Integrated Phase Error vs DSA Setting at 400 MHz**



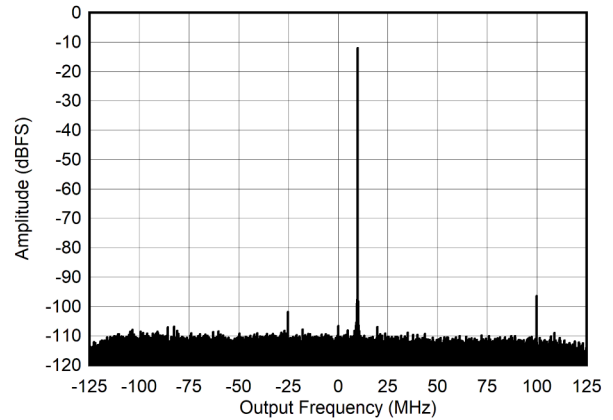
$f_{\text{NCO}} = 400\text{MHz}$

**Figure 6-38. RX Output FFT at 405 MHz and -3dBFS**



$f_{\text{NCO}} = 400\text{MHz}$

**Figure 6-39. RX Output FFT at 405 MHz and -6dBFS**

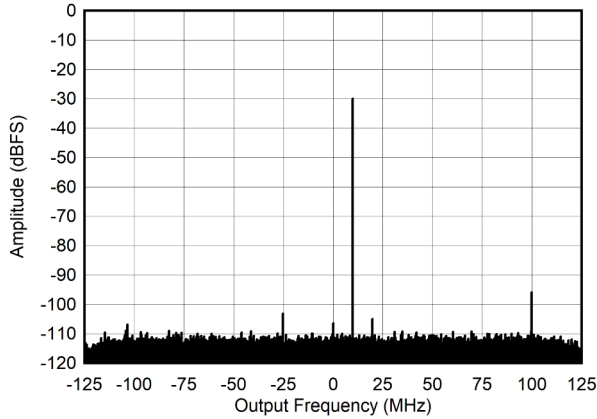


$f_{\text{NCO}} = 400\text{MHz}$

**Figure 6-40. RX Output FFT at 405 MHz and -12dBFS**

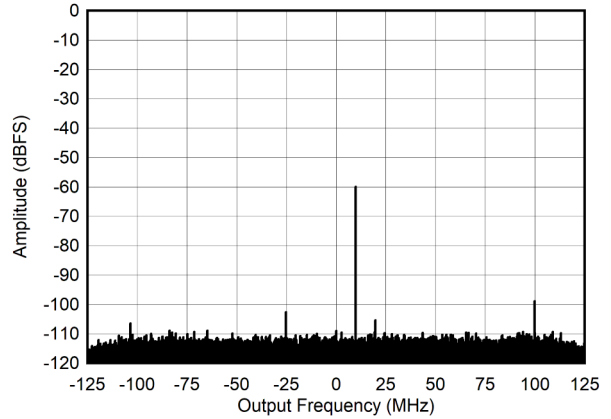
**6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB.



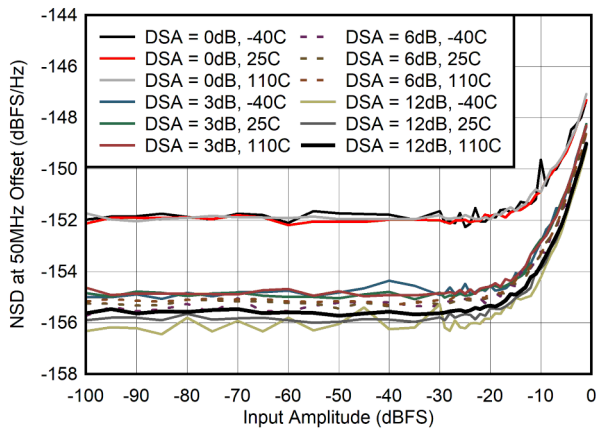
$f_{\text{NCO}} = 400\text{MHz}$

**Figure 6-41. RX Output FFT at 405 MHz and -30dBFS**



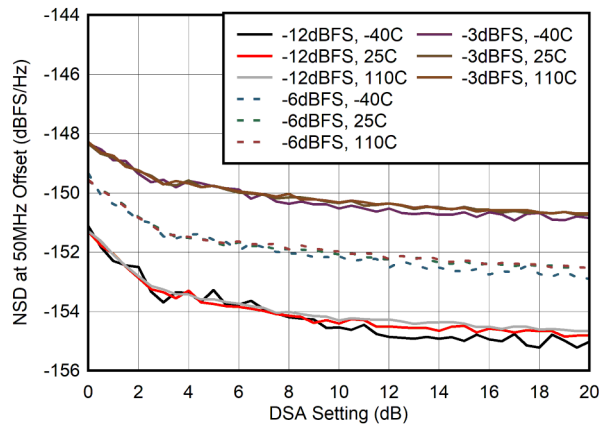
$f_{\text{NCO}} = 400\text{MHz}$

**Figure 6-42. RX Output FFT at 405 MHz and -60dBFS**



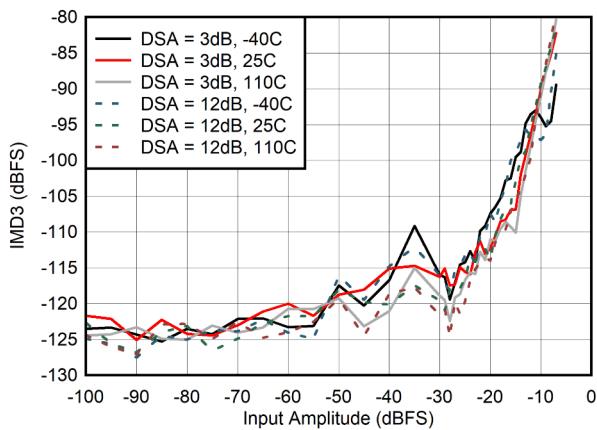
$f_{\text{OFFSET}} = 50\text{MHz}$

**Figure 6-43. NSD vs Input Amplitude at 400MHz**

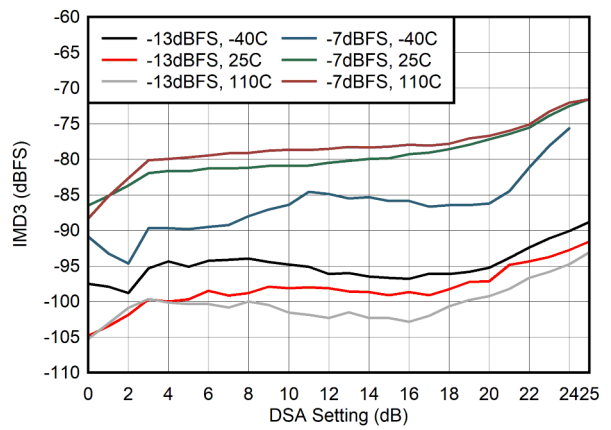


$f_{\text{OFFSET}} = 50\text{MHz}$

**Figure 6-44. NSD vs DSA Setting at 400MHz**



**Figure 6-45. IMD3 vs Input Amplitude at 400MHz**



**Figure 6-46. IMD3 vs DSA Setting at 400MHz**

### 6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{REF} = 500$  MHz,  $A_{IN} = -3$  dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{REF} = 500$  MHz,  $A_{IN} = -3$  dBFS, DSA setting = 3 dB.

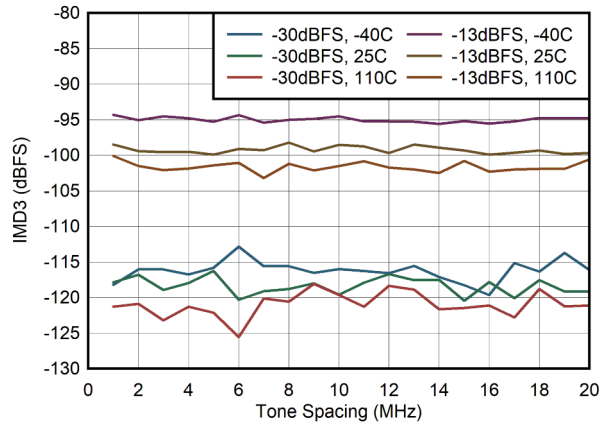


Figure 6-47. IMD3 vs Tone Spacing at 400MHz

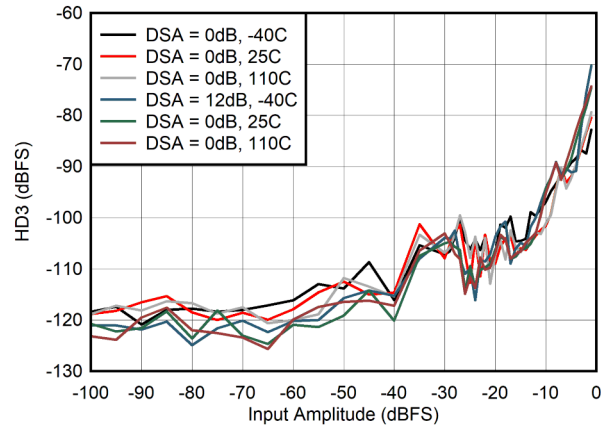


Figure 6-48. HD3 vs Input Amplitude at 400MHz

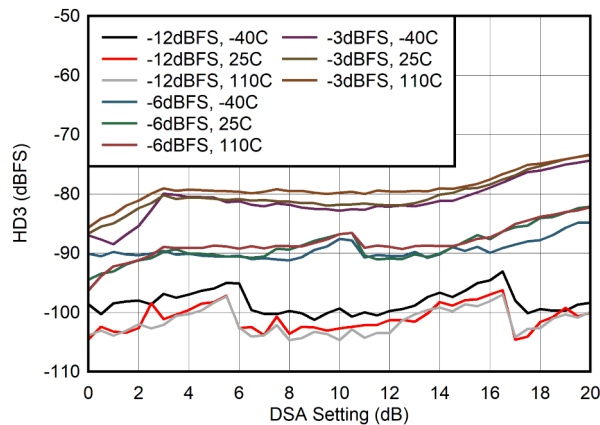
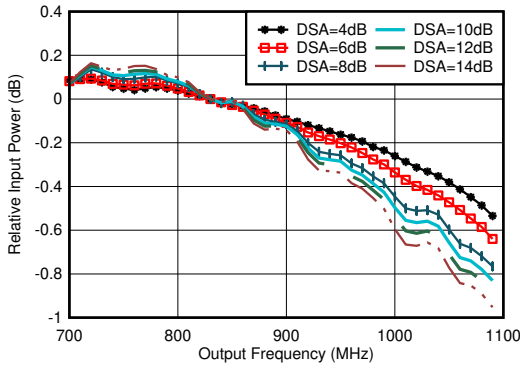


Figure 6-49. HD3 vs DSA Setting at 400MHz

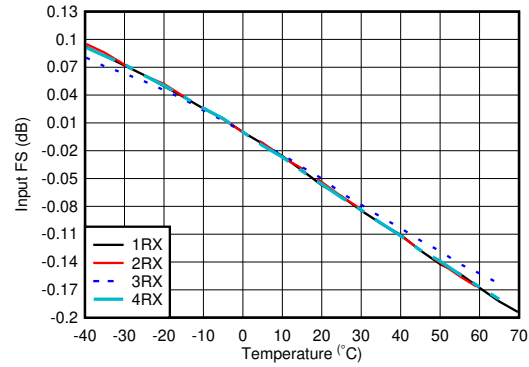
### 6.12.2 RX Typical Characteristics at 800MHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4 dB.



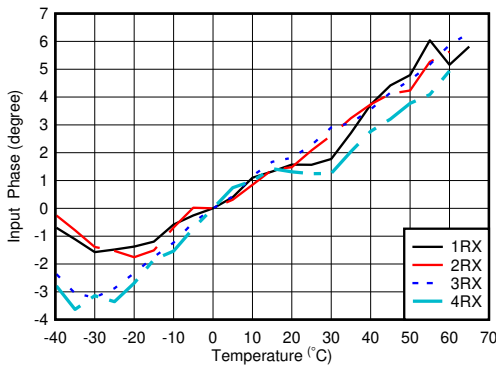
With 0.8 GHz matching, normalized to 830 MHz

**Figure 6-50. RX In-Band Gain Flatness for Channel 1RX,  $f_{IN} = 830\text{ MHz}$**



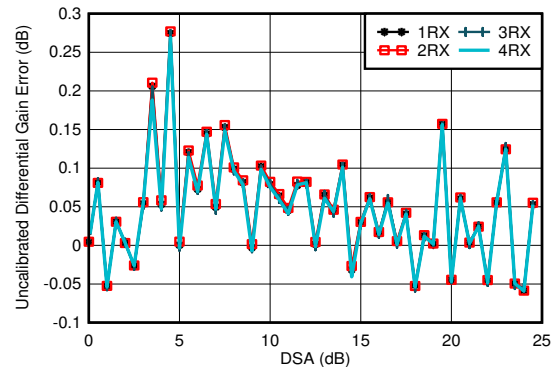
With 0.8 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

**Figure 6-51. RX Input Fullscale vs Temperature and Channel at 800MHz**



With 0.8 GHz matching, normalized to phase at  $25^\circ\text{C}$

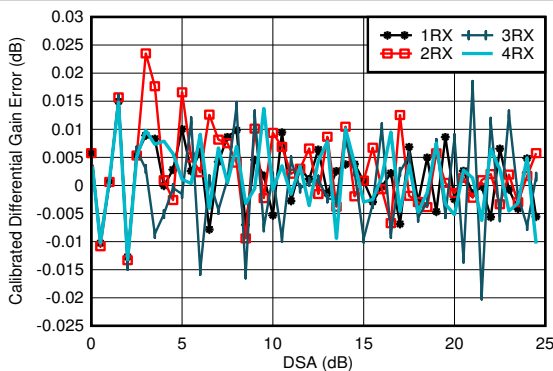
**Figure 6-52. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 0.8\text{ GHz}$**



With 0.8 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

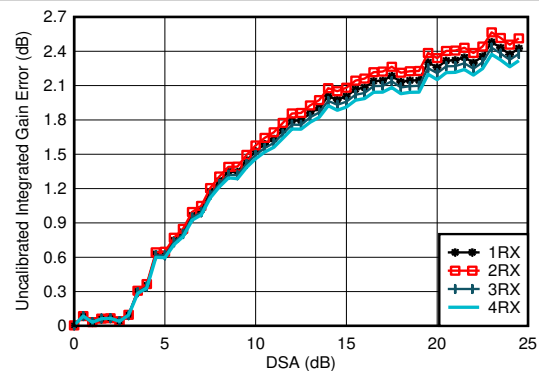
**Figure 6-53. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz**



With 0.8 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

**Figure 6-54. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz**



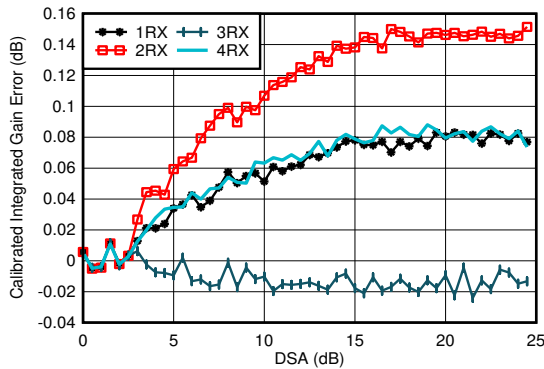
With 0.8 GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-55. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz**

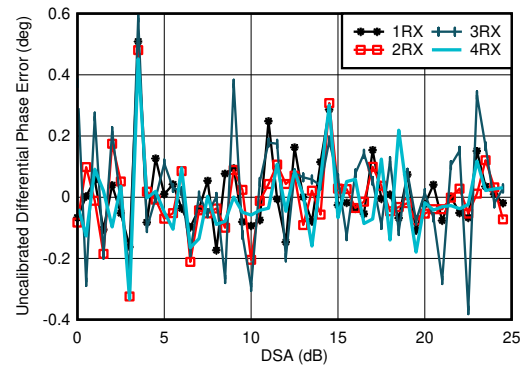
### 6.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



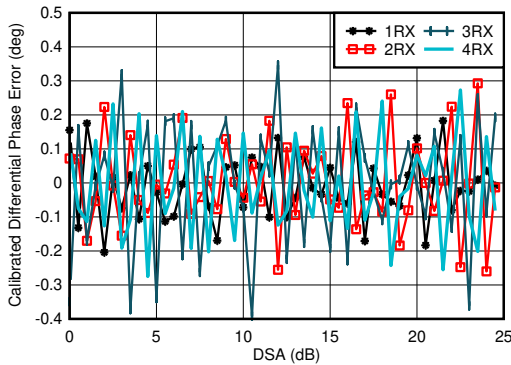
With 0.8 GHz matching  
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-56. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz**



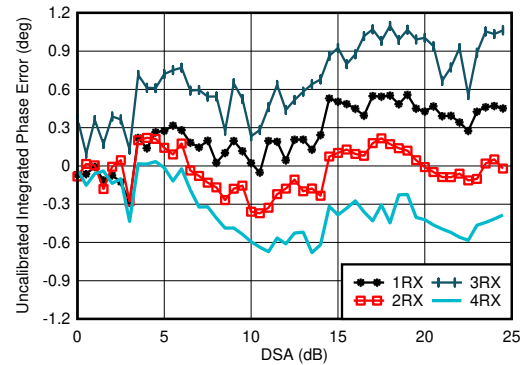
With 0.8 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-57. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz**



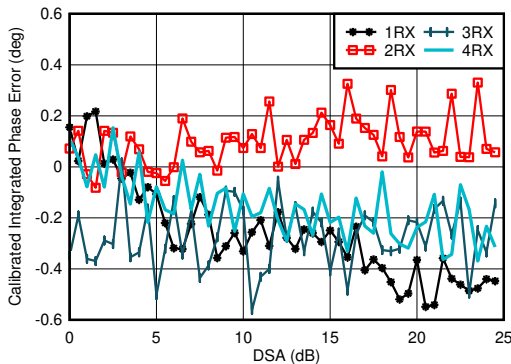
With 0.8 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-58. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz**



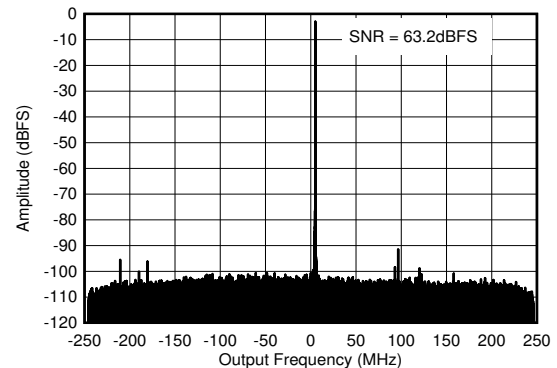
With 0.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-59. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz**



With 0.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-60. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz**



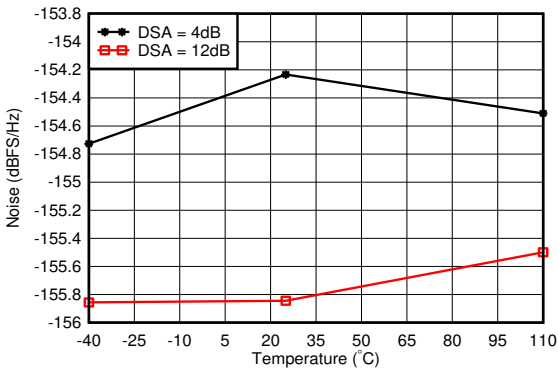
With 0.8 GHz matching,  $f_{IN} = 840\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

**Figure 6-61. RX Output FFT at 0.8 GHz**



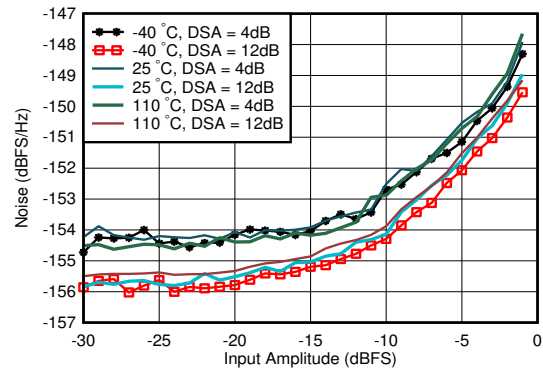
### 6.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



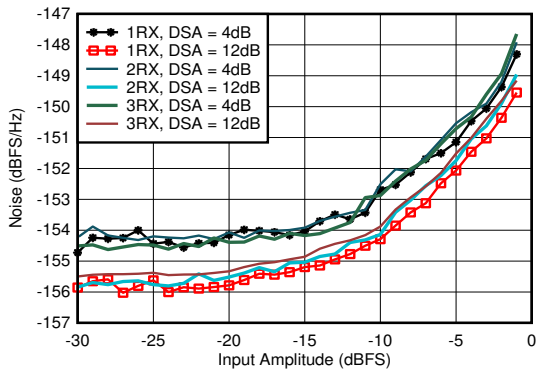
With 0.8 GHz matching, 12.5-MHz offset from tone

**Figure 6-62. RX Noise Spectral Density vs Temperature at 0.8 GHz**



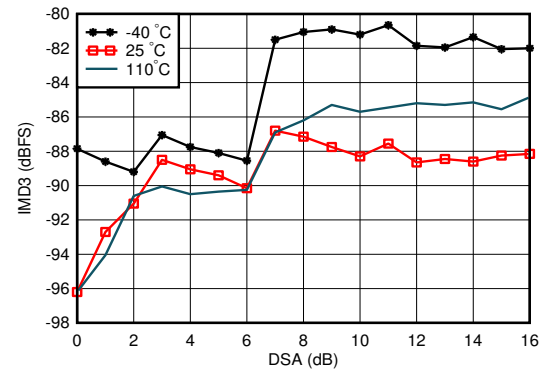
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 6-63. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz**



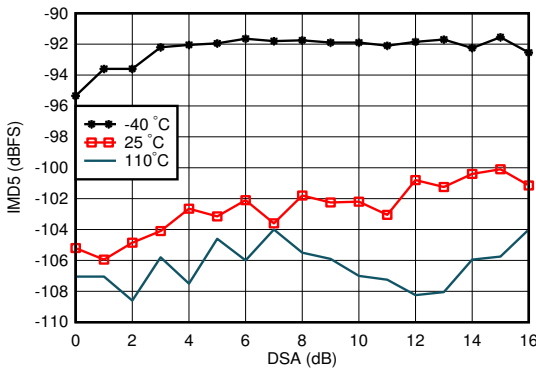
With 0.8 GHz matching, 12.5-MHz offset from tone

**Figure 6-64. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz**



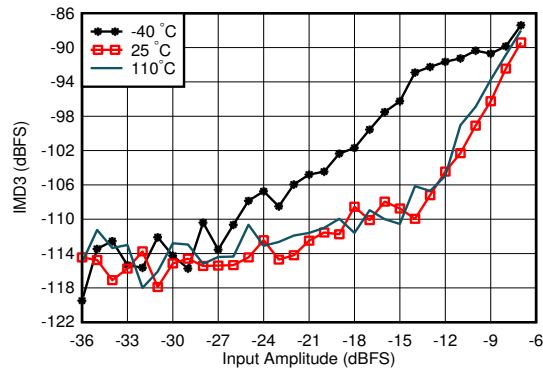
A. With 0.8 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-65. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz**



With 0.8 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-66. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz**



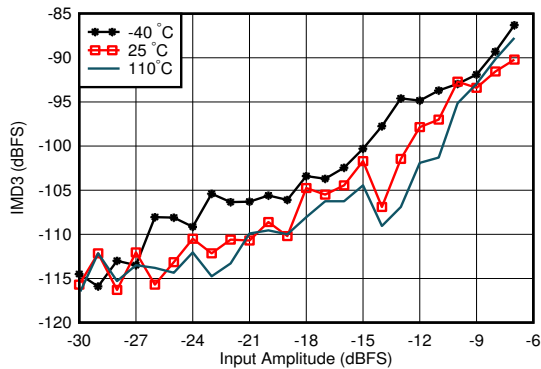
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 6-67. RX IMD3 vs Input Level and Temperature at 0.8 GHz**



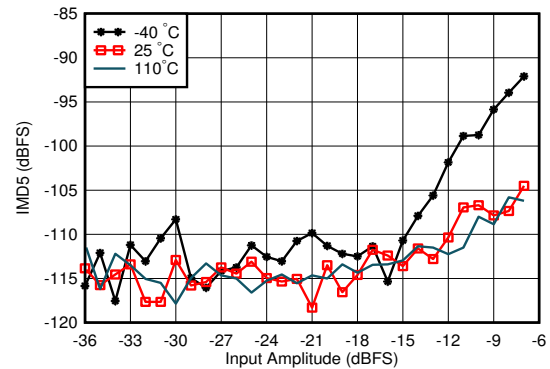
### 6.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4 dB.



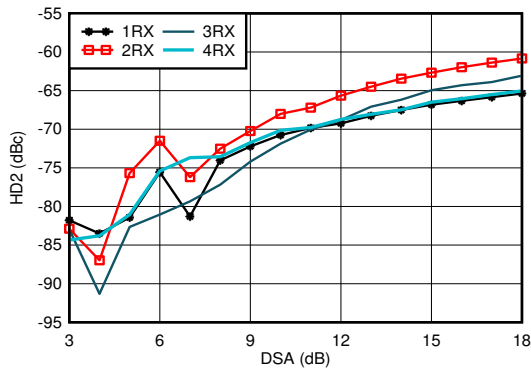
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-68. RX IMD3 vs Input Level and Temperature at 0.8 GHz**



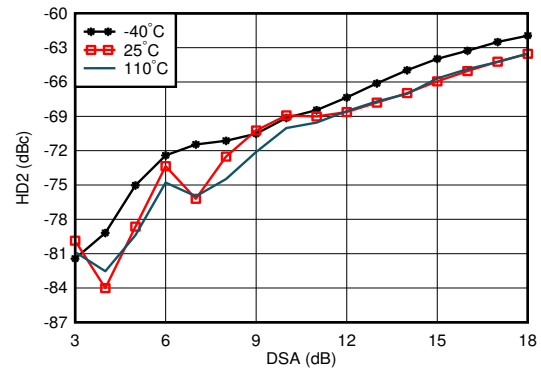
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-69. RX IMD5 vs Input Level and Temperature at 0.8 GHz**



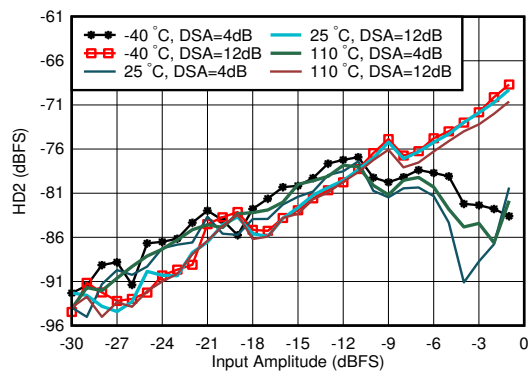
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-70. RX HD2 vs DSA Setting and Channel at 0.8 GHz**



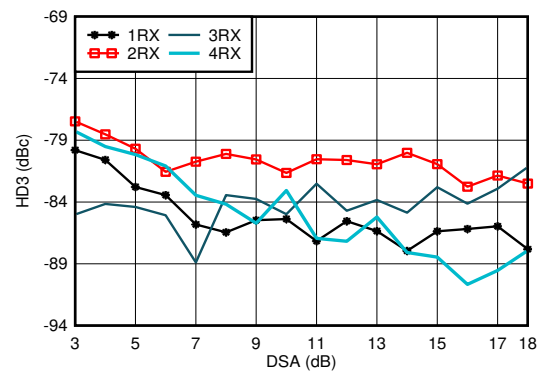
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-71. RX HD2 vs DSA Setting and Temperature at 0.8 GHz**



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-72. RX HD2 vs Input Level and Temperature at 0.8 GHz**

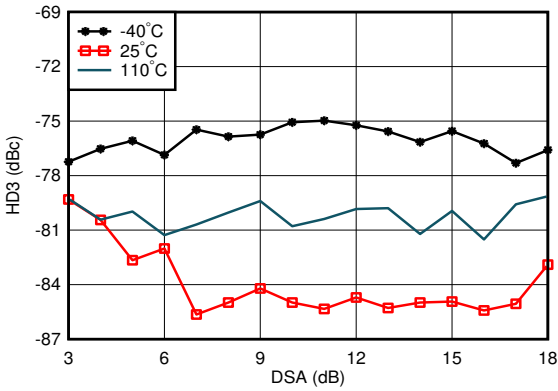


With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-73. RX HD3 vs DSA Setting and Channel at 0.8 GHz**

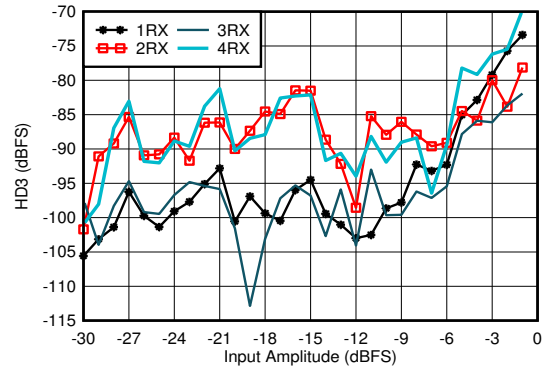
### 6.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



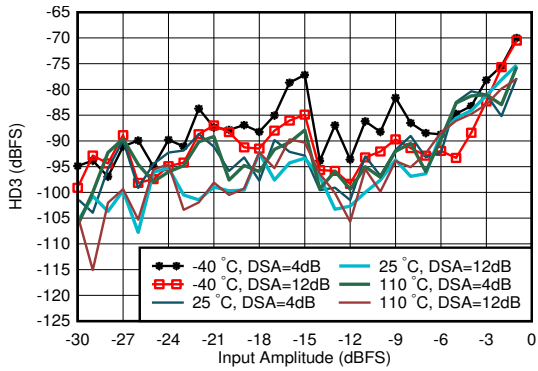
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-74. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



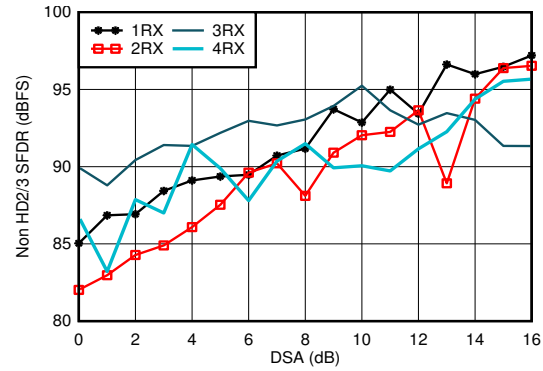
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-75. RX HD3 vs Input Level and Channel at 0.8 GHz



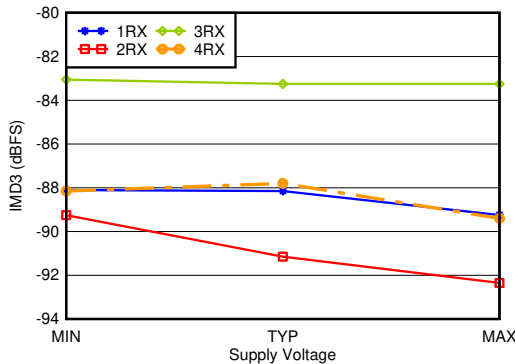
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-76. RX HD3 vs Input Level and Temperature at 0.8 GHz



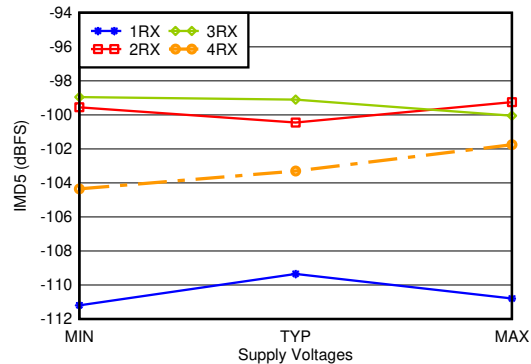
With 0.8 GHz matching

Figure 6-77. RX Non-HD2/3 vs DSA Setting at 0.8 GHz



With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-78. RX IMD3 vs Supply and Channel at 0.8 GHz

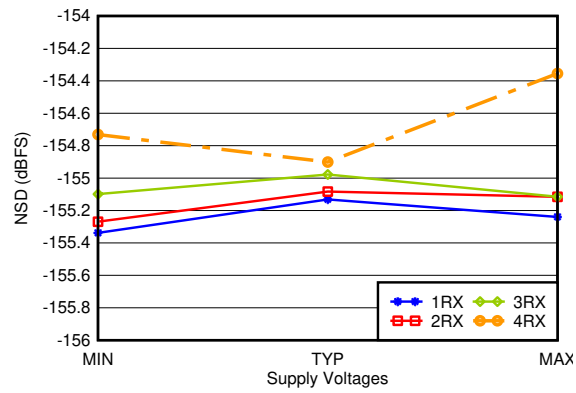


With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-79. RX IMD5 vs Supply and Channel at 0.8 GHz

### 6.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3 \text{ dBFS}$ , DSA setting = 4 dB.

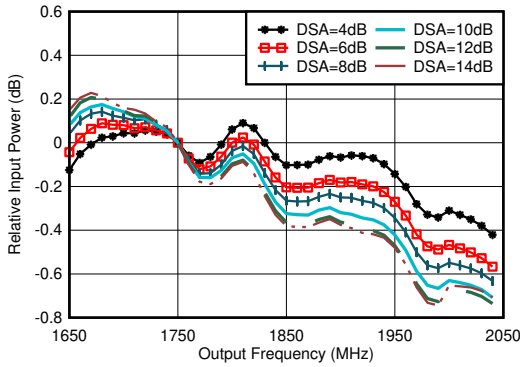


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-80. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz**

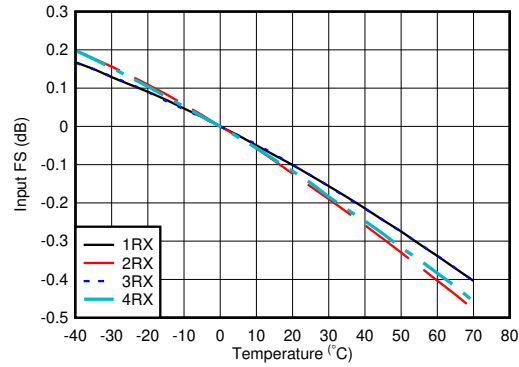
### 6.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



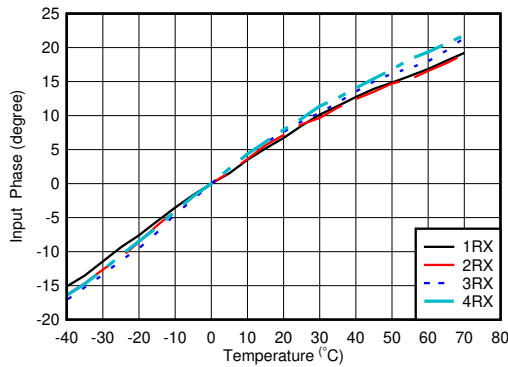
With 1.8 GHz matching, normalized to 1.75 GHz

**Figure 6-81. RX In-Band Gain Flatness,  $f_{IN} = 1750\text{ MHz}$**



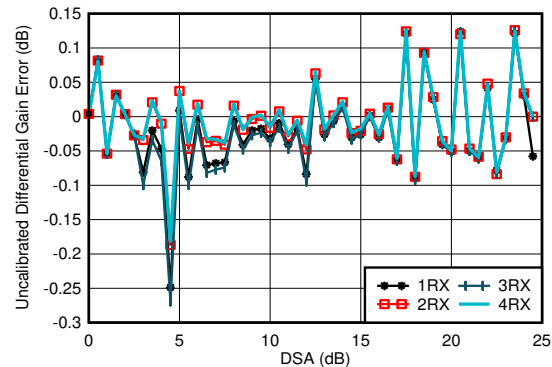
With 1.8 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

**Figure 6-82. RX Input Fullscale vs Temperature and Channel at 1.75 GHz**



With 2.6 GHz matching, normalized to phase at  $25^\circ\text{C}$

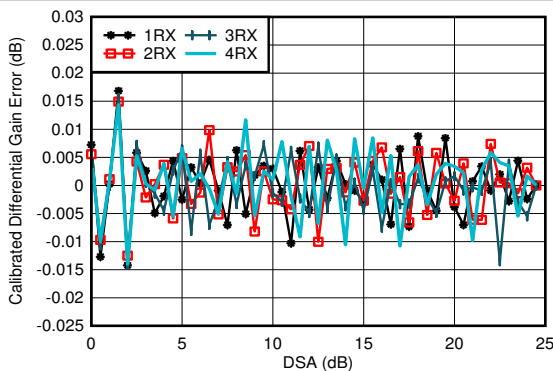
**Figure 6-83. RX Input Phase vs Temperature and DSA at  $f_{IN} = 1.75\text{ GHz}$**



With 1.8 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

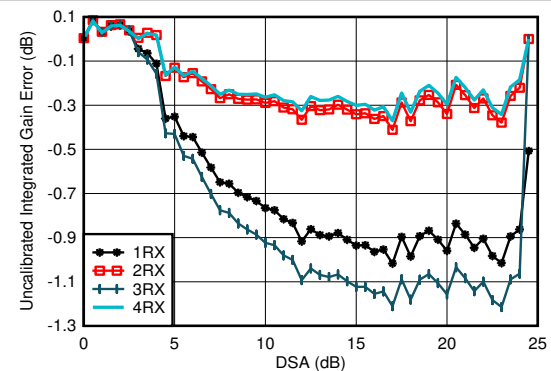
**Figure 6-84. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

**Figure 6-85. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz**



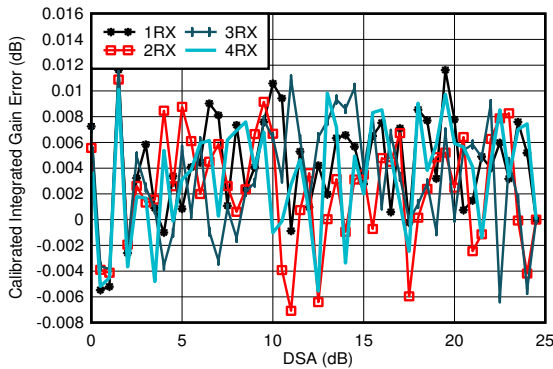
With 1.8 GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-86. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz**

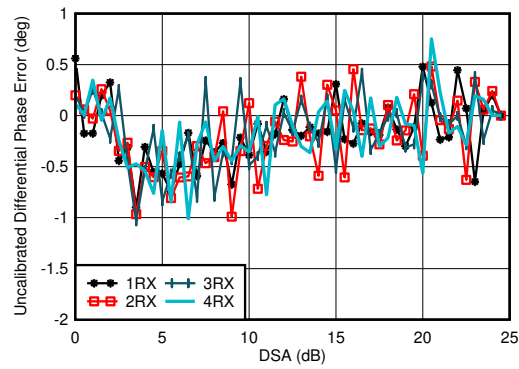
### 6.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



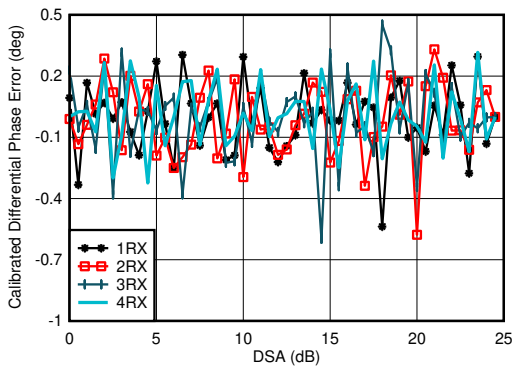
With 1.8 GHz matching  
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 6-87. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



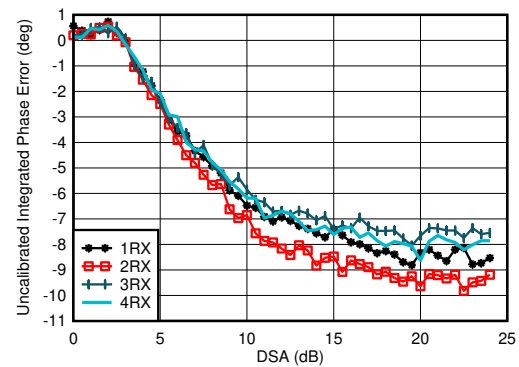
With 1.8 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

Figure 6-88. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



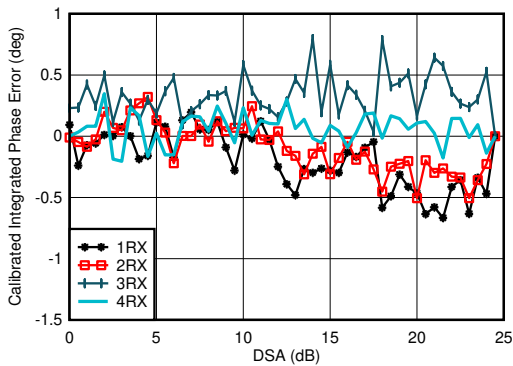
With 1.8 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

Figure 6-89. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



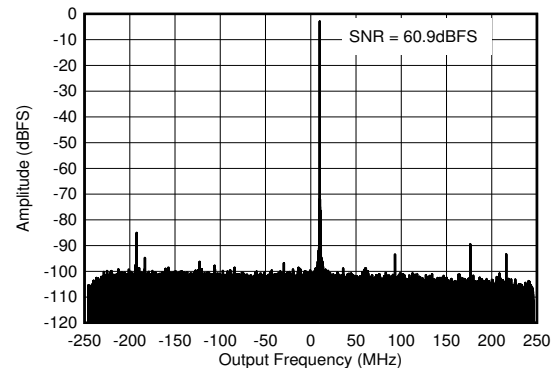
With 1.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 6-90. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 6-91. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

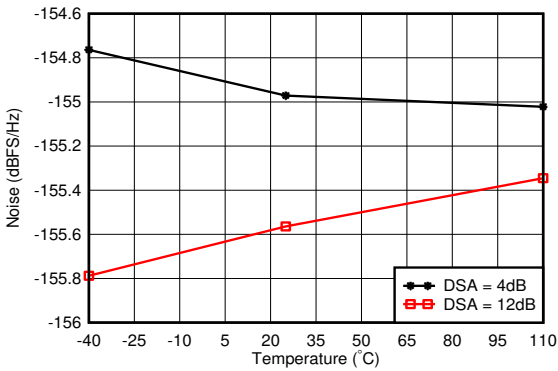


With 1.8 GHz matching,  $f_{IN} = 2610\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

Figure 6-92. RX Output FFT at 1.75 GHz

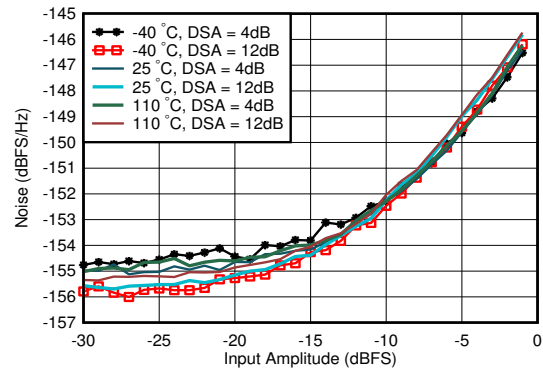
**6.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



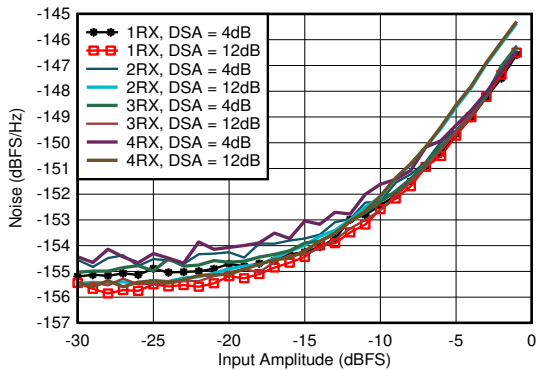
With 1.8 GHz matching, 12.5-MHz offset from tone

**Figure 6-93. RX Noise Spectral Density vs Temperature at 1.75 GHz**



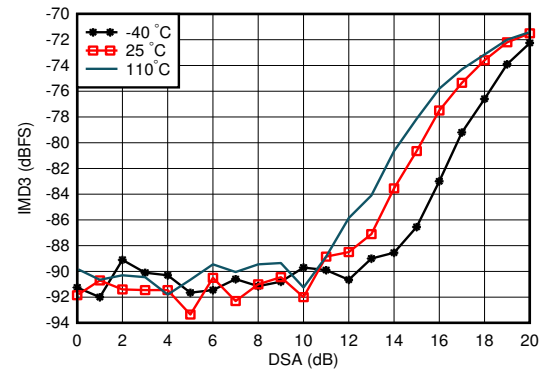
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 6-94. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz**



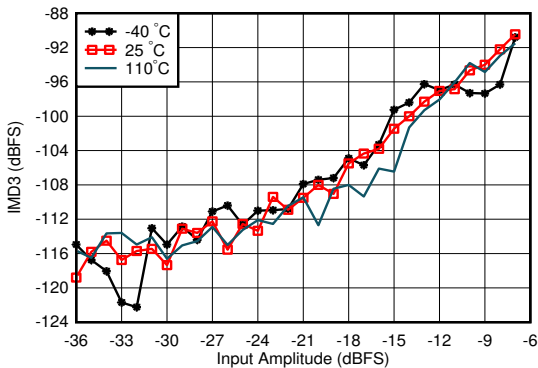
With 1.8 GHz matching, 12.5-MHz offset from tone

**Figure 6-95. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz**



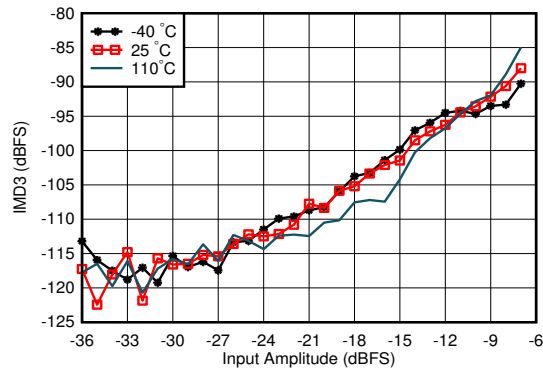
With 1.8 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-96. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz**



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 6-97. RX IMD3 vs Input Level and Temperature at 1.75 GHz**

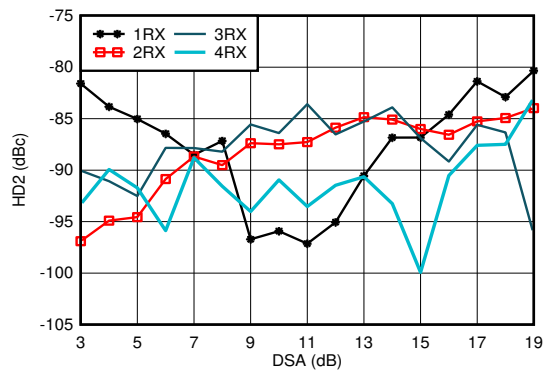


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-98. RX IMD3 vs Input Level and Temperature at 1.75 GHz**

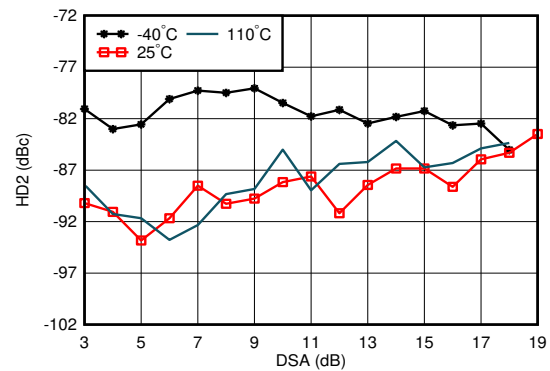
### 6.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



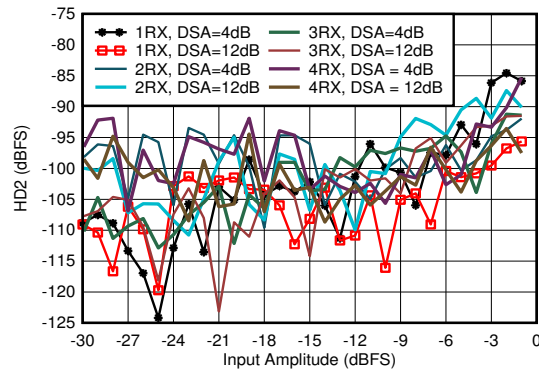
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-99. RX HD2 vs DSA Setting and Channel at 1.9 GHz**



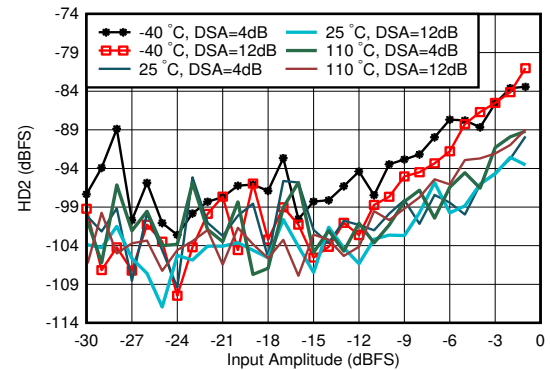
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-100. RX HD2 vs DSA Setting and Temperature at 1.9 GHz**



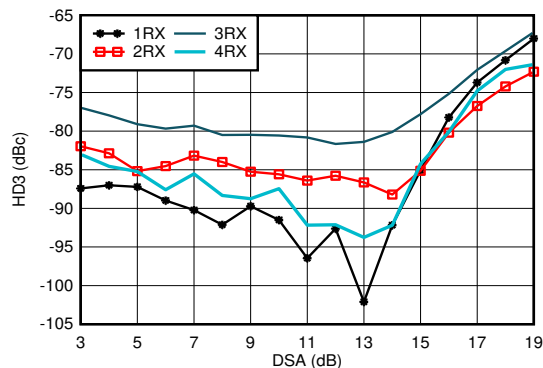
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-101. RX HD2 vs Input Amplitude and Channel at 1.9 GHz**



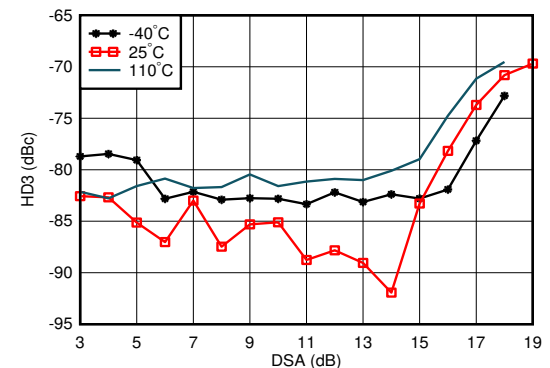
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-102. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz**



With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 6-103. RX HD3 vs DSA Setting and Channel at 1.9 GHz**



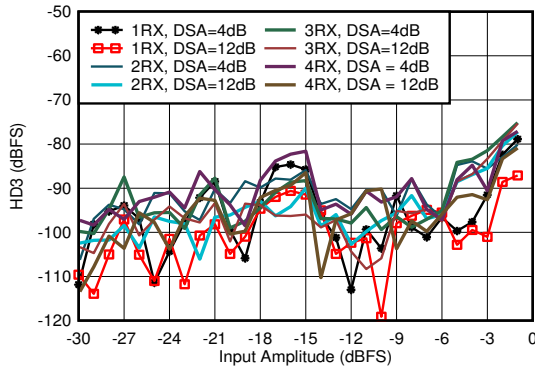
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 6-104. RX HD3 vs DSA Setting and Temperature at 1.9 GHz**



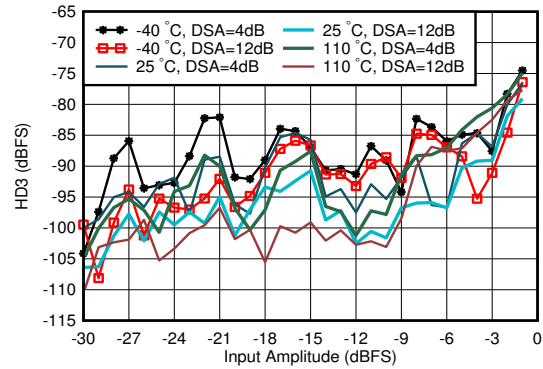
### 6.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



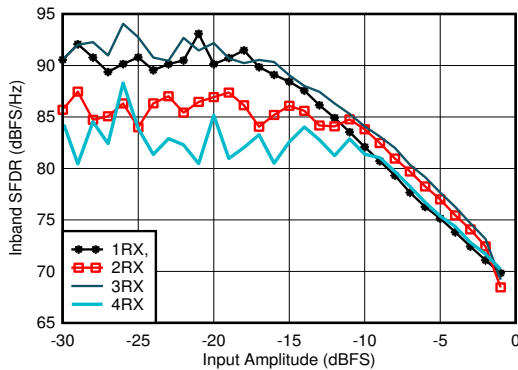
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 6-105. RX HD3 vs Input Level and Channel at 1.9 GHz**



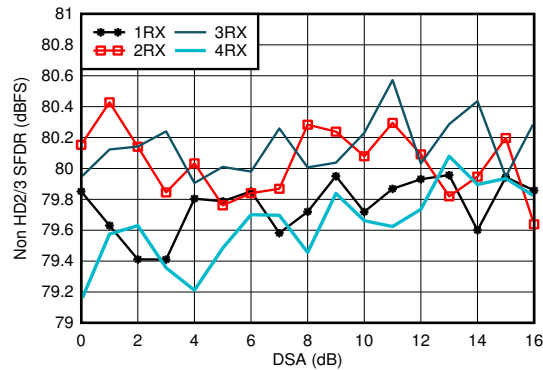
With 1.8 GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 6-106. RX HD3 vs Input Level and Temperature at 1.9 GHz**



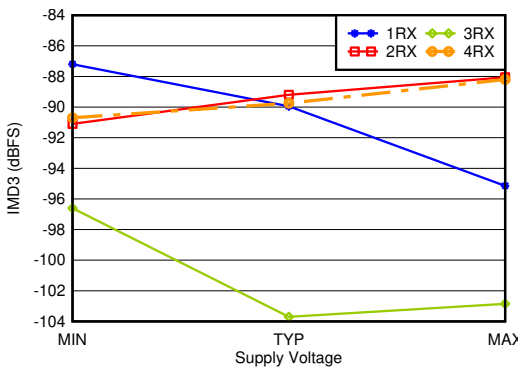
With 1.8 GHz matching, decimated by 3

**Figure 6-107. RX In-Band SFDR ( $\pm 400\text{ MHz}$ ) vs Input Amplitude at 1.75 GHz**



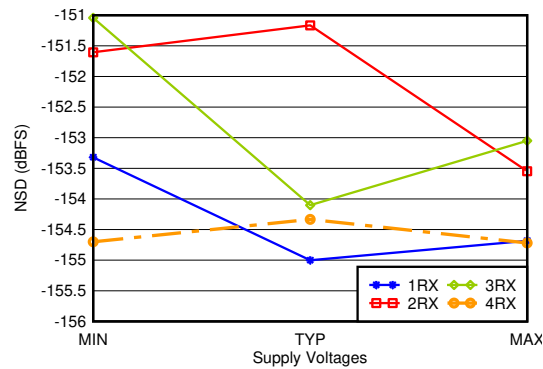
With 1.8 GHz matching

**Figure 6-108. RX Non-HD2/3 vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-109. RX IMD3 vs Supply and Channel at 1.75 GHz**



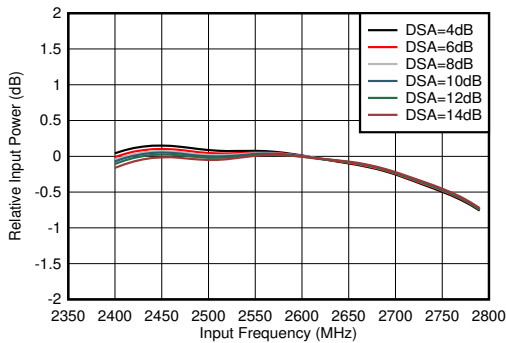
With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-110. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz**



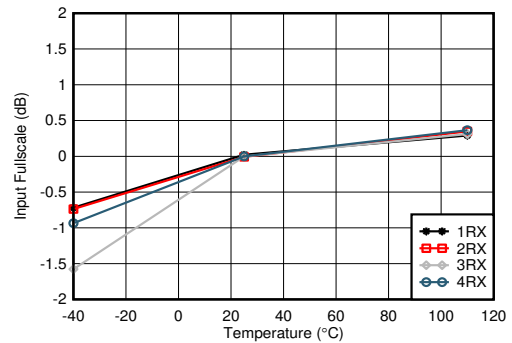
### 6.12.4 RX Typical Characteristics 2.6GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



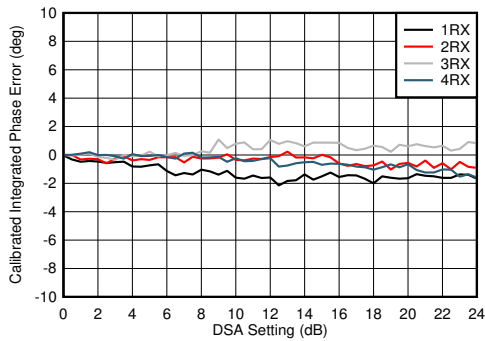
With matching, normalized to power at 2.6 GHz for each DSA setting

**Figure 6-111. RX Inband Gain Flatness,  $f_{IN} = 2600\text{ MHz}$**



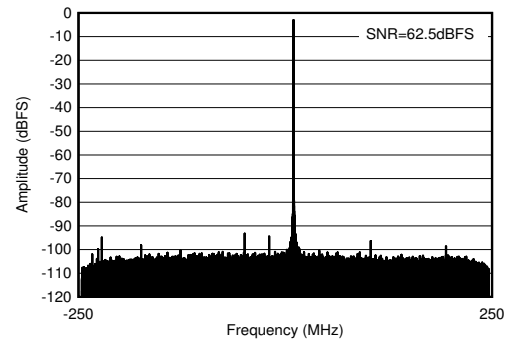
With 2.6 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

**Figure 6-112. RX Input Fullscale vs Temperature and Channel at 2.6 GHz**



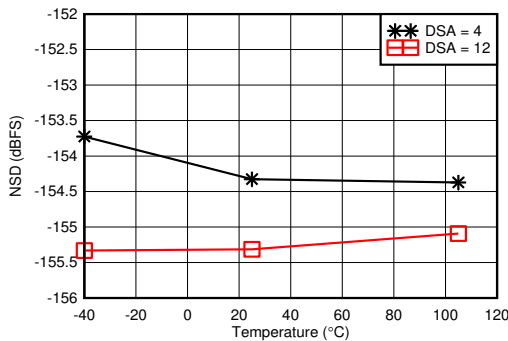
With 2.6 GHz matching  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-113. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz**



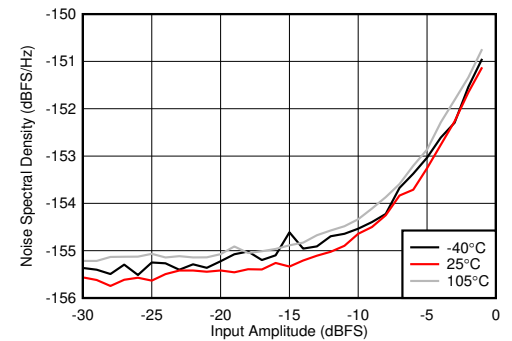
With 2.6 GHz matching,  $f_{IN} = 2610\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

**Figure 6-114. RX Output FFT at 2.6 GHz**



With 2.6 GHz matching, 12.5-MHz offset from tone

**Figure 6-115. RX Noise Spectral Density vs Temperature at 2.6 GHz**

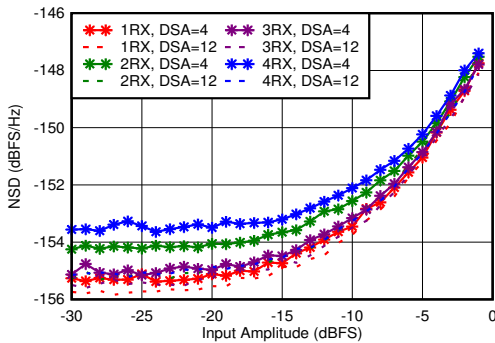


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 6-116. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz**

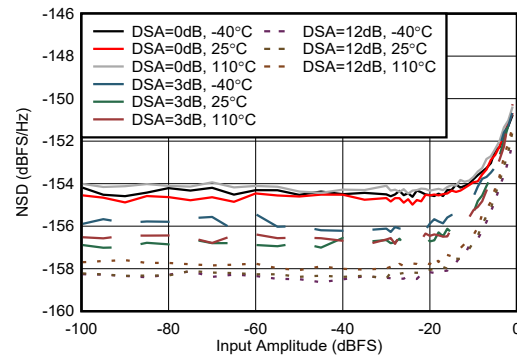
### 6.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



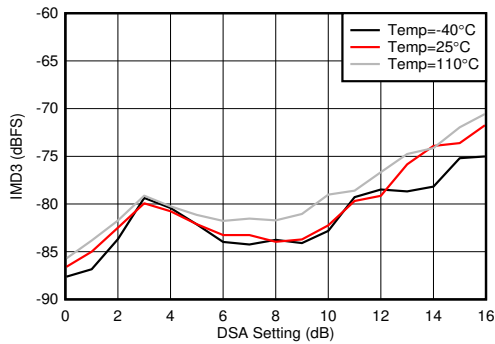
With 2.6 GHz matching, 12.5-MHz offset from tone

**Figure 6-117. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz**



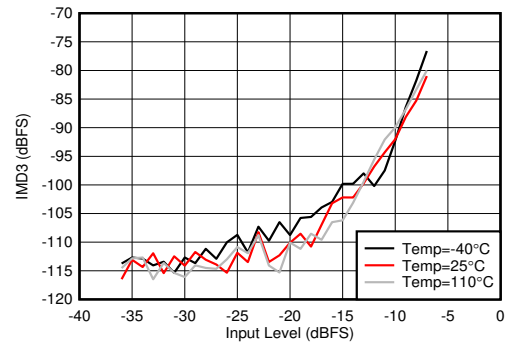
50-MHz offset from tone, external clock mode

**Figure 6-118. RX Noise Spectral Density vs Input Amplitude at 2.61 GHz (Ext. Clock)**



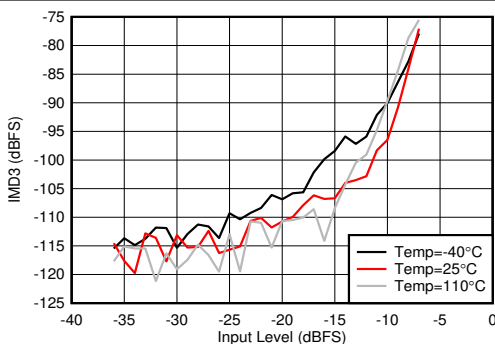
With 2.6 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-119. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz**



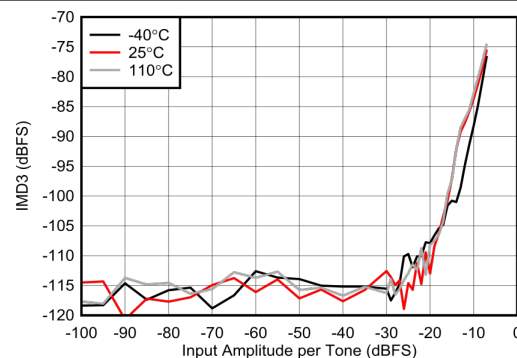
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 6-120. RX IMD3 vs Input Level and Temperature at 2.6 GHz**



With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-121. RX IMD3 vs Input Level and Temperature at 2.6 GHz**

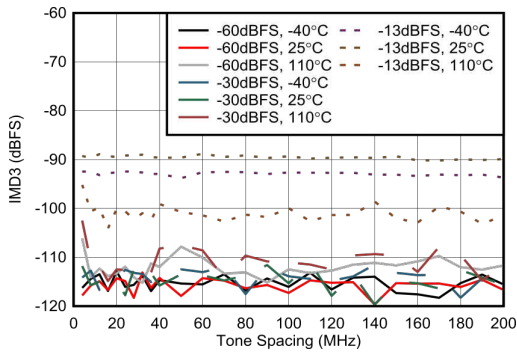


Tone spacing = 50 MHz, External clock mode

**Figure 6-122. RX IMD3 vs Input Level at 2.6 GHz (Ext. Clock)**

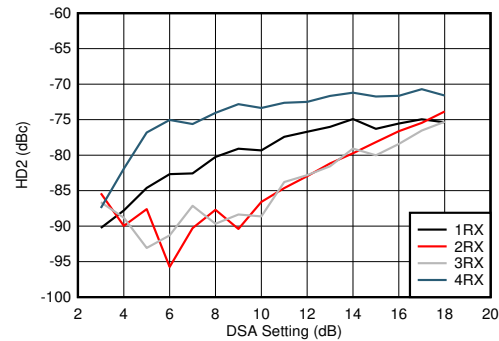
### 6.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



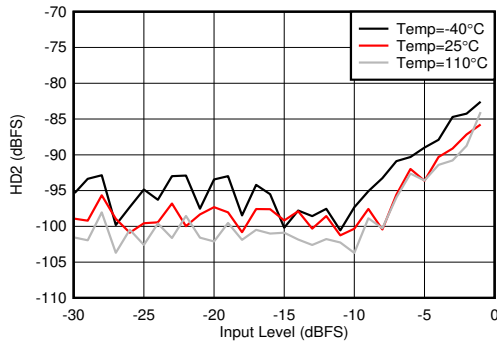
External clock mode

Figure 6-123. RX IMD3 vs Tone Spacing at 2.6 GHz (Ext. Clock)



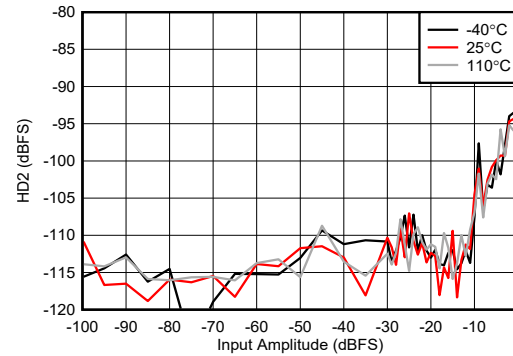
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-124. RX HD2 vs DSA Setting and Channel at 2.6 GHz



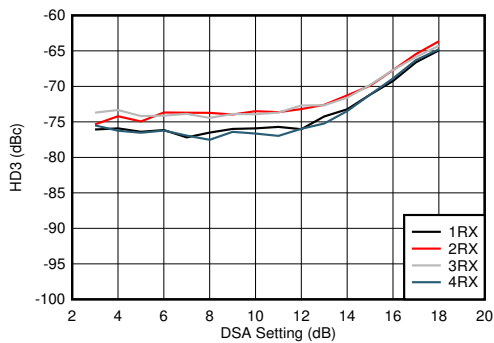
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-125. RX HD2 vs Input Level and Temperature at 2.6 GHz



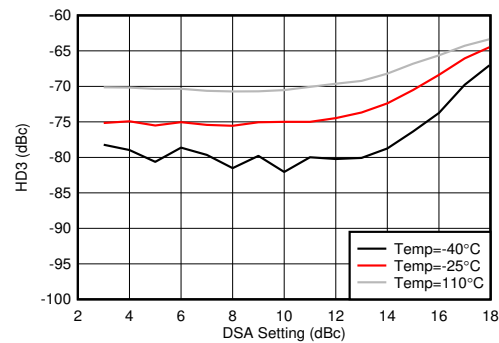
External clock mode

Figure 6-126. RX HD2 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-127. RX HD3 vs DSA Setting and Channel at 2.6 GHz

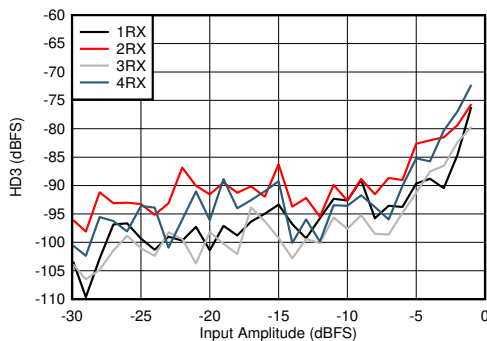


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-128. RX HD3 vs DSA Setting and Temperature at 2.6 GHz

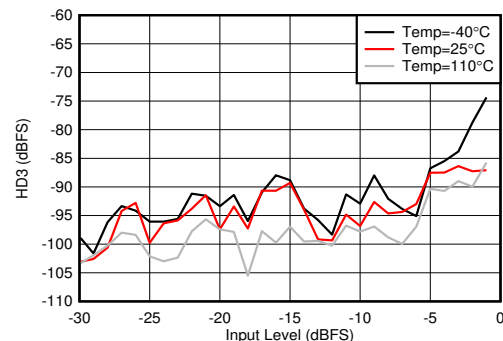
### 6.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4 dB.



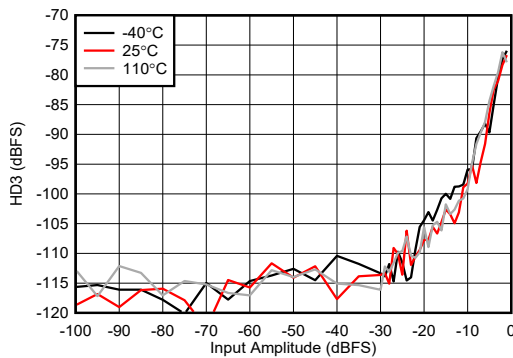
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-129. RX HD3 vs Input Level and Channel at 2.6 GHz**



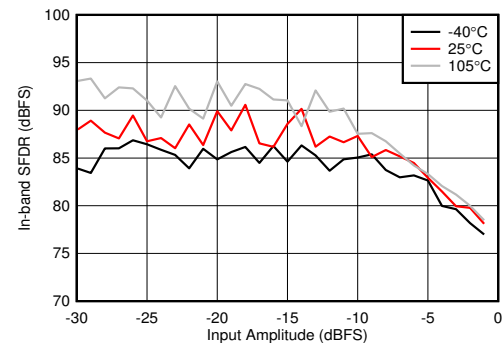
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-130. RX HD3 vs Input Level and Temperature at 2.6 GHz**



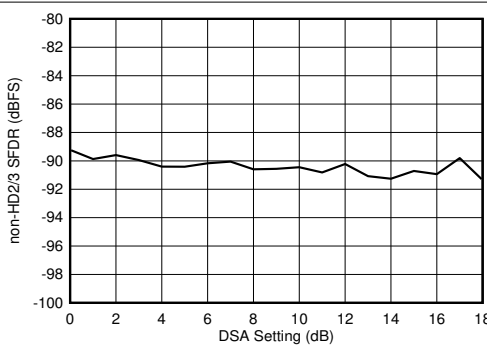
External clock mode

**Figure 6-131. RX HD3 vs Input Level and Temperature at 2.6 GHz**



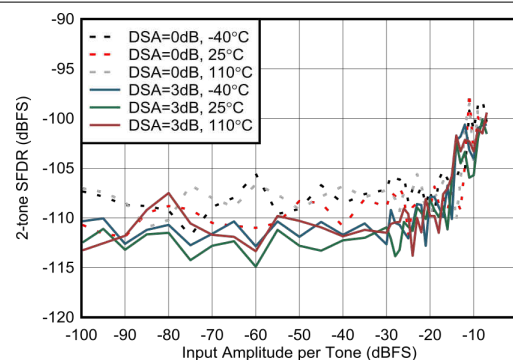
With 2.6 GHz matching, decimate by 4

**Figure 6-132. RX In-Band SFDR ( $\pm 300\text{ MHz}$ ) vs Input Amplitude and Temperature at 2.6 GHz**



With 2.6 GHz matching

**Figure 6-133. RX Non-HD2/3 vs DSA Setting at 2.6 GHz**

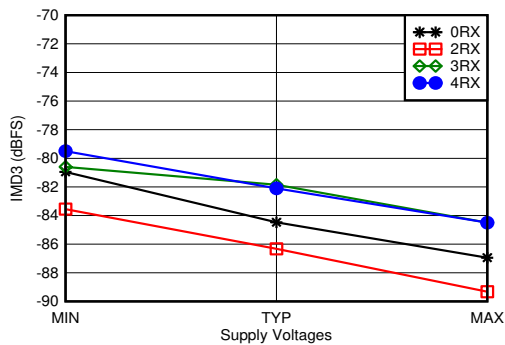


External clock mode, 50MHz tone spacing, excluding 3<sup>rd</sup> order distortion

**Figure 6-134. RX 2-tone SFDR vs Input Amplitude at 2.6 GHz**

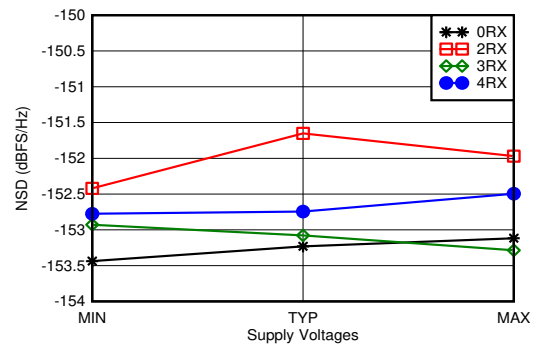
### 6.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 2.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-135. RX IMD3 vs Supply and Channel at 2.6 GHz

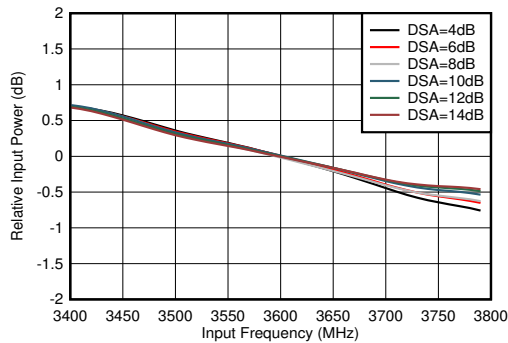


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-136. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

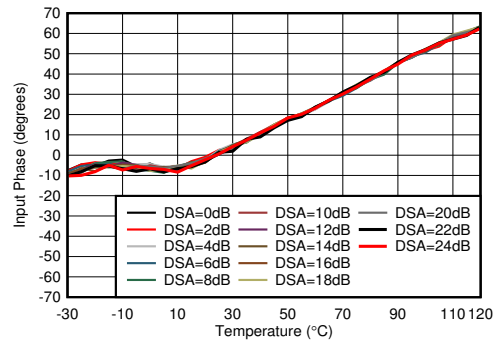
### 6.12.5 RX Typical Characteristics 3.5GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



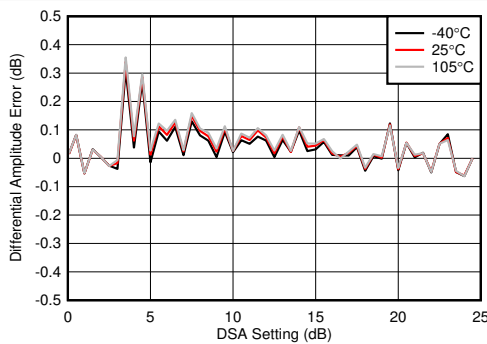
With 3.6 GHz matching, normalized to 3.6 GHz

**Figure 6-137. RX In-Band Gain Flatness,  $f_{IN} = 3600 \text{ MHz}$**



With 3.6 GHz matching, normalized to phase at 25°C

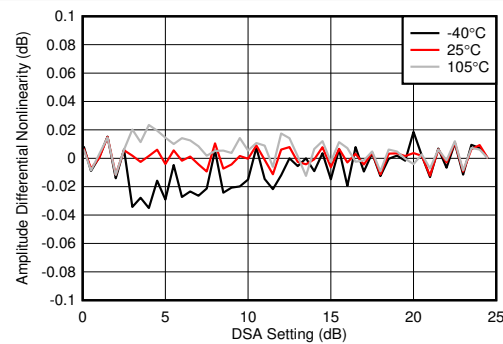
**Figure 6-138. RX Input Phase vs Temperature at 3.6 GHz**



With 3.6 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

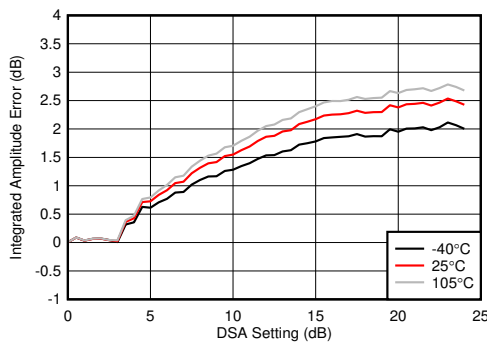
**Figure 6-139. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

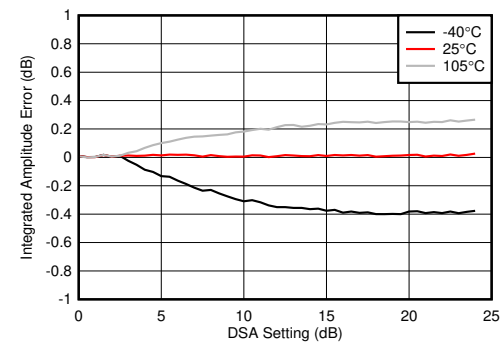
**Figure 6-140. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

**Figure 6-141. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz**



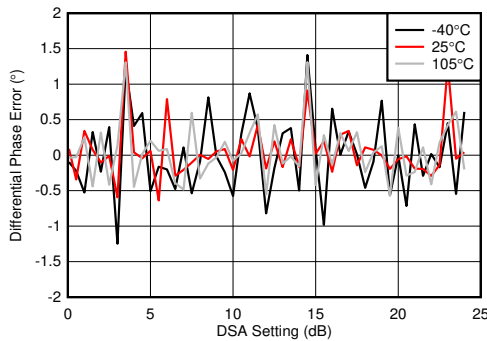
With 3.6 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

**Figure 6-142. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz**

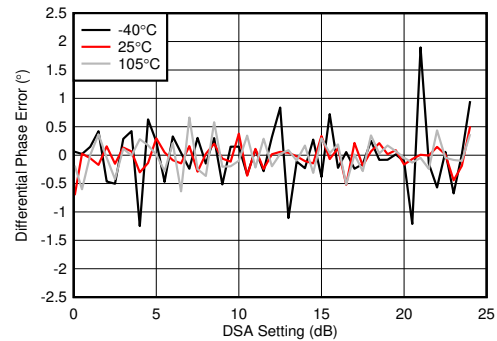
### 6.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



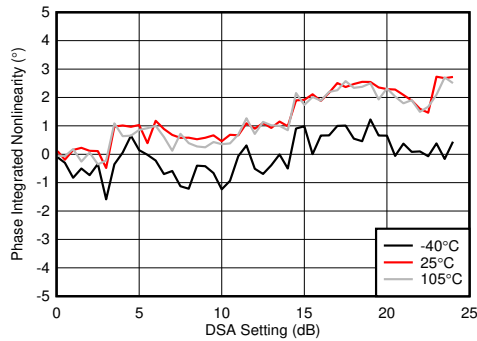
With 3.6 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-143. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz**



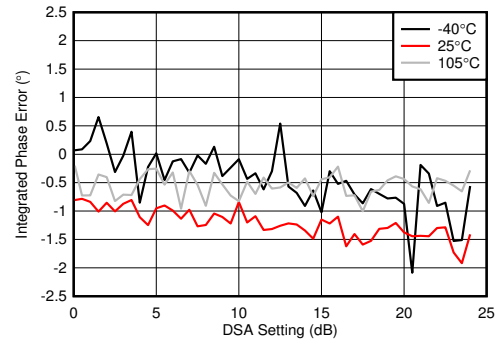
With 3.6 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-144. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz**



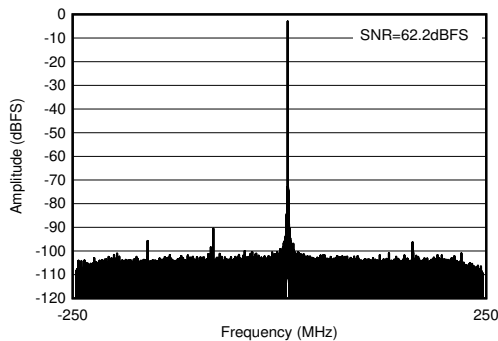
With 3.6 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-145. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz**



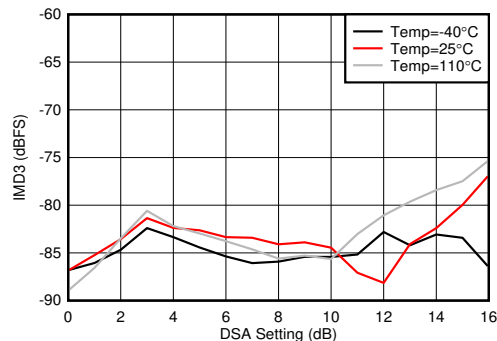
With 3.6 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-146. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching,  $f_{IN} = 3610\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

**Figure 6-147. RX Output FFT at 3.6 GHz**

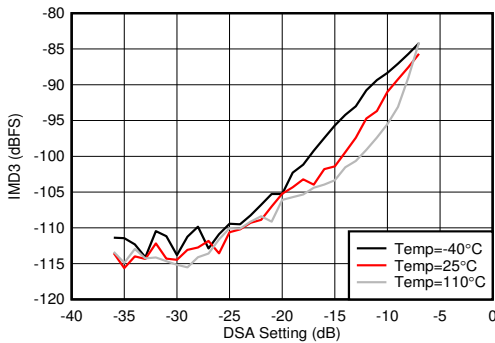


With 3.5 GHz matching, each tone at  $-7\text{ dBFS}$ , 20-MHz tone spacing

**Figure 6-148. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz**

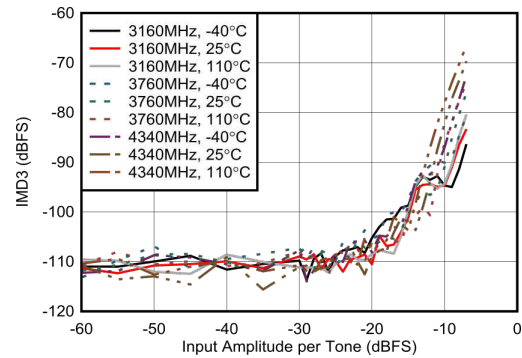
**6.12.5 RX Typical Characteristics 3.5GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



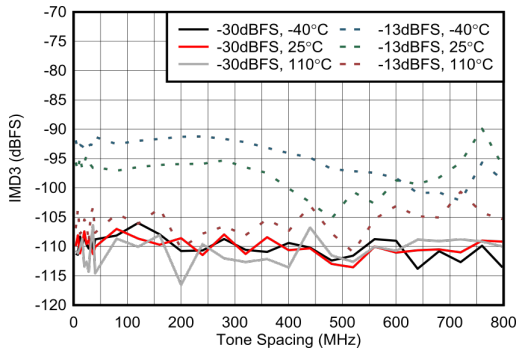
With 3.5 GHz matching, 20-MHz tone spacing

**Figure 6-149. RX IMD3 vs Input Level and Temperature at 3.6 GHz**



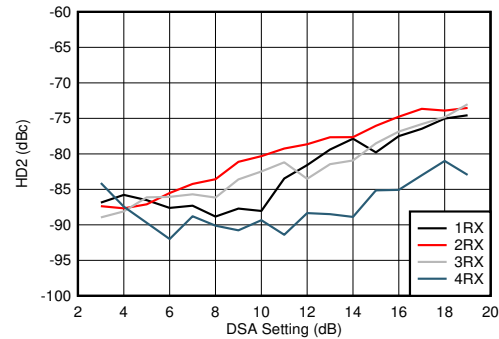
External clock mode, 20-MHz tone spacing, 2x Decimation

**Figure 6-150. RX IMD3 vs Input Level**



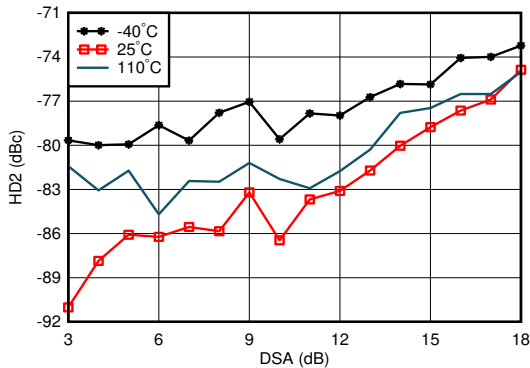
External clock mode, 2x Decimation

**Figure 6-151. RX IMD3 vs Tone Spacing at 3.76GHz**



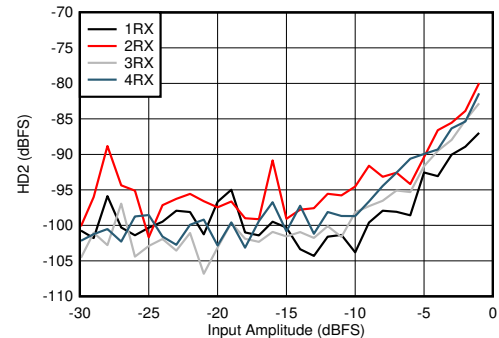
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-152. RX HD2 vs DSA Setting and Channel at 3.6 GHz**



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-153. RX HD2 vs DSA Setting and Temperature at 3.6 GHz**



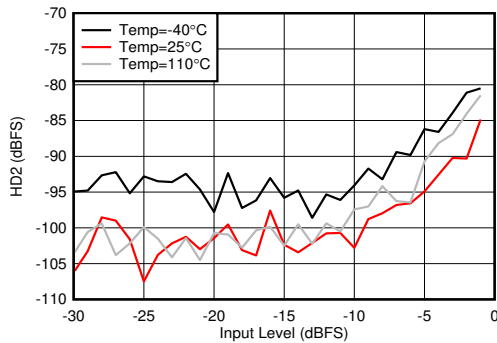
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-154. RX HD2 vs Input Level and Channel at 3.6 GHz**



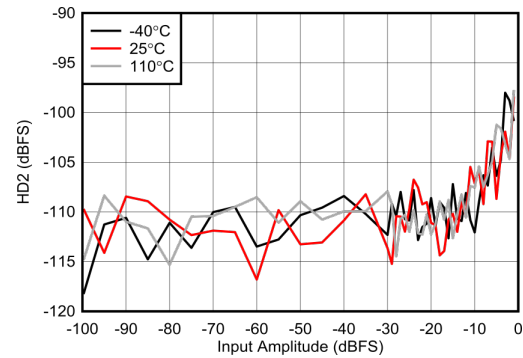
### 6.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



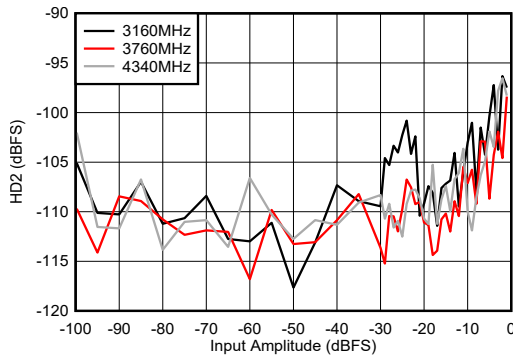
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-155. RX HD2 vs Input Level and Temperature at 3.6 GHz**



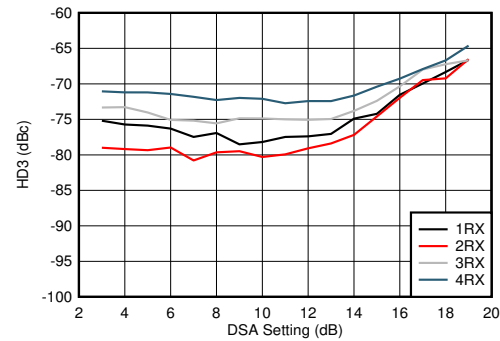
External clock mode, 2x Decimation

**Figure 6-156. RX HD2 vs Input Level at 3.76 GHz**



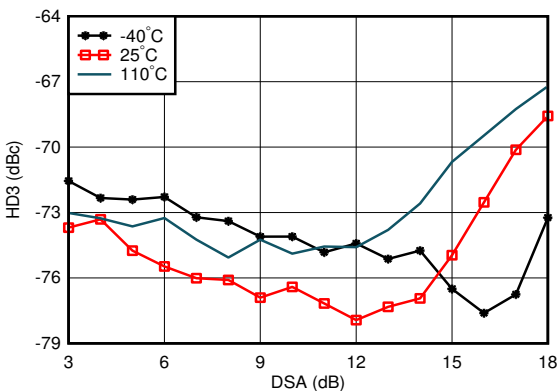
External clock mode, 25°C, 2x Decimation

**Figure 6-157. RX HD2 vs Input Level**



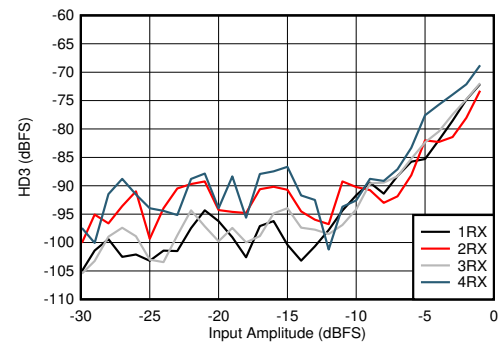
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-158. RX HD3 vs DSA Setting and Channel at 3.6 GHz**



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-159. RX HD3 vs DSA Setting and Temperature at 3.6 GHz**

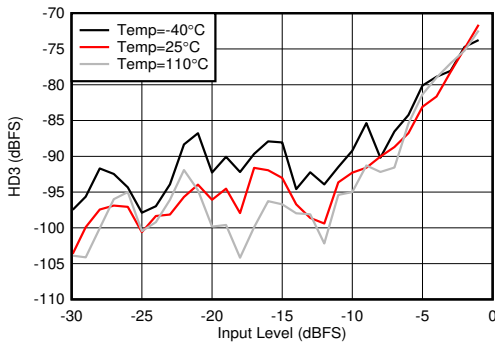


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-160. RX HD3 vs Input Level and Channel at 3.6 GHz**

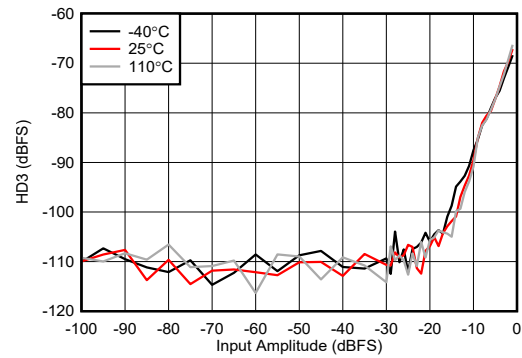
### 6.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



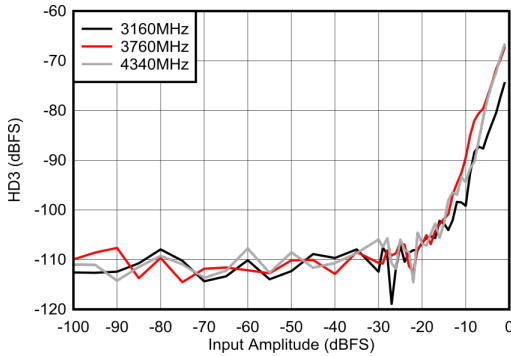
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-161. RX HD3 vs Input Level and Temperature at 3.6 GHz**



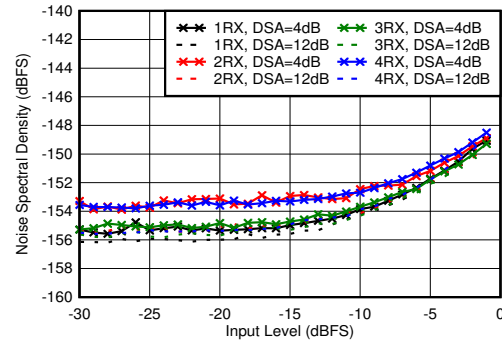
External clock mode, 2x Decimation

**Figure 6-162. RX HD3 vs Input Level at 3.76GHz**



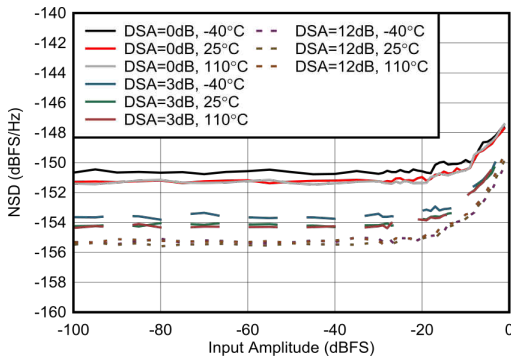
External clock mode, 25°C, 2x Decimation

**Figure 6-163. RX HD3 vs Input Level**



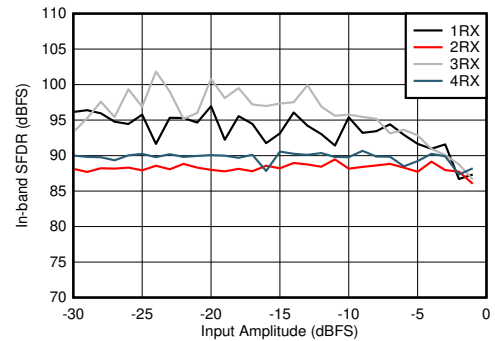
With 3.5 GHz matching, 12.5-MHz offset from tone

**Figure 6-164. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz**



External clock mode, 25°C, 2x Decimation

**Figure 6-165. RX Noise Spectral Density vs Input Level at 3.76GHz**

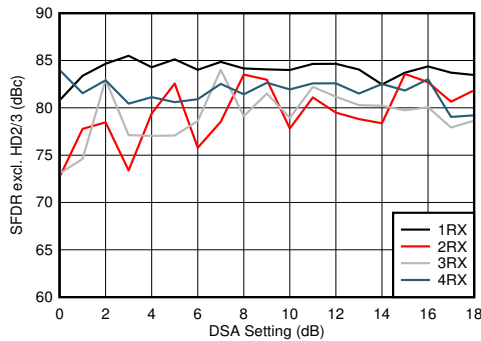


With 3.5 GHz matching

**Figure 6-166. RX In-Band SFDR ( $\pm 200\text{ MHz}$ ) vs Input Level and Channel at 3.6 GHz**

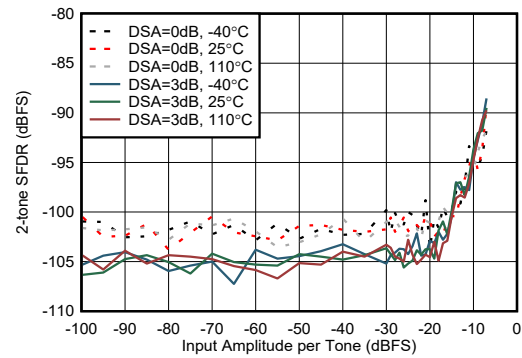
### 6.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



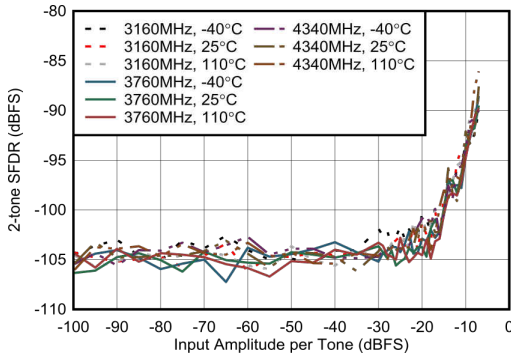
With 3.5 GHz matching

Figure 6-167. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz



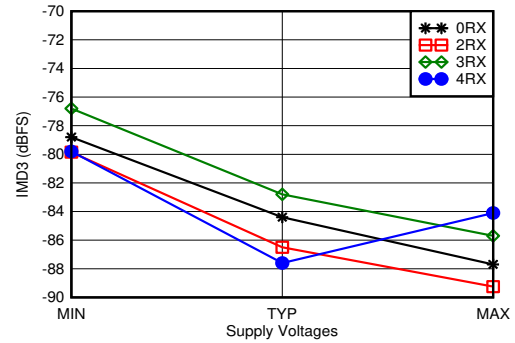
External clock mode, 20MHz tone spacing, excluding 3<sup>rd</sup> order distortion

Figure 6-168. RX 2-tone SFDR vs Input Amplitude and DSA Setting at 3.7 GHz



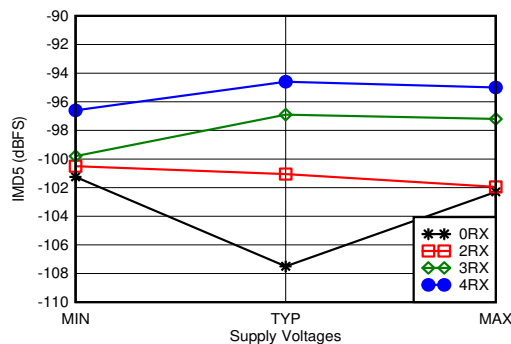
External clock mode, 20MHz tone spacing, excluding 3<sup>rd</sup> order distortion

Figure 6-169. RX 2-tone SFDR vs Input Amplitude and Frequency at 3.7 GHz



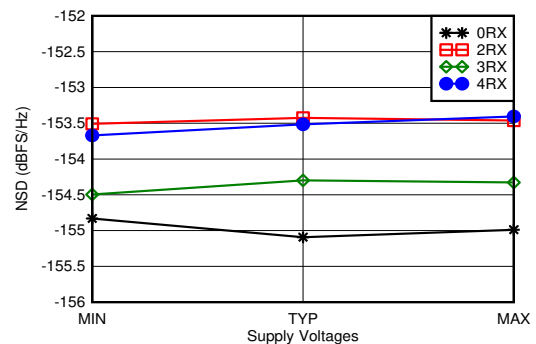
With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-170. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz



With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-171. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

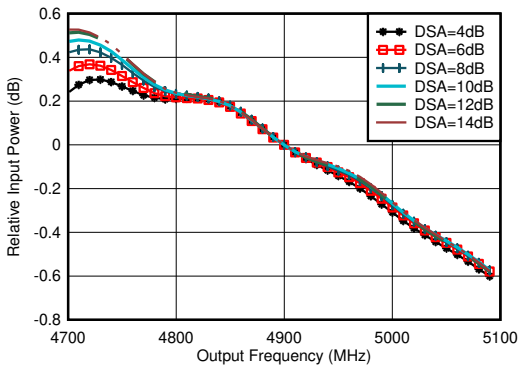


With 3.6 GHz matching, tone at -20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-172. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

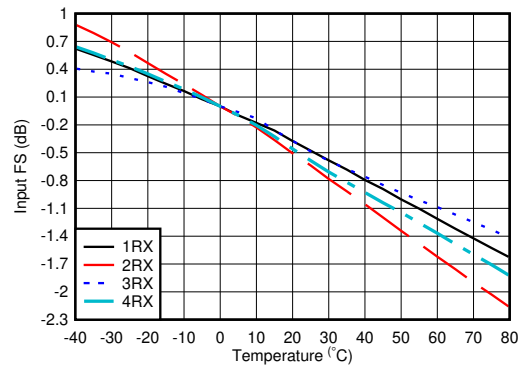
### 6.12.6 RX Typical Characteristics 4.9GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4 dB.



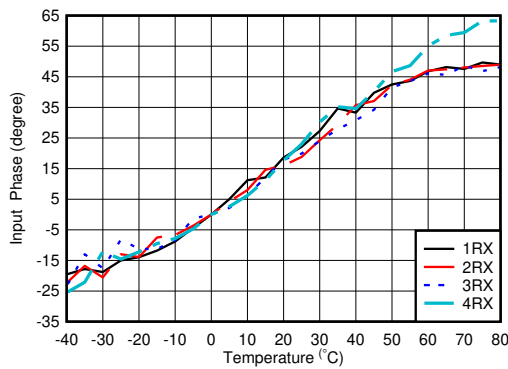
With matching, normalized to power at 4.9GHz for each DSA setting

**Figure 6-173. RX Inband Gain Flatness,  $f_{IN} = 4900\text{ MHz}$**



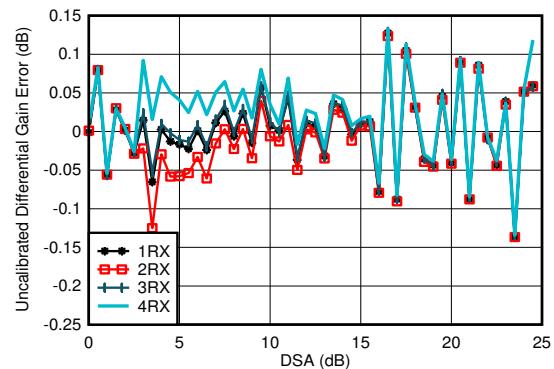
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

**Figure 6-174. RX Input Fullscale vs Temperature and Channel at 4.9 GHz**



With 4.9 GHz matching, normalized to phase at 25°C

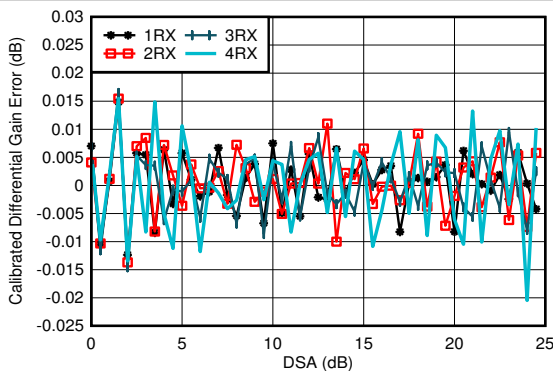
**Figure 6-175. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 4.9\text{ GHz}$**



With 4.9 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

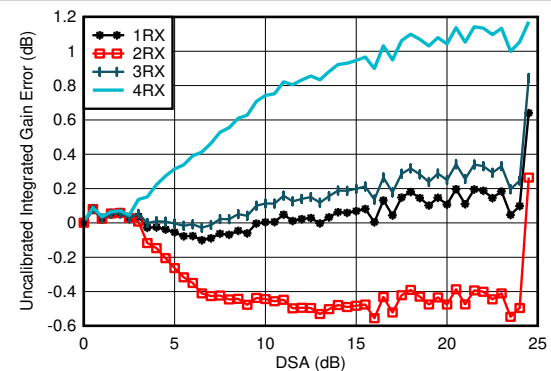
**Figure 6-176. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

**Figure 6-177. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz**



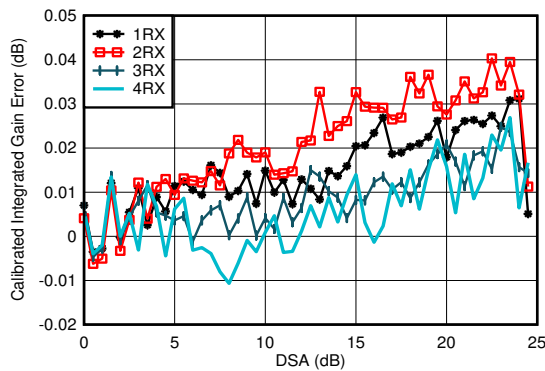
With 4.9 GHz matching

$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

**Figure 6-178. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz**

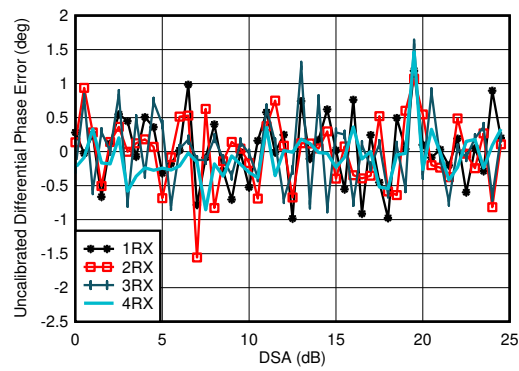
### 6.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



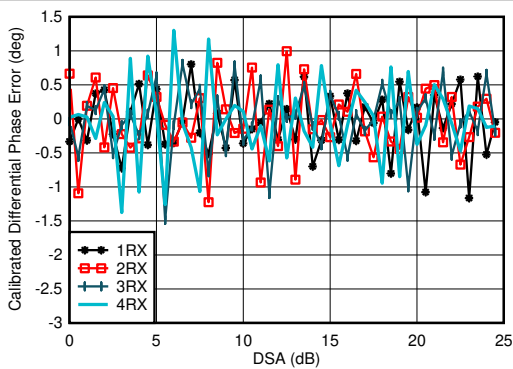
With 4.9 GHz matching  
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-179. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz**



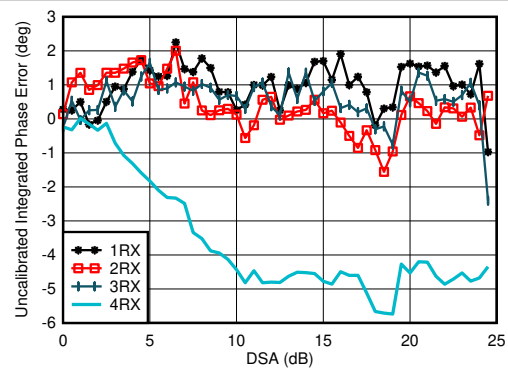
With 4.9 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-180. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz**



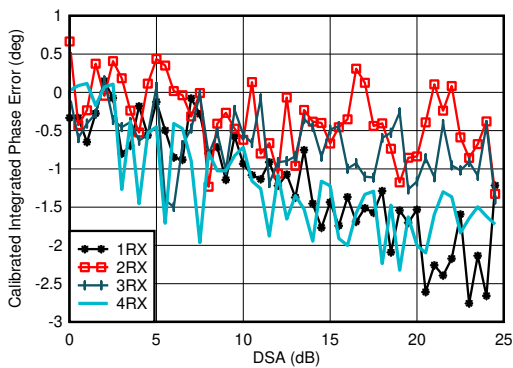
With 4.9 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-181. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz**



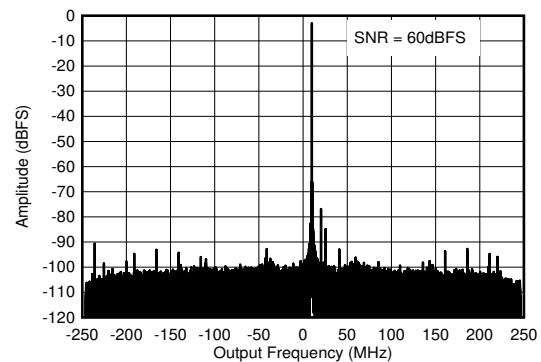
With 4.9 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-182. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-183. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz**

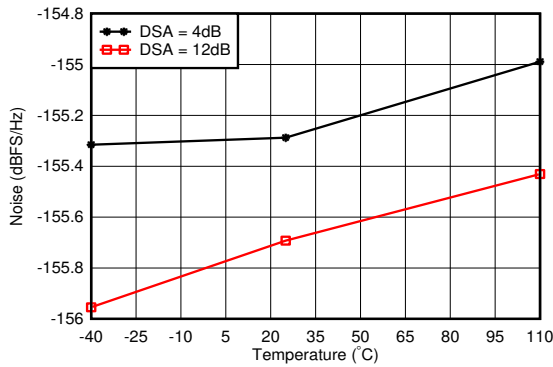


With 4.9 GHz matching,  $f_{IN} = 4910\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

**Figure 6-184. RX Output FFT at 4.9 GHz**

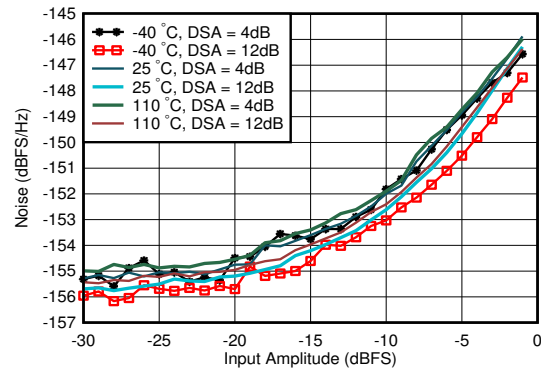
### 6.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



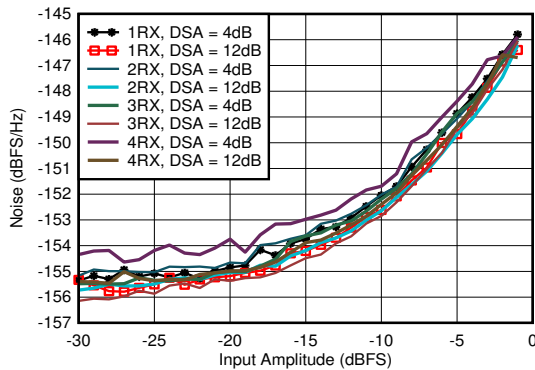
With 4.9 GHz matching, 12.5-MHz offset from tone

**Figure 6-185. RX Noise Spectral Density vs Temperature at 4.9 GHz**



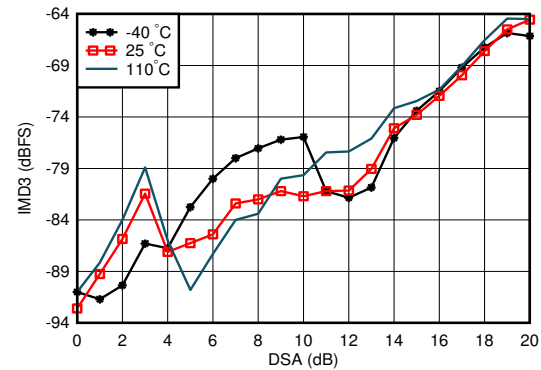
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 6-186. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz**



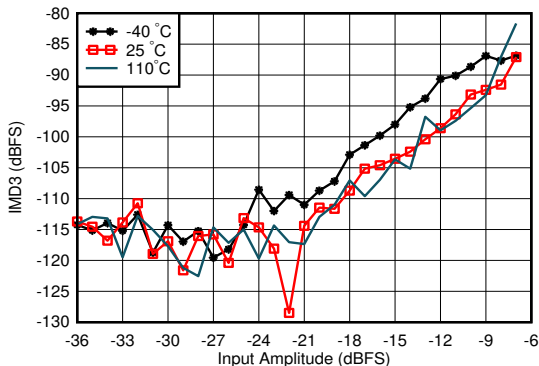
With 4.9 GHz matching, 12.5-MHz offset from tone

**Figure 6-187. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz**



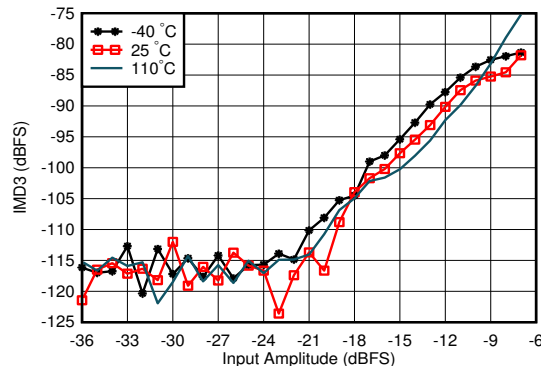
With 4.9 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-188. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz**



With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 6-189. RX IMD3 vs Input Level and Temperature at 4.9 GHz**

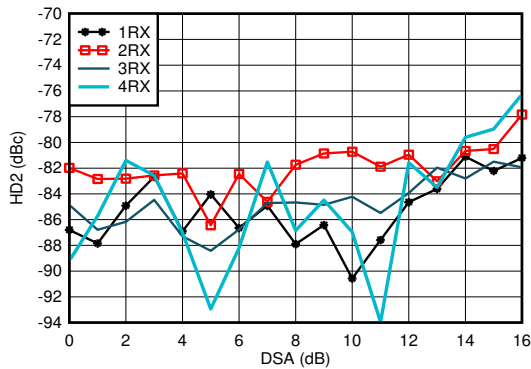


With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-190. RX IMD3 vs Input Level and Temperature at 4.9 GHz**

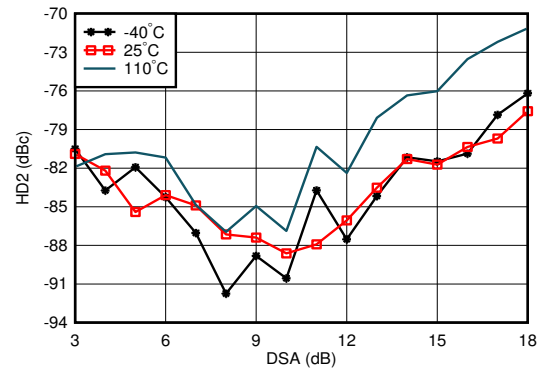
### 6.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4 dB.



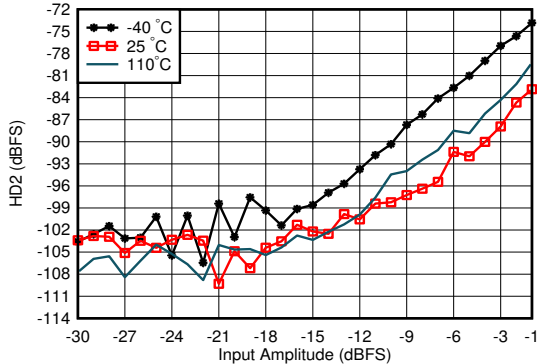
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-191. RX HD2 vs DSA Setting and Channel at 4.9 GHz



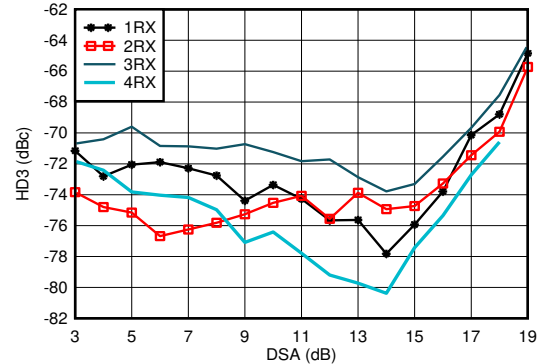
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-192. RX HD2 vs DSA and Temperature at 4.9 GHz



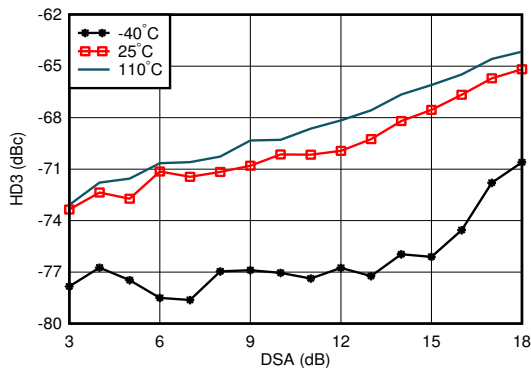
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-193. RX HD2 vs Input Level and Temperature at 4.9 GHz



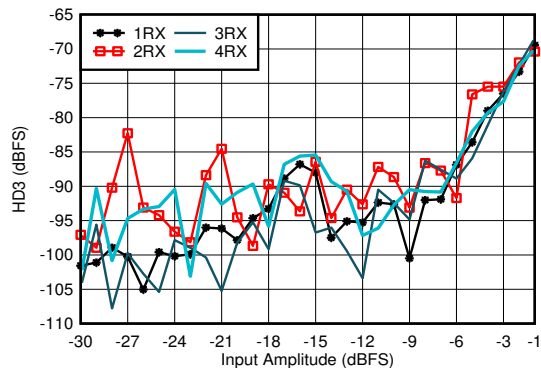
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-194. RX HD3 vs DSA Setting and Channel at 4.9 GHz



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-195. RX HD3 vs DSA Setting and Temperature at 4.9 GHz



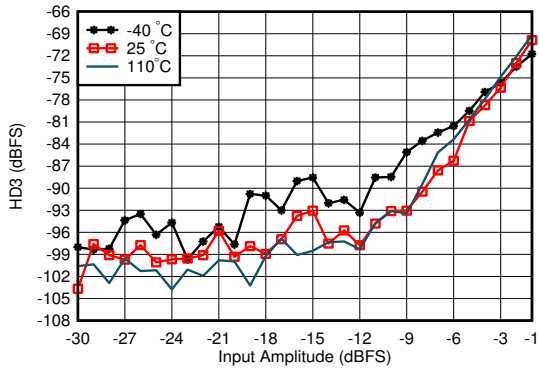
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-196. RX HD3 vs Input Level and Channel at 4.9 GHz



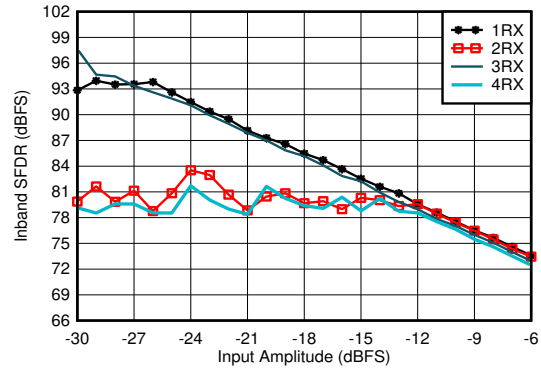
### 6.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



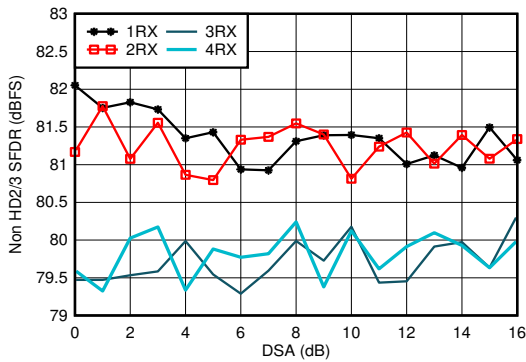
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-197. RX HD3 vs Input Level and Temperature at 4.9 GHz**



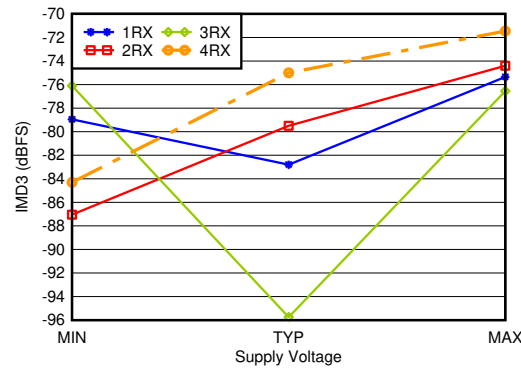
With 4.9 GHz matching, decimate by 3

**Figure 6-198. RX In-Band SFDR ( $\pm 400\text{ MHz}$ ) vs Input Amplitude and Channel at 4.9 GHz**



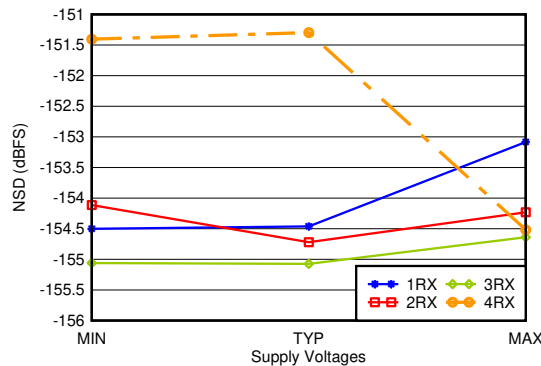
With 4.9 GHz matching

**Figure 6-199. RX Non-HD2/3 vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-200. RX IMD3 vs Supply and Channel at 4.9 GHz**



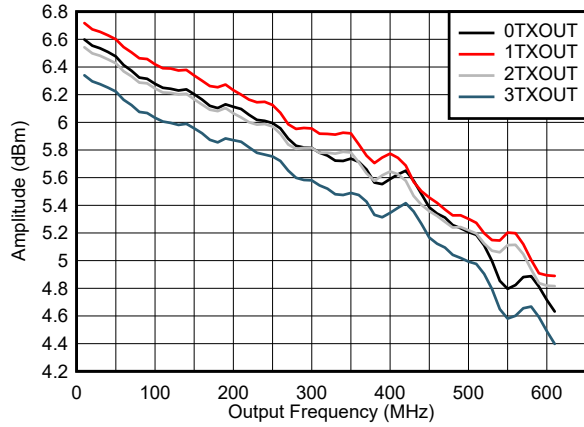
With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-201. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz**



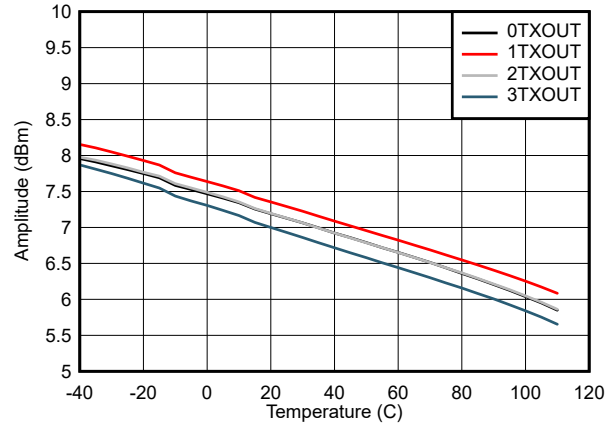
### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



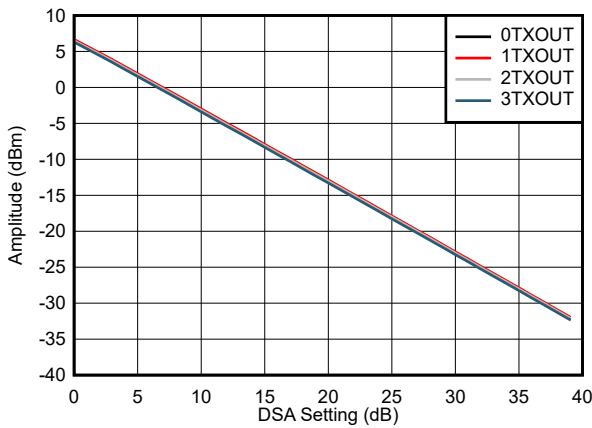
including PCB and cable losses

**Figure 6-202. TX Output Fullscale vs Output Frequency: 5 MHz - 600 MHz**



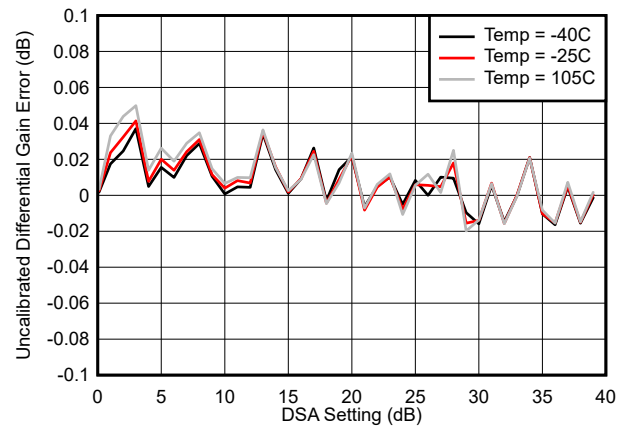
including PCB and cable losses

**Figure 6-203. TX Output Fullscale vs Temperature at 30 MHz**



including PCB and cable losses

**Figure 6-204. TX Output Fullscale vs DSA Setting at 30 MHz**

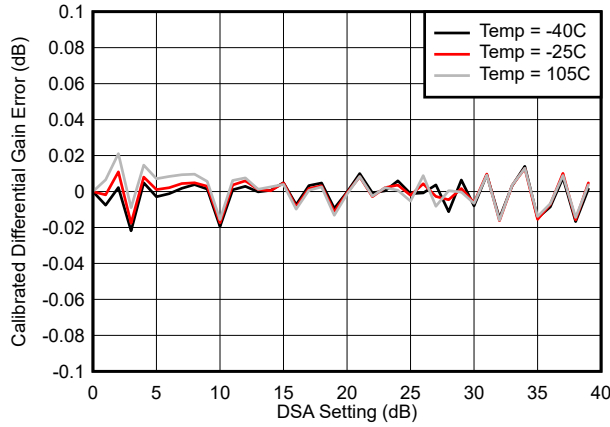


Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-205. Uncalibrated TX Differential Gain Error (DNL) at 30 MHz**

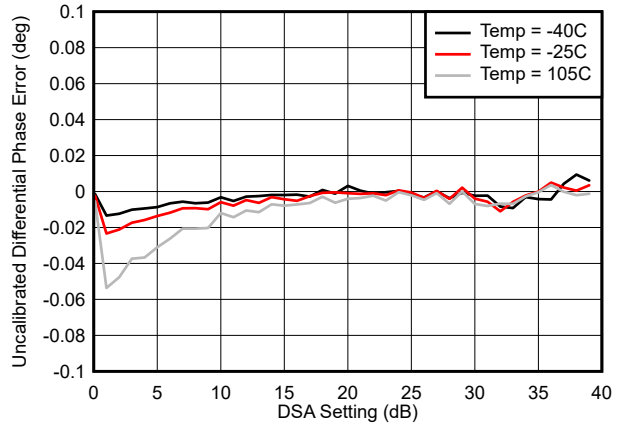
### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



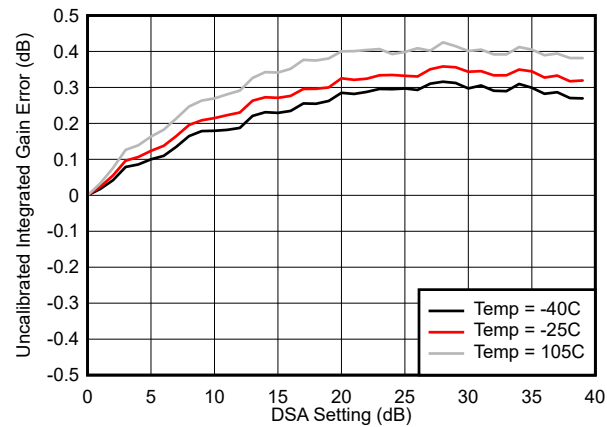
$$\text{Differential Gain Error} = P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$$

**Figure 6-206. Calibrated TX Differential Gain Error (DNL) at 30MHz**



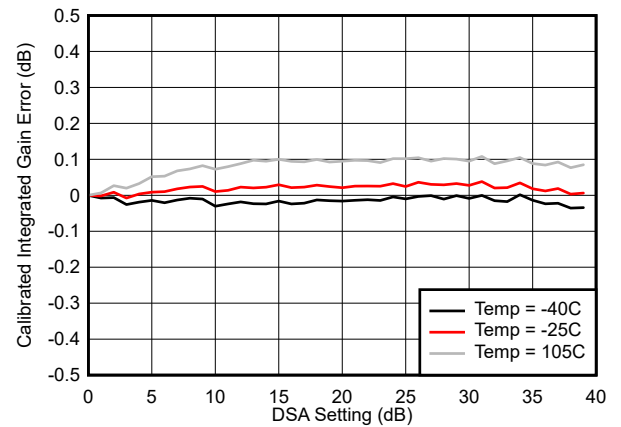
$$\text{Differential Gain Error} = P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$$

**Figure 6-207. Calibrated TX Differential Gain Error (DNL) at 30 MHz**



$$\text{Integrated Gain Error} = P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSASetting} = 0) + (\text{DSA Setting})$$

**Figure 6-208. Uncalibrated TX Integrated Gain Error (INL) at 30 MHz**

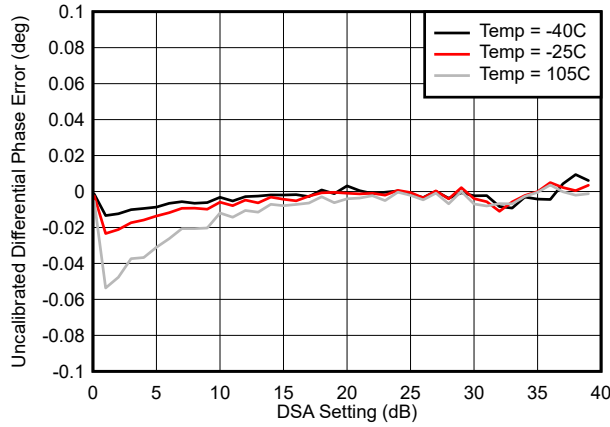


$$\text{Integrated Gain Error} = P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSASetting} = 0) + (\text{DSA Setting})$$

**Figure 6-209. Calibrated TX Integrated Gain Error (INL) at 30 MHz**

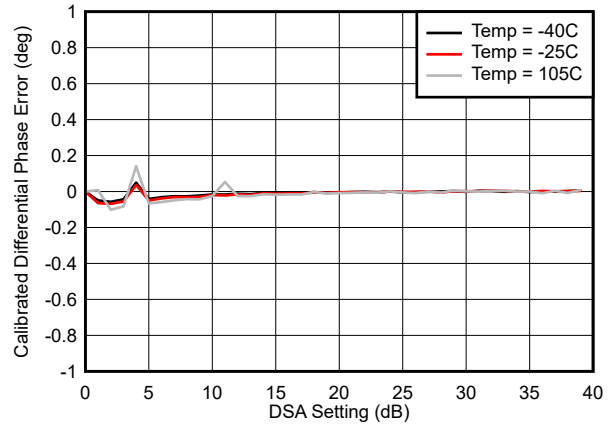
### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



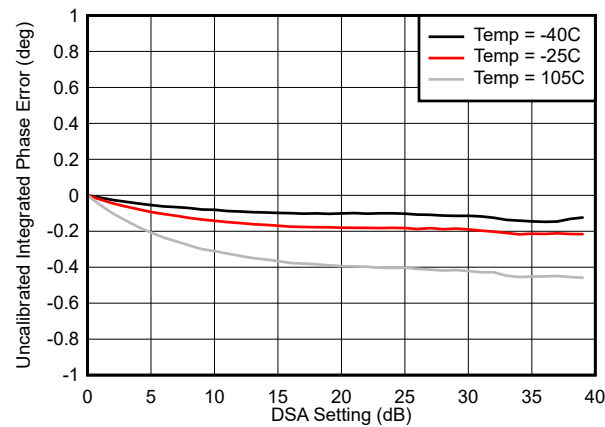
$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

**Figure 6-210. Uncalibrated TX Differential Phase Error (DNL) at 30 MHz**



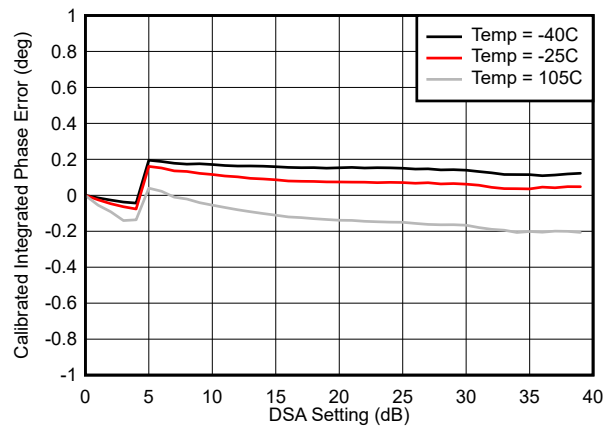
$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

**Figure 6-211. Calibrated TX Differential Phase Error (DNL) at 30 MHz**



$$\text{Integrated Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSASetting} = 0)$$

**Figure 6-212. Uncalibrated TX Integrated Phase Error (INL) at 30 MHz**



$$\text{Integrated Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSASetting} = 0)$$

**Figure 6-213. Calibrated TX Integrated Phase Error (INL) at 30 MHz**

### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

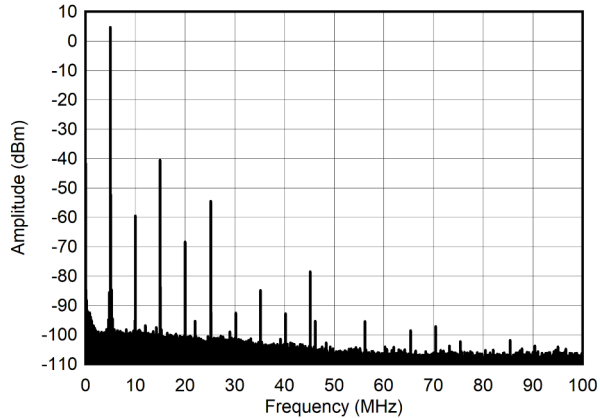


Figure 6-214. Single Tone Spectrum at 5 MHz and -1 dBFS (0 - 100 MHz)

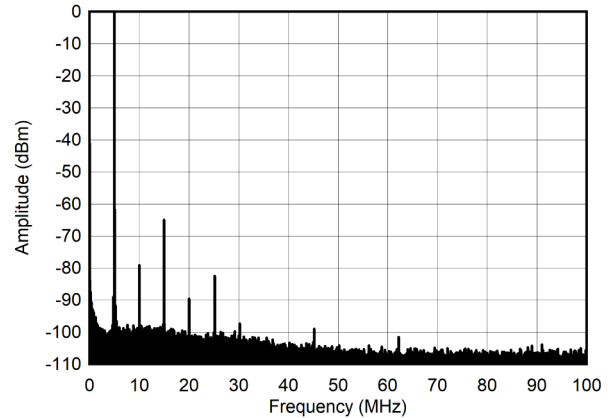


Figure 6-215. Single Tone Spectrum at 5 MHz and -6 dBFS (0 - 100 MHz)

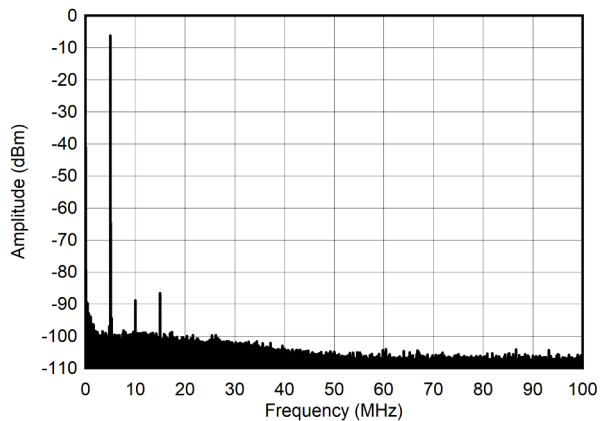


Figure 6-216. Single Tone Spectrum at 5 MHz and -12 dBFS (0 - 100 MHz)

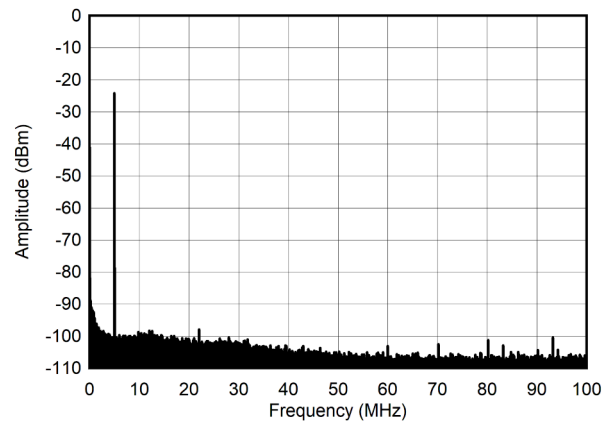


Figure 6-217. Single Tone Spectrum at 5 MHz and -30 dBFS (0 - 100 MHz)

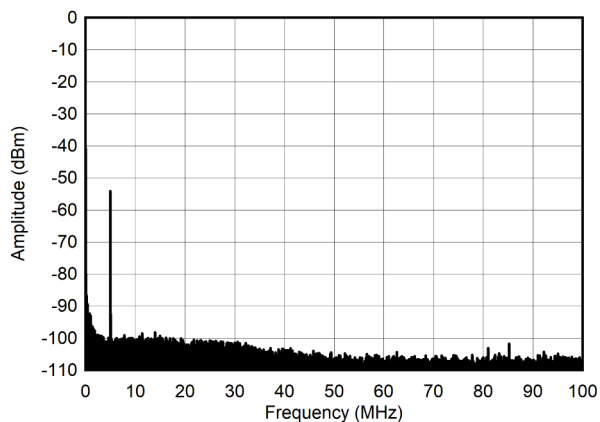


Figure 6-218. Single Tone Spectrum at 5 MHz and -60 dBFS (0 - 100 MHz)

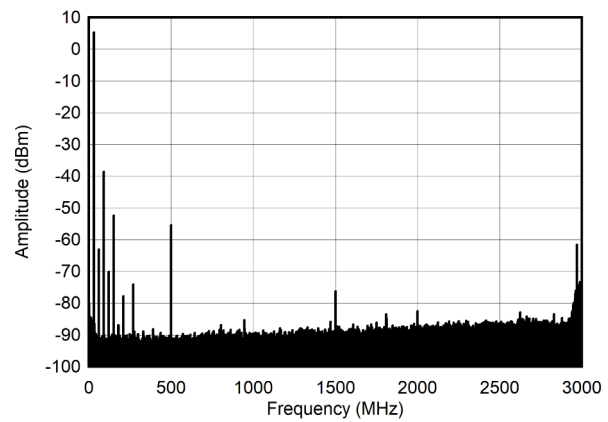


Figure 6-219. Single Tone Spectrum at 30 MHz and -1 dBFS (Nyquist)

### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

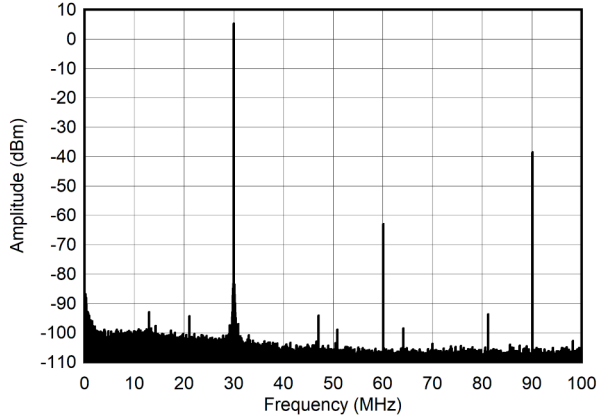


Figure 6-220. Single Tone Spectrum at 30 MHz and -1 dBFS (0 - 100 MHz)

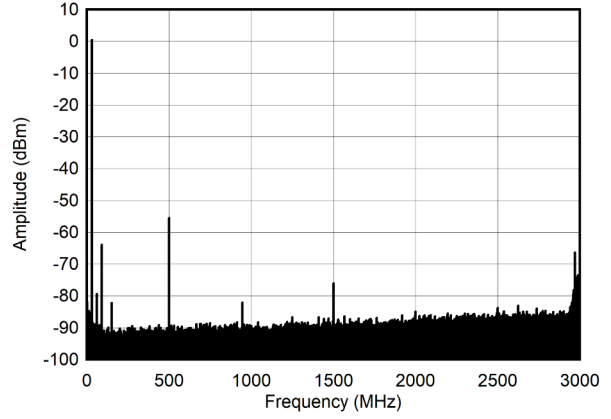


Figure 6-221. Single Tone Spectrum at 30 MHz and -6 dBFS (Nyquist)

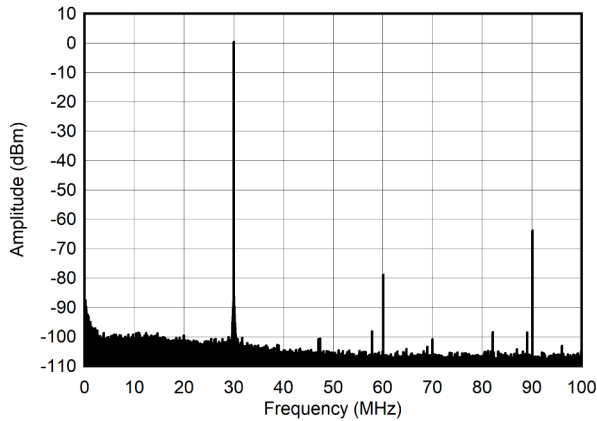


Figure 6-222. Single Tone Spectrum at 30 MHz and -6 dBFS (0 - 100 MHz)

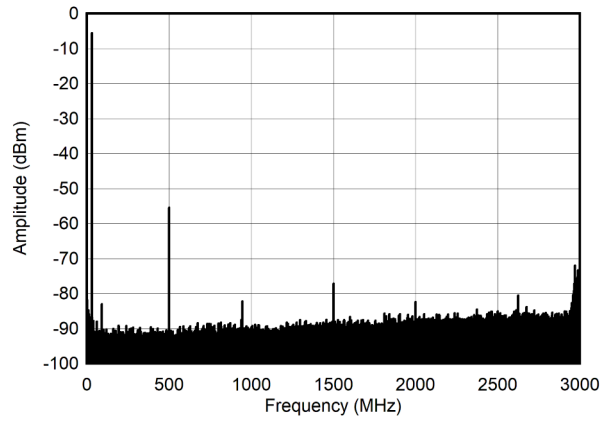


Figure 6-223. Single Tone Spectrum at 30 MHz and -12 dBFS (Nyquist)

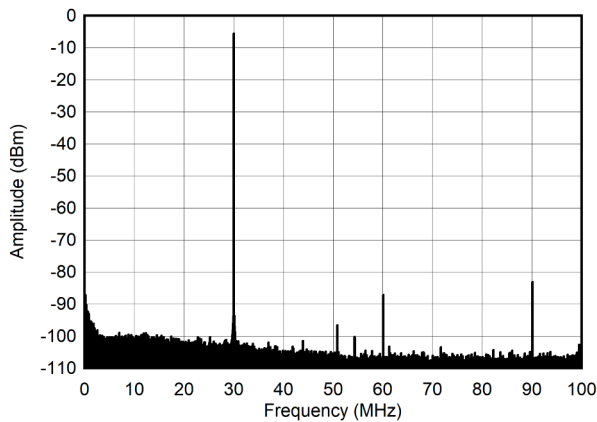


Figure 6-224. Single Tone Spectrum at 30 MHz and -12 dBFS (0 - 100 MHz)

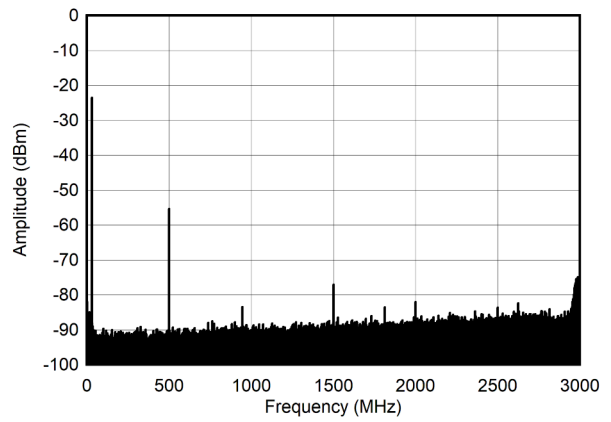


Figure 6-225. Single Tone Spectrum at 30 MHz and -30 dBFS (Nyquist)

### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

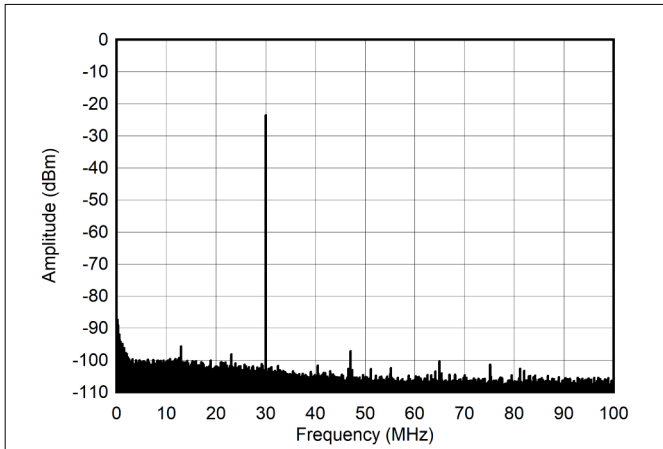


Figure 6-226. Single Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

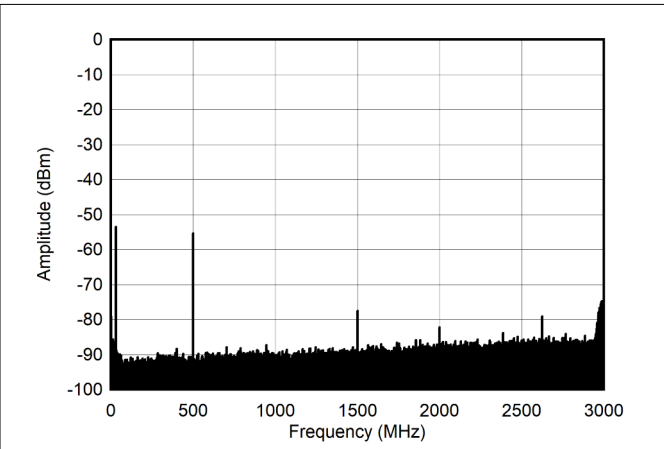


Figure 6-227. Single Tone Spectrum at 30 MHz and -60 dBFS (Nyquist)

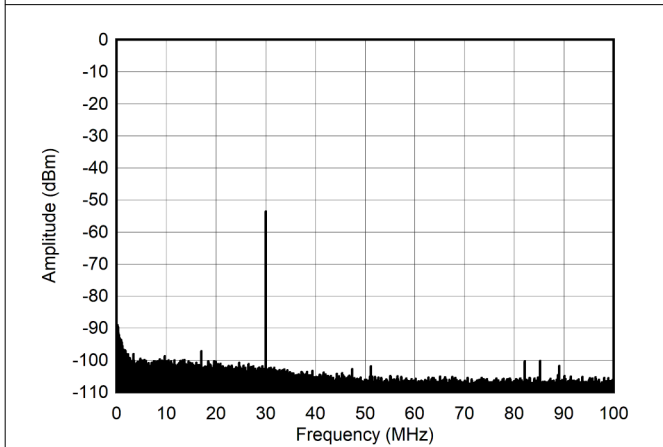


Figure 6-228. Single Tone Spectrum at 30 MHz and -60 dBFS (0 - 100 MHz)

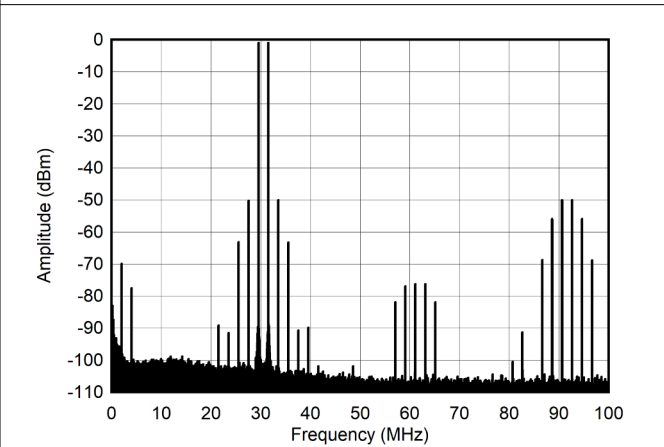


Figure 6-229. Dual Tone Spectrum at 30 MHz and -7 dBFS (0 - 100 MHz)

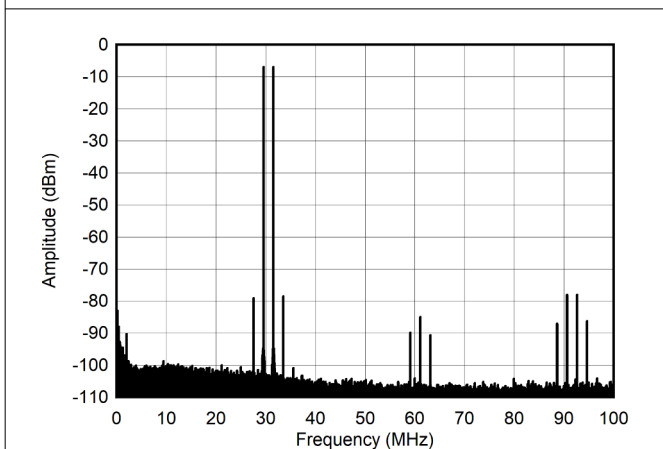


Figure 6-230. Dual Tone Spectrum at 30 MHz and -13 dBFS (0 - 100 MHz)

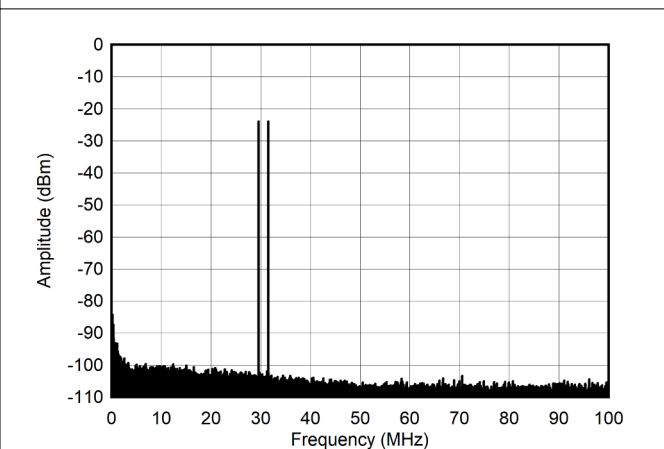


Figure 6-231. Dual Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

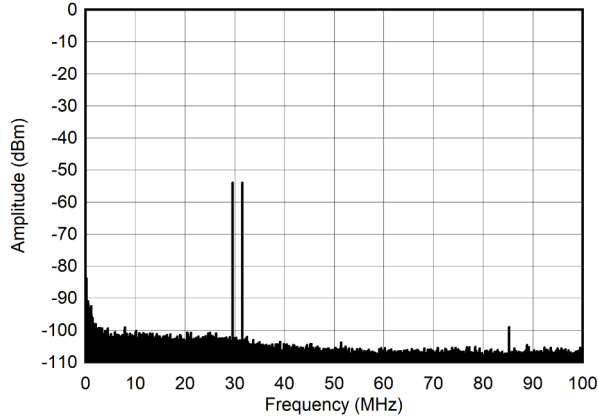
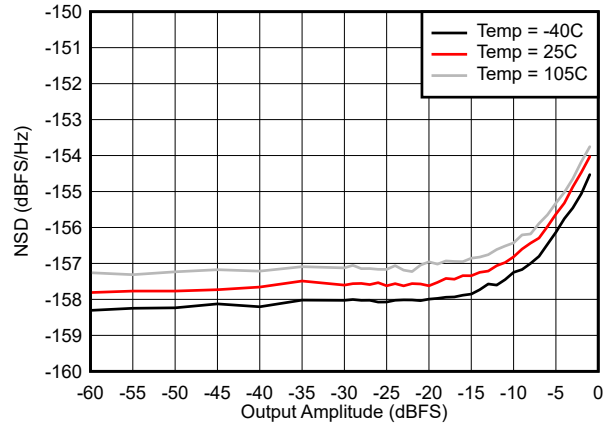
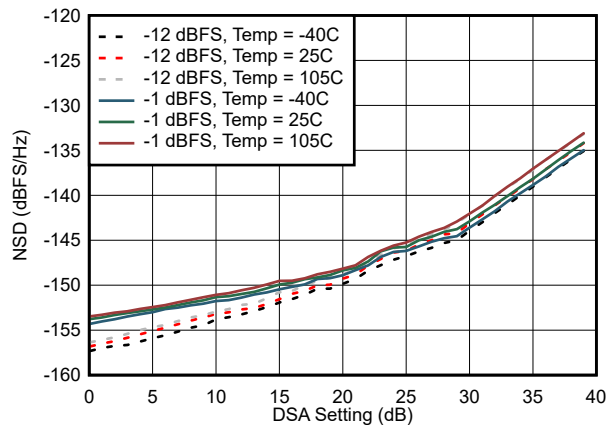


Figure 6-232. Dual Tone Spectrum at 30 MHz and -60d BFS (0 - 100 MHz)



measured at +50 MHz offset

Figure 6-233. Noise Spectral Density vs Digital Amplitude at 30 MHz



measured at +50 MHz offset

Figure 6-234. Noise Spectral Density vs DSA Setting at 30 MHz

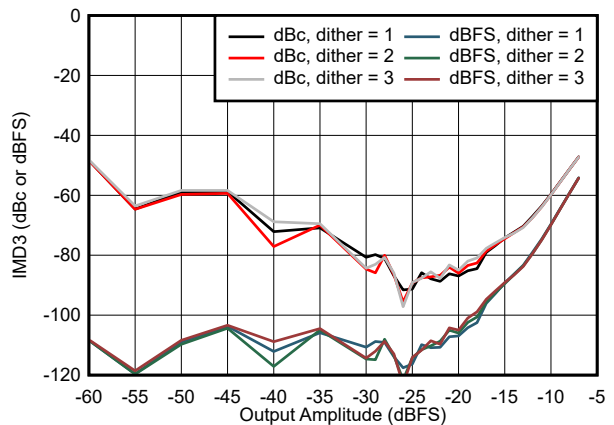


Figure 6-235. IMD3 vs Digital Amplitude at 30 MHz

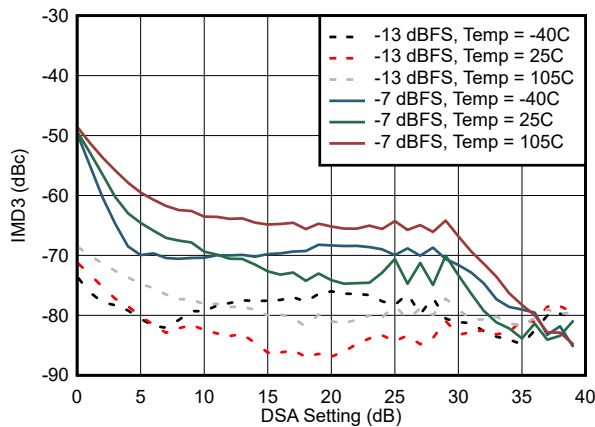


Figure 6-236. IMD3 vs DSA Setting at 30 MHz

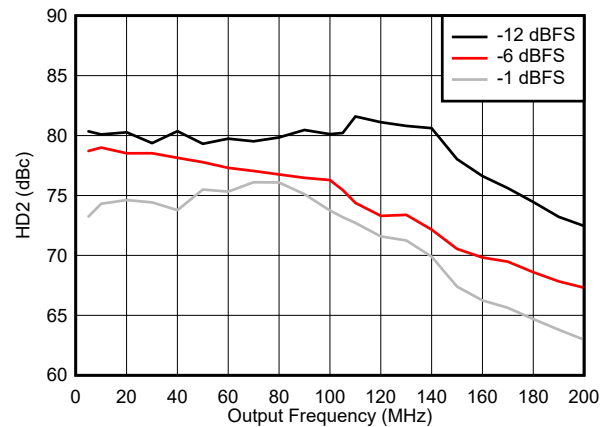


Figure 6-237. HD2 vs Frequency 0 - 200 MHz

### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

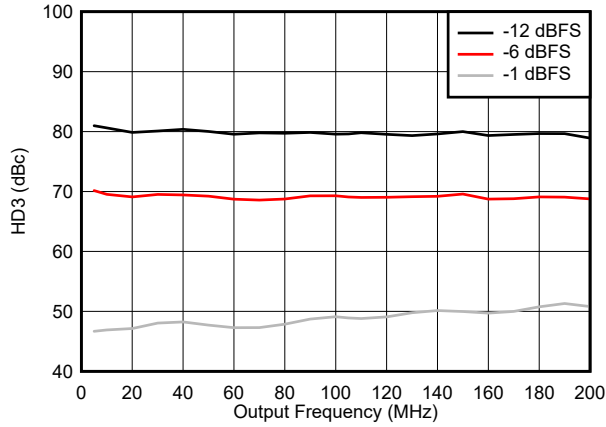
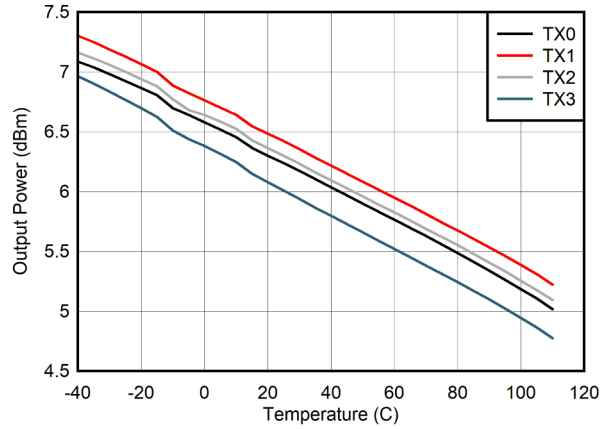
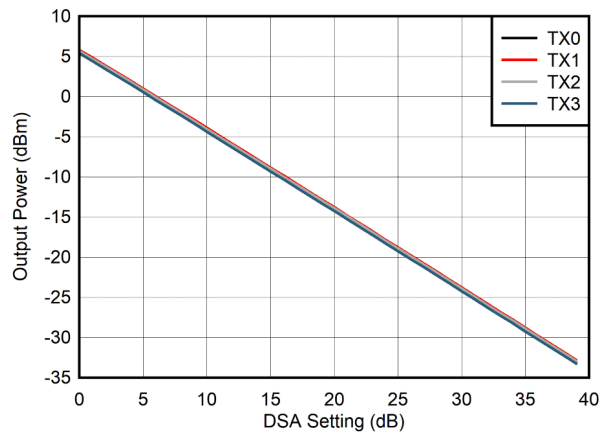


Figure 6-238. HD3 vs Frequency 0 - 200 MHz



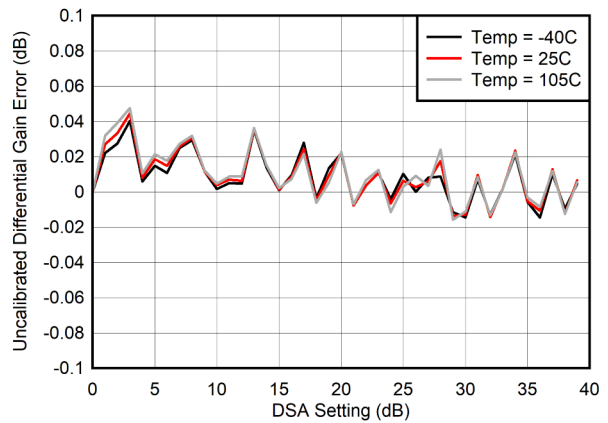
including PCB and cable losses

Figure 6-239. TX Output Fullscale vs Temperature at 400 MHz



including PCB and cable losses

Figure 6-240. TX Output Fullscale vs DSA Setting at 400 MHz



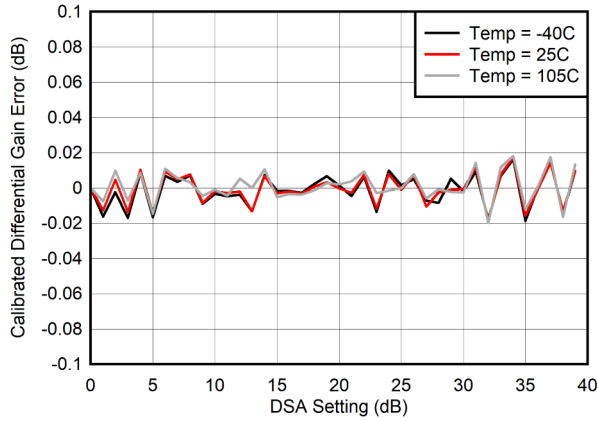
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 6-241. Uncalibrated TX Differential Gain Error (DNL) at 400 MHz



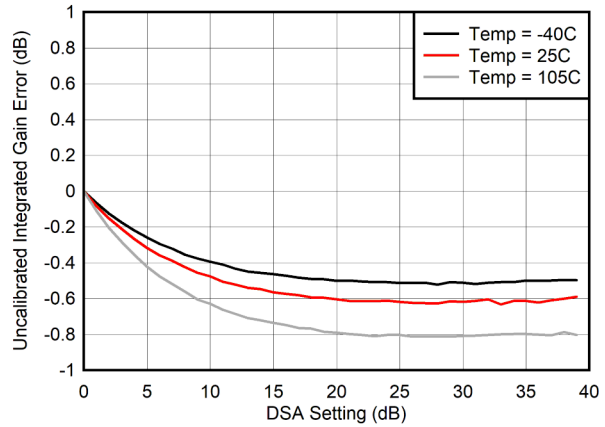
### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



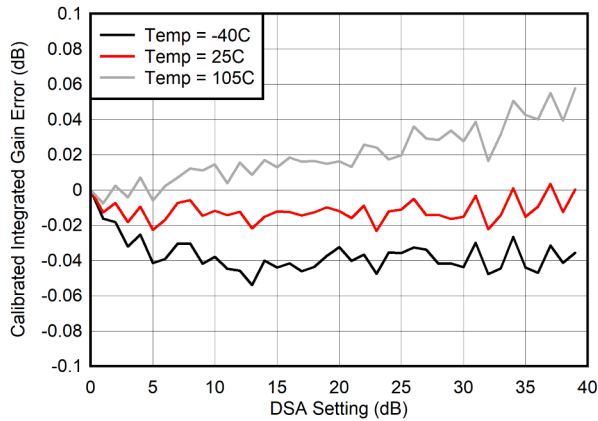
$$\text{Differential Gain Error} = P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$$

Figure 6-242. Calibrated TX Differential Gain Error (DNL) at 400 MHz



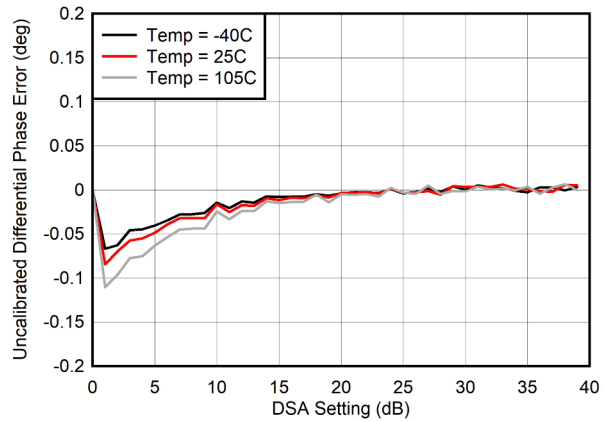
$$\text{Integrated Gain Error} = P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSASetting} = 0) + (\text{DSA Setting})$$

Figure 6-243. Uncalibrated TX Integrated Gain Error (INL) at 400 MHz



$$\text{Integrated Gain Error} = P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSASetting} = 0) + (\text{DSA Setting})$$

Figure 6-244. Calibrated TX Integrated Gain Error (INL) at 400 MHz

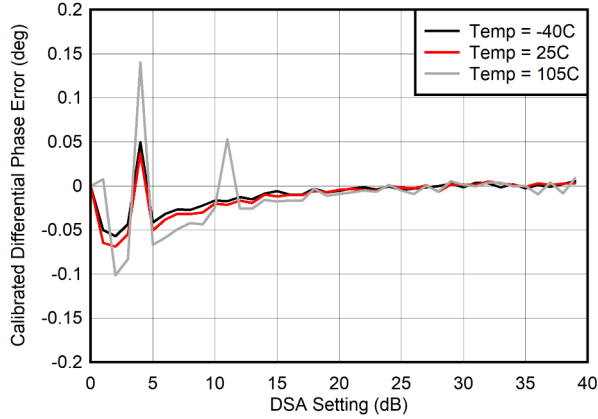


$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

Figure 6-245. Uncalibrated TX Differential Phase Error (DNL) at 400 MHz

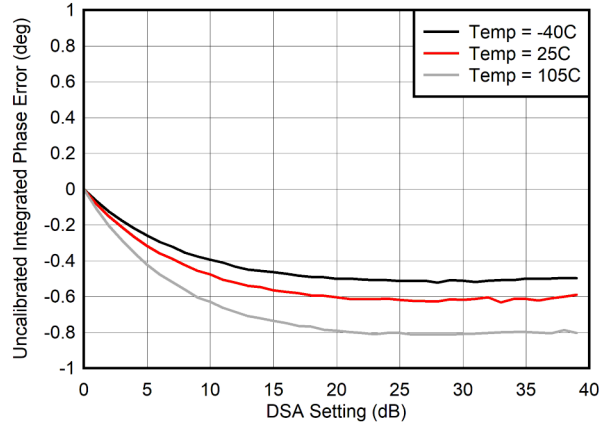
### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



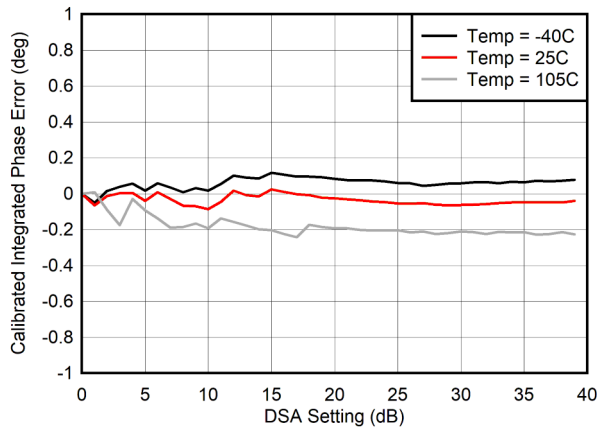
$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

**Figure 6-246. Calibrated TX Differential Phase Error (DNL) at 400 MHz**



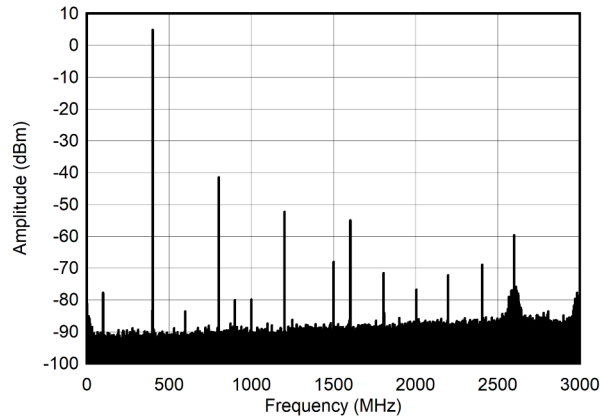
$$\text{Integrated Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSASetting} = 0)$$

**Figure 6-247. Uncalibrated TX Integrated Phase Error (INL) at 400 MHz**



$$\text{Integrated Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSASetting} = 0)$$

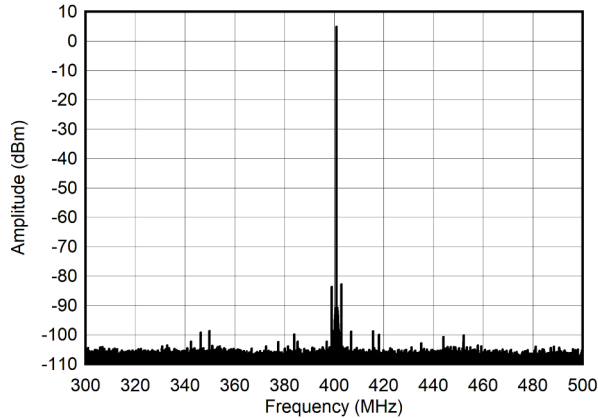
**Figure 6-248. Calibrated TX Integrated Phase Error (INL) at 400 MHz**



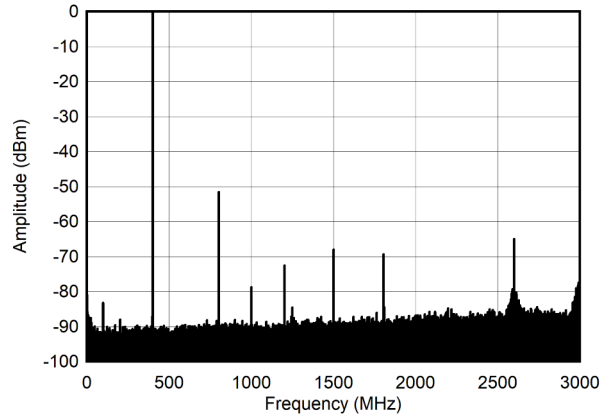
**Figure 6-249. Single Tone Spectrum at 400 MHz and -1 dBFS (Nyquist)**

### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

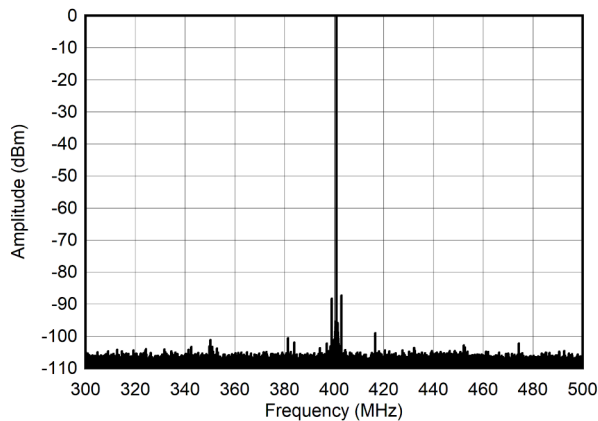
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



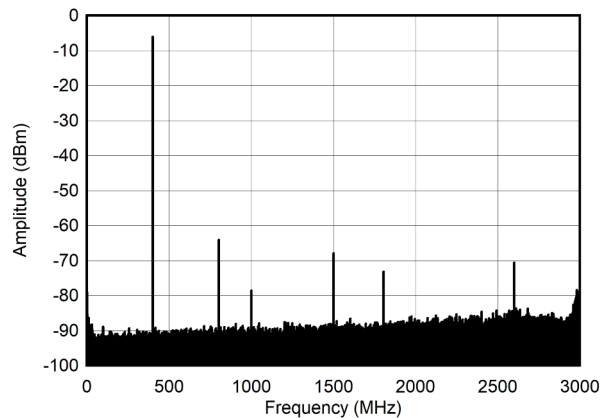
**Figure 6-250. Single Tone Spectrum at 400 MHz and -1 dBFS ( $\pm 100\text{MHz}$ )**



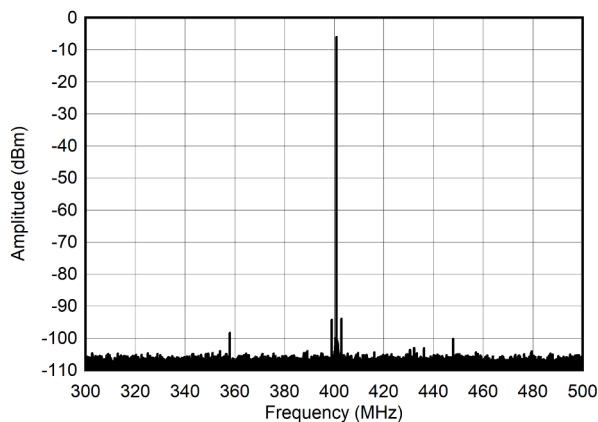
**Figure 6-251. Single Tone Spectrum at 400 MHz and -6 dBFS (Nyquist)**



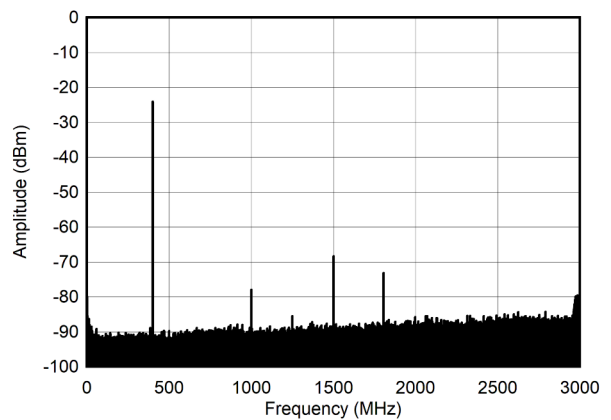
**Figure 6-252. Single Tone Spectrum at 400 MHz and -6 dBFS ( $\pm 100\text{MHz}$ )**



**Figure 6-253. Single Tone Spectrum at 400 MHz and -12 dBFS (Nyquist)**



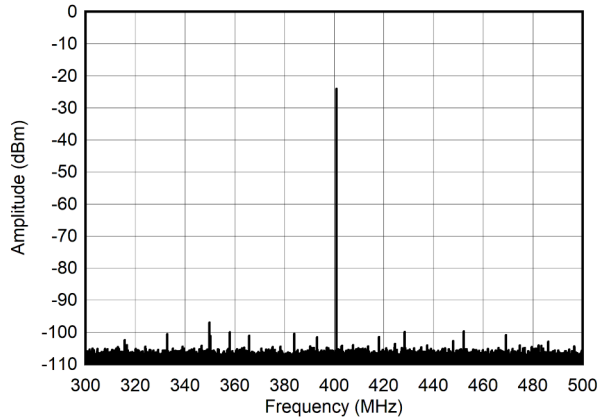
**Figure 6-254. Single Tone Spectrum at 400 MHz and -12 dBFS ( $\pm 100\text{MHz}$ )**



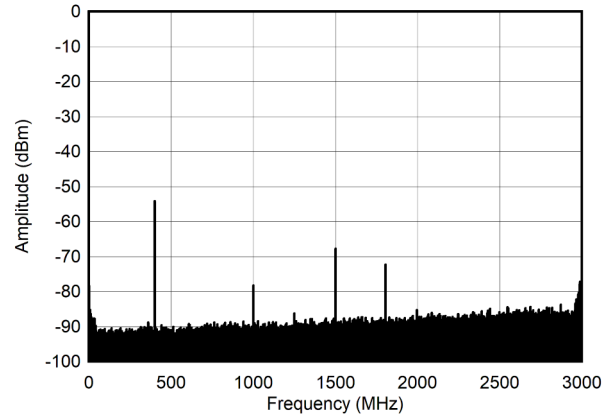
**Figure 6-255. Single Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)**

### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

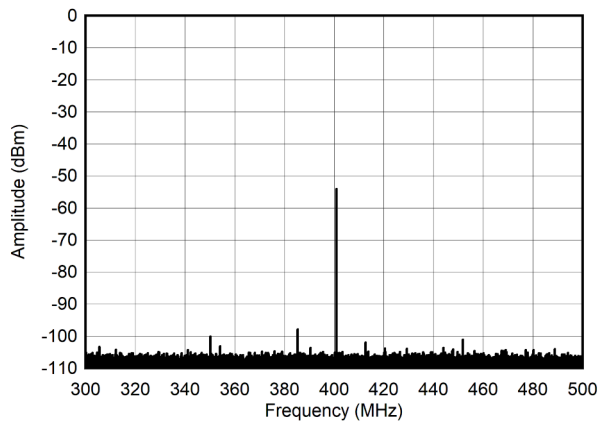
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



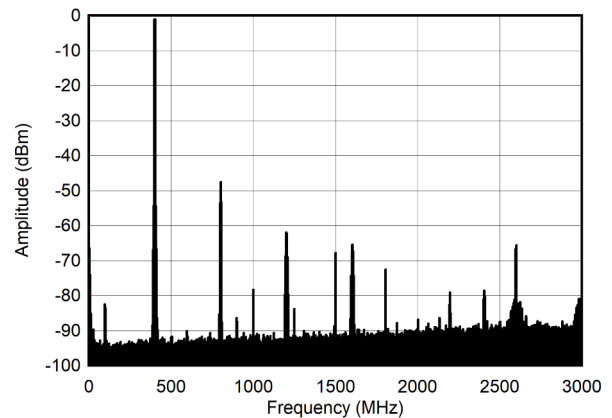
**Figure 6-256. Single Tone Spectrum at 400 MHz and -30 dBFS ( $\pm 100\text{MHz}$ )**



**Figure 6-257. Single Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)**



**Figure 6-258. Single Tone Spectrum at 400 MHz and -60 dBFS ( $\pm 100\text{MHz}$ )**

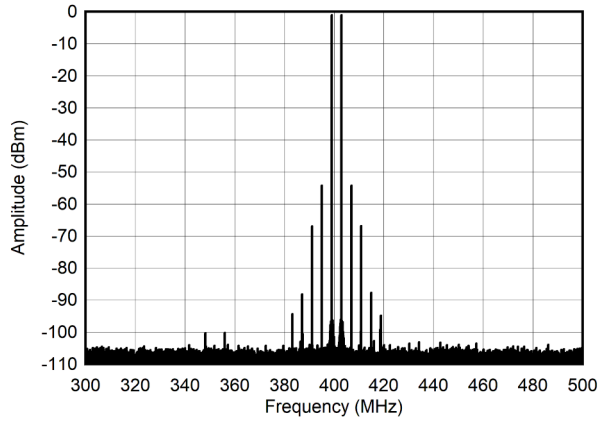


Tone Spacing = 4 MHz

**Figure 6-259. Dual Tone Spectrum at 400 MHz and -7 dBFS (Nyquist)**

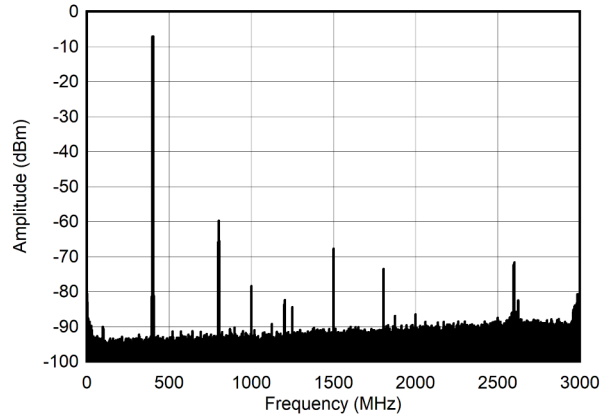
### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



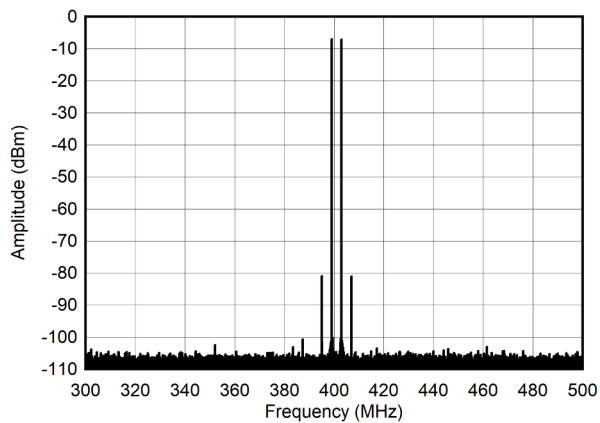
Tone Spacing = 4 MHz

**Figure 6-260. Dual Tone Spectrum at 400 MHz and -7 dBFS (±100MHz)**



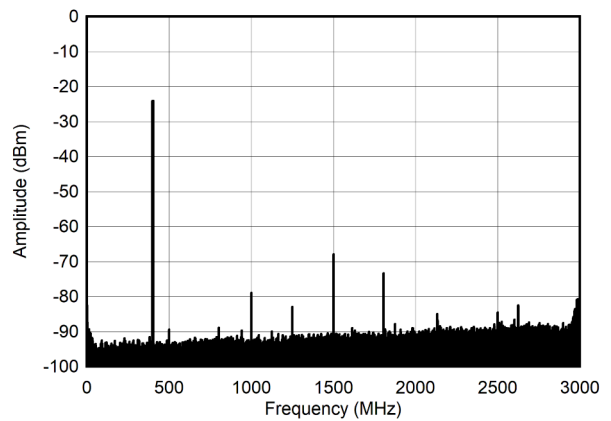
Tone Spacing = 4 MHz

**Figure 6-261. Dual Tone Spectrum at 400 MHz and -13 dBFS (Nyquist)**



Tone Spacing = 4 MHz

**Figure 6-262. Dual Tone Spectrum at 400 MHz and -13 dBFS (±100MHz)**

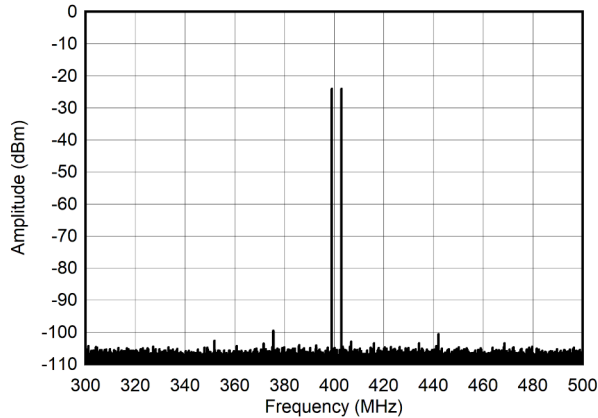


Tone Spacing = 4 MHz

**Figure 6-263. Dual Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)**

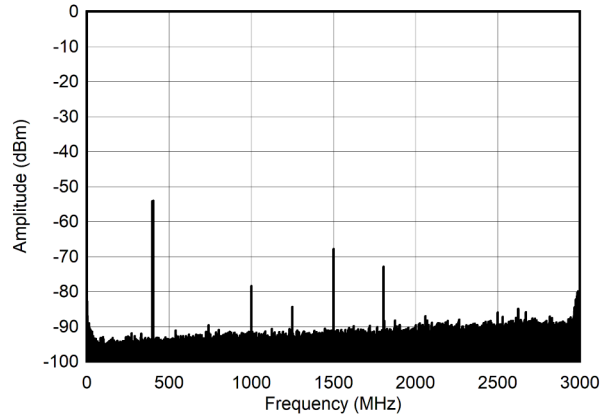
### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{DAC} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 500$  MHz. Additional default conditions for all plots,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



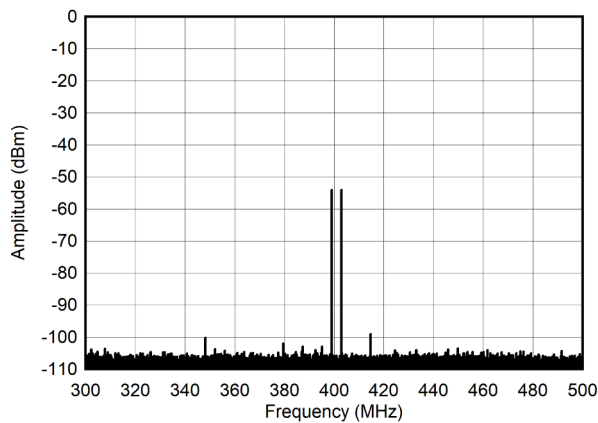
Tone Spacing = 4 MHz

Figure 6-264. Dual Tone Spectrum at 400 MHz and -30 dBFS (±100MHz)



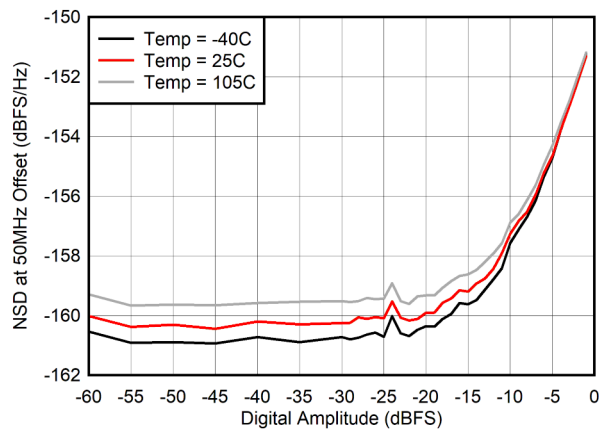
Tone Spacing = 4 MHz

Figure 6-265. Dual Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)



Tone Spacing = 4 MHz

Figure 6-266. Dual Tone Spectrum at 400 MHz and -60 dBFS (±100MHz)

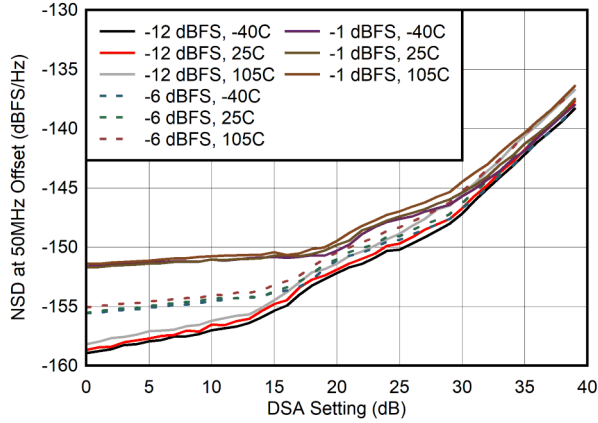


measured at 50 MHz offset

Figure 6-267. Noise Spectral Density vs Digital Amplitude at 400 MHz

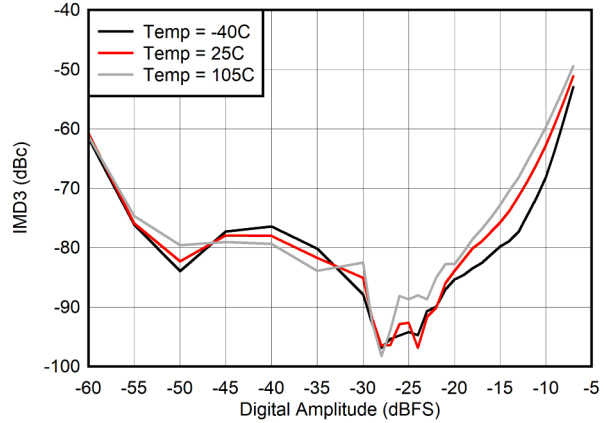
### 6.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 125 MSPS,  $f_{\text{DAC}} = 6000$  MSPS (48x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 500$  MHz. Additional default conditions for all plots,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



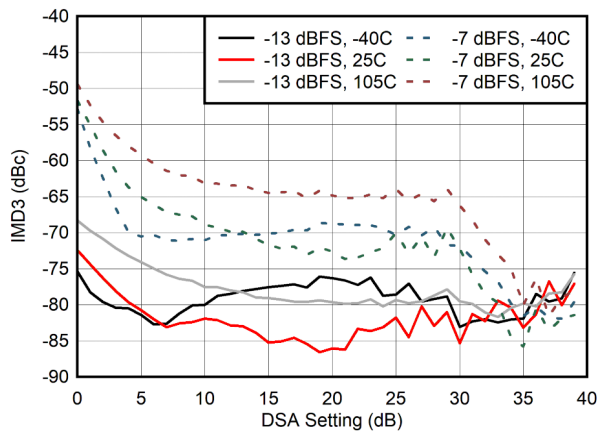
measured at 50 MHz offset

**Figure 6-268. Noise Spectral Density vs DSA Setting at 400 MHz**



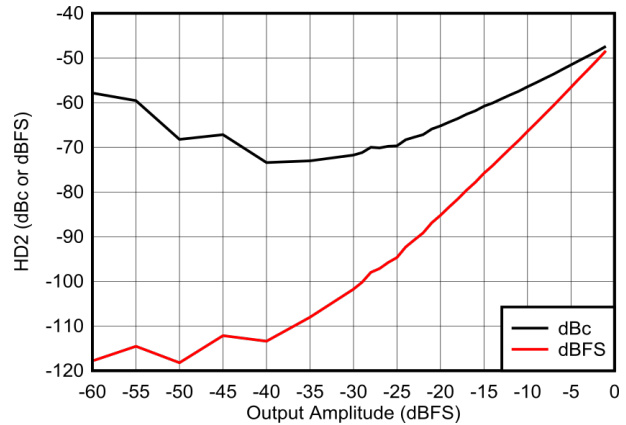
Tone Spacing = 4 MHz

**Figure 6-269. IMD3 vs Digital Amplitude at 400 MHz**

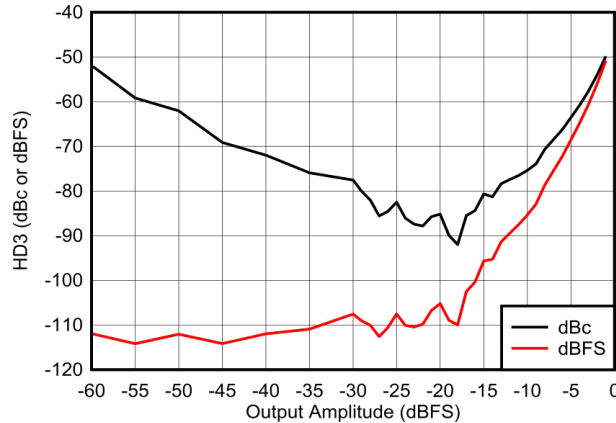


Tone Spacing = 4 MHz

**Figure 6-270. IMD3 vs DSA Setting at 400 MHz**



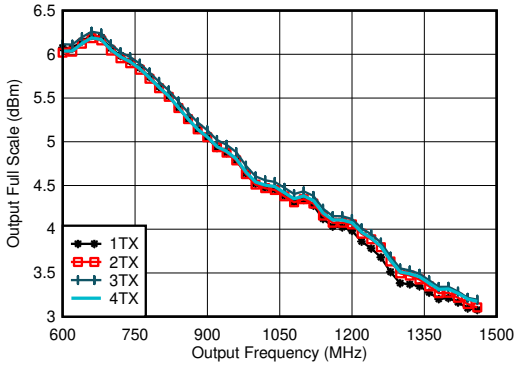
**Figure 6-271. HD2 vs Amplitude at 400 MHz**



**Figure 6-272. HD3 vs Amplitude at 400 MHz**

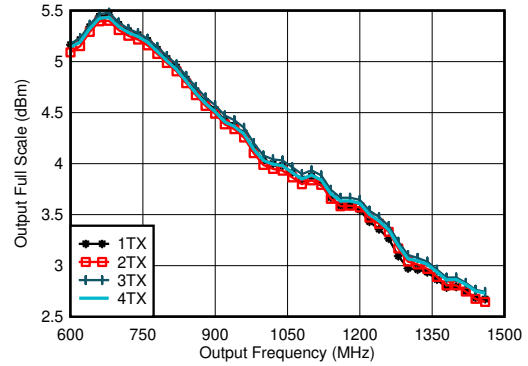
### 6.12.8 TX Typical Characteristics at 800MHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{REF} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



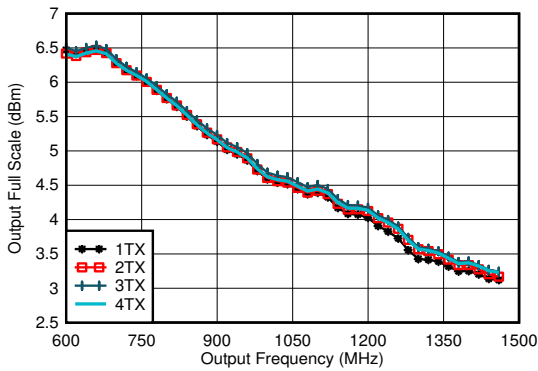
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 0.8 GHz matching

**Figure 6-273. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode**



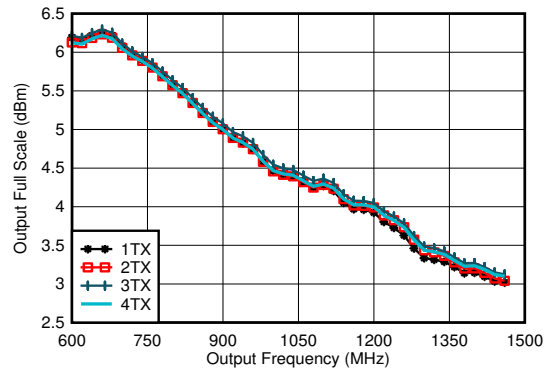
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 0.8 GHz matching

**Figure 6-274. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode**



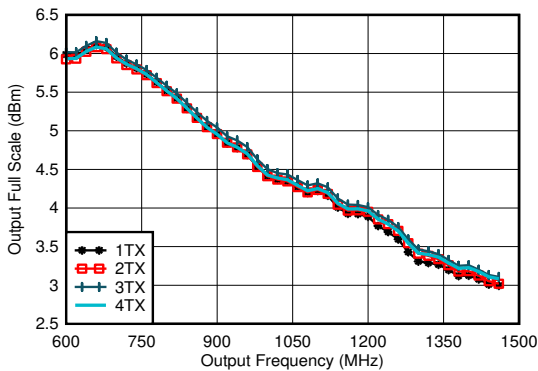
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 0.8 GHz matching

**Figure 6-275. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Interleave Mode**



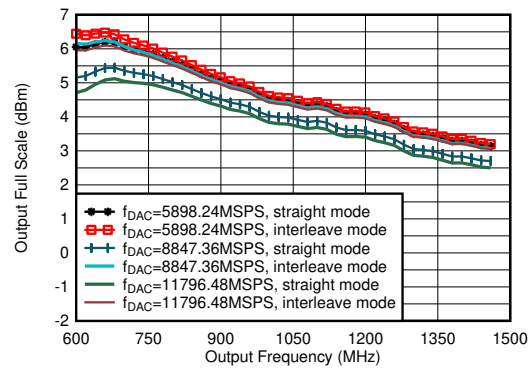
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 0.8 GHz matching

**Figure 6-276. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Interleave Mode**



Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 0.8 GHz matching

**Figure 6-277. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS, Interleave Mode**



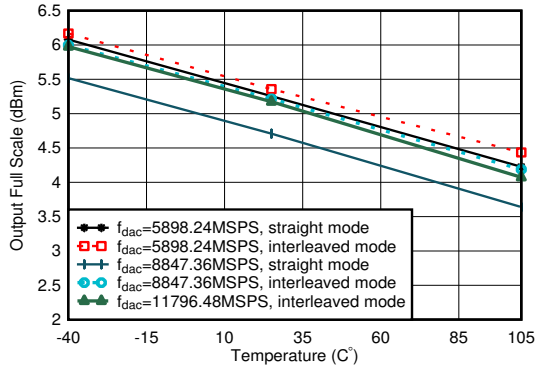
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 0.8 GHz matching

**Figure 6-278. TX Output Fullscale vs Output Frequency**



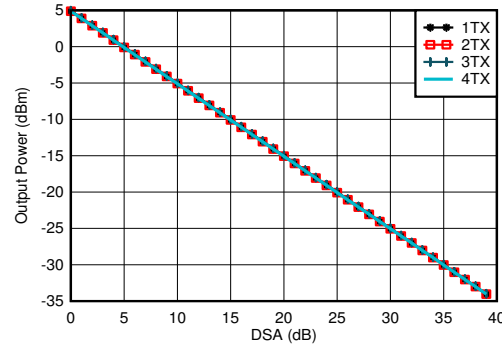
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



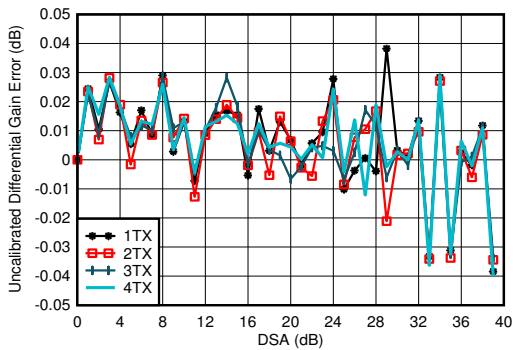
including PCB and cable losses,  $A_{\text{out}} = -0.5\text{dFBS}$ , DSA = 0, 0.8 GHz matching

**Figure 6-279. TX Output Fullscale vs Temperature**



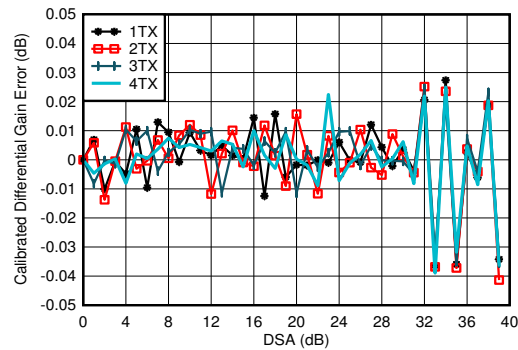
$f_{\text{DAC}} = 11796.48\text{ MSPS}$ , interleave mode,  $A_{\text{out}} = -0.5\text{dFBS}$ , matching 0.8 GHz

**Figure 6-280. TX Output Power vs DSA Setting and Channel at 0.85 GHz**



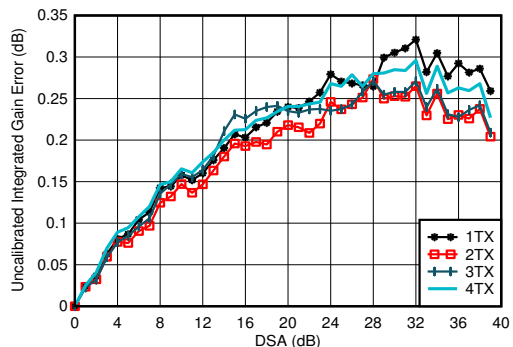
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-281. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz**



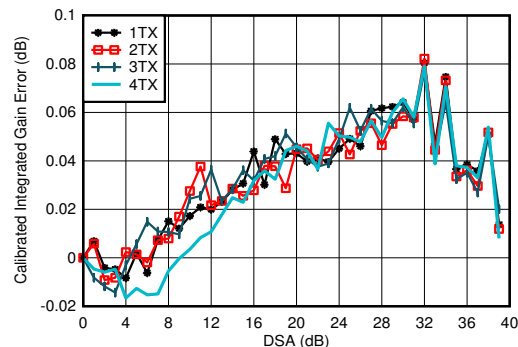
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-282. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Settings}$

**Figure 6-283. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz**

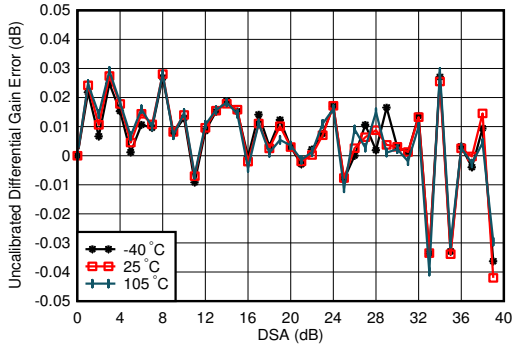


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 6-284. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz**

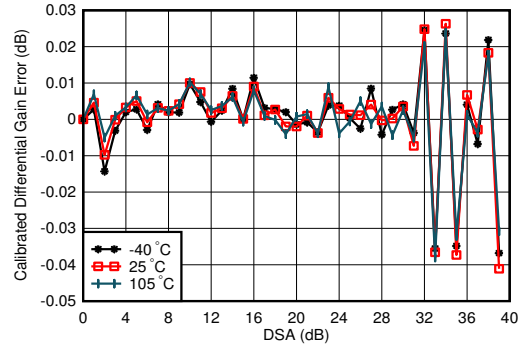
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



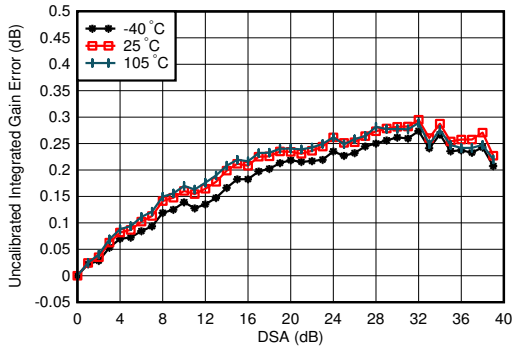
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-285. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz**



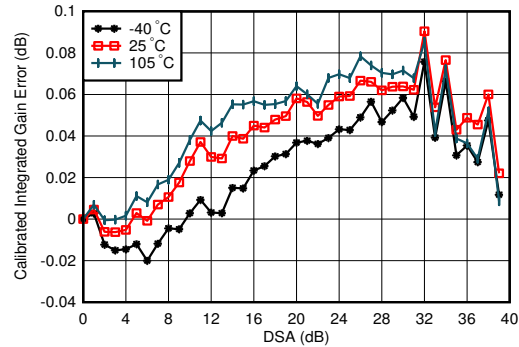
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-286. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz**



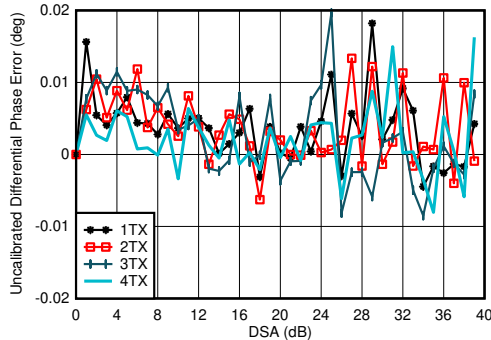
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 6-287. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz**



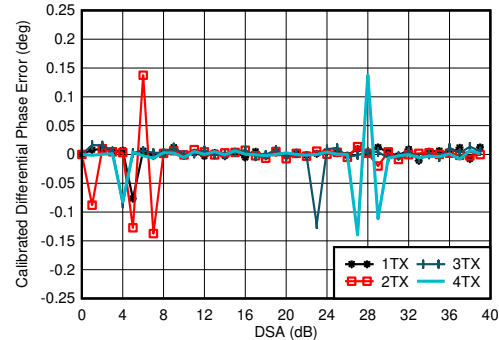
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 6-288. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-289. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz**

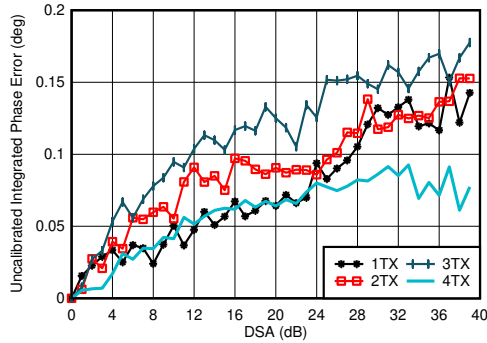


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
 Phase DNL spike may occur at any DSA setting.

**Figure 6-290. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz**

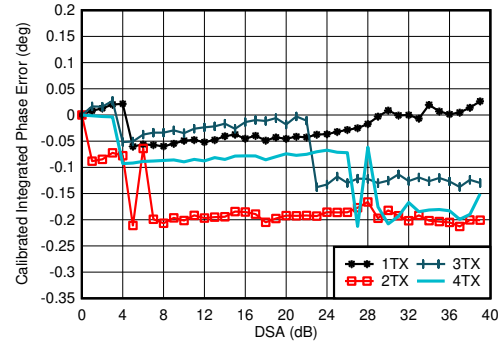
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



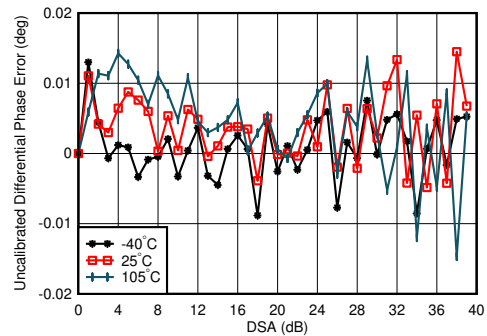
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 6-291. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz**



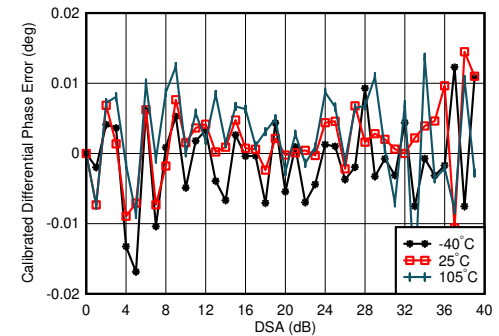
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 6-292. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz**



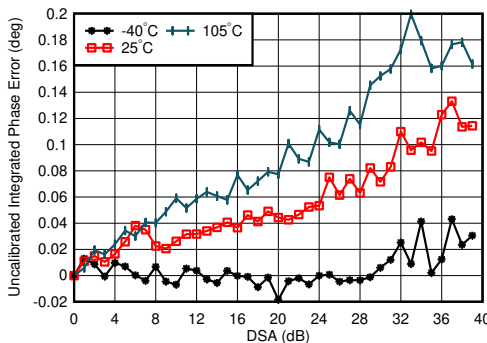
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} + 1)$

**Figure 6-293. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz**



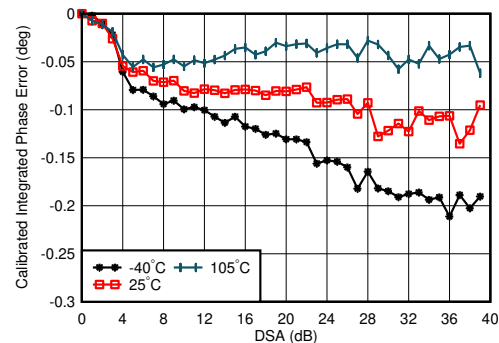
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} + 1)$

**Figure 6-294. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 6-295. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz**

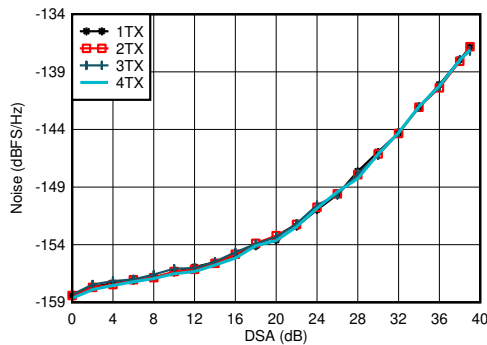


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 6-296. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz**

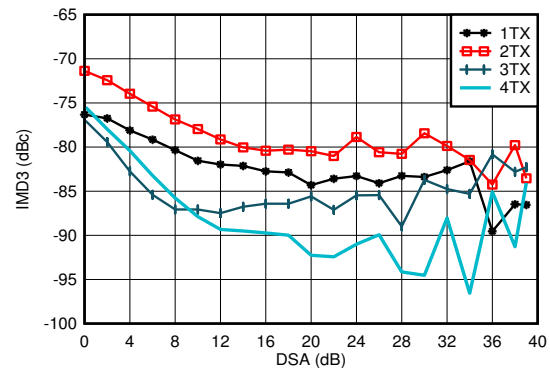
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



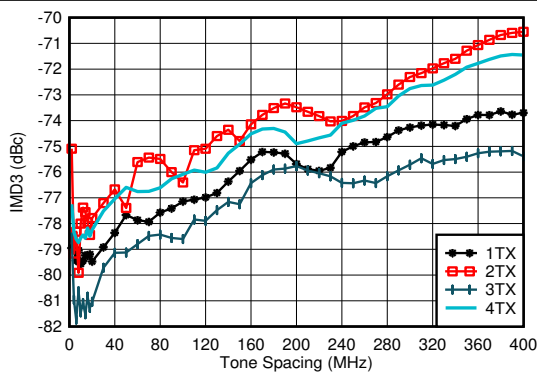
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8 GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

**Figure 6-297. TX Output Noise vs Channel and Attenuation at 0.85 GHz**



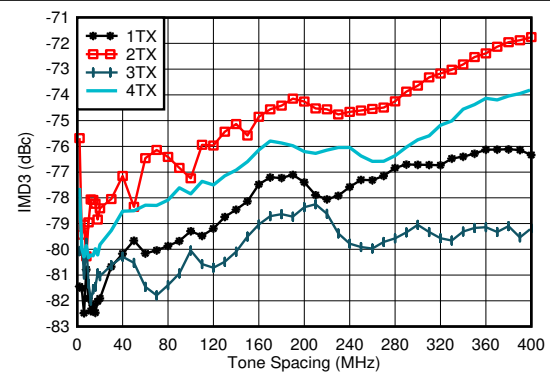
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ , matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone

**Figure 6-298. TX IMD3 vs DSA Setting at 0.85 GHz**



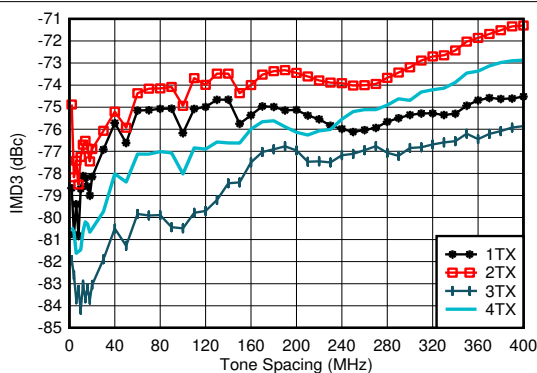
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ , matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone

**Figure 6-299. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz**



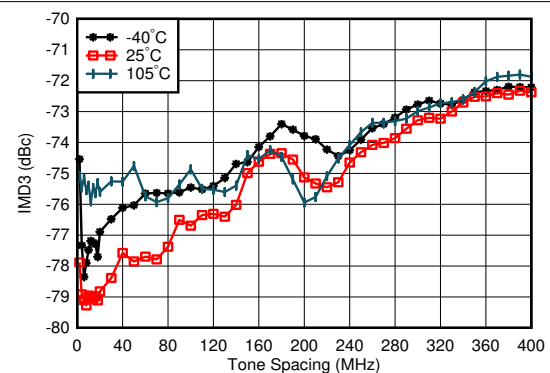
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ , matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone

**Figure 6-300. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ , matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone

**Figure 6-301. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz**

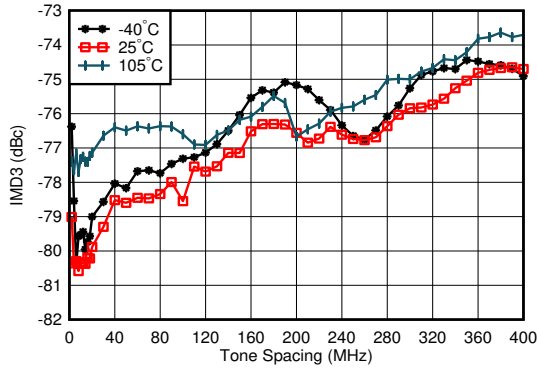


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ , matching at 0.8 GHz,  $-13\text{ dBFS}$  each tone, worst channel

**Figure 6-302. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz**

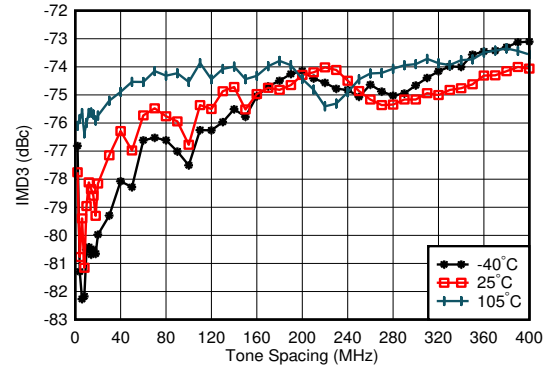
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



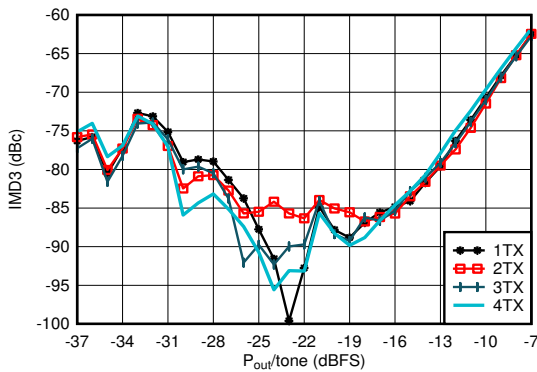
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone, worst channel

**Figure 6-303. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz**



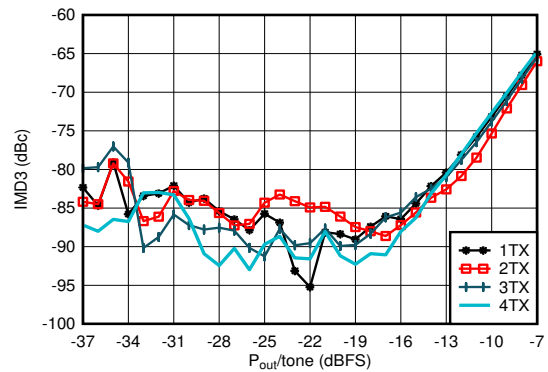
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ , matching at 0.8 GHz, -13 dBFS each tone, worst channel

**Figure 6-304. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz**



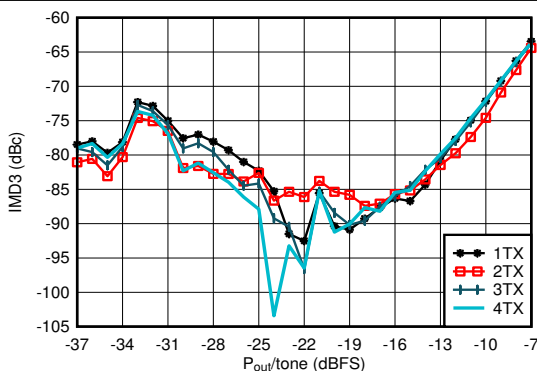
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ ,  $f_{\text{SPACING}} = 20\text{ MHz}$ , matching at 0.8 GHz

**Figure 6-305. TX IMD3 vs Digital Level at 0.85 GHz**



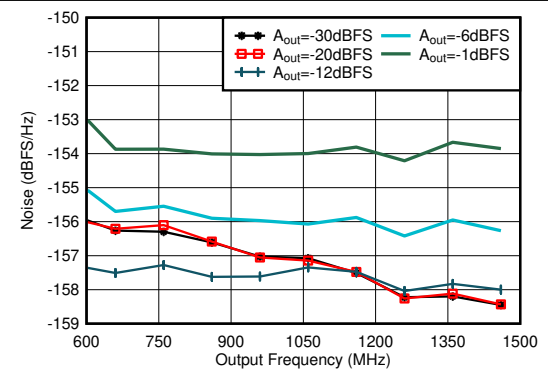
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ ,  $f_{\text{SPACING}} = 20\text{ MHz}$ , matching at 0.8 GHz

**Figure 6-306. TX IMD3 vs Digital Level at 0.85 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 0.85\text{ GHz}$ ,  $f_{\text{SPACING}} = 20\text{ MHz}$ , matching at 0.8 GHz

**Figure 6-307. TX IMD3 vs Digital Level at 0.85 GHz**

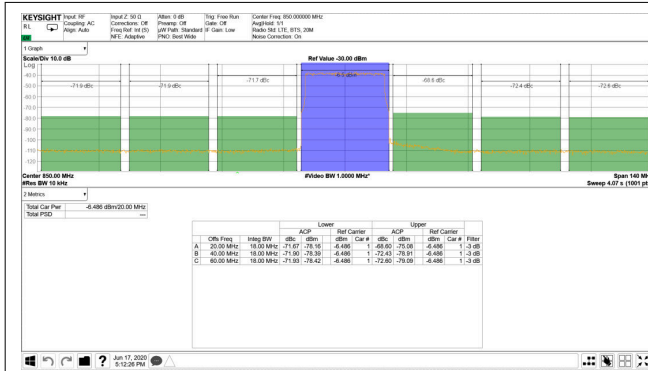


Matching at 0.8 GHz, Single tone,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset, DSA = 0dB

**Figure 6-308. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz**

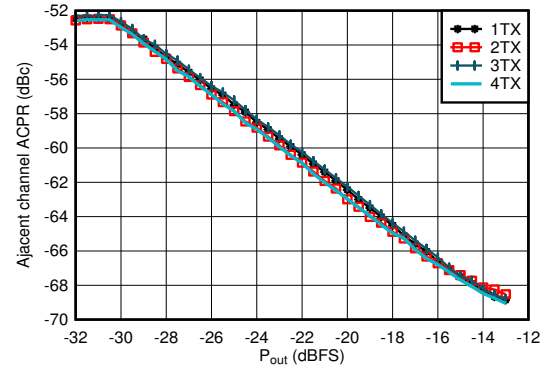
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



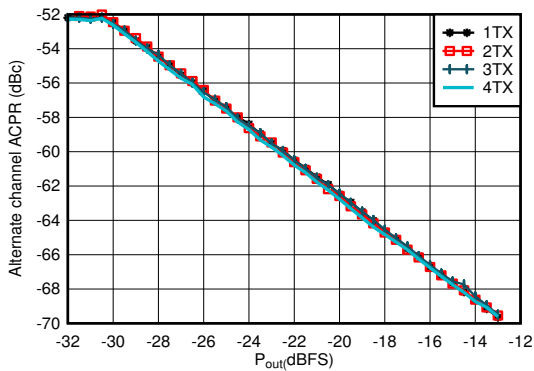
TM1.1,  $P_{\text{OUT,RMS}} = -13\text{ dBFS}$

**Figure 6-309. TX 20-MHz LTE Output Spectrum at 0.85 GHz**



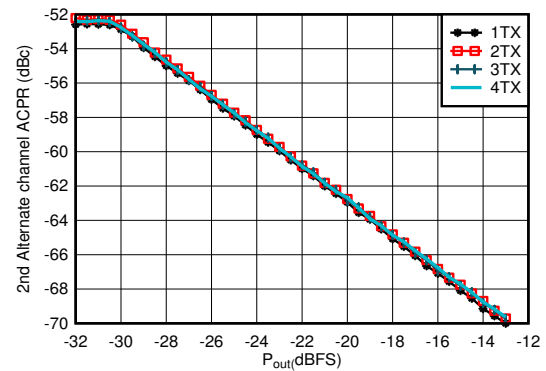
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-310. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz**



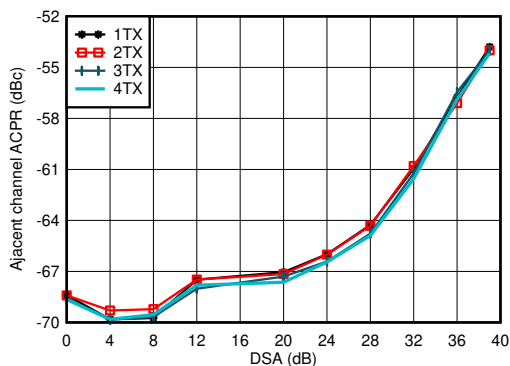
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-311. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz**



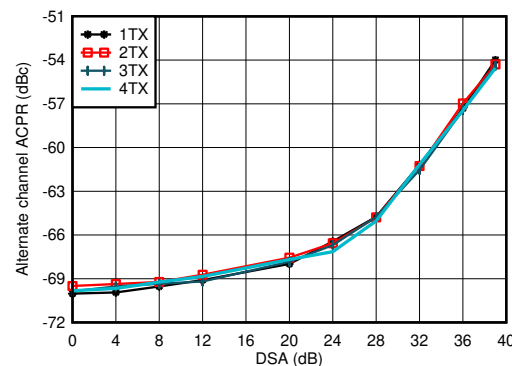
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-312. TX 20-MHz LTE alt2-ACPR vs Digital Level at 0.85 GHz**



Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-313. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz**



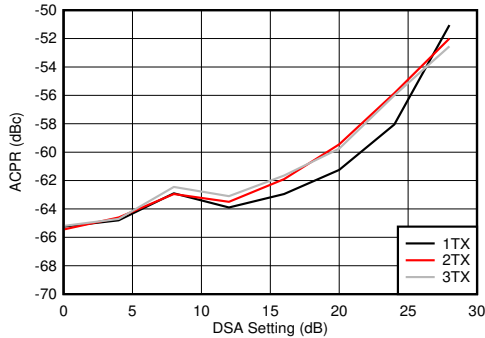
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-314. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz**

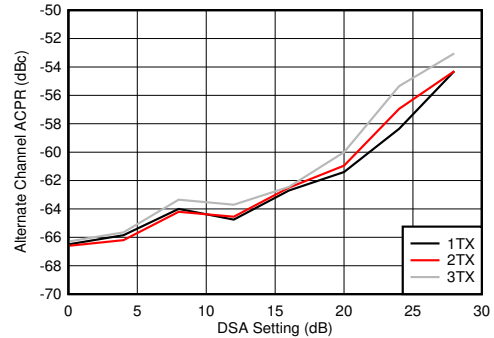


### 6.12.8 TX Typical Characteristics at 800MHz (continued)

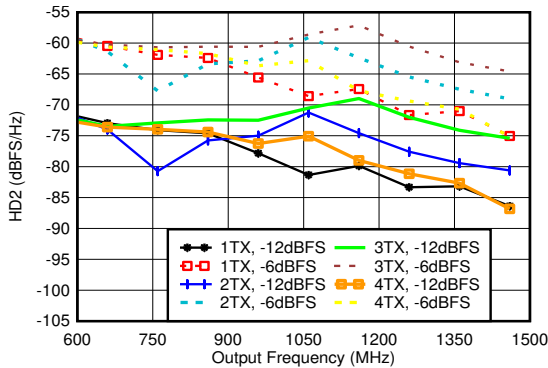
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



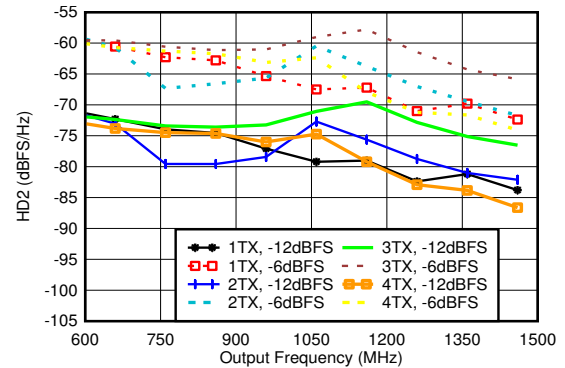
Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR  
**Figure 6-315. TX 100-MHz NR ACPR vs DSA at 0.85 GHz**



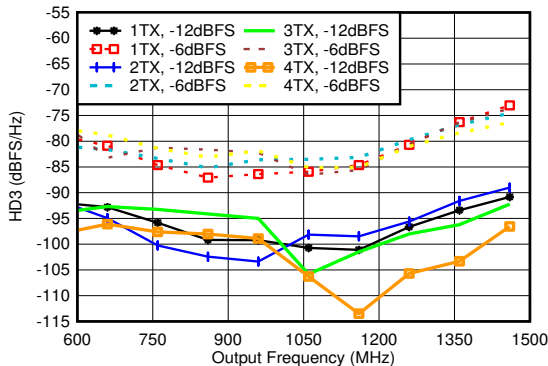
Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR  
**Figure 6-316. TX 100-MHz NR alt-ACPR vs DSA at 0.85 GHz**



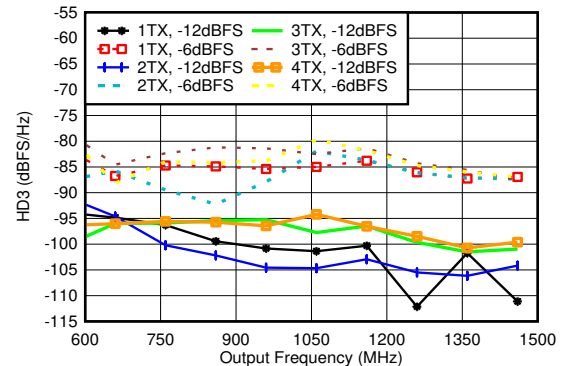
Matching at 0.8 GHz,  $f_{\text{DAC}} = 5898.24\text{GSPS}$ , straight mode  
**Figure 6-317. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz**



Matching at 0.8 GHz,  $f_{\text{DAC}} = 8847.36\text{GSPS}$ , straight mode  
**Figure 6-318. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz**



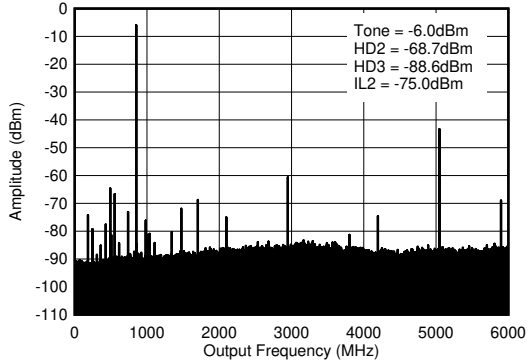
Matching at 0.8 GHz,  $f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode, normalized to output power at harmonic frequency  
**Figure 6-319. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz**



Matching at 0.8 GHz,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, normalized to output power at harmonic frequency  
**Figure 6-320. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz**

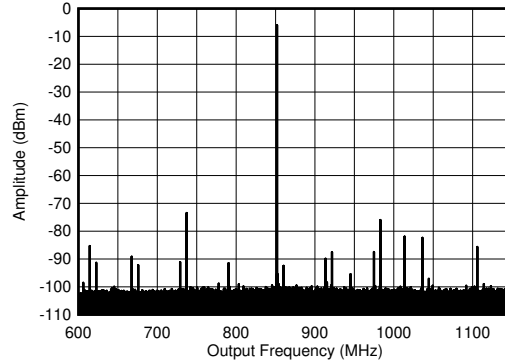
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



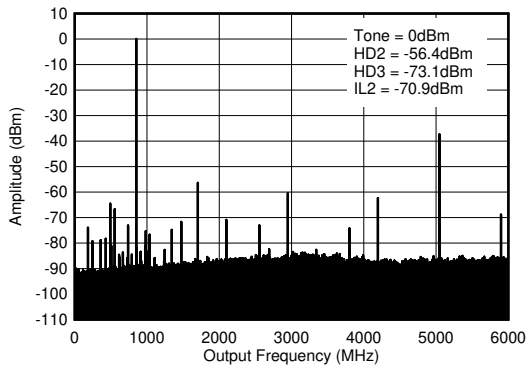
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-321. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**



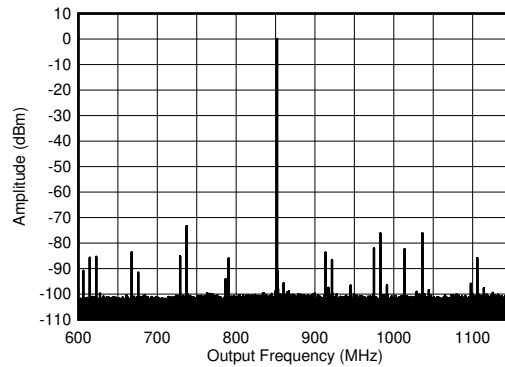
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses

**Figure 6-322. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ( $\pm 300\text{ MHz}$ )**



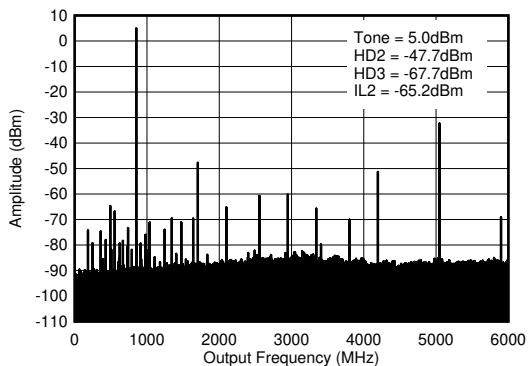
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-323. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**



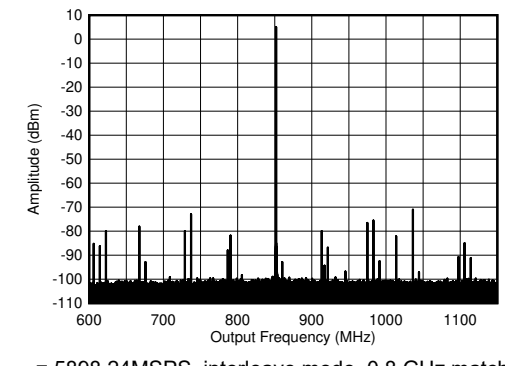
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses

**Figure 6-324. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ( $\pm 300\text{ MHz}$ )**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-325. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**



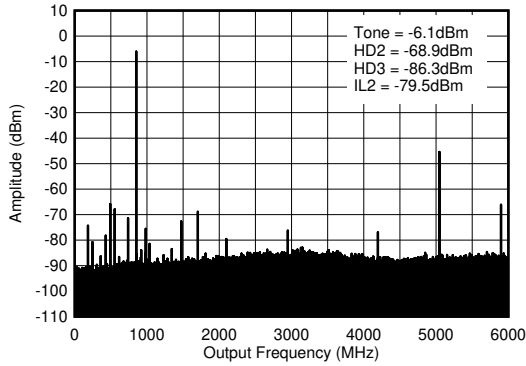
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, 0.8 GHz matching, includes PCB and cable losses

**Figure 6-326. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ( $\pm 300\text{ MHz}$ )**



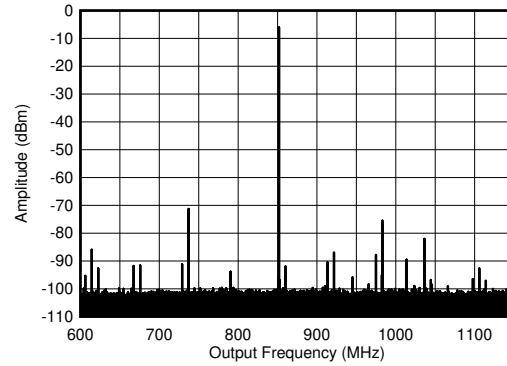
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



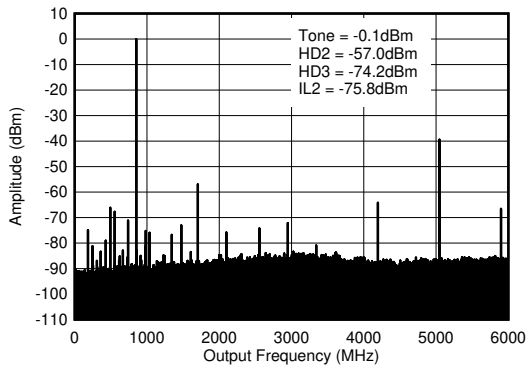
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-327. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**



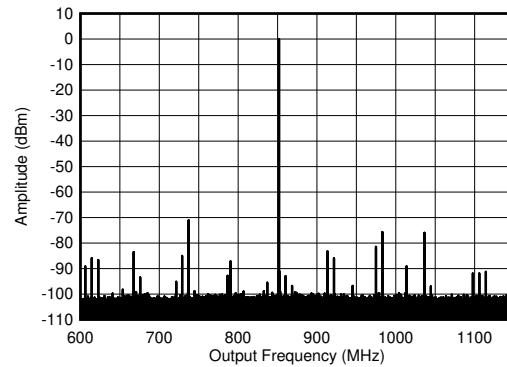
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode, 0.8 GHz matching, includes PCB and cable losses

**Figure 6-328. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ( $\pm 300\text{ MHz}$ )**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-329. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**

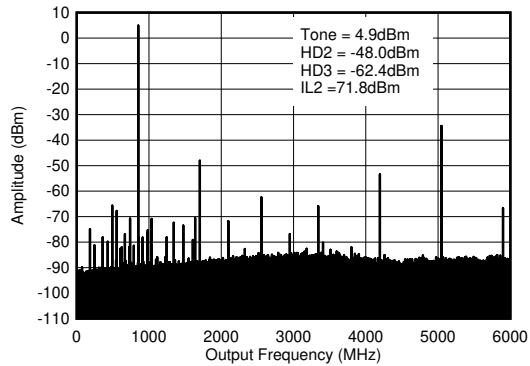


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode, 0.8 GHz matching, includes PCB and cable losses

**Figure 6-330. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ( $\pm 300\text{ MHz}$ )**

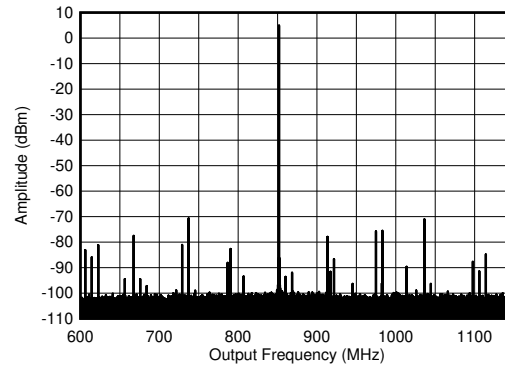
### 6.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-331. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**

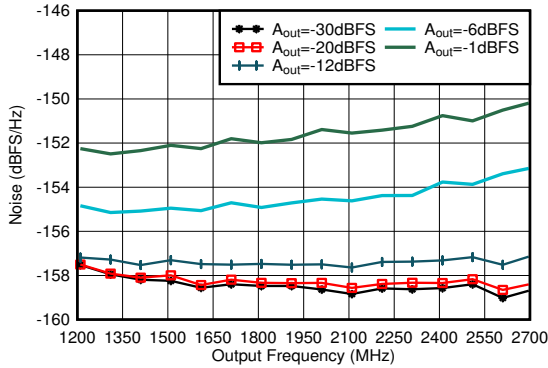


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode, 0.8 GHz matching, includes PCB and cable losses

**Figure 6-332. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ( $\pm 300\text{ MHz}$ )**

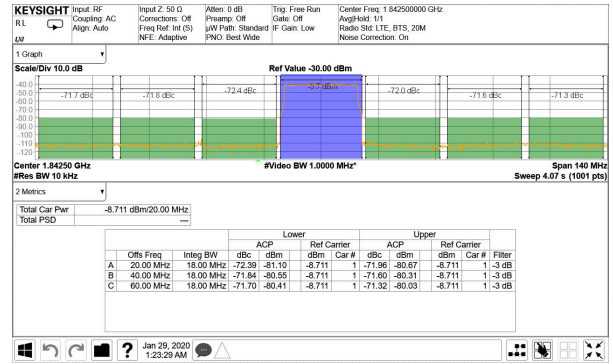
### 6.12.9 TX Typical Characteristics at 1.8GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



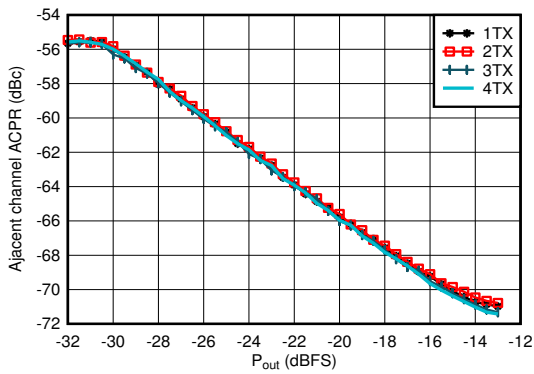
Matching at 2.6 GHz, Single tone,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset

Figure 6-333. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz



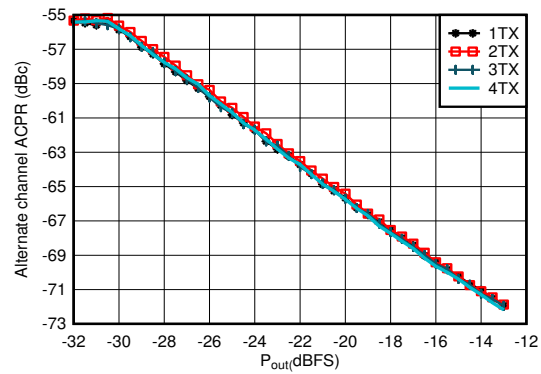
TM1.1,  $P_{\text{OUT\_RMS}} = -13\text{dBFS}$

Figure 6-334. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



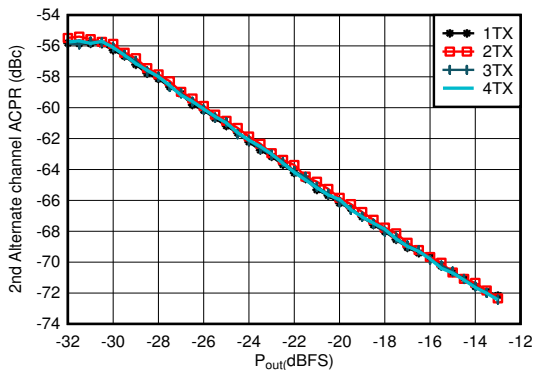
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 6-335. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



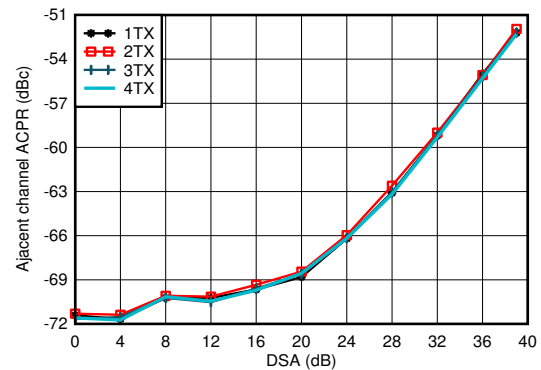
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 6-336. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 6-337. TX 20-MHz LTE alt2-ACPR vs Digital Level at 1.8425 GHz

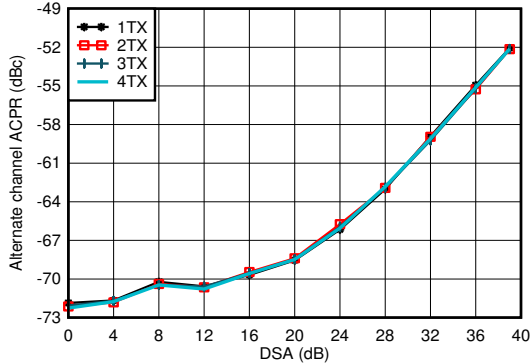


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

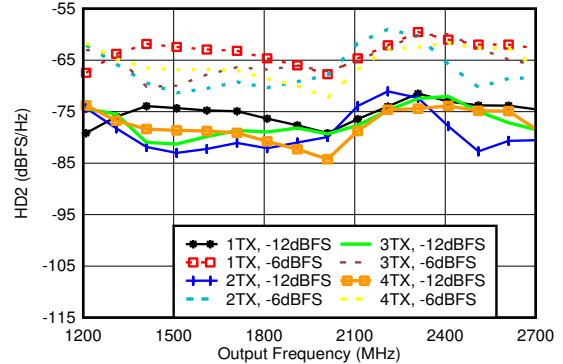
Figure 6-338. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz

**6.12.9 TX Typical Characteristics at 1.8GHz (continued)**

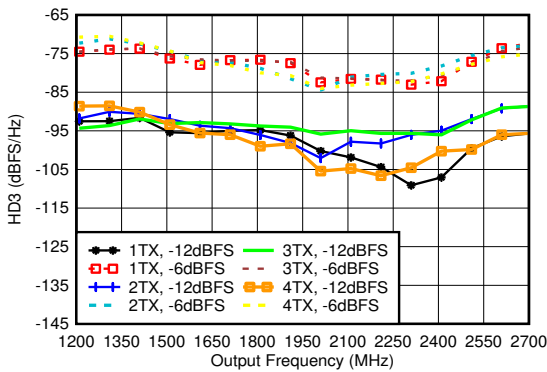
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



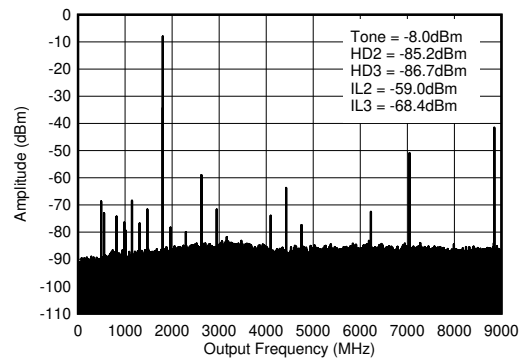
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE  
**Figure 6-339. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz**



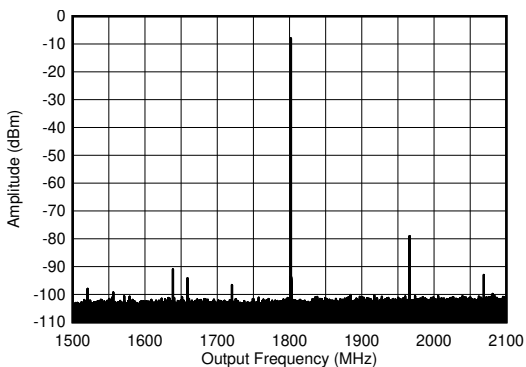
Matching at 1.8 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency  
**Figure 6-340. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz**



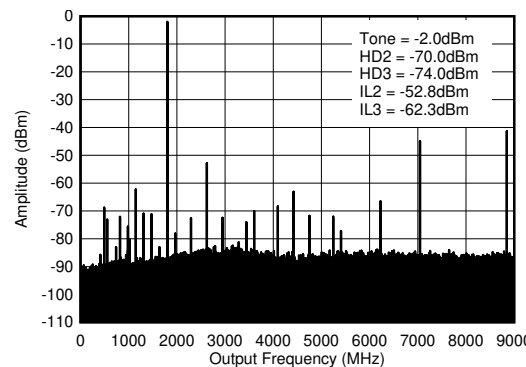
Matching at 1.8 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency  
**Figure 6-341. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .  
**Figure 6-342. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{\text{DAC}}$ )**



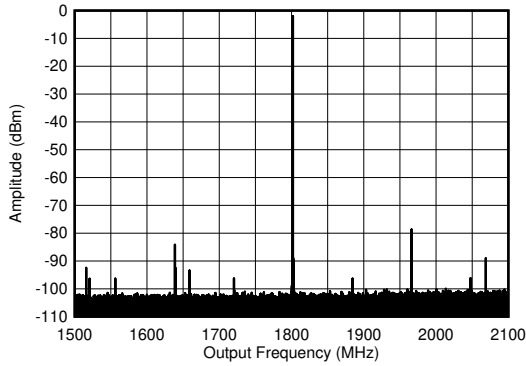
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode, 1.8 GHz matching, includes PCB and cable losses  
**Figure 6-343. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ( $\pm 300\text{ MHz}$ )**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .  
**Figure 6-344. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{\text{DAC}}$ )**

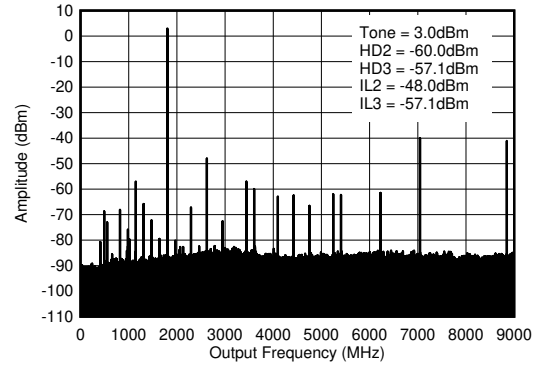
### 6.12.9 TX Typical Characteristics at 1.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



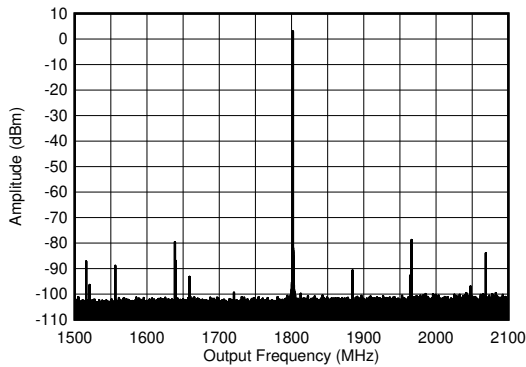
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode, 1.8 GHz matching, includes PCB and cable losses

**Figure 6-345. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ( $\pm 300\text{ MHz}$ )**



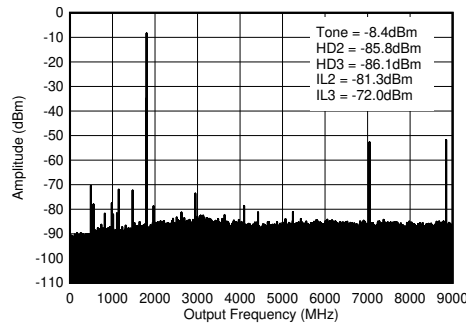
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-346. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{\text{DAC}}$ )**



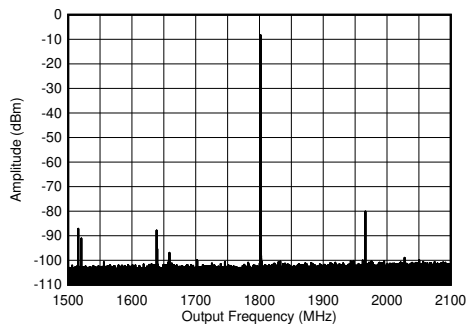
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode, 1.8 GHz matching, includes PCB and cable losses

**Figure 6-347. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ( $\pm 300\text{ MHz}$ )**



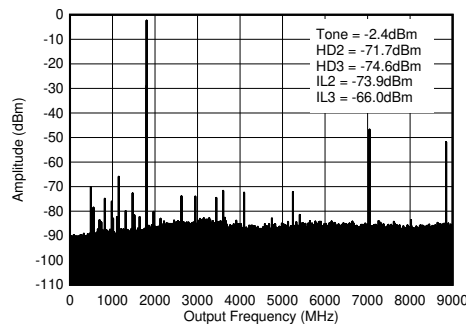
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-348. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{\text{DAC}}$ )**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses

**Figure 6-349. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ( $\pm 300\text{ MHz}$ )**

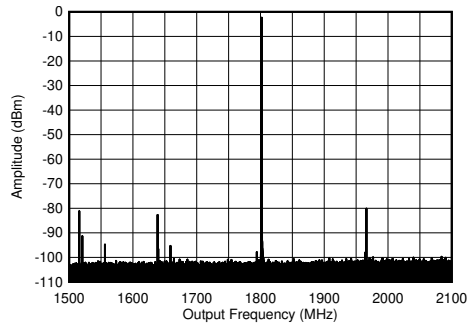


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-350. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{\text{DAC}}$ )**

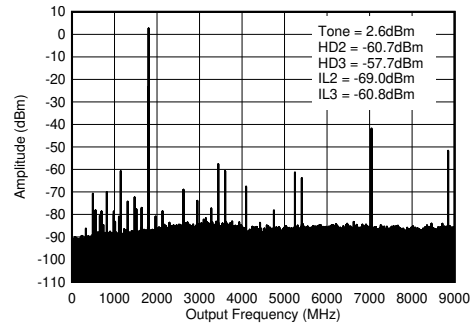
### 6.12.9 TX Typical Characteristics at 1.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



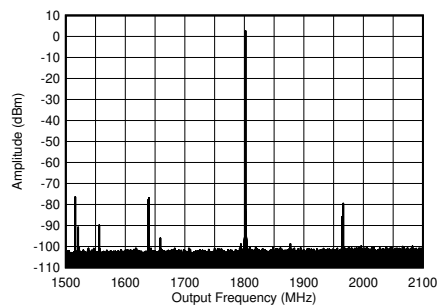
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses

**Figure 6-351. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ( $\pm 300$  MHz)**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_{\text{sig}}/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-352. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{\text{DAC}}$ )**

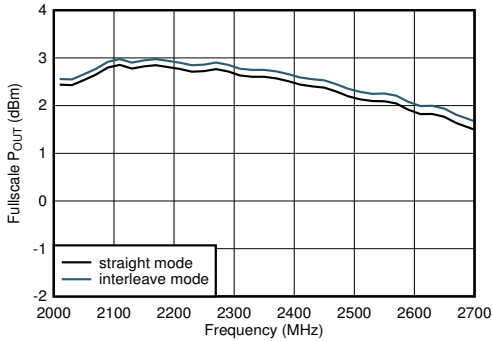


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8 GHz matching, includes PCB and cable losses

**Figure 6-353. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ( $\pm 300$  MHz)**

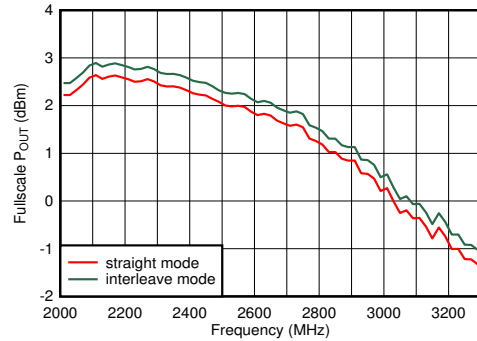
### 6.12.10 TX Typical Characteristics at 2.6GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{REF} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



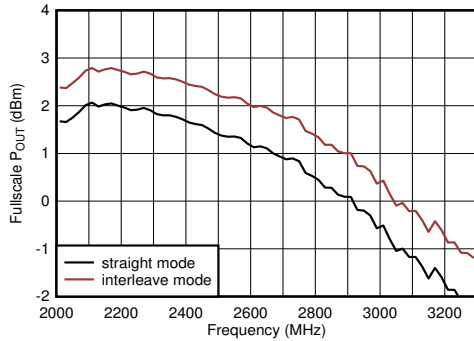
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 2.6 GHz matching

**Figure 6-354. TX Full Scale vs RF Frequency at 5898.24MSPS**



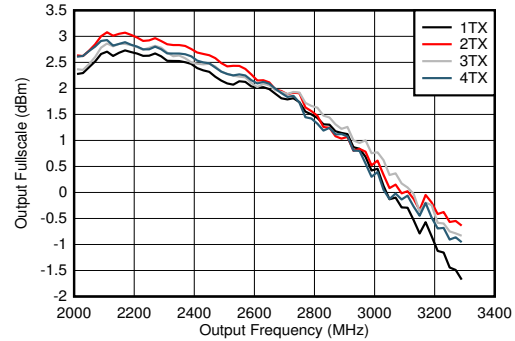
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 2.6 GHz matching

**Figure 6-355. TX Full Scale vs RF Frequency at 8847.36MSPS**



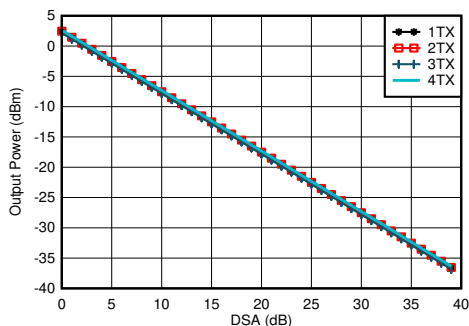
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 2.6 GHz matching

**Figure 6-356. TX Full Scale vs RF Frequency at 11796.48MSPS**



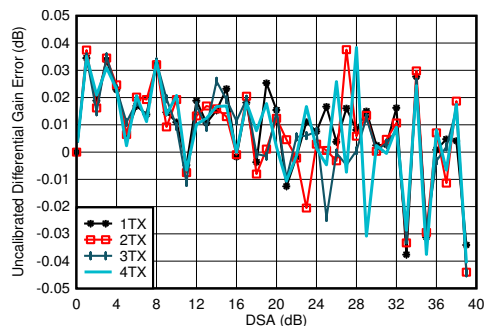
$f_{DAC} = 8847.36\text{MSPS}$ , interleave mode, including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 2.6 GHz matching

**Figure 6-357. TX Output Fullscale vs Output Frequency and Channel**



$f_{DAC} = 8847.36\text{ MSPS}$ ,  $A_{out} = -0.5\text{dBFS}$ , matching 2.6 GHz

**Figure 6-358. TX Output Power vs DSA Setting and Channel at 2.6 GHz**

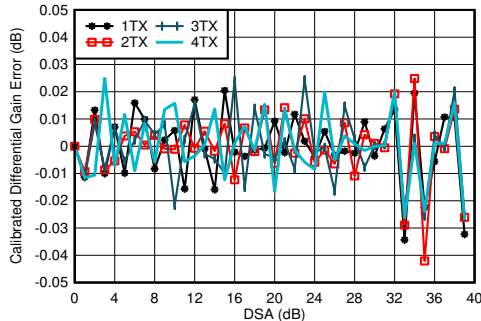


$f_{DAC} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

**Figure 6-359. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz**

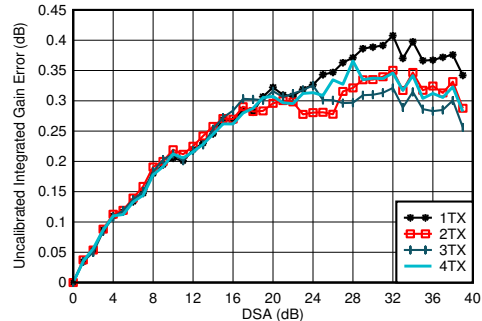
### 6.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



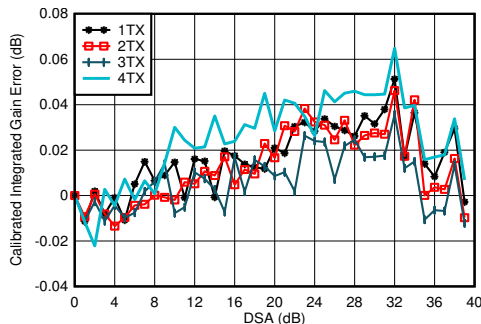
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 6-360. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



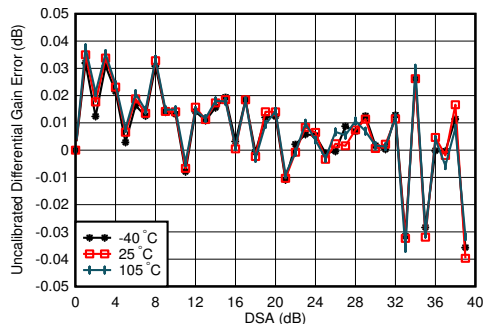
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 6-361. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



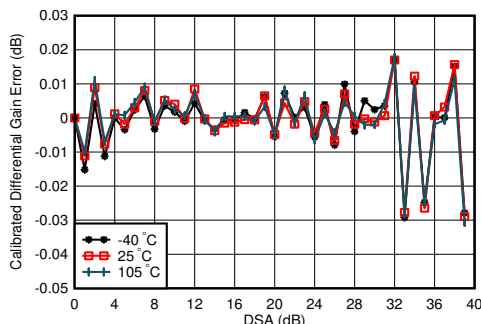
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 6-362. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



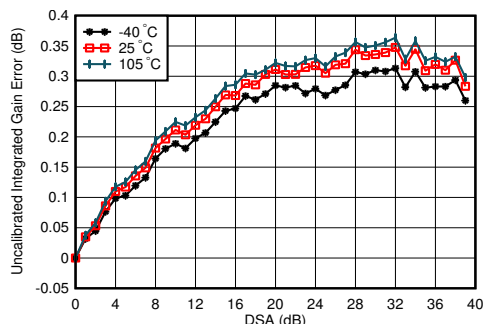
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 6-363. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 6-364. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



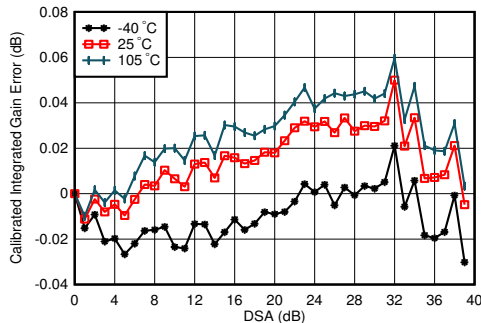
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 6-365. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz



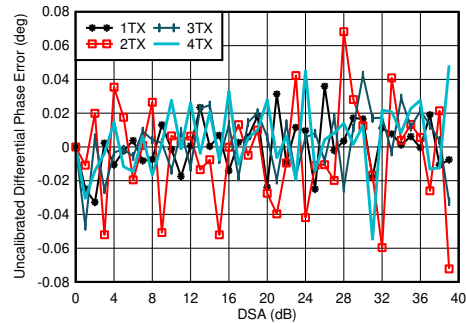
### 6.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



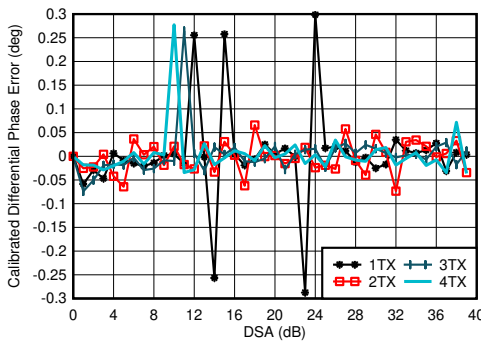
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-366. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz**



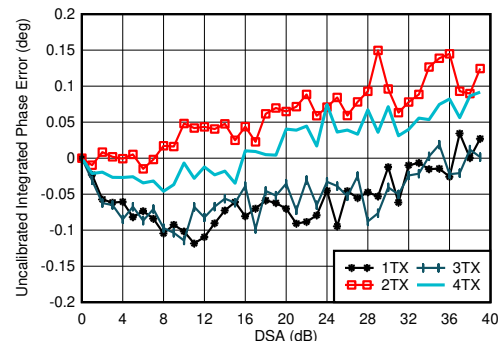
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-367. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
Phase DNL spike may occur at any DSA setting.

**Figure 6-368. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz**

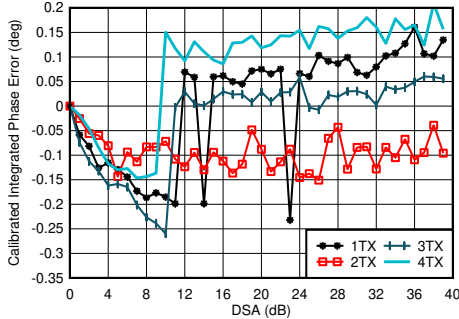


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-369. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz**

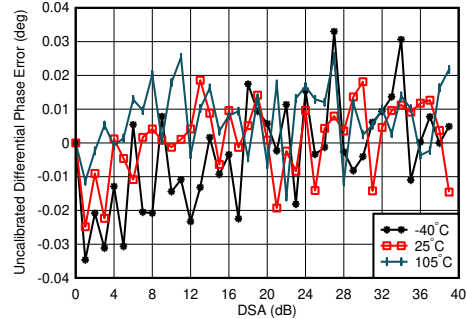
**6.12.10 TX Typical Characteristics at 2.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



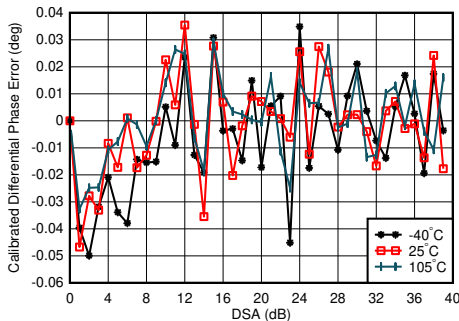
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-370. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz**



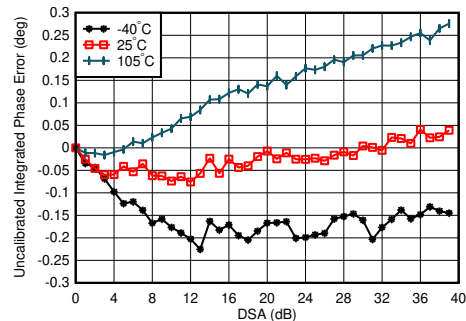
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at  $25^\circ\text{C}$   
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-371. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz**



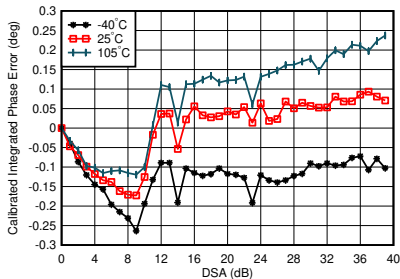
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at  $25^\circ\text{C}$   
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-372. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz**



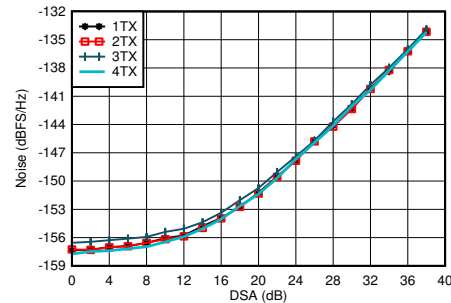
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at  $25^\circ\text{C}$   
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-373. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at  $25^\circ\text{C}$   
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-374. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz**

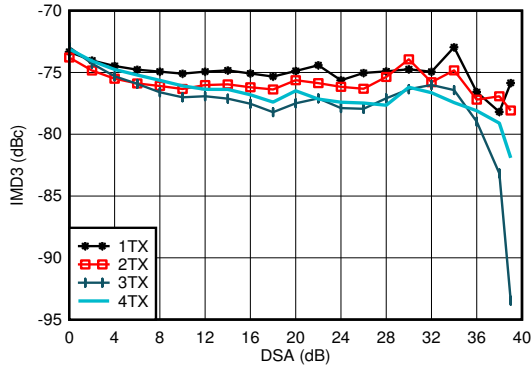


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6 GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

**Figure 6-375. TX Output Noise vs Channel and Attenuation at 2.6 GHz**

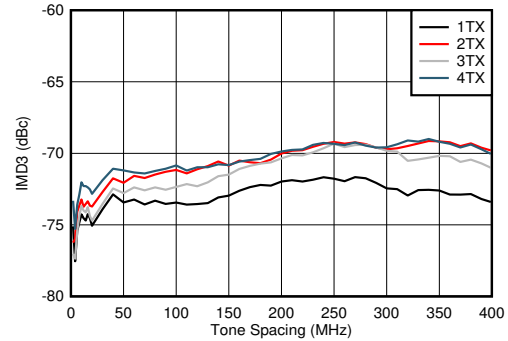
### 6.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



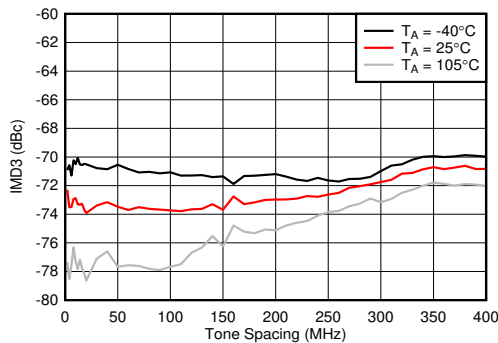
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ , matching at 2.6 GHz, -13 dBFS each tone

**Figure 6-376. TX IMD3 vs DSA Setting at 2.6 GHz**



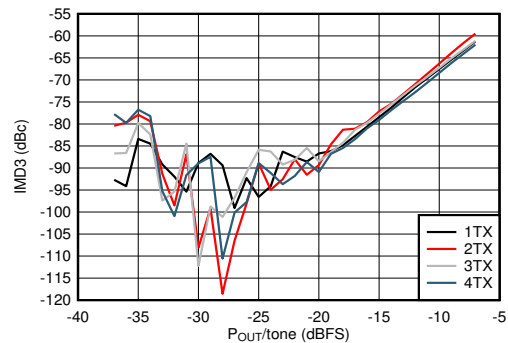
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ , matching at 2.6 GHz, -13 dBFS each tone

**Figure 6-377. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz**



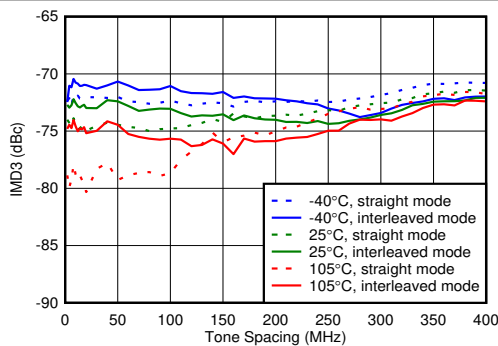
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ , matching at 2.6 GHz, -13 dBFS each tone, worst channel, dither = 1.

**Figure 6-378. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz**



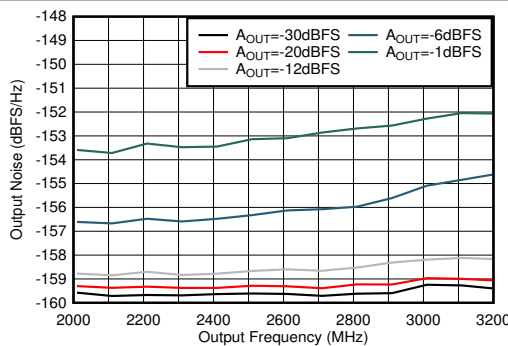
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ ,  $f_{\text{SPACING}} = 20\text{ MHz}$ , dither = 1, matching at 2.6 GHz

**Figure 6-379. TX IMD3 vs Digital Level at 2.6 GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{ GHz}$ , matching at 2.6 GHz, -13 dBFS each tone

**Figure 6-380. TX IMD3 vs Tone Spacing and Temperature**



Matching at 2.6 GHz, Single tone,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset

**Figure 6-381. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz**

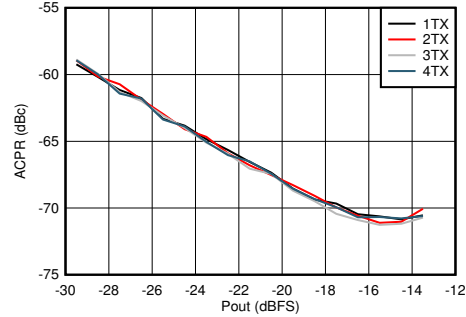
6.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



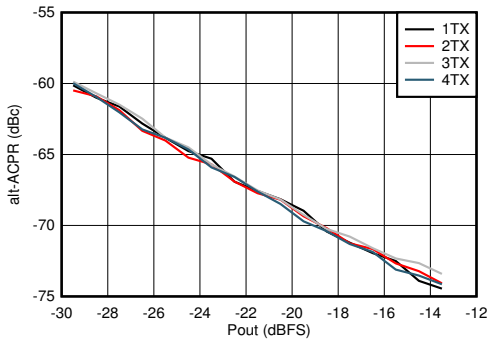
TM1.1,  $P_{\text{OUT,RMS}} = -13\text{ dBFS}$

Figure 6-382. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)



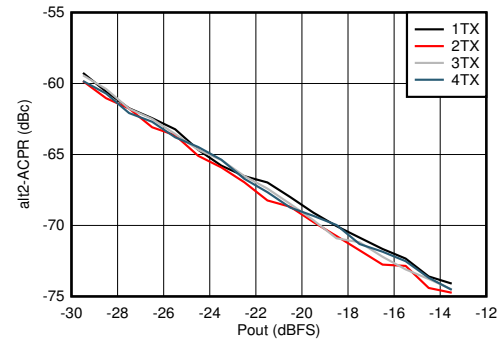
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 6-383. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz



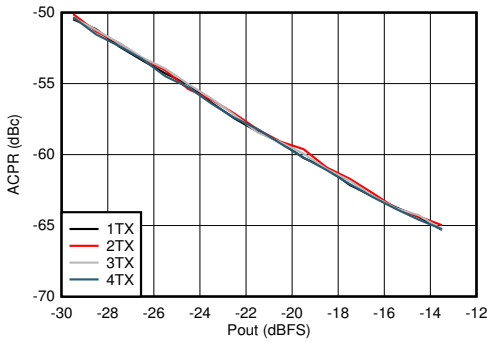
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 6-384. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



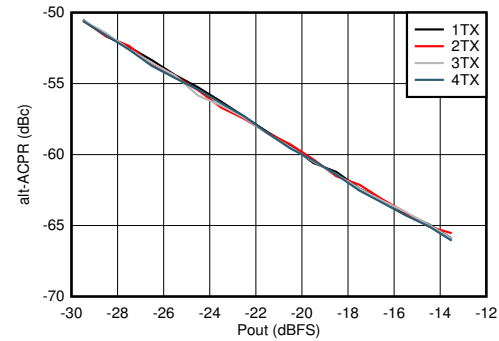
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 6-385. TX 20-MHz LTE alt2-ACPR vs Digital Level at 2.6 GHz



Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 6-386. TX 100-MHz NR ACPR vs Digital Level at 2.6 GHz

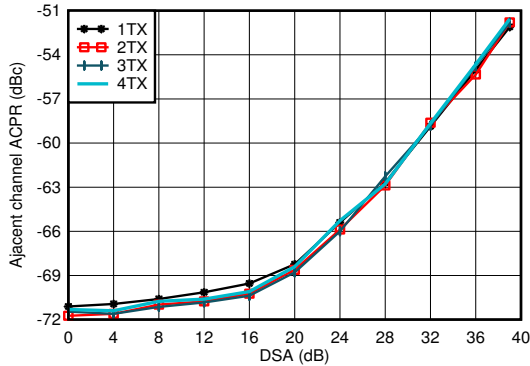


Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

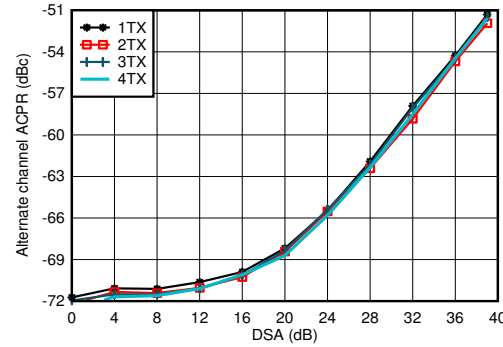
Figure 6-387. TX 100-MHz NR alt-ACPR vs Digital Level at 2.6 GHz

### 6.12.10 TX Typical Characteristics at 2.6GHz (continued)

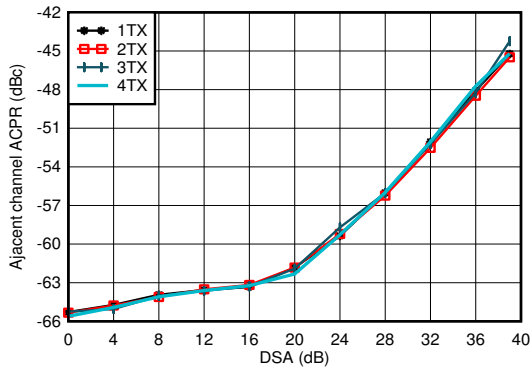
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{REF} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



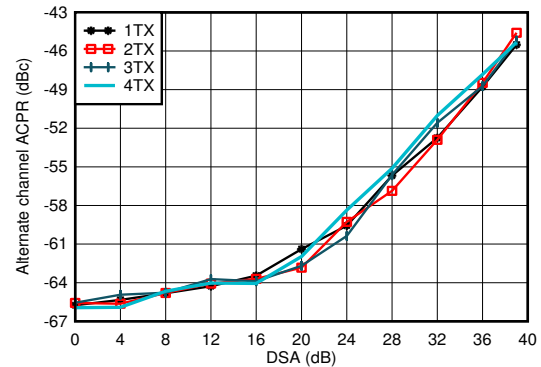
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE  
**Figure 6-388. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz**



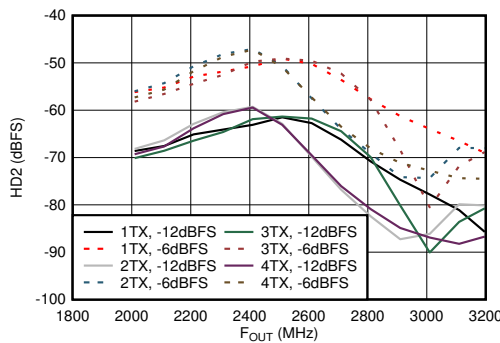
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE  
**Figure 6-389. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz**



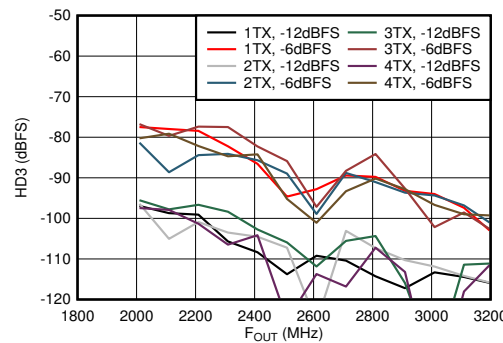
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR  
**Figure 6-390. TX 100-MHz NR ACPR vs DSA at 2.6 GHz**



Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR  
**Figure 6-391. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz**



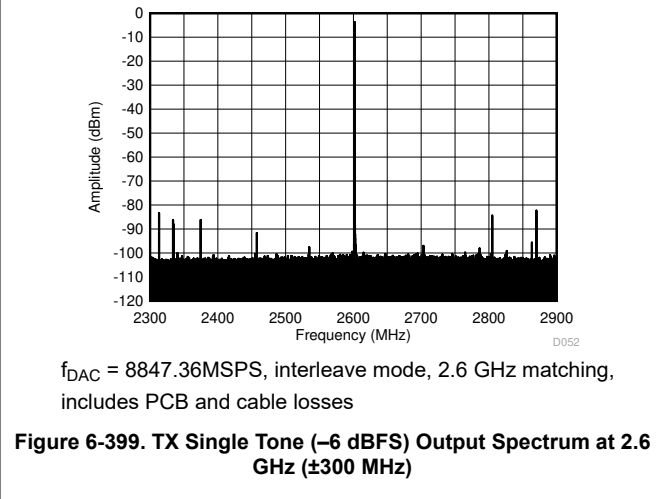
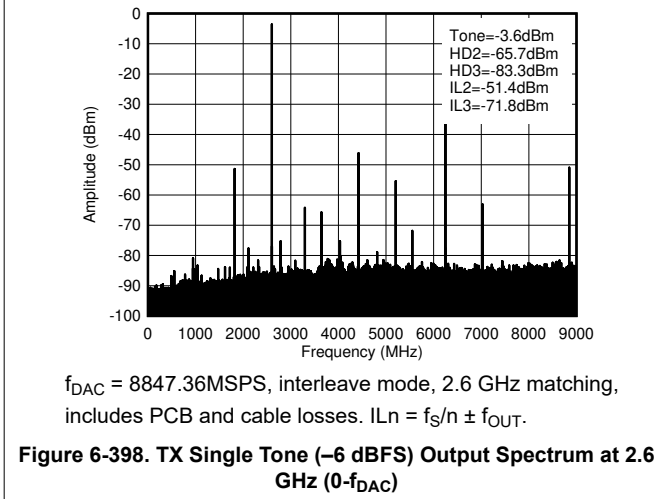
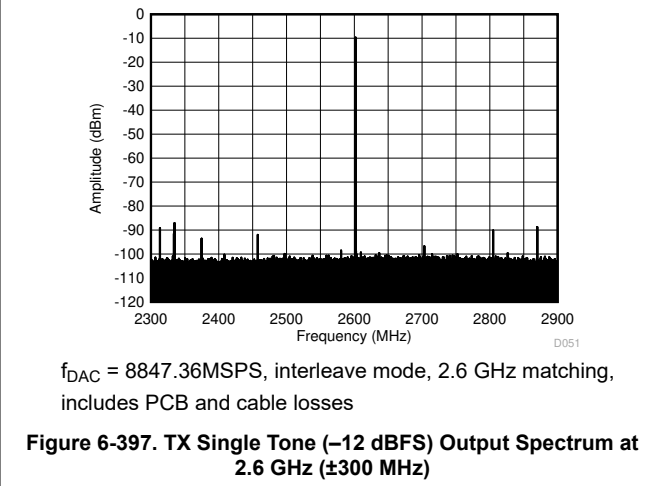
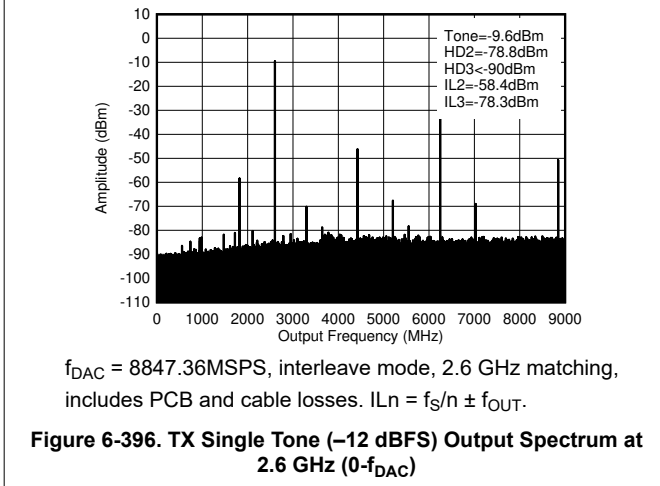
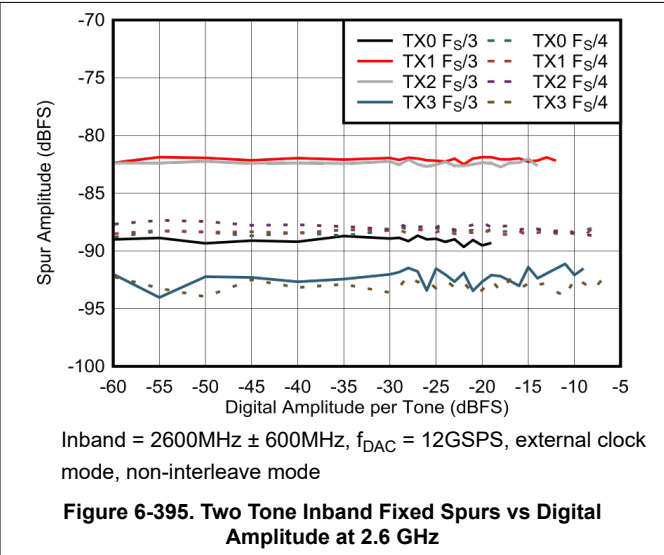
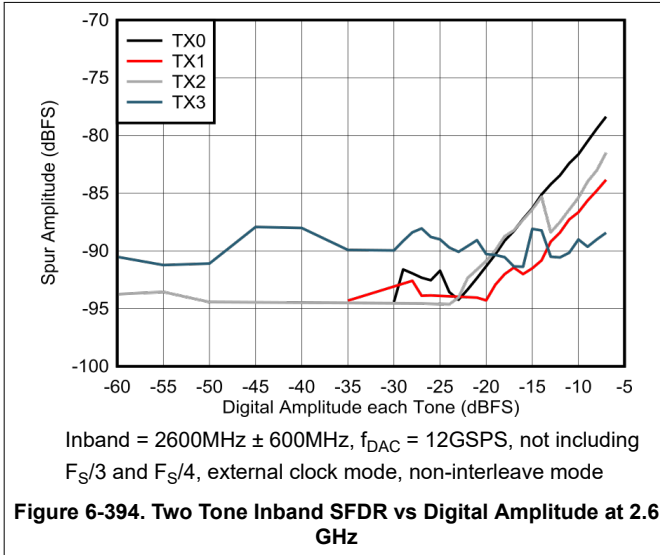
Matching at 2.6 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency  
**Figure 6-392. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz**



Matching at 2.6 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency  
**Figure 6-393. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz**

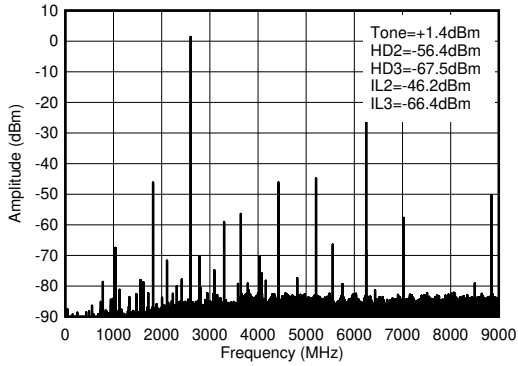
**6.12.10 TX Typical Characteristics at 2.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{REF} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



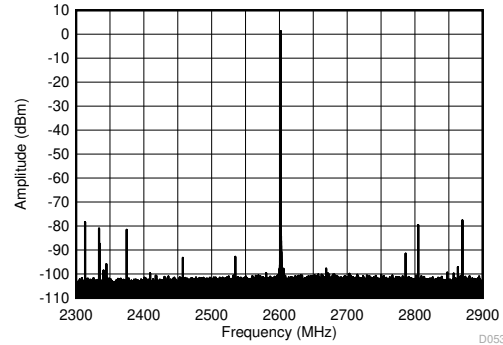
### 6.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



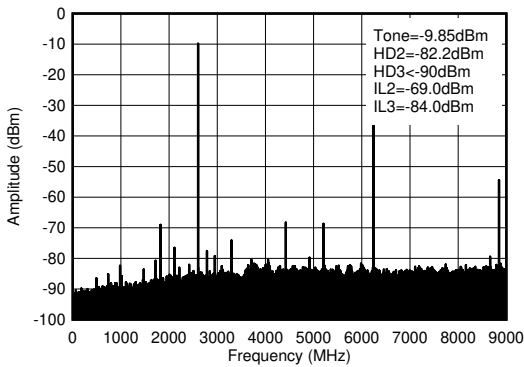
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode, 2.6 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-400. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )**



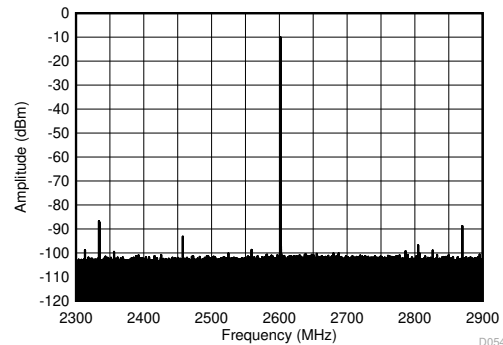
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , interleave mode, 2.6 GHz matching, includes PCB and cable losses

**Figure 6-401. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ( $\pm 300\text{ MHz}$ )**



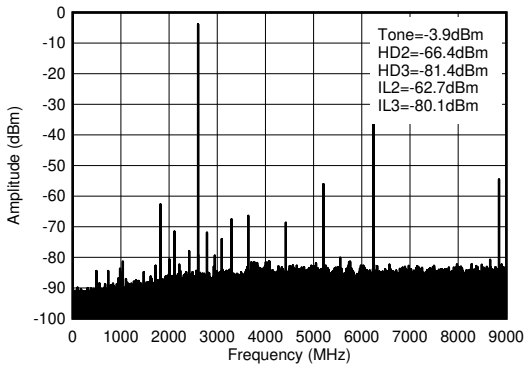
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-402. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )**



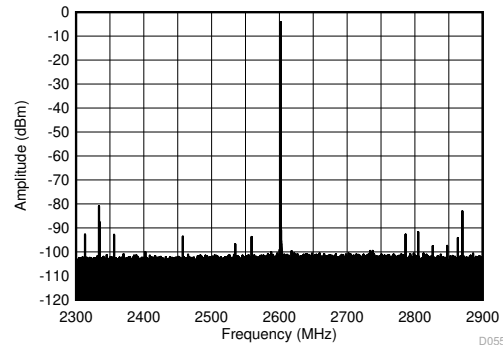
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses

**Figure 6-403. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ( $\pm 300\text{ MHz}$ )**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses.  $\text{ILn} = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-404. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )**



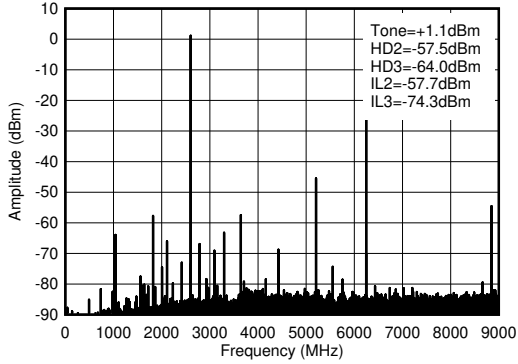
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses

**Figure 6-405. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ( $\pm 300\text{ MHz}$ )**



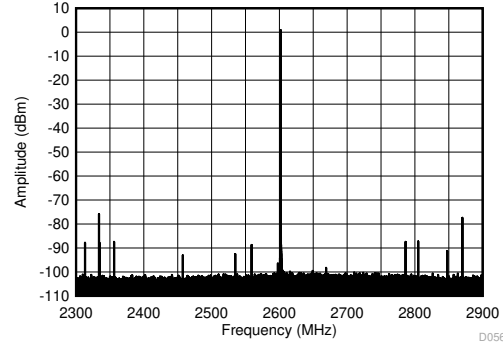
**6.12.10 TX Typical Characteristics at 2.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



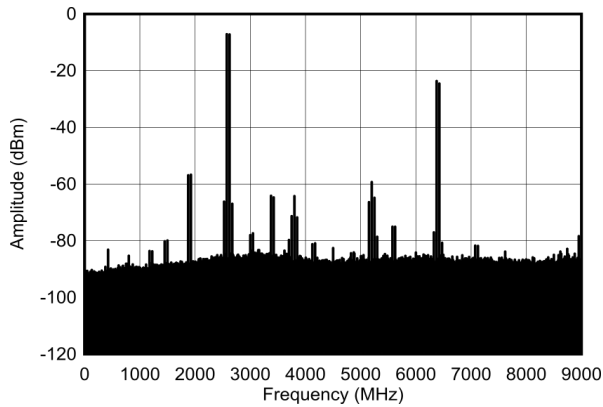
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-406. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ( $0 - f_{\text{DAC}}$ )**



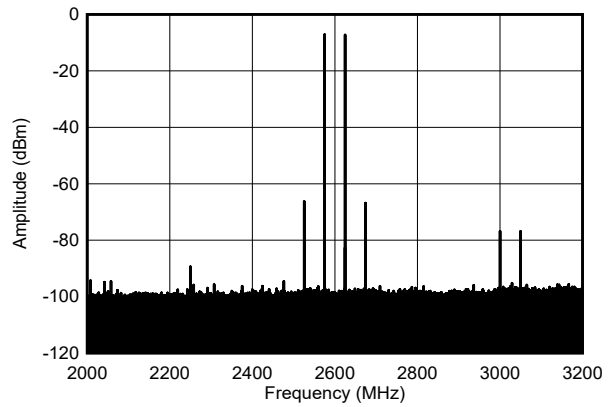
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6 GHz matching, includes PCB and cable losses

**Figure 6-407. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ( $\pm 300\text{ MHz}$ )**



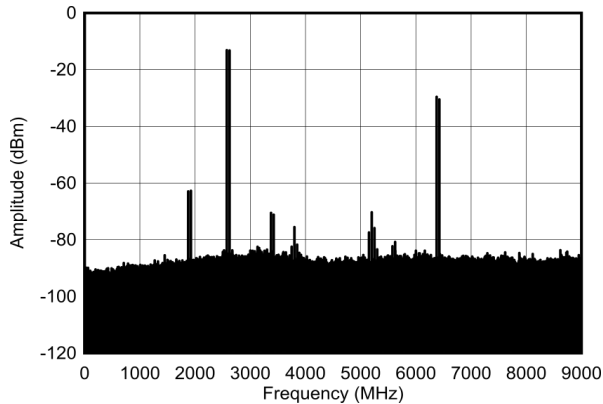
$f_{\text{DAC}} = 9000\text{MSPS}$ , external clock mode, non-interleave mode

**Figure 6-408. TX Dual Tone Output Spectrum at 2.6 GHz, -7dBFS each ( $0 - f_{\text{DAC}}$ )**



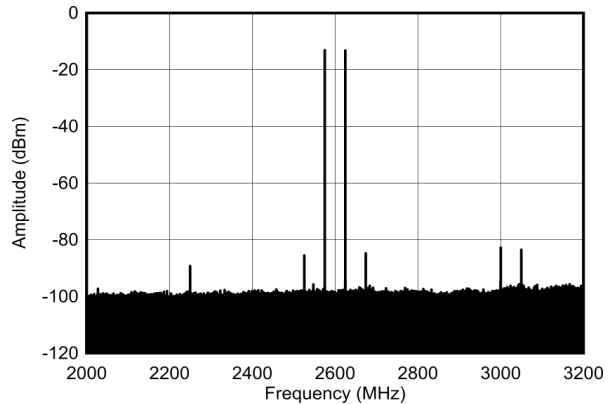
$f_{\text{DAC}} = 9000\text{MSPS}$ , external clock mode, non-interleave mode

**Figure 6-409. TX Dual Tone Output Spectrum at 2.6 GHz, -7dBFS each ( $\pm 600\text{ MHz}$ )**



$f_{\text{DAC}} = 9000\text{MSPS}$ , external clock mode, non-interleave mode

**Figure 6-410. TX Dual Tone Output Spectrum at 2.6 GHz, -13dBFS each ( $0 - f_{\text{DAC}}$ )**



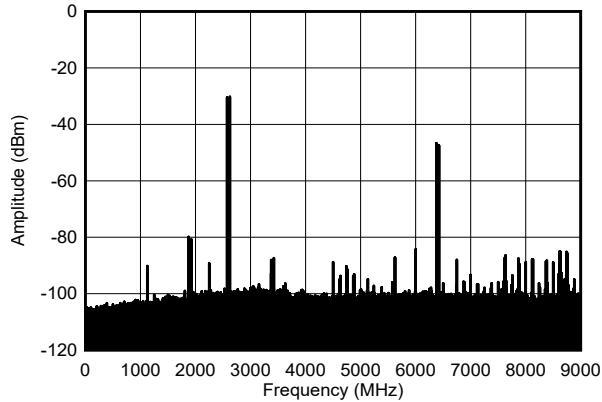
$f_{\text{DAC}} = 9000\text{MSPS}$ , external clock mode, non-interleave mode

**Figure 6-411. TX Dual Tone Output Spectrum at 2.6 GHz, -13dBFS each ( $\pm 600\text{ MHz}$ )**



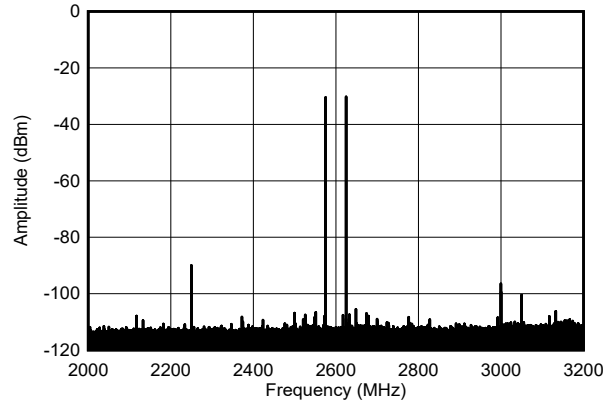
### 6.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



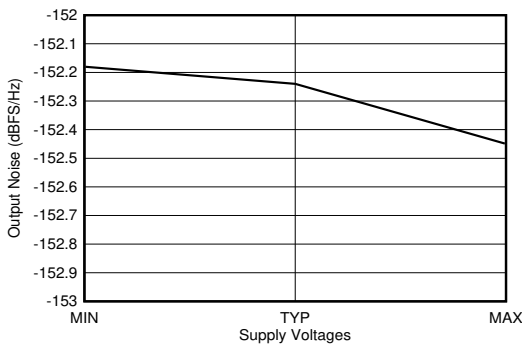
$f_{\text{DAC}} = 9000\text{MSPS}$ , external clock mode, non-interleave mode

**Figure 6-412. TX Dual Tone Output Spectrum at 2.6 GHz, -30dBFS each ( $0 - \text{DAC}$ )**



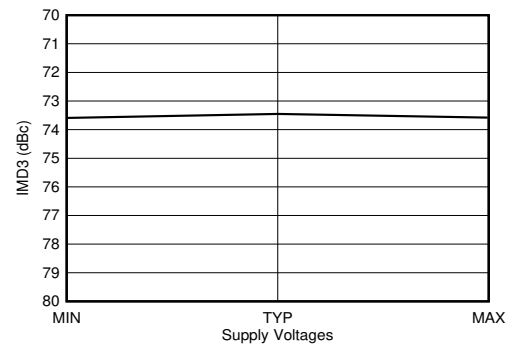
$f_{\text{DAC}} = 9000\text{MSPS}$ , external clock mode, non-interleave mode

**Figure 6-413. TX Dual Tone Output Spectrum at 2.6 GHz, -30dBFS each ( $\pm 600\text{ MHz}$ )**



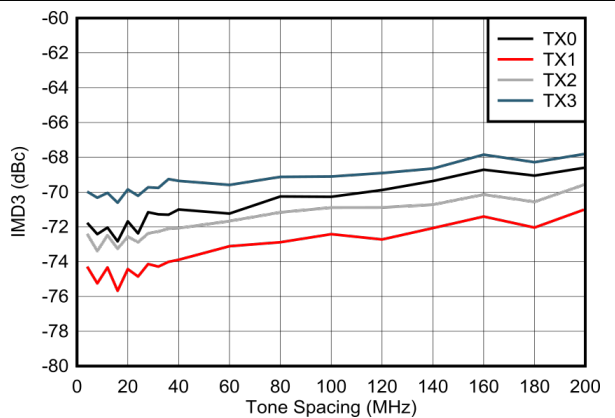
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power =  $-1\text{ dBFS}$ . All supplies simultaneously at MIN, TYP, or MAX voltages.

**Figure 6-414. TX Output Noise vs Supply Voltage at 2.6 GHz**



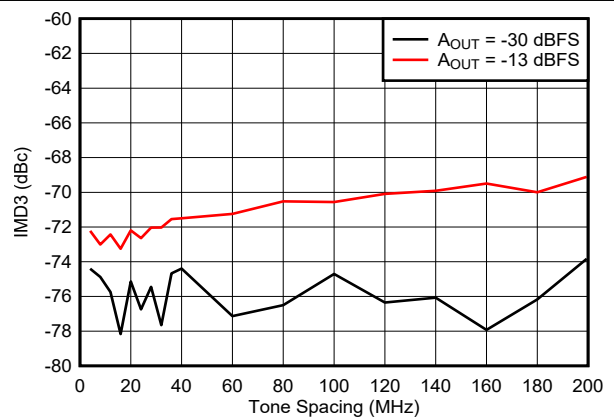
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power =  $-13\text{ dBFS}$ . All supplies simultaneously at MIN, TYP, or MAX voltages.

**Figure 6-415. TX IMD3 vs Supply Voltage at 2.6 GHz**



$f_{\text{DAC}} = 9000\text{MSPS}$ , non-interleave mode, external clock mode

**Figure 6-416. IMD3 vs Tone Spacing and Channel at 2.6 GHz**



$f_{\text{DAC}} = 9000\text{MSPS}$ , non-interleave mode, external clock mode

**Figure 6-417. IMD3 vs Tone Spacing and Amplitude at 2.6 GHz**

### 6.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

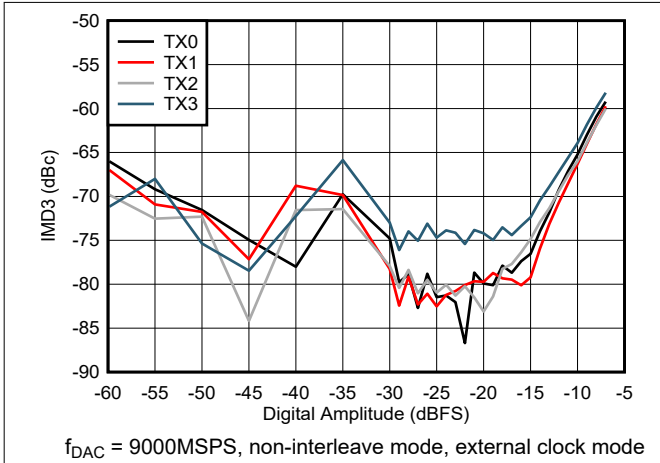


Figure 6-418. IMD3 vs Digital Amplitude and Channel at 2.6 GHz

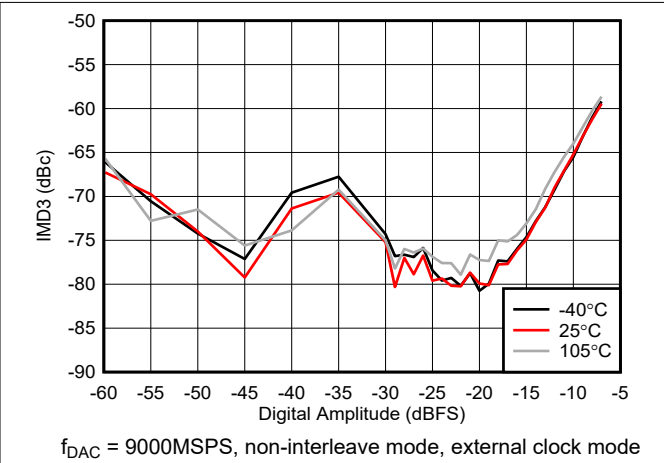


Figure 6-419. IMD3 vs Digital Amplitude and Temperature at 2.6 GHz

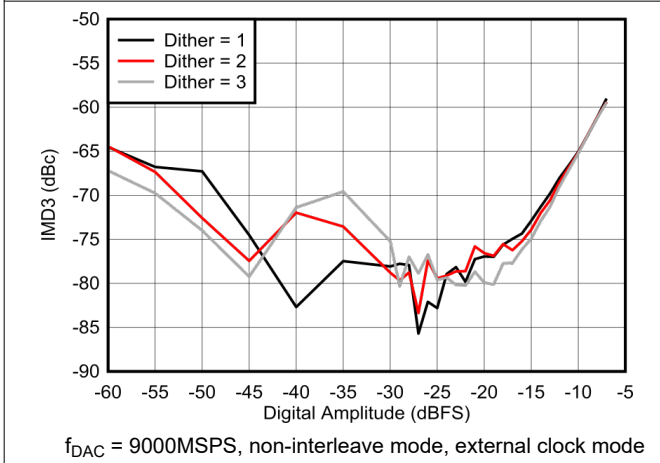


Figure 6-420. IMD3 vs Digital Amplitude and Dither at 2.6 GHz

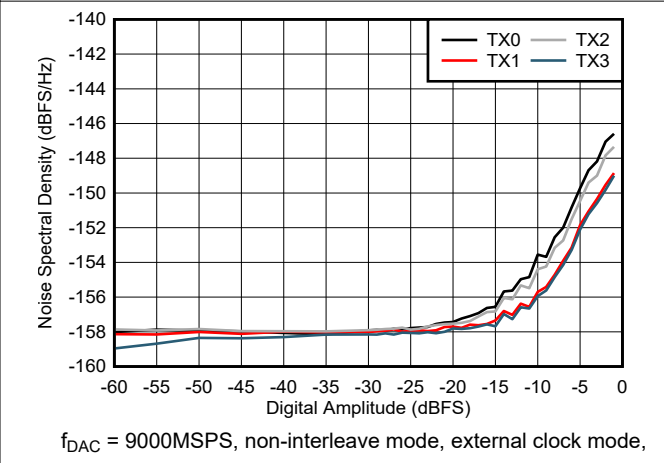
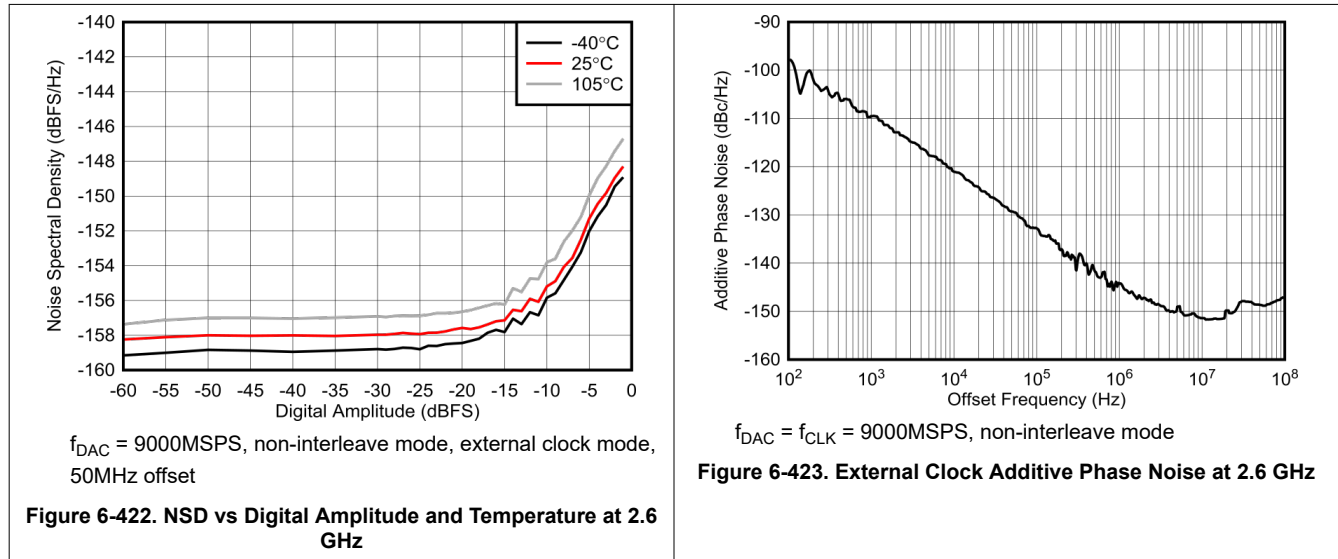


Figure 6-421. NSD vs Digital Amplitude and Channel at 2.6 GHz

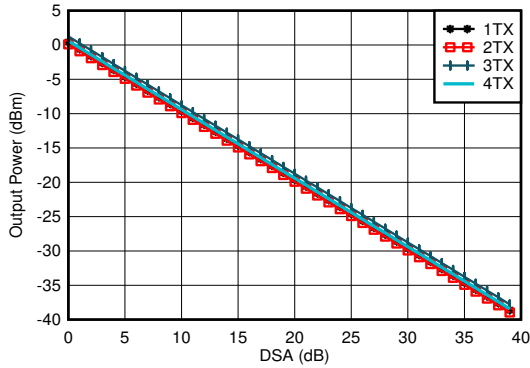
### 6.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



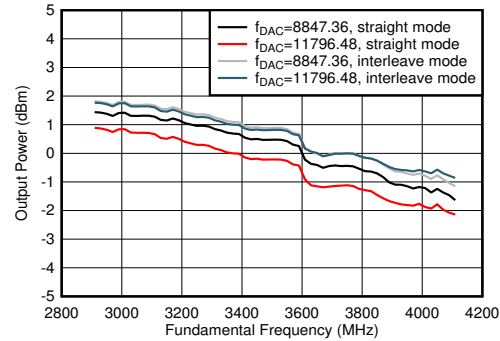
### 6.12.11 TX Typical Characteristics at 3.5GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



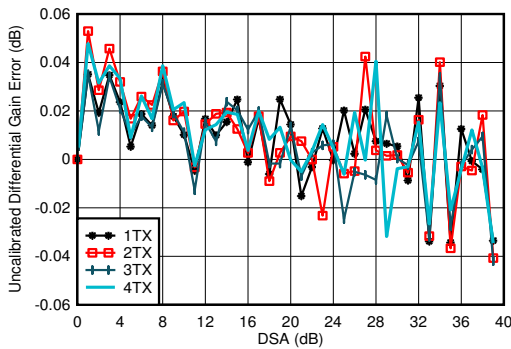
$A_{\text{out}} = -0.5\text{dBFS}$ , 3.5 GHz Matching, included PCB and cable losses

**Figure 6-424. TX Output Power vs DSA Setting at 3.5 GHz**



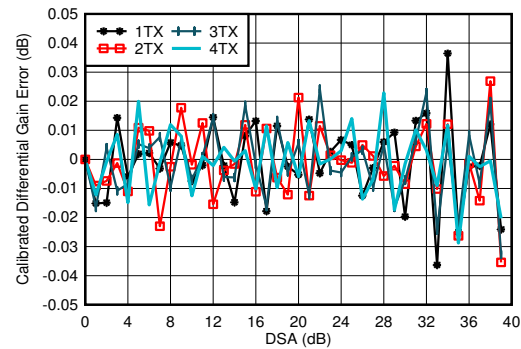
$A_{\text{out}} = -0.5\text{dBFS}$ , 3.5 GHz Matching, included PCB and cable losses

**Figure 6-425. TX Output Power vs Frequency**



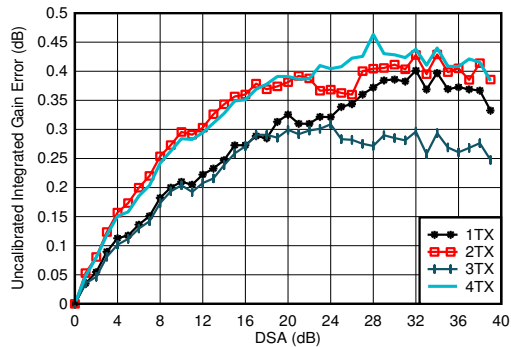
3.5 GHz Matching, included PCB and cable losses  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-426. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz**



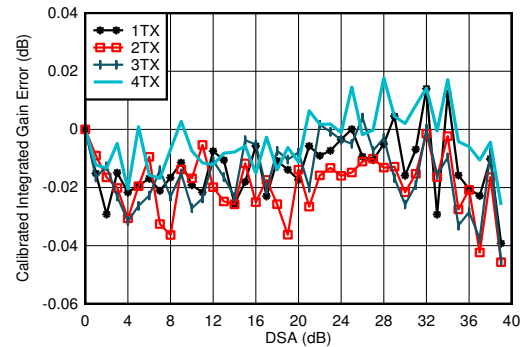
3.5 GHz Matching, included PCB and cable losses  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-427. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz**



3.5 GHz Matching, included PCB and cable losses  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-428. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz**

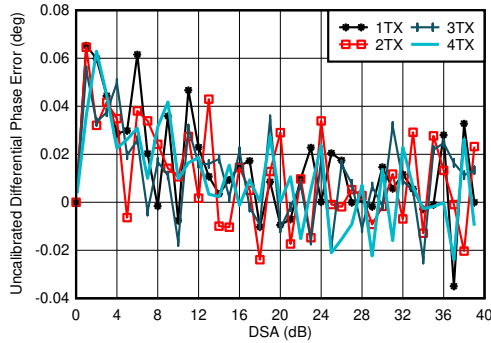


3.5 GHz Matching, included PCB and cable losses  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-429. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz**

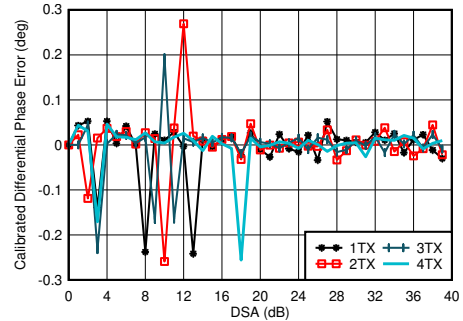
### 6.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



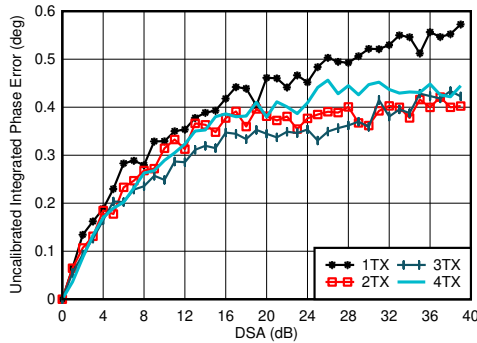
3.5 GHz Matching, included PCB and cable losses  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-430. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz**



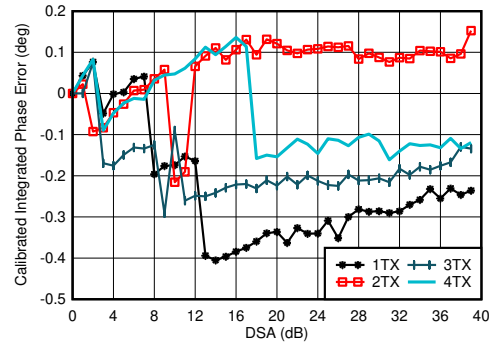
3.5 GHz Matching, included PCB and cable losses  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$ . Phase DNL spike may occur at any DSA setting.

**Figure 6-431. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz**



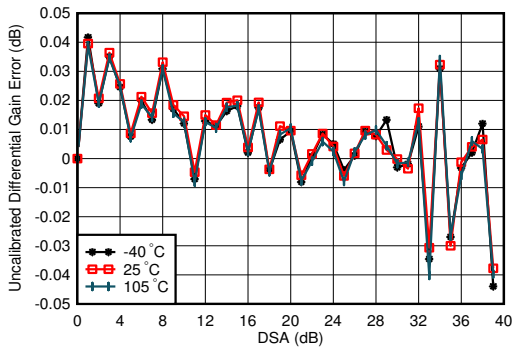
3.5 GHz Matching, included PCB and cable losses  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-432. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz**



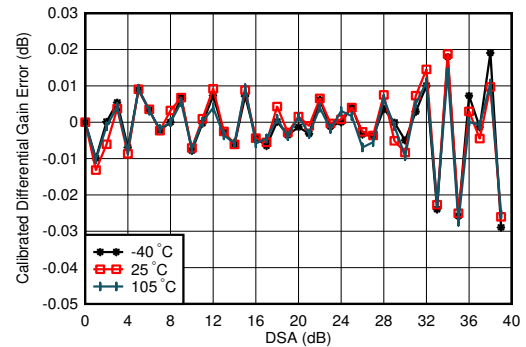
3.5 GHz Matching, included PCB and cable losses  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-433. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz**



3.5 GHz Matching, 0TX  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-434. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz**

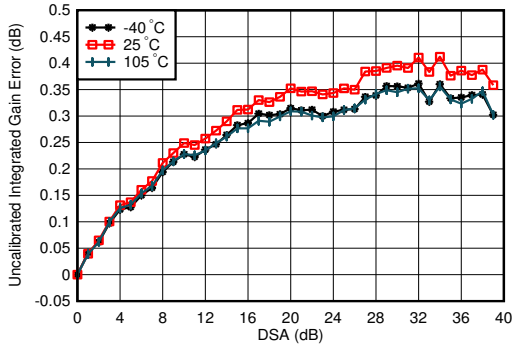


3.5 GHz Matching, 0TX, Calibrated at 25°C  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-435. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz**

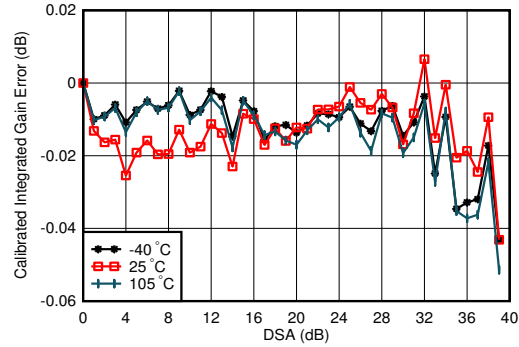
### 6.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



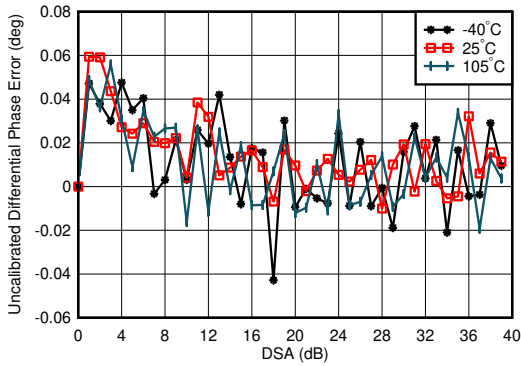
3.5 GHz Matching, 0TX  
 Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-436. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz**



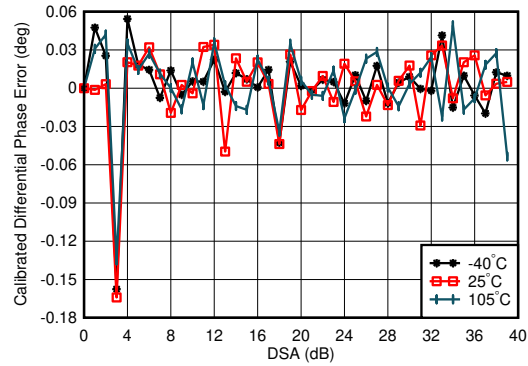
3.5 GHz Matching, 0TX, Calibrated at 25°C  
 Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-437. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz**



3.5 GHz Matching, 0TX  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-438. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz**

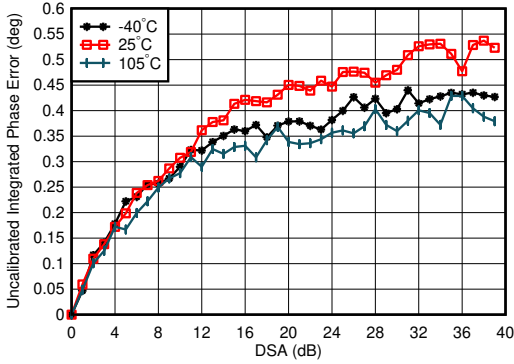


3.5 GHz Matching, 0TX, Calibrated at 25°C  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-439. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz**

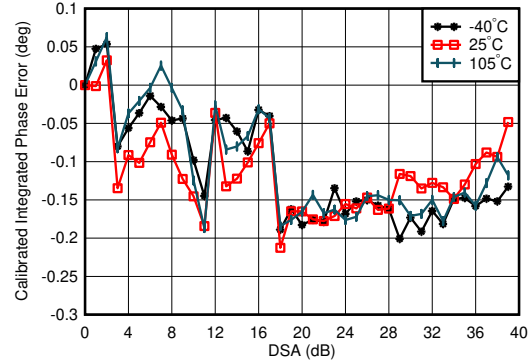
### 6.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



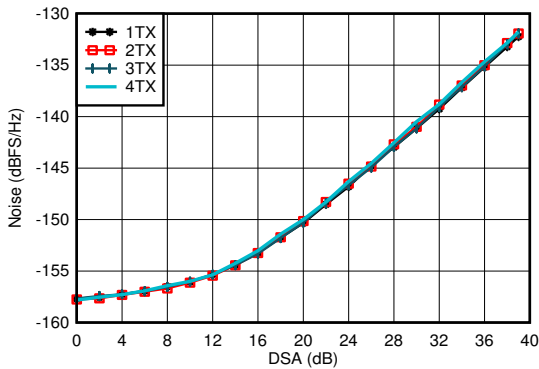
3.5 GHz Matching, 0TX  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting=0)

**Figure 6-440. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz**



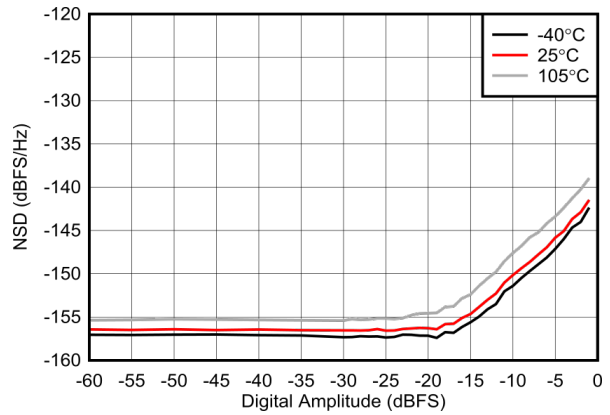
3.5 GHz Matching, 0TX, Calibrated at 25°C  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-441. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz**



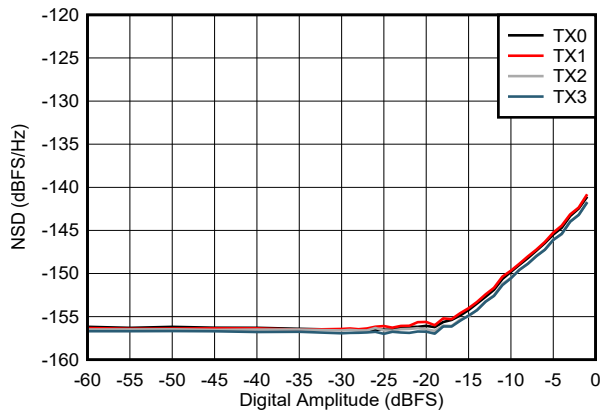
A.  $f_{\text{DAC}}=11796.48\text{MSPS}$ , interleave mode, matching at 3.5GHz,  $A_{\text{out}} = -13\text{ dBFS}$ .

**Figure 6-442. TX NSD vs DSA Setting at 3.5 GHz**



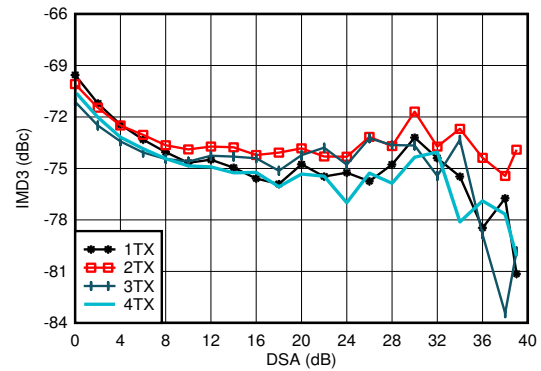
A.  $f_{\text{DAC}}=12\text{MSPS}$ , external clock mode, non-interleave mode

**Figure 6-443. TX NSD vs Digital Amplitude and Temperature at 3.75 GHz**



A.  $f_{\text{DAC}}=12\text{MSPS}$ , external clock mode, non-interleave mode

**Figure 6-444. TX NSD vs Digital Amplitude and Channel at 3.75 GHz**

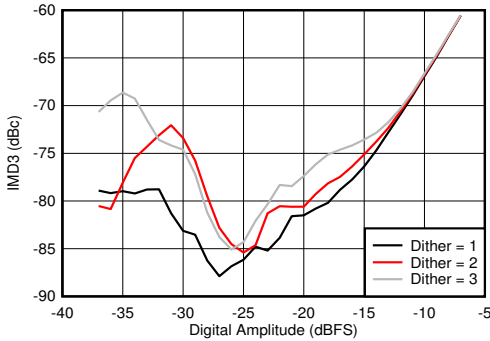


20-MHz tone spacing, 3.5 GHz Matching, -13 dBFS each tone, included PCB and cable losses

**Figure 6-445. TX IMD3 vs DSA Setting at 3.5 GHz**

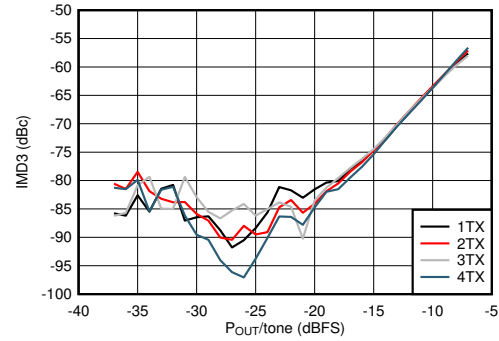
**6.12.11 TX Typical Characteristics at 3.5GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



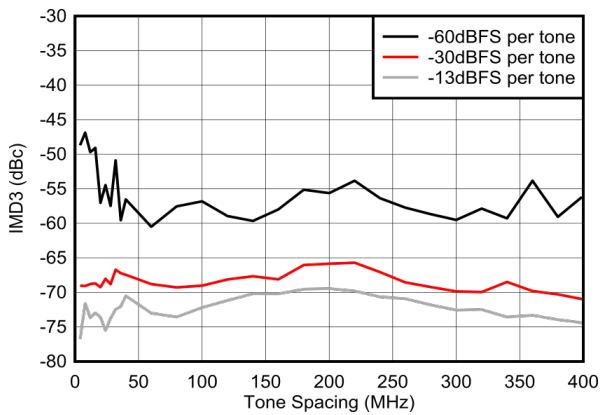
20-MHz tone spacing, 3.5 GHz Matching, included PCB and cable losses

**Figure 6-446. TX IMD3 vs Digital Amplitude and Dither Setting at 3.5 GHz**



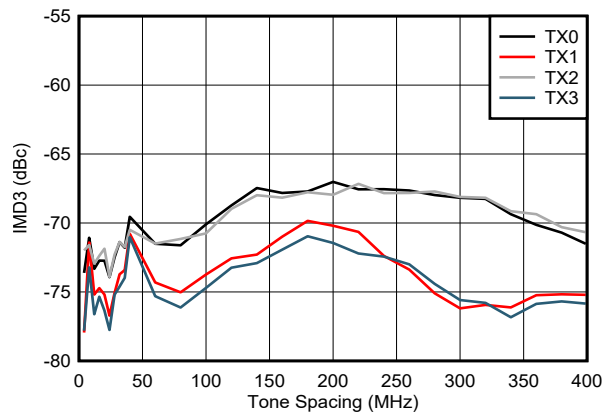
20-MHz tone spacing, 3.5 GHz Matching

**Figure 6-447. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz**



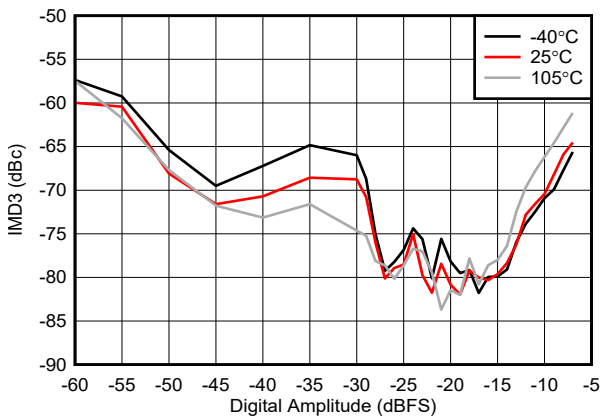
50-MHz tone spacing, external clock mode, non-interleave mode

**Figure 6-448. TX IMD3 vs Tone Spacing and Amplitude at 3.75GHz**



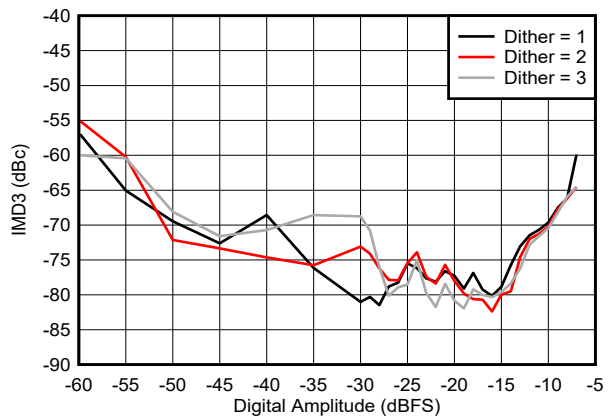
50-MHz tone spacing, external clock mode, non-interleave mode

**Figure 6-449. TX IMD3 vs Tone Spacing and Channel at 3.75GHz**



50-MHz tone spacing, external clock mode, non-interleave mode

**Figure 6-450. TX IMD3 vs Digital Amplitude and Temperature at 3.75GHz**



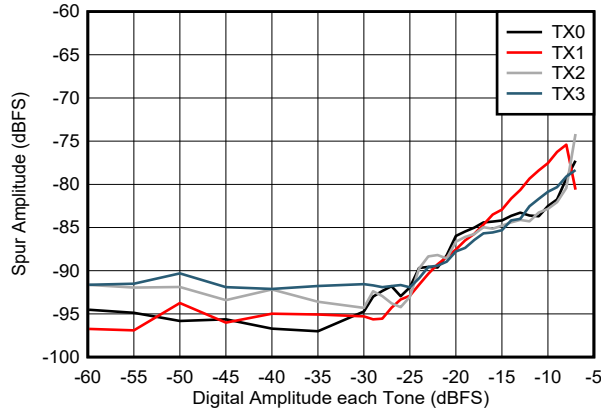
50-MHz tone spacing, external clock mode, non-interleave mode

**Figure 6-451. TX IMD3 vs Digital Amplitude and Dither at 3.75GHz**



### 6.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



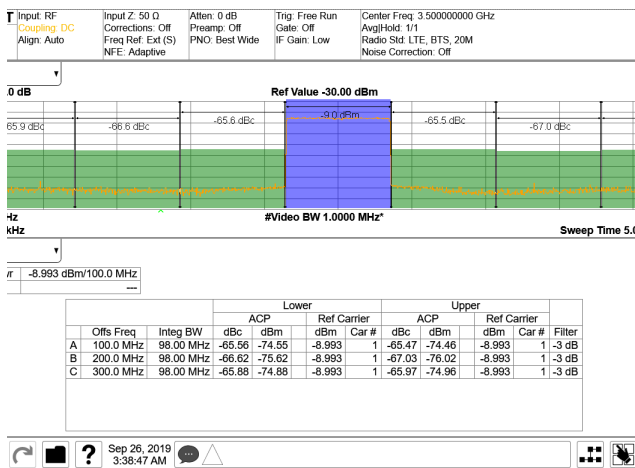
Inband = 3.75GHz  $\pm$  600MHz,  $f_{\text{DAC}} = 9\text{GSPS}$ , external clock mode, non-interleave mode.

Figure 6-452. Two Tone Inband SFDR vs Digital Amplitude at 3.75GHz



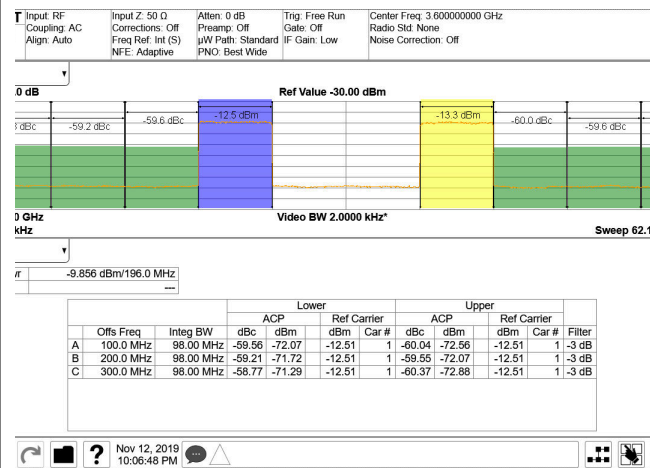
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 6-453. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 6-454. TX 100-MHz NR Output Spectrum at 3.5 GHz (Band 42)

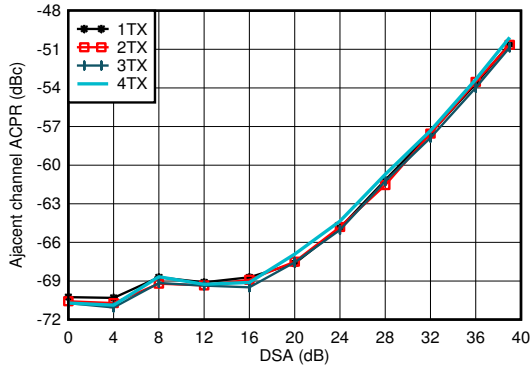


3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 6-455. TX 2 carrier 100-MHz NR Output Spectrum at 3.45 GHz and 3.75 GHz

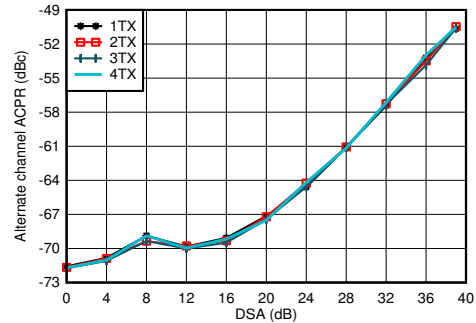
### 6.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{REF} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



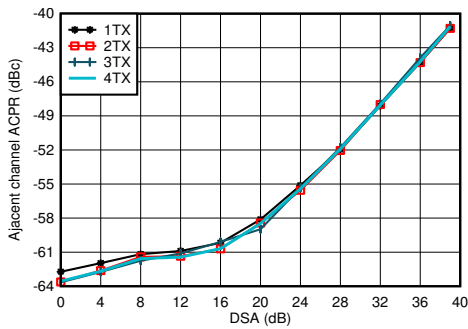
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 6-456. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz



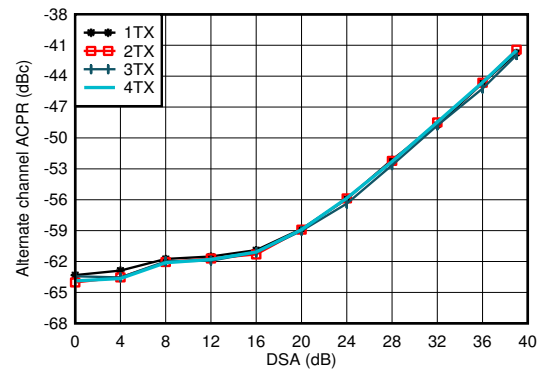
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 6-457. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz



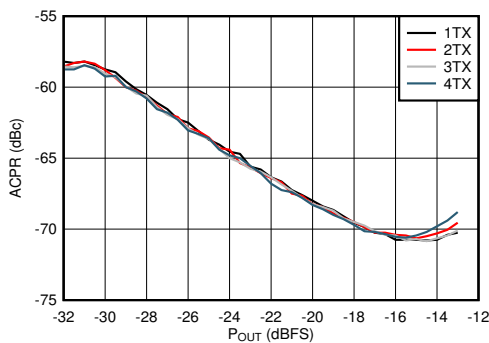
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 6-458. TX 100-MHz NR ACPR vs DSA Setting at 3.5 GHz



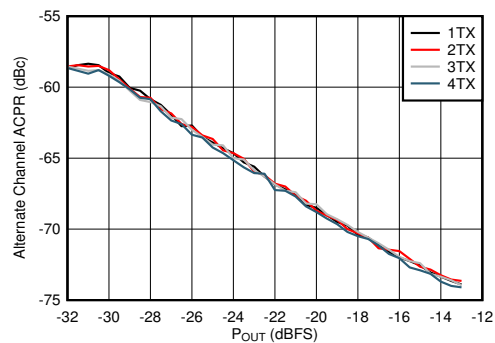
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 6-459. TX 100-MHz NR alt-ACPR vs DSA Setting at 3.5 GHz



3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 6-460. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz

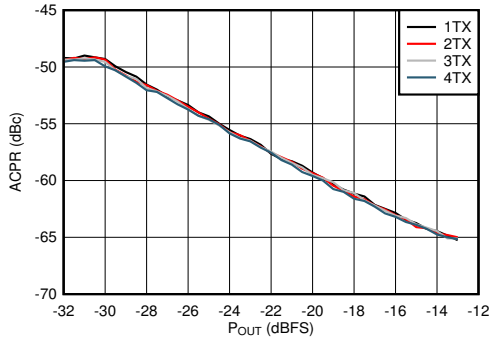


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 6-461. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz

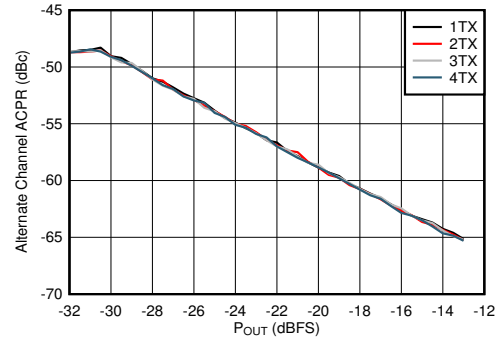
### 6.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{REF} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



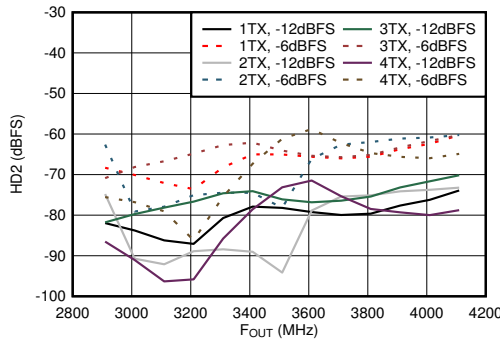
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

**Figure 6-462. TX 100-MHz NR ACPR vs Digital Level at 3.5 GHz**



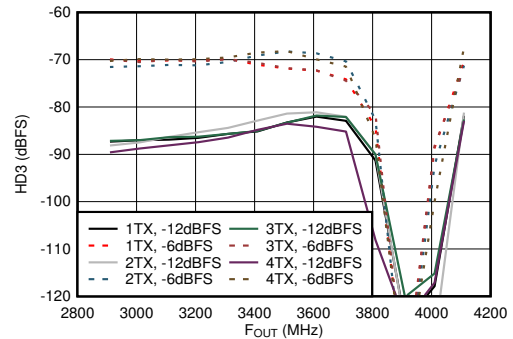
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

**Figure 6-463. TX 100-MHz NR alt-ACPR vs Digital Level at 3.5 GHz**



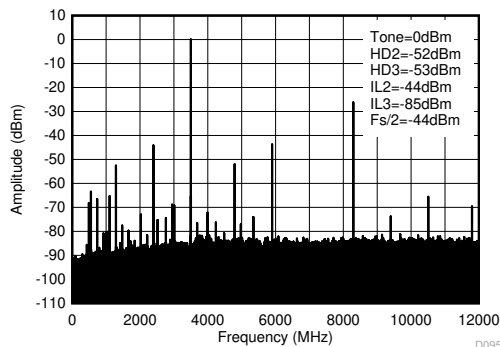
Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

**Figure 6-464. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz**



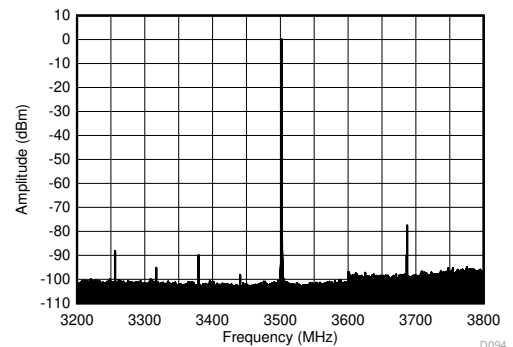
Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

**Figure 6-465. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz**



Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 6-466. TX Single Tone (-1 dBFS) Output Spectrum at 3.5 GHz (0 -  $f_{DAC}$ )**

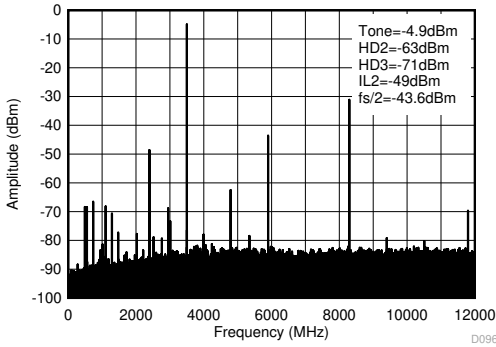


Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 6-467. TX Single Tone (-1 dBFS) Output Spectrum at 3.5 GHz ( $\pm 300\text{ MHz}$ )**

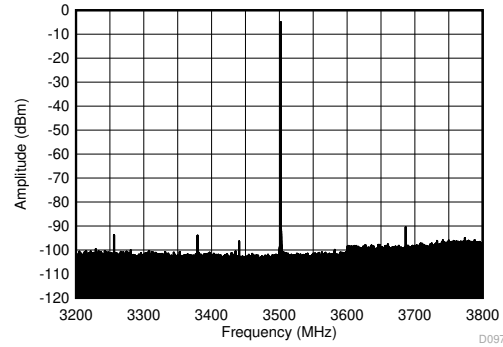
**6.12.11 TX Typical Characteristics at 3.5GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{REF} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



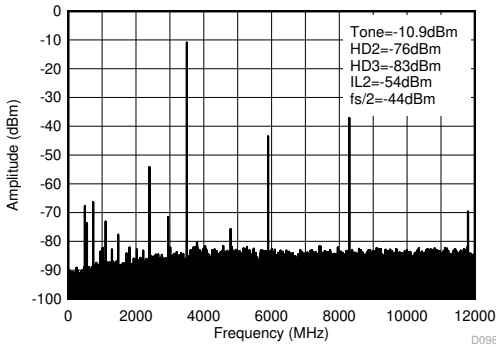
Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 6-468. TX Single Tone (-6 dBFS) Output Spectrum at 3.5 GHz (0- $f_{DAC}$ )**



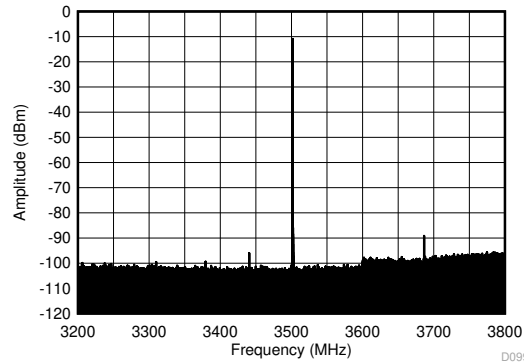
Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 6-469. TX Single Tone (-6 dBFS) Output Spectrum at 3.5 GHz ( $\pm 300\text{ MHz}$ )**



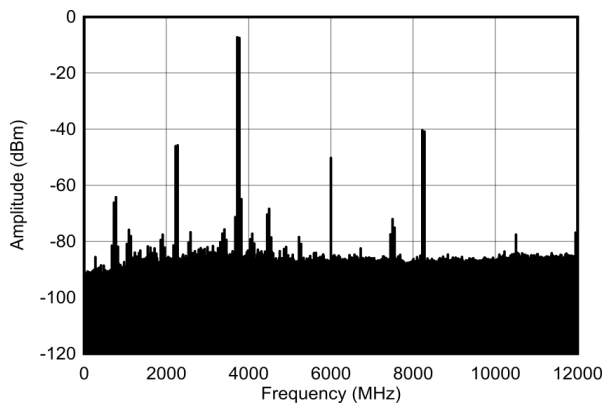
Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 6-470. TX Single Tone (-12 dBFS) Output Spectrum at 3.5 GHz (0- $f_{DAC}$ )**



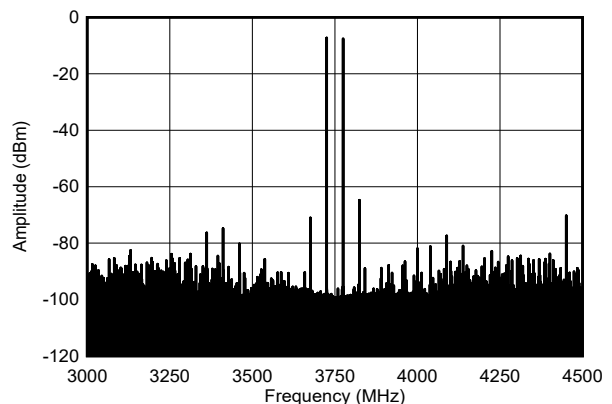
Matching at 3.5 GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 6-471. TX Single Tone (-12 dBFS) Output Spectrum at 3.5 GHz ( $\pm 300\text{ MHz}$ )**



Matching at 3.5 GHz, 50MHz tone spacing,  $f_{DAC} = 12\text{GSPS}$ , non-interleave mode.

**Figure 6-472. TX Dual Tone Output Spectrum at 3.75 GHz, -7dBFS each (0 -  $f_{DAC}$ )**

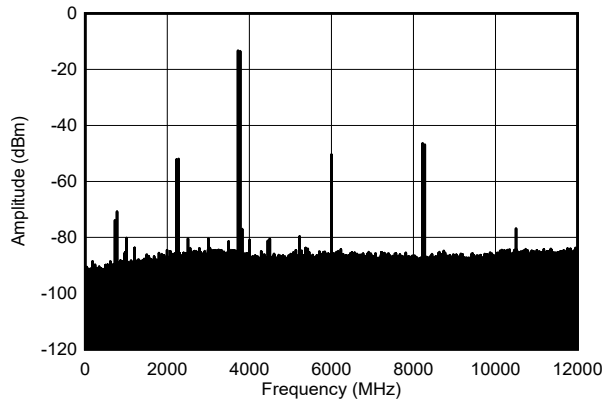


Matching at 3.5 GHz, 50MHz tone spacing,  $f_{DAC} = 12\text{GSPS}$ , non-interleave mode.

**Figure 6-473. TX Dual Tone Output Spectrum at 3.75 GHz, -7dBFS each ( $\pm 600\text{ MHz}$ )**

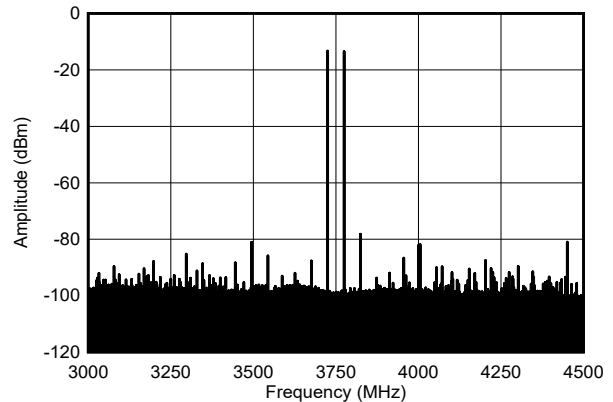
### 6.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



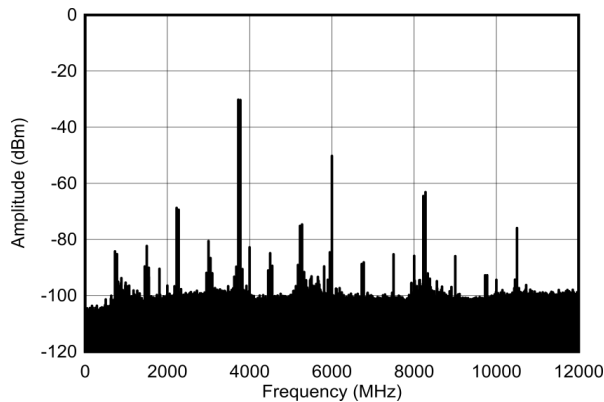
Matching at 3.5 GHz, 50MHz tone spacing,  $f_{\text{DAC}} = 12\text{GSPS}$ , non-interleave mode.

**Figure 6-474. TX Dual Tone Output Spectrum at 3.75 GHz, -13dBFS each (0 -  $f_{\text{DAC}}$ )**



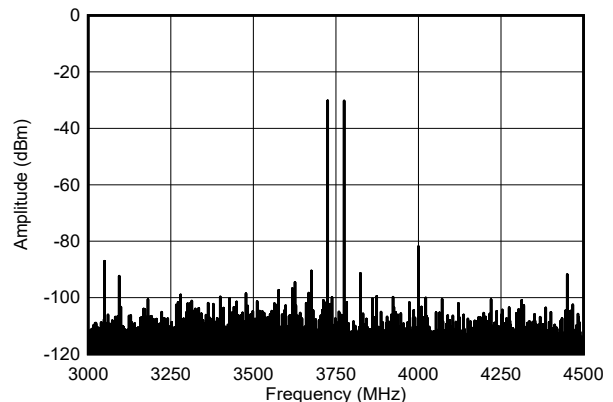
Matching at 3.5 GHz, 50MHz tone spacing,  $f_{\text{DAC}} = 12\text{GSPS}$ , non-interleave mode.

**Figure 6-475. TX Dual Tone Output Spectrum at 3.75 GHz, -13dBFS each ( $\pm 600\text{ MHz}$ )**



Matching at 3.5 GHz, 50MHz tone spacing,  $f_{\text{DAC}} = 12\text{GSPS}$ , non-interleave mode.

**Figure 6-476. TX Dual Tone Output Spectrum at 3.75 GHz, -30dBFS each (0 -  $f_{\text{DAC}}$ )**

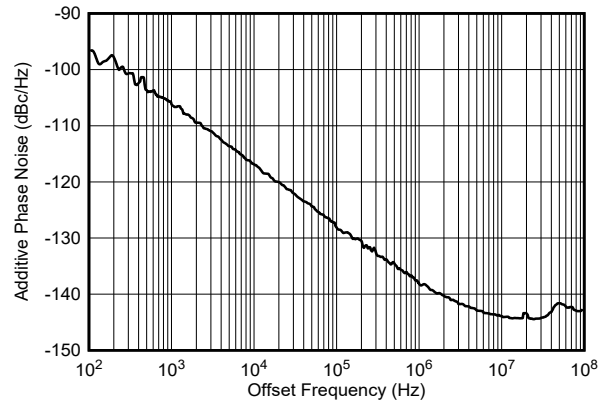


Matching at 3.5 GHz, 50MHz tone spacing,  $f_{\text{DAC}} = 12\text{GSPS}$ , non-interleave mode.

**Figure 6-477. TX Dual Tone Output Spectrum at 3.75 GHz, -30dBFS each ( $\pm 600\text{ MHz}$ )**

### 6.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

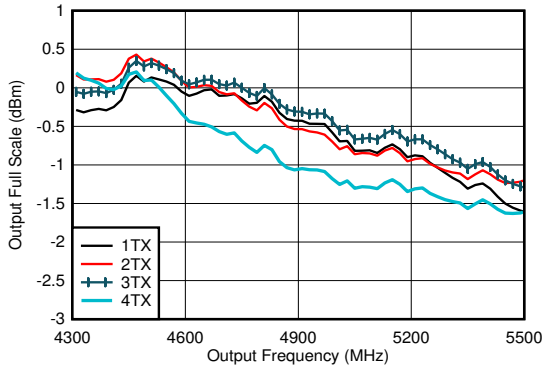


$f_{\text{DAC}} = f_{\text{CLK}} = 12\text{GSPS}$ , non-interleave mode.

**Figure 6-478. External Clock Additive Phase Noise at 3.7GHz**

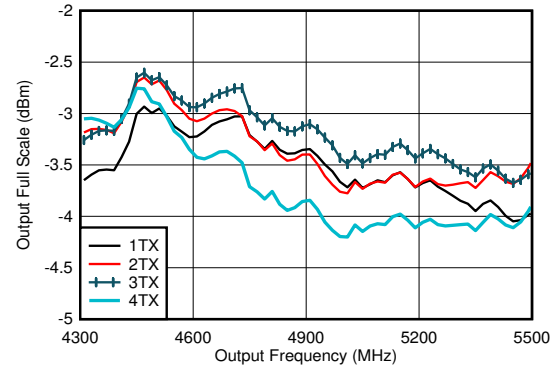
### 6.12.12 TX Typical Characteristics at 4.9GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



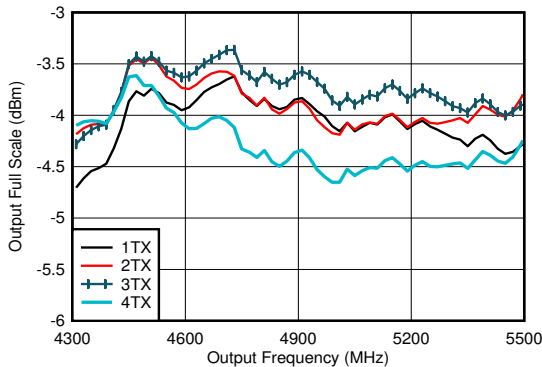
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{dBFS}$ , DSA = 0, 4.9 GHz matching

**Figure 6-479. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS**



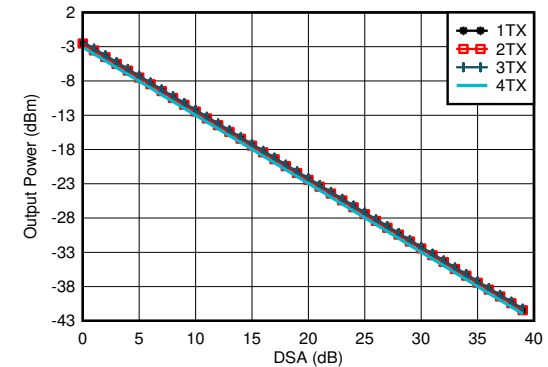
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{dBFS}$ , DSA = 0, 4.9 GHz matching

**Figure 6-480. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode, 2nd Nyquist Zone**



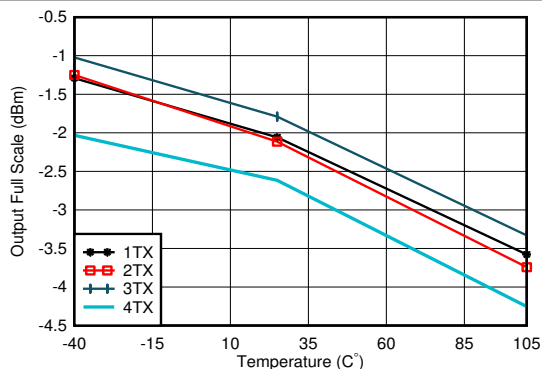
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{dBFS}$ , DSA = 0, 4.9 GHz matching

**Figure 6-481. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode, 2nd Nyquist Zone**



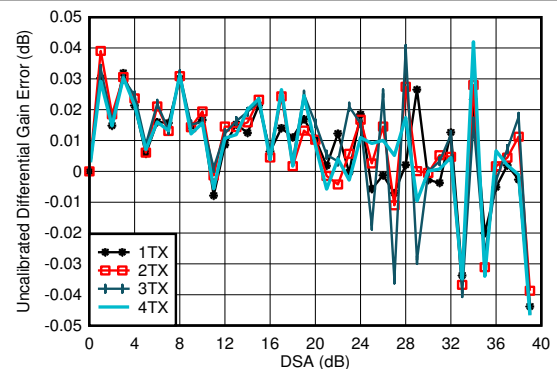
$f_{\text{DAC}} = 11796.48\text{ MSPS}$ ,  $A_{\text{out}} = -0.5\text{dBFS}$ , matching 4.9 GHz

**Figure 6-482. TX Output Power vs DSA Setting and Channel at 4.9 GHz**



$A_{\text{out}} = -0.5\text{dBFS}$ , 4.9 GHz Matching, PCB and cable losses included.

**Figure 6-483. TX Full Scale Output Power vs Temperature and Channel at 4.9 GHz**

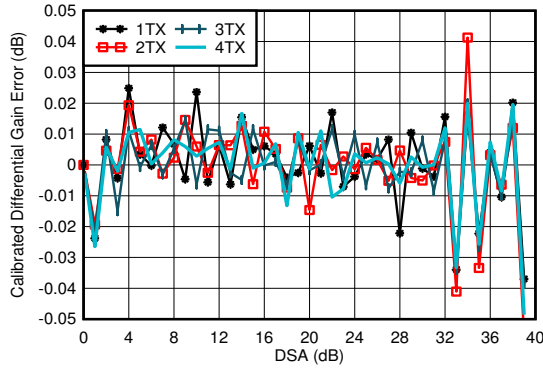


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-484. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz**

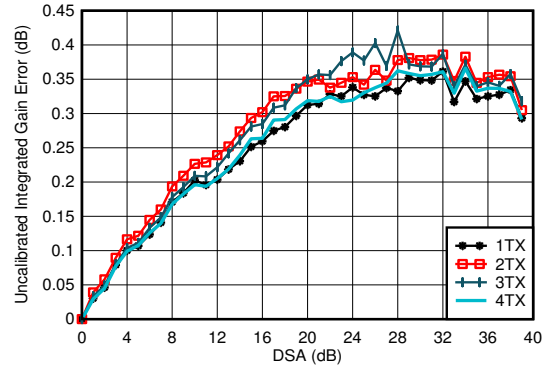
### 6.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



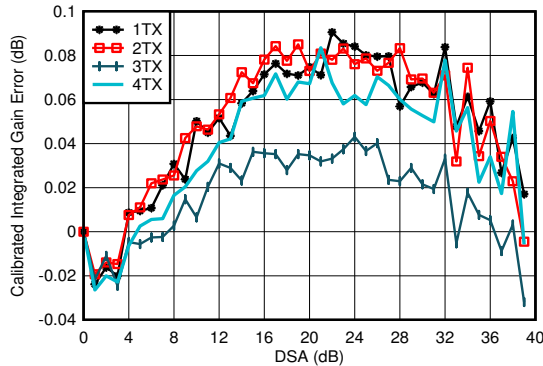
$f_{\text{DAC}}=11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-485. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz**



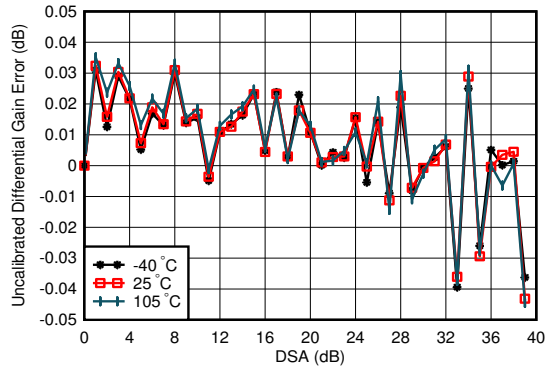
$f_{\text{DAC}}=11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-486. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-487. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz**



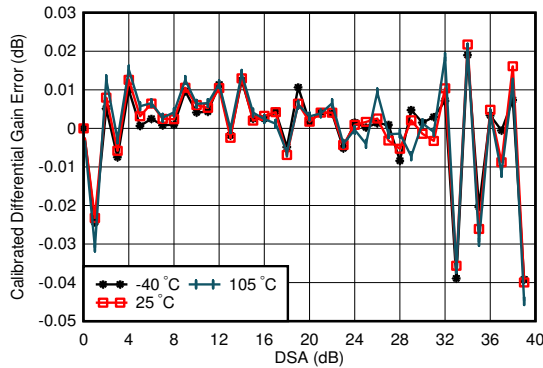
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-488. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz**



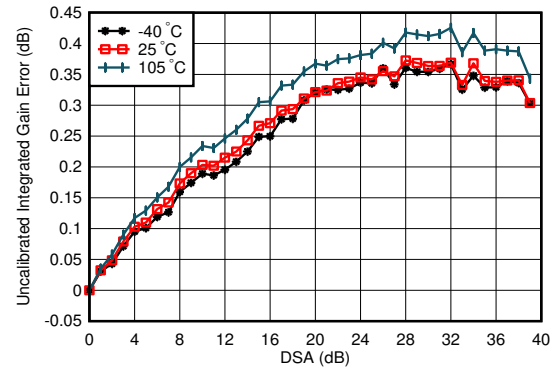
### 6.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



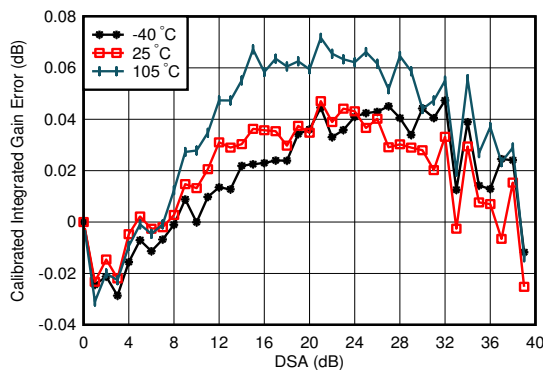
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-489. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz**



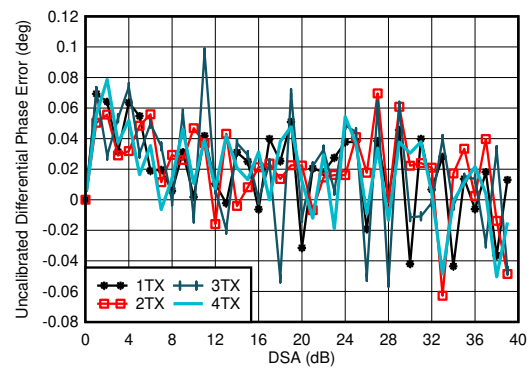
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-490. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-491. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz**

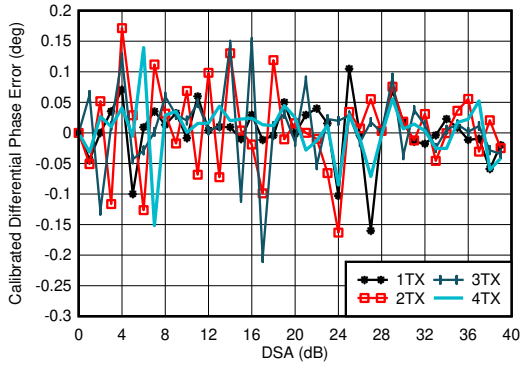


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-492. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz**

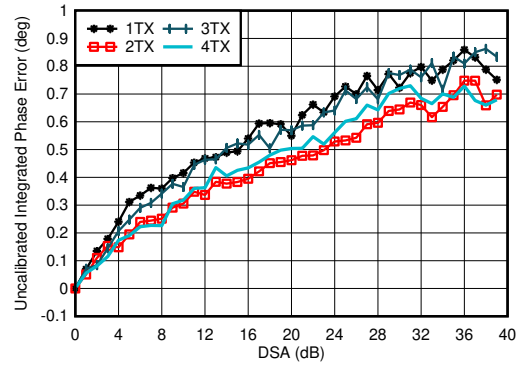
### 6.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



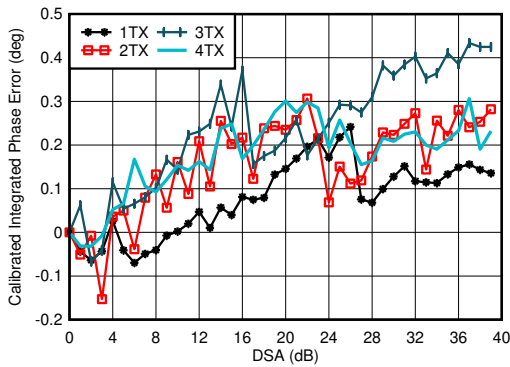
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
 Phase DNL spike may occur at any DSA setting.

**Figure 6-493. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz**



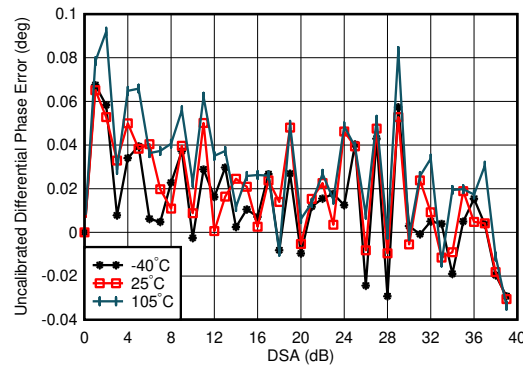
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-494. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-495. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz**

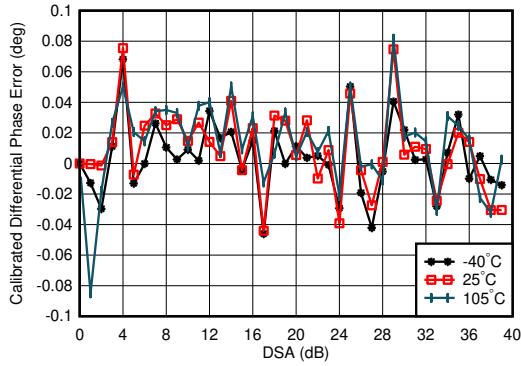


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-496. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz**

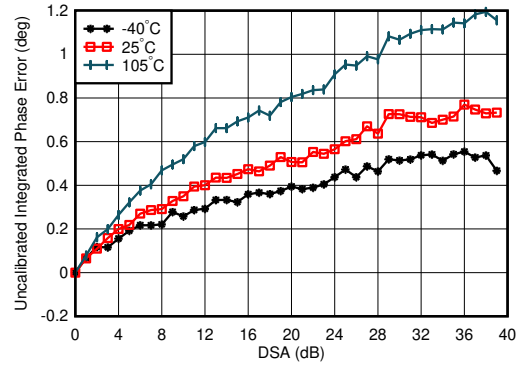
### 6.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



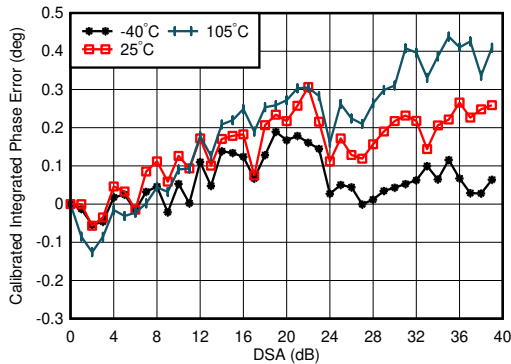
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-497. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz**



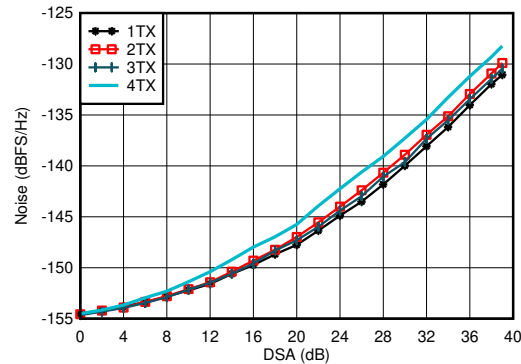
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-498. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-499. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz**

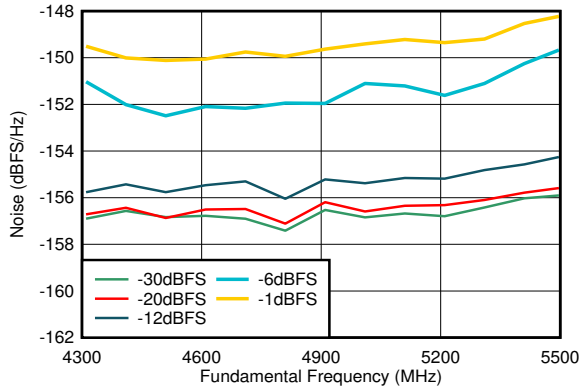


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

**Figure 6-500. TX Output Noise vs Channel and Attenuation at 4.9 GHz**

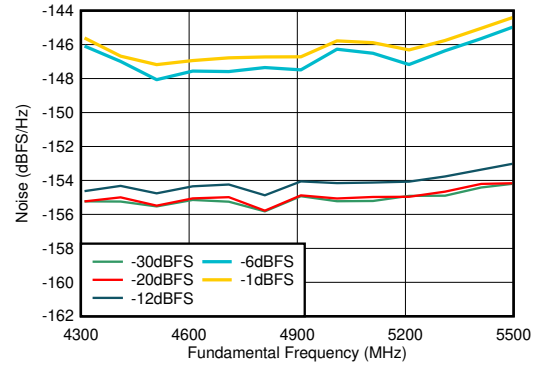
### 6.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



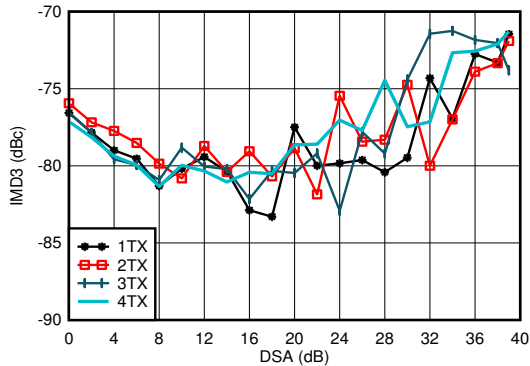
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9GHz,  $A_{\text{out}} = -13\text{ dBFS}$ .

**Figure 6-501. TX NSD vs Output Frequency and Digital Amplitude at 4.9 GHz (DSA=0dB)**



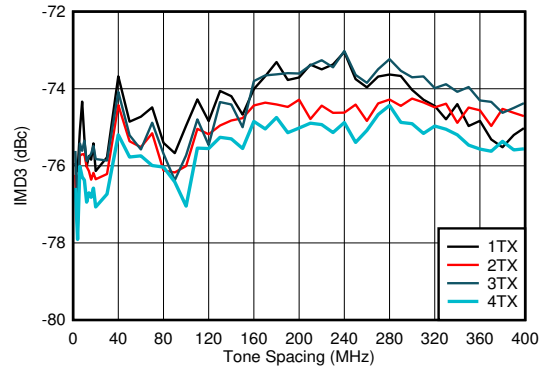
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9GHz,  $A_{\text{out}} = -13\text{ dBFS}$ .

**Figure 6-502. TX NSD vs Output Frequency and Digital Amplitude at 4.9GHz (DSA=6dB)**



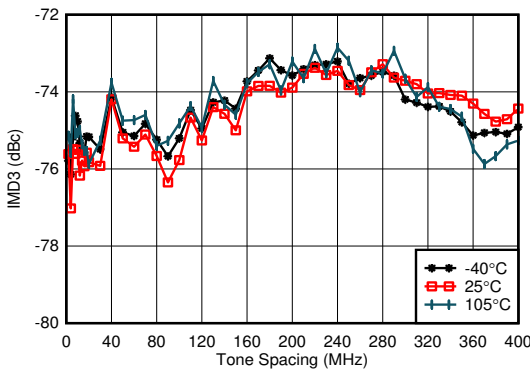
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone

**Figure 6-503. TX IMD3 vs DSA Setting at 4.9 GHz**



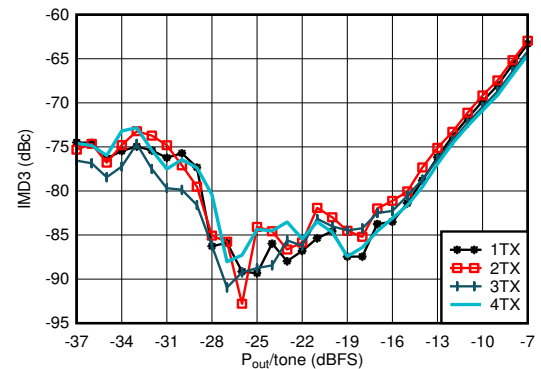
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone

**Figure 6-504. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone, worst channel

**Figure 6-505. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz**

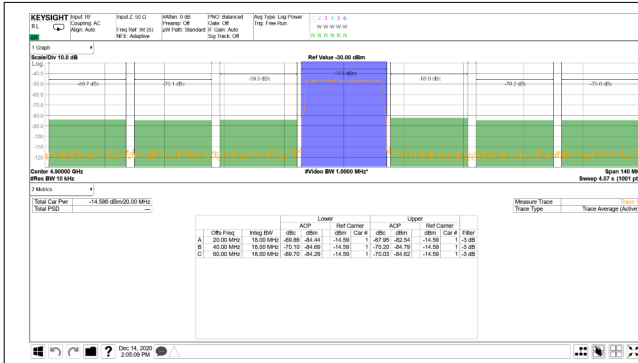


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ ,  $f_{\text{SPACING}} = 20\text{ MHz}$

**Figure 6-506. TX IMD3 vs Digital Level at 4.9 GHz**

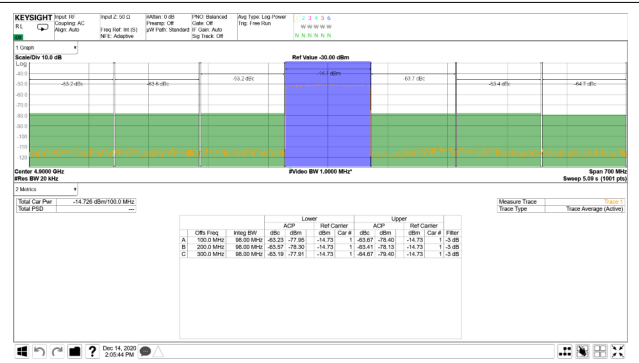
### 6.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



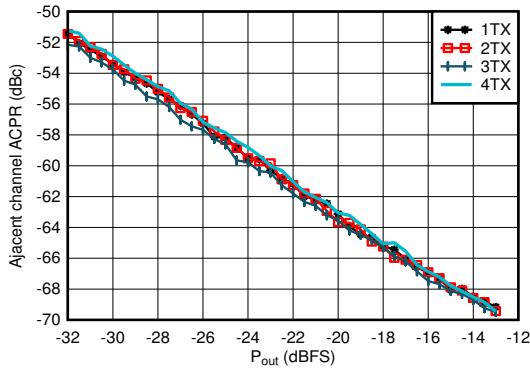
TM1.1,  $P_{\text{OUT\_RMS}} = -13\text{ dBFS}$

Figure 6-507. TX 20-MHz LTE Output Spectrum at 4.9 GHz



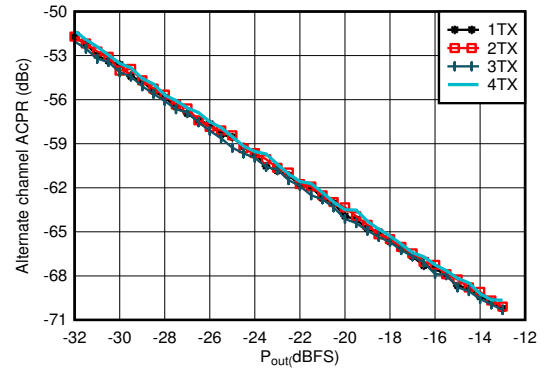
TM1.1,  $P_{\text{OUT\_RMS}} = -13\text{ dBFS}$

Figure 6-508. TX 100-MHz NR Output Spectrum at 4.9 GHz



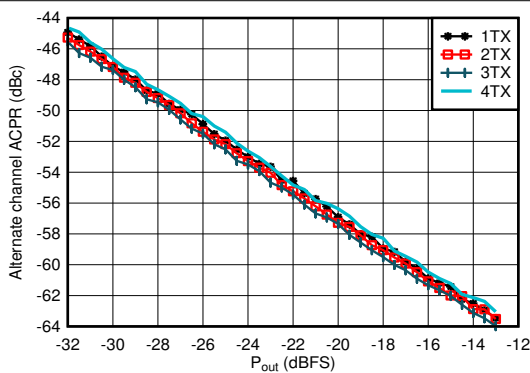
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 6-509. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



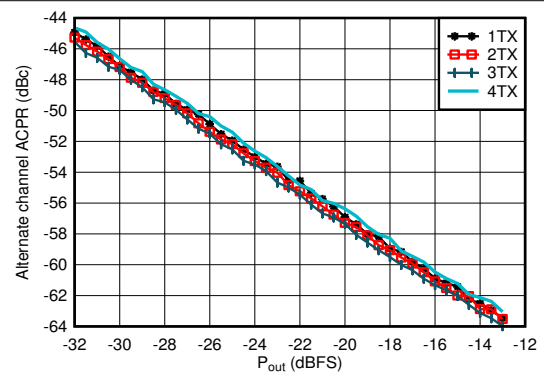
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 6-510. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 6-511. TX 100-MHz NR ACPR vs Digital Level at 4.9 GHz

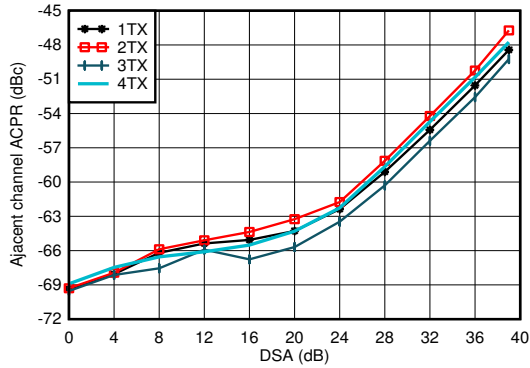


Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

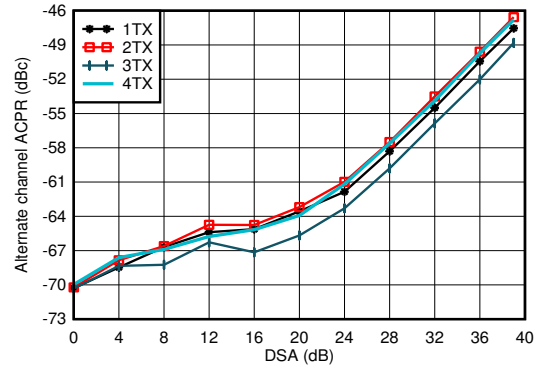
Figure 6-512. TX 100-MHz NR alt-ACPR vs Digital Level at 4.9 GHz

### 6.12.12 TX Typical Characteristics at 4.9GHz (continued)

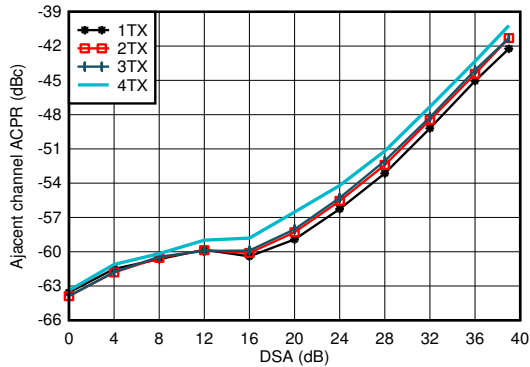
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



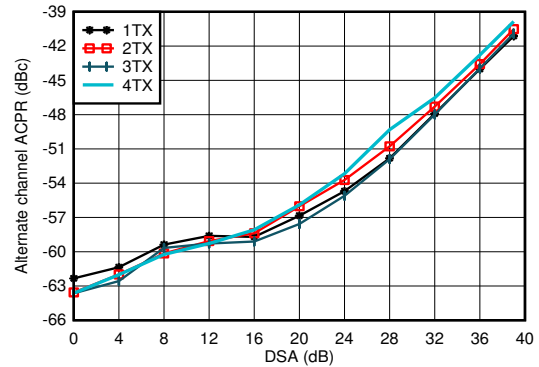
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE  
**Figure 6-513. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz**



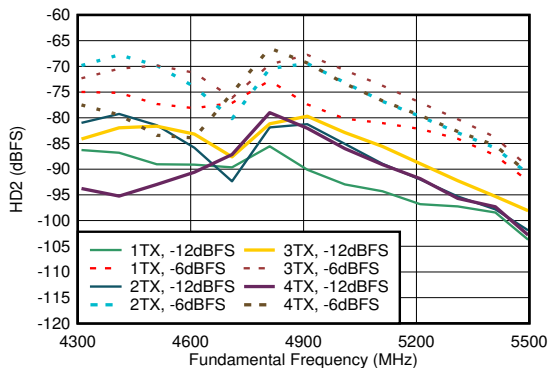
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE  
**Figure 6-514. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz**



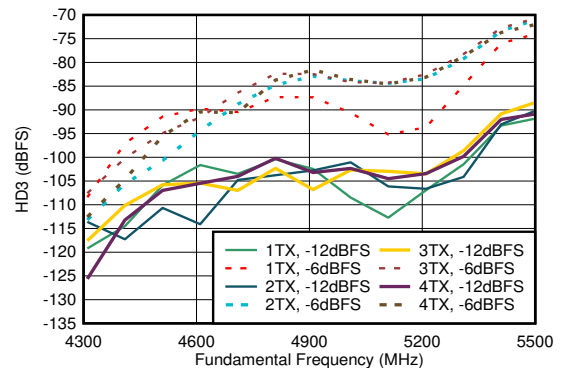
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR  
**Figure 6-515. TX 100-MHz NR ACPR vs DSA at 4.9 GHz**



Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR  
**Figure 6-516. TX 100-MHz NR alt-ACPR vs DSA at 4.9 GHz**



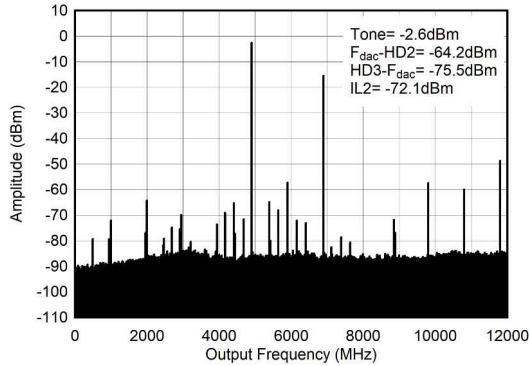
Matching at 4.9 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency  
**Figure 6-517. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz**



Matching at 4.9 GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency  
**Figure 6-518. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz**

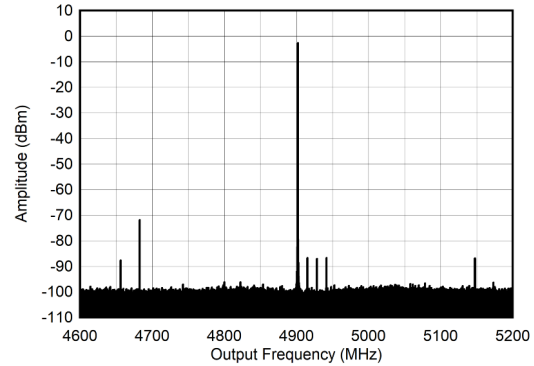
### 6.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{\text{REF}} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



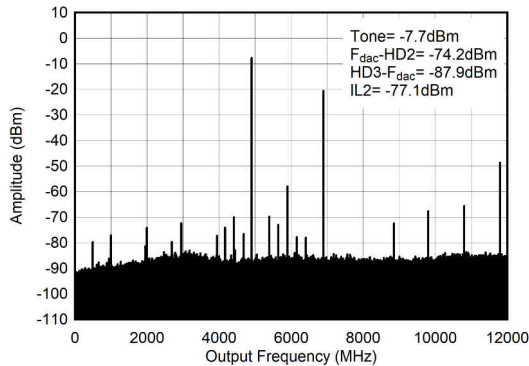
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-519. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz (0- $f_{\text{DAC}}$ )**



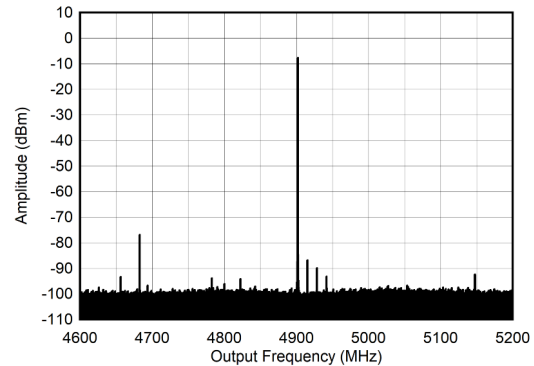
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses

**Figure 6-520. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz ( $\pm 300\text{ MHz}$ )**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-521. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz (0- $f_{\text{DAC}}$ )**

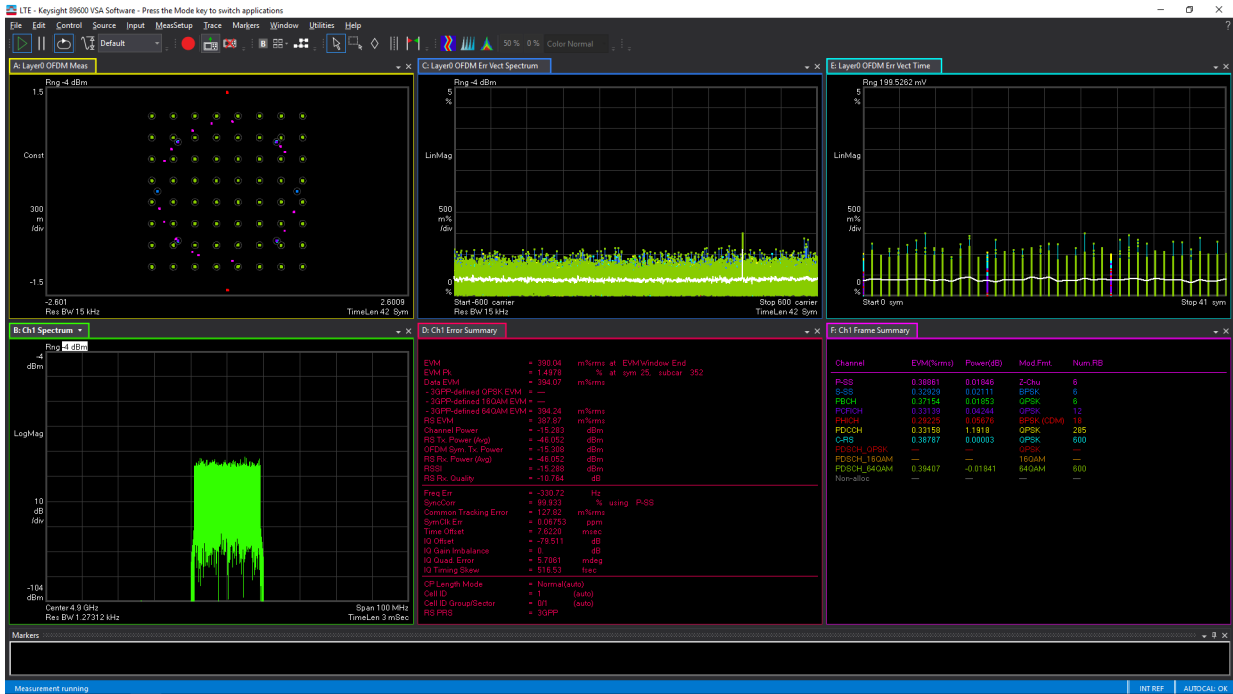
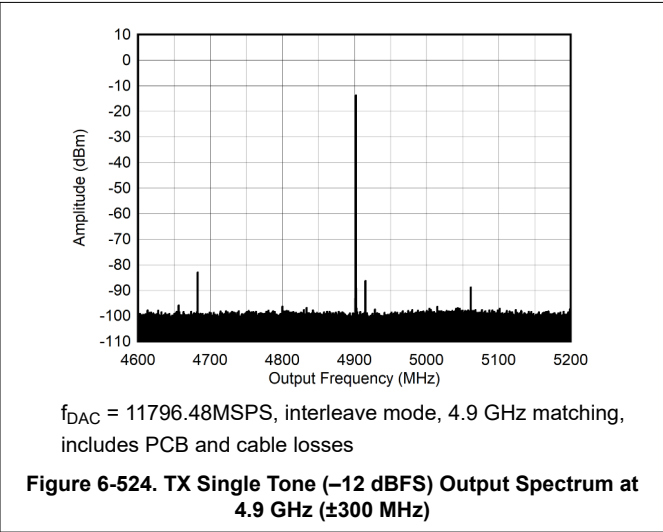
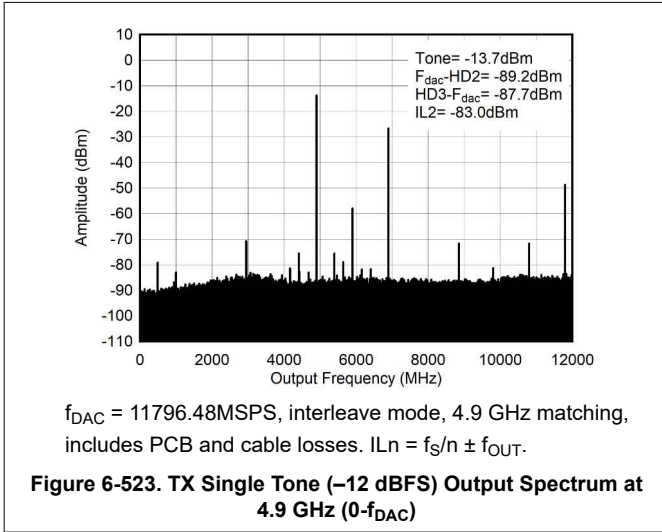


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9 GHz matching, includes PCB and cable losses

**Figure 6-522. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz ( $\pm 300\text{ MHz}$ )**

**6.12.12 TX Typical Characteristics at 4.9GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, Internal PLL,  $f_{REF} = 491.52\text{MSPS}$ , 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

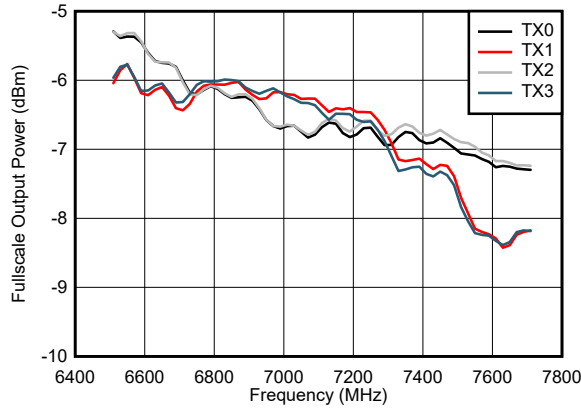


**Figure 6-525. TX 20-MHz LTE Error Vector Magnitude at 4.9 GHz**



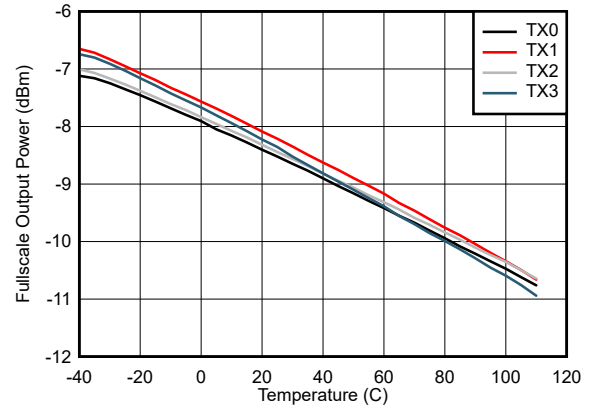
### 6.12.13 TX Typical Characteristics at 7.1GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS,  $f_{DAC} = 9000\text{MSPS}$ , non-interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



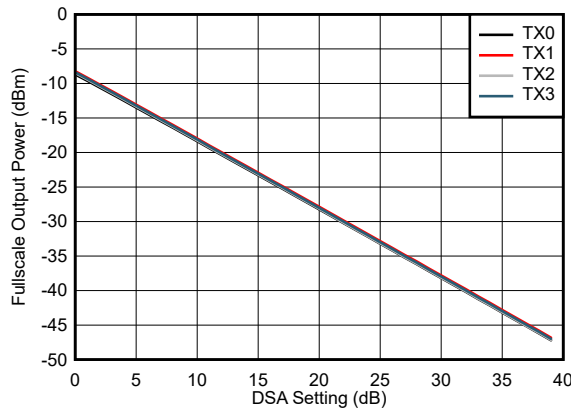
Excluding PCB and cable losses

**Figure 6-526. TX Full Scale vs RF Frequency and Channel**



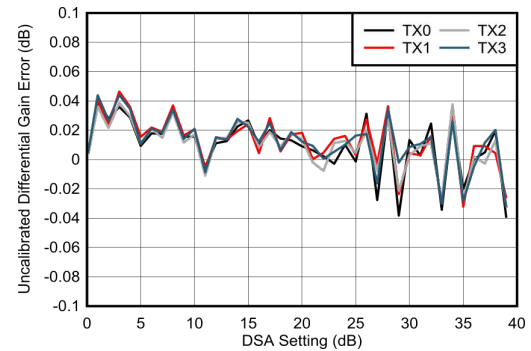
Excluding PCB and cable losses

**Figure 6-527. TX Full Scale vs Temperature and Channel at 7.1GHz**



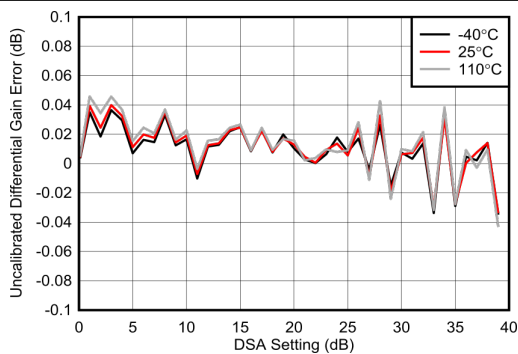
Excluding PCB and cable losses

**Figure 6-528. TX Full Scale vs DSA Setting and Channel at 7.1 GHz**



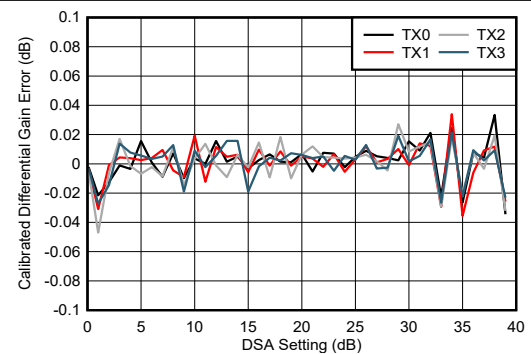
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

**Figure 6-529. Uncalibrated Differential Gain Error vs Channel at 7.1 GHz**



Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

**Figure 6-530. Uncalibrated Differential Gain Error vs Temperature at 7.1 GHz**

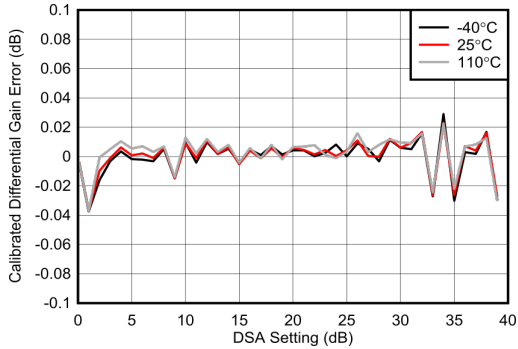


Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

**Figure 6-531. Calibrated Differential Gain Error vs Channel at 7.1 GHz**

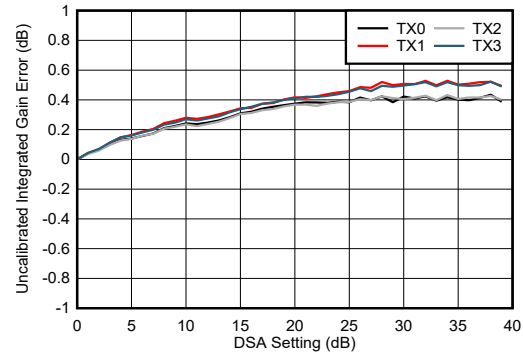
**6.12.13 TX Typical Characteristics at 7.1GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS,  $f_{DAC} = 9000\text{MSPS}$ , non-interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



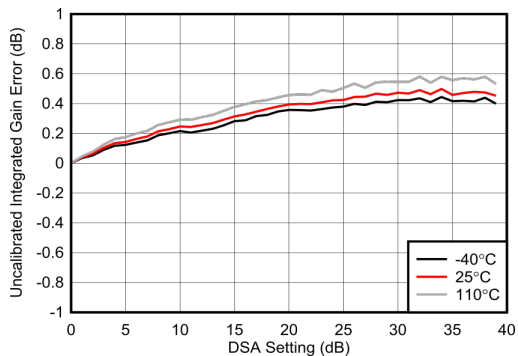
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

**Figure 6-532. Calibrated Differential Gain Error vs Temperature at 7.1 GHz**



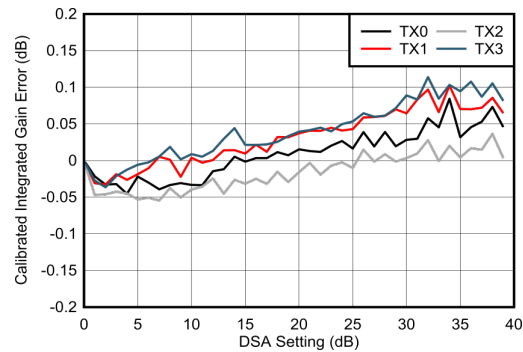
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

**Figure 6-533. Uncalibrated Integrated Gain Error vs Channel at 7.1 GHz**



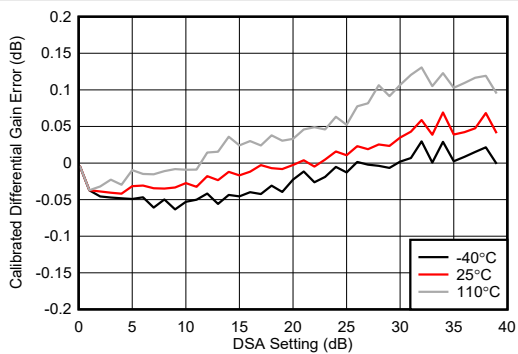
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

**Figure 6-534. Uncalibrated Integrated Gain Error vs Temperature at 7.1 GHz**



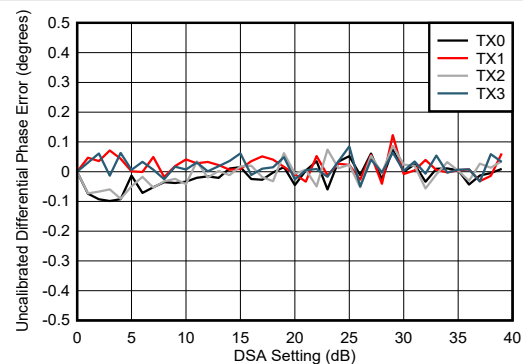
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

**Figure 6-535. Calibrated Integrated Gain Error vs Channel at 7.1 GHz**



Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

**Figure 6-536. Calibrated Integrated Gain Error vs Temperature at 7.1 GHz**

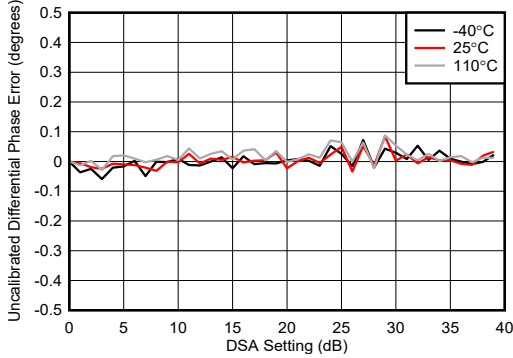


Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

**Figure 6-537. Uncalibrated Differential Phase Error vs Channel at 7.1 GHz**

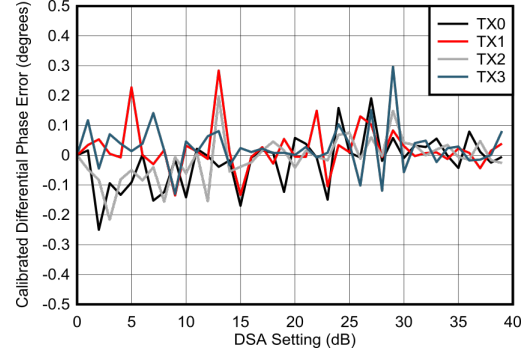
### 6.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS,  $f_{\text{DAC}} = 9000\text{MSPS}$ , non-interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



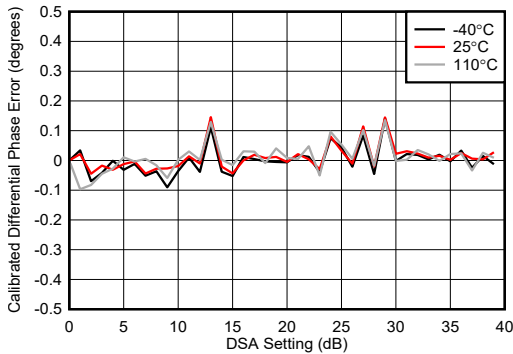
$$\text{Differential Phase Error} = \text{Phase}(\text{DSA Setting} - 1) - \text{Phase}(\text{DSA Setting})$$

**Figure 6-538. Uncalibrated Differential Phase Error vs Temperature at 7.1 GHz**



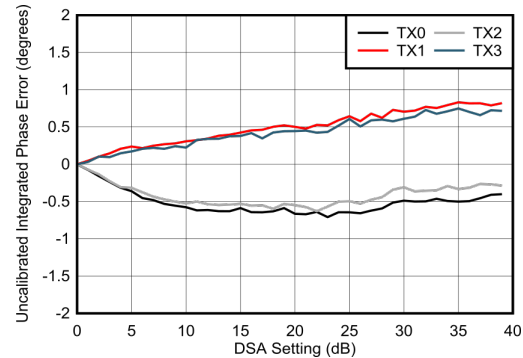
$$\text{Differential Phase Error} = \text{Phase}(\text{DSA Setting} - 1) - \text{Phase}(\text{DSA Setting})$$

**Figure 6-539. Calibrated Differential Phase Error vs Channel at 7.1 GHz**



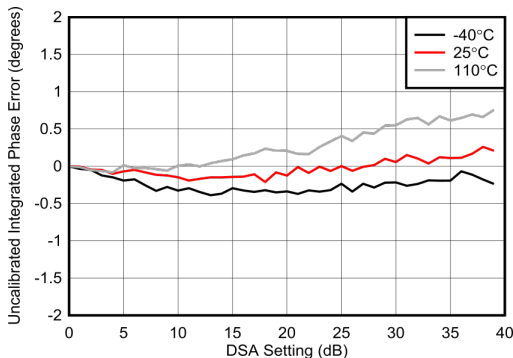
$$\text{Differential Phase Error} = \text{Phase}(\text{DSA Setting} - 1) - \text{Phase}(\text{DSA Setting})$$

**Figure 6-540. Calibrated Differential Phase Error vs Temperature at 7.1 GHz**



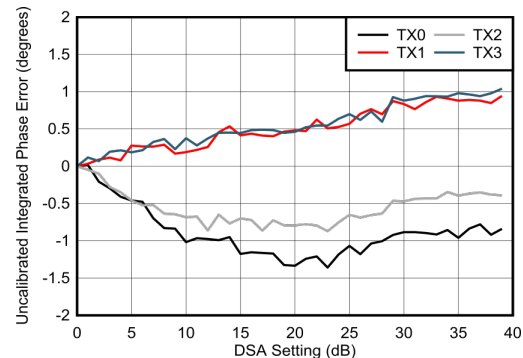
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 6-541. Uncalibrated Integrated Phase Error vs Channel at 7.1 GHz**



$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 6-542. Uncalibrated Integrated Phase Error vs Temperature at 7.1 GHz**

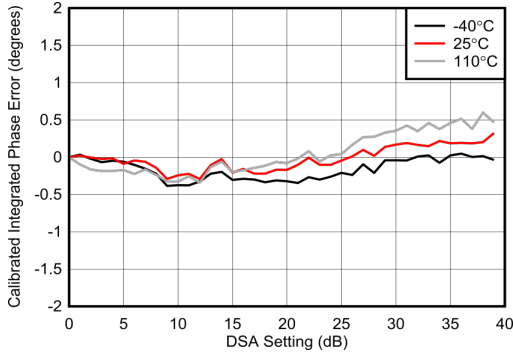


$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 6-543. Calibrated Integrated Phase Error vs Channel at 7.1 GHz**

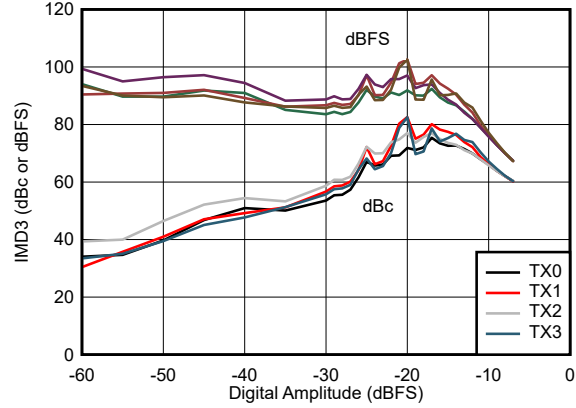
### 6.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS,  $f_{DAC} = 9000\text{MSPS}$ , non-interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



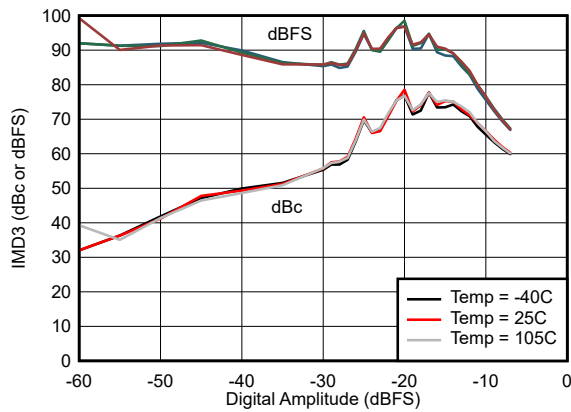
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 6-544. Calibrated Integrated Phase Error vs Temperature at 7.1 GHz



Tone spacing = 50MHz

Figure 6-545. IMD3 vs Digital Amplitude and Channel at 7.1 GHz



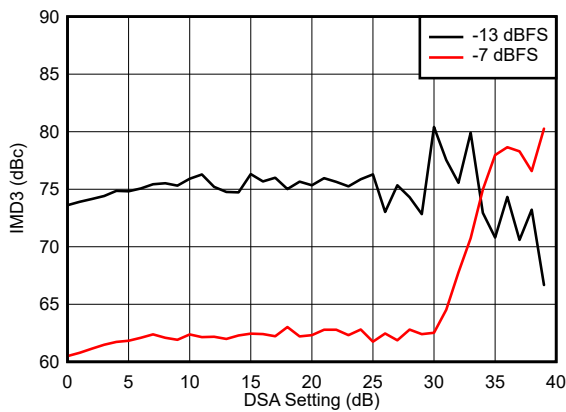
Tone spacing = 50MHz

Figure 6-546. IMD3 vs Digital Amplitude and Temperature at 7.1 GHz



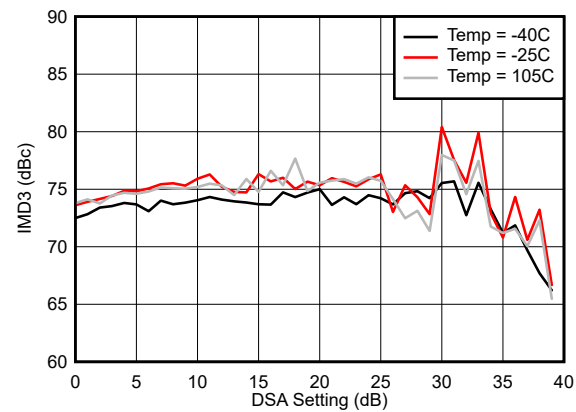
Tone spacing = 50MHz

Figure 6-547. IMD3 vs DSA Setting and Channel at 7.1 GHz



Tone spacing = 50MHz

Figure 6-548. IMD3 vs DSA Setting and Digital Amplitude at 7.1 GHz



Tone spacing = 50MHz

Figure 6-549. IMD3 vs DSA Setting and Temperature at 7.1 GHz

### 6.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS,  $f_{DAC} = 9000\text{MSPS}$ , non-interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.

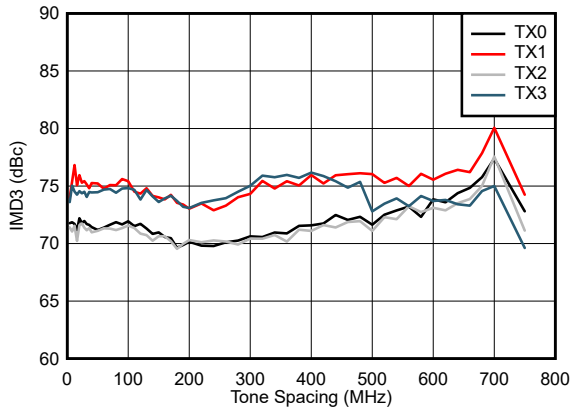


Figure 6-550. IMD3 vs Tone Spacing and Channel at 7.1 GHz

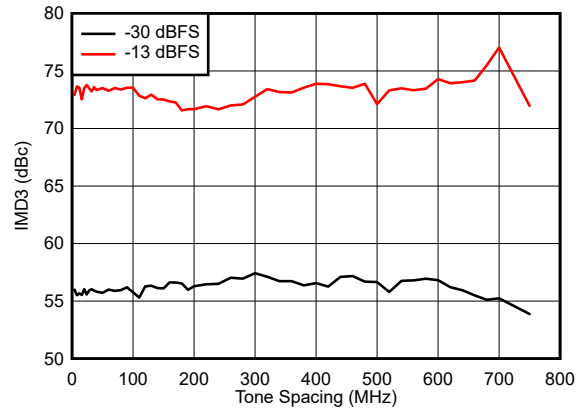


Figure 6-551. IMD3 vs Tone Spacing and Digital Amplitude at 7.1 GHz

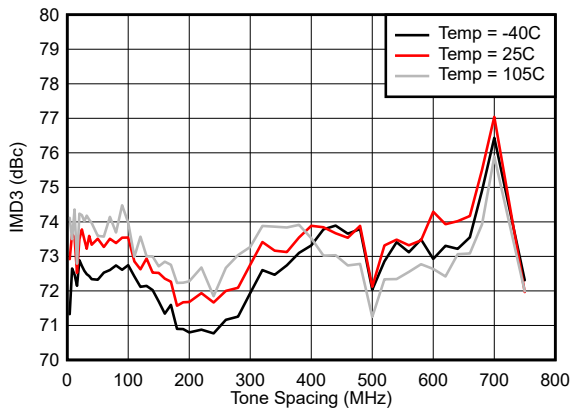
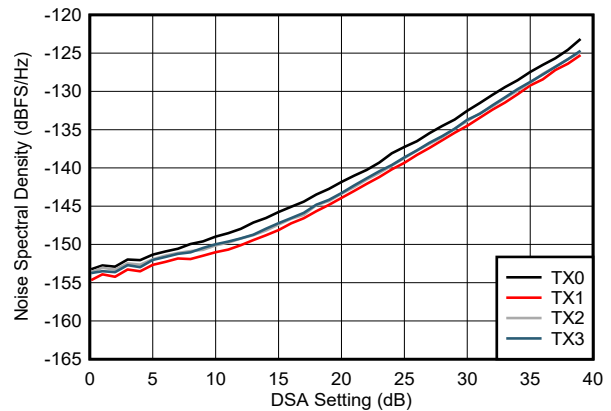
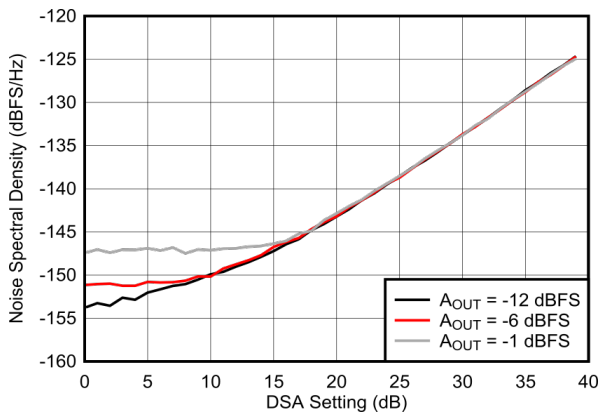


Figure 6-552. IMD3 vs Tone Spacing and Temperature at 7.1 GHz



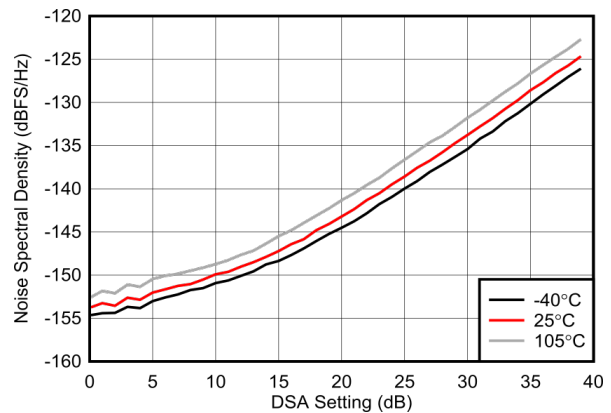
Tone at -12dBFS, 50MHz offset from tone

Figure 6-553. NSD vs DSA Setting and Channel at 7.1 GHz



50MHz offset from tone

Figure 6-554. NSD vs DSA Setting and Amplitude at 7.1 GHz

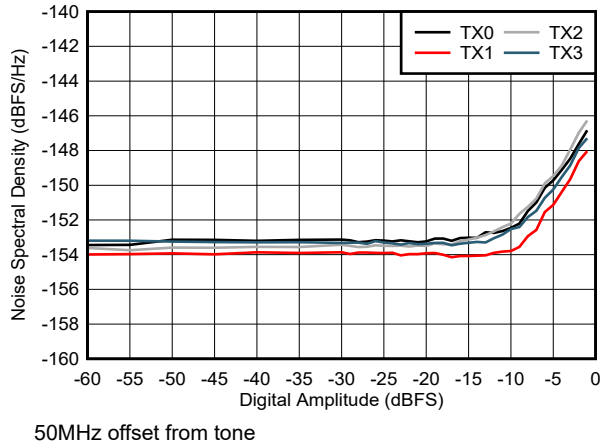


Tone at -12dBFS, 50MHz offset from tone

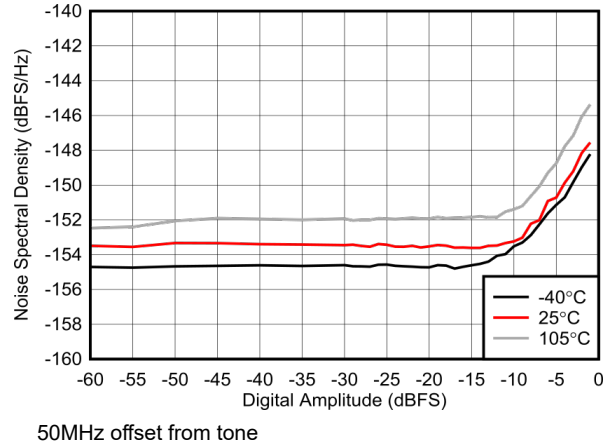
Figure 6-555. NSD vs DSA Setting and Temperature at 7.1 GHz

**6.12.13 TX Typical Characteristics at 7.1GHz (continued)**

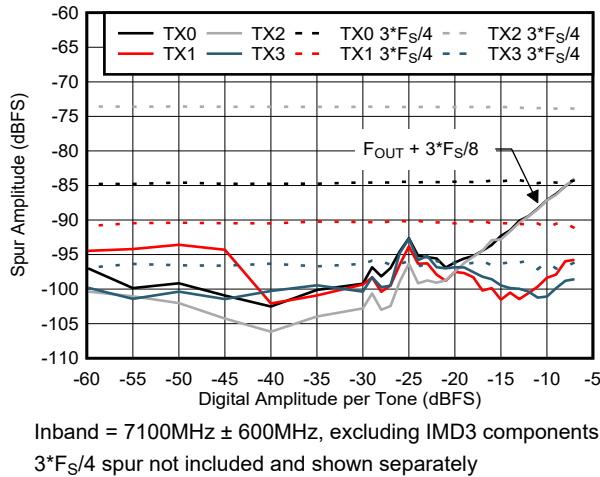
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS,  $f_{DAC} = 9000\text{MSPS}$ , non-interleave mode,  $A_{OUT} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



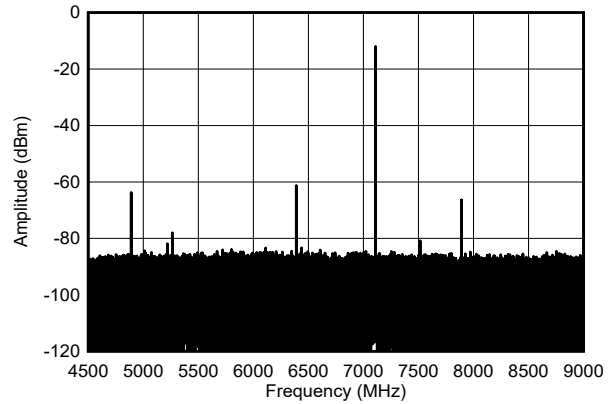
**Figure 6-556. NSD vs Digital Amplitude and Channel at 7.1 GHz**



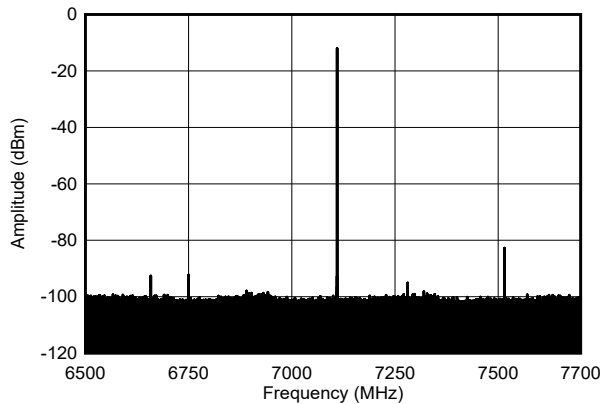
**Figure 6-557. NSD vs Digital Amplitude and Temperature at 7.1 GHz**



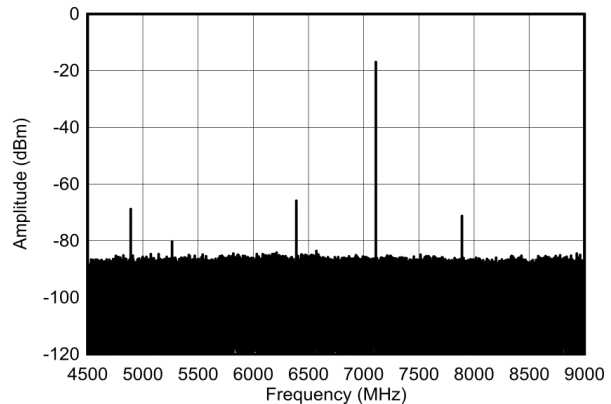
**Figure 6-558. Two Tone Inband SFDR vs Digital Amplitude at 7.1 GHz**



**Figure 6-559. Single Tone Output Spectrum at 7.1GHz, -1dBFS (Nyquist)**



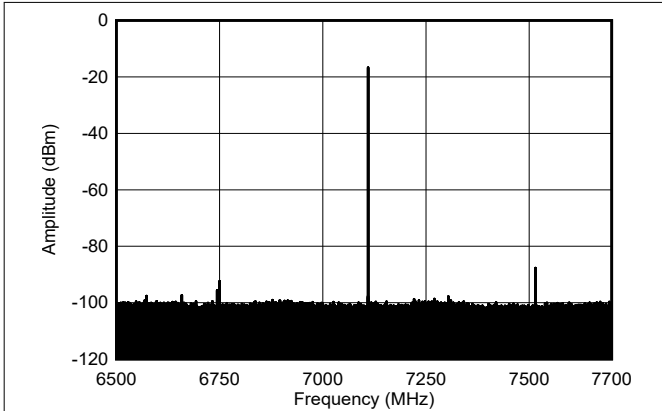
**Figure 6-560. Single Tone Output Spectrum at 7.1GHz, -1dBFS (Inband)**



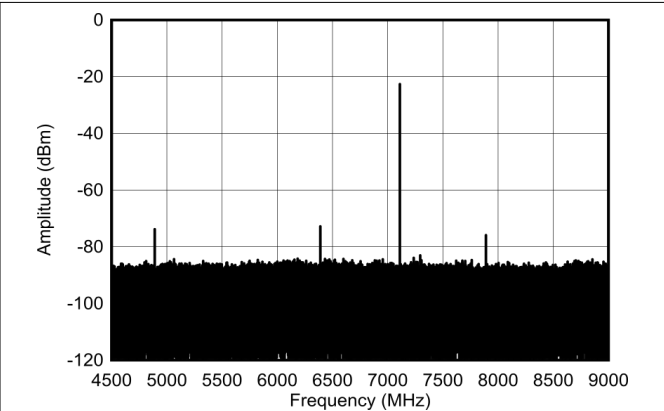
**Figure 6-561. Single Tone Output Spectrum at 7.1GHz, -6dBFS (Nyquist)**

### 6.12.13 TX Typical Characteristics at 7.1GHz (continued)

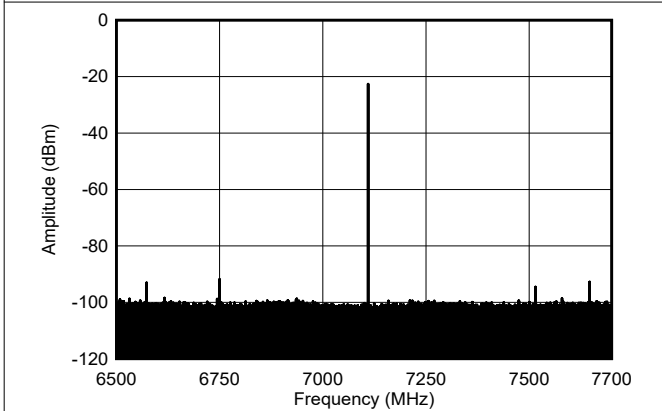
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS,  $f_{\text{DAC}} = 9000\text{MSPS}$ , non-interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



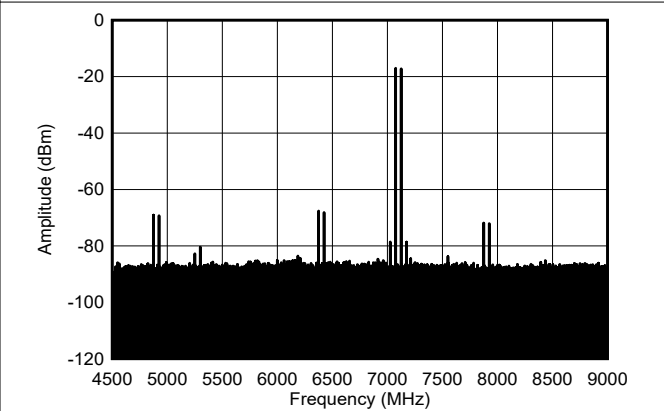
**Figure 6-562. Single Tone Output Spectrum at 7.1GHz, -6dBFS (Inband)**



**Figure 6-563. Single Tone Output Spectrum at 7.1GHz, -12dBFS (Nyquist)**

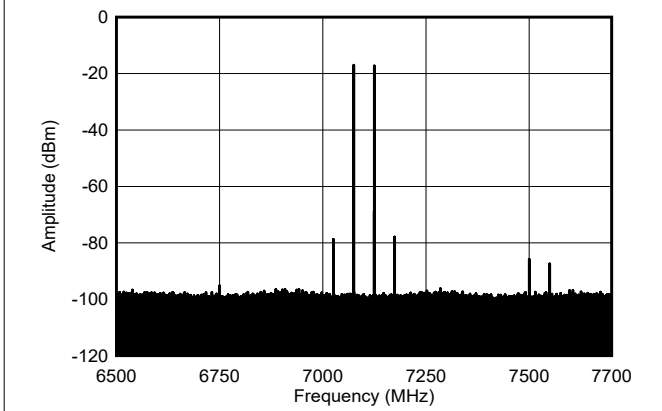


**Figure 6-564. Single Tone Output Spectrum at 7.1GHz, -12dBFS (Inband)**



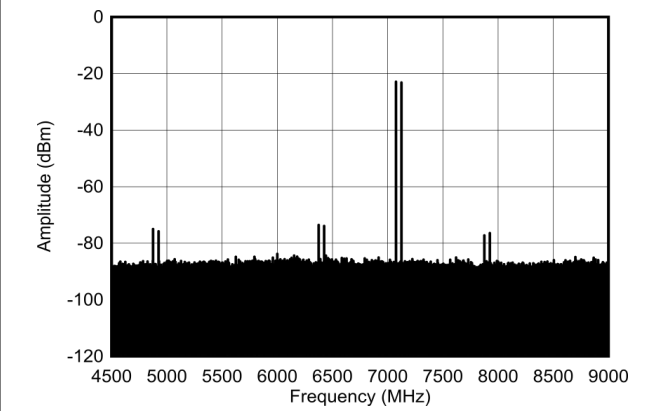
50MHz Tone Spacing

**Figure 6-565. Two Tone Output Spectrum at 7.1GHz, -7dBFS each (Nyquist)**



50MHz Tone Spacing

**Figure 6-566. Two Tone Output Spectrum at 7.1GHz, -7dBFS each (Inband)**

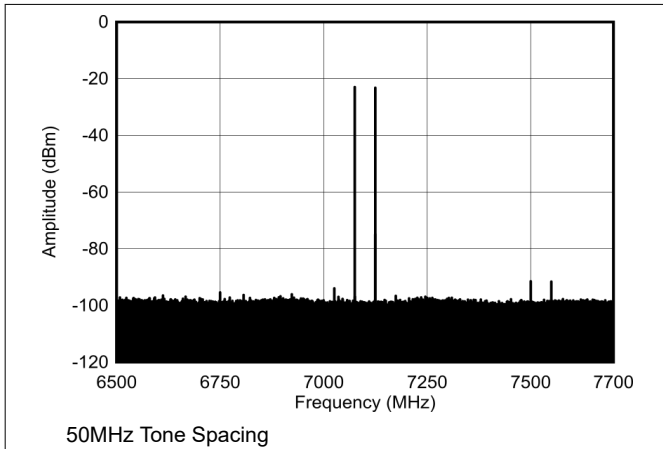


50MHz Tone Spacing

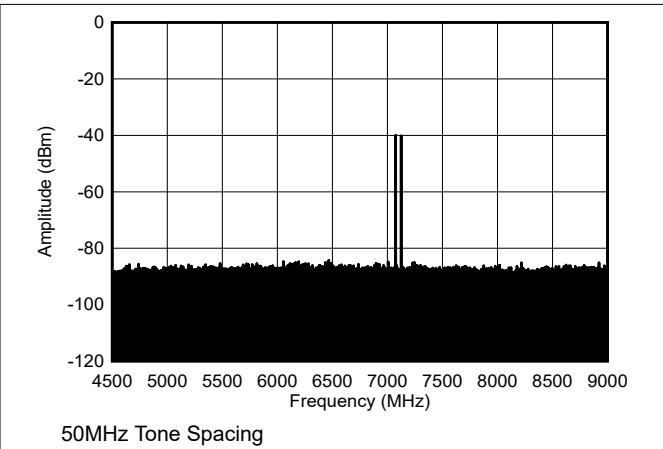
**Figure 6-567. Two Tone Output Spectrum at 7.1GHz, -13dBFS each (Nyquist)**

### 6.12.13 TX Typical Characteristics at 7.1GHz (continued)

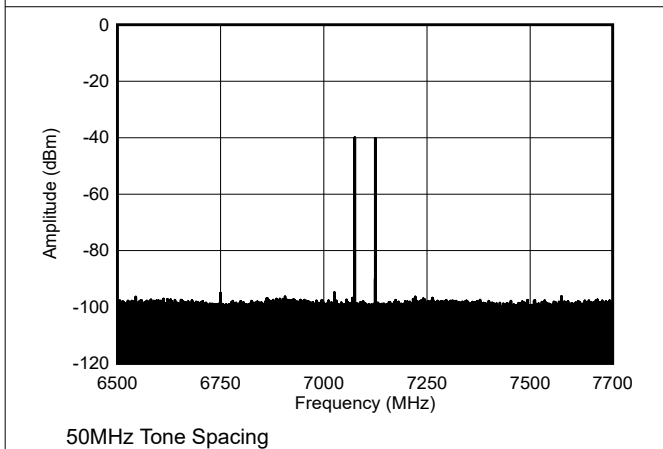
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS,  $f_{\text{DAC}} = 9000\text{MSPS}$ , non-interleave mode,  $A_{\text{OUT}} = -1\text{ dBFS}$ , 1<sup>st</sup> Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



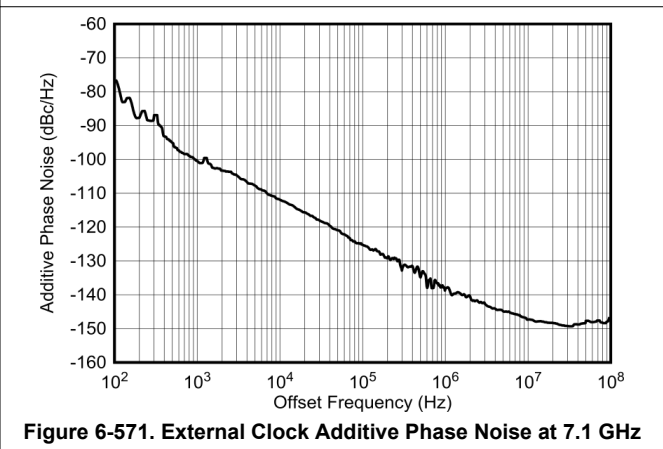
**Figure 6-568. Two Tone Output Spectrum at 7.1GHz, -13dBFS each (Inband)**



**Figure 6-569. Two Tone Output Spectrum at 7.1GHz, -30dBFS each (Nyquist)**



**Figure 6-570. Two Tone Output Spectrum at 7.1GHz, -30dBFS each (Inband)**

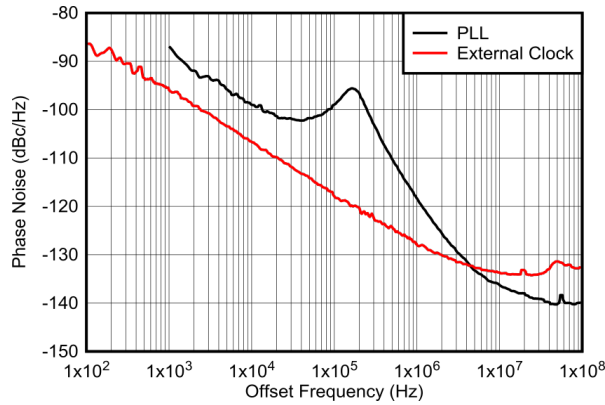


**Figure 6-571. External Clock Additive Phase Noise at 7.1 GHz**



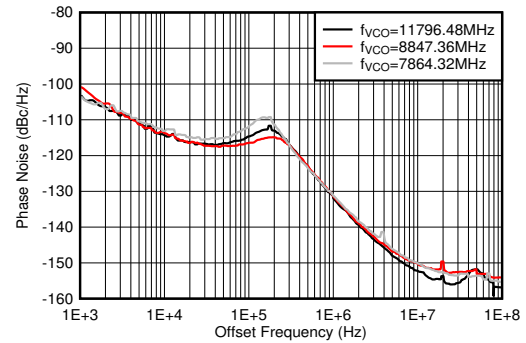
### 6.12.14 PLL and Clock Typical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted,  $f_{\text{REF}} = 491.52 \text{ MHz}$ , Phase noise measured at TX output



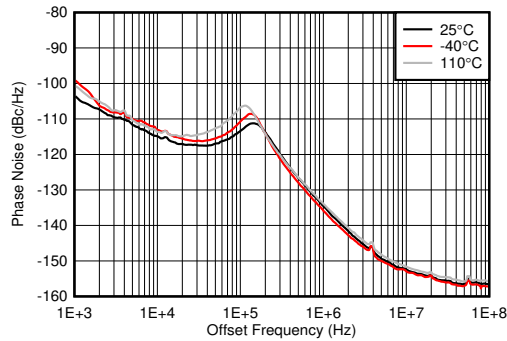
measured at TX output, normalized to 12GHz by  $20 \cdot \log_{10}(12\text{GHz}/F_{\text{OUT}})$

**Figure 6-572. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz**



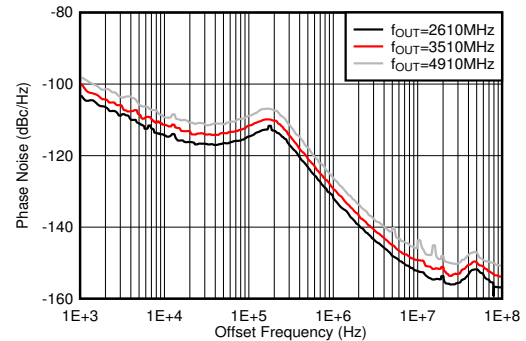
PLL enabled,  $f_{\text{REF}} = 491.52\text{MSPS}$ , measured at 2TXOUT

**Figure 6-573. Phase Noise vs Offset Frequency and  $f_{\text{VCO}}$  at  $f_{\text{OUT}} = 2610 \text{ MHz}$**



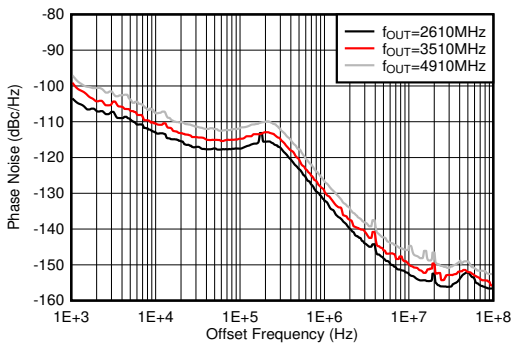
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52\text{MSPS}$ , measured at 2TXOUT

**Figure 6-574. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at  $f_{\text{OUT}} = 1910 \text{ MHz}$**



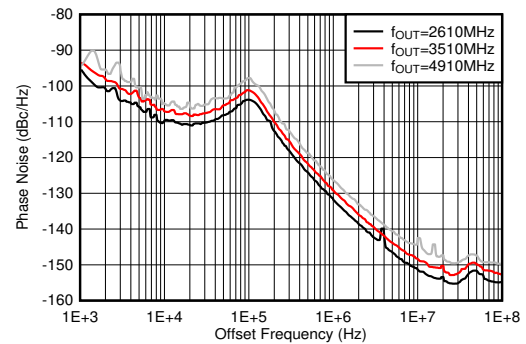
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52\text{MSPS}$ , measured at 2TXOUT

**Figure 6-575. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{\text{OUT}}$  at  $25^\circ\text{C}$**



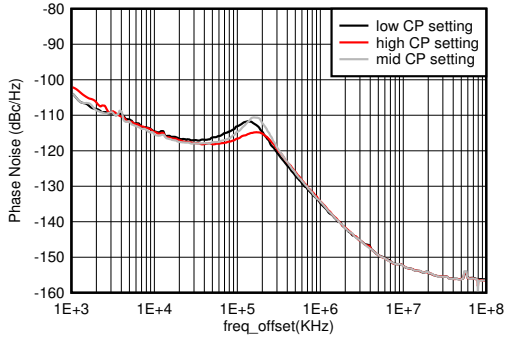
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52\text{MSPS}$ , measured at 2TXOUT

**Figure 6-576. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{\text{OUT}}$  at  $-40^\circ\text{C}$**



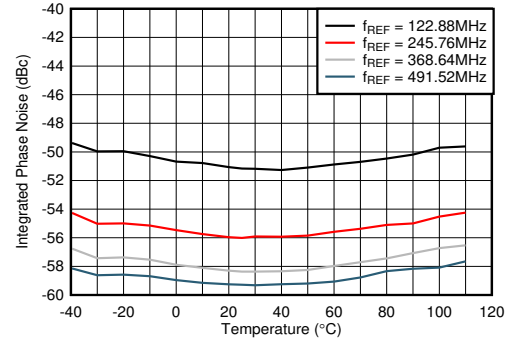
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52\text{MSPS}$ , measured at 2TXOUT

**Figure 6-577. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{\text{OUT}}$  at  $110^\circ\text{C}$**



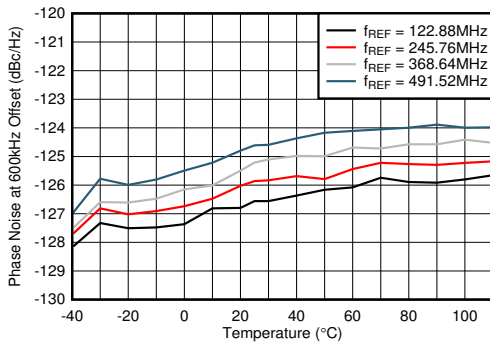
PLL enabled,  $f_{VCO} = 11796.48$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-578. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at  $f_{OUT} = 2.6$  GHz**



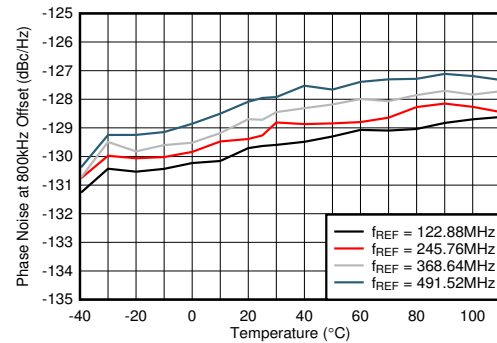
PLL enabled,  $f_{VCO} = 11796.48$  MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

**Figure 6-579. Integrated Phase Noise for 12-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



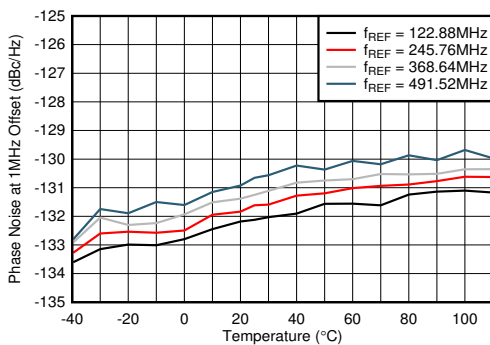
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 6-580. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



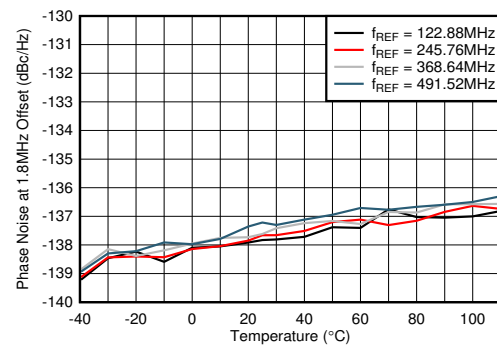
A. PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 6-581. Phase Noise for 12-GHz VCO at 800kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



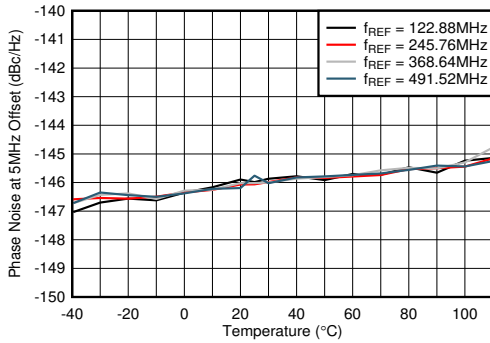
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 6-582. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



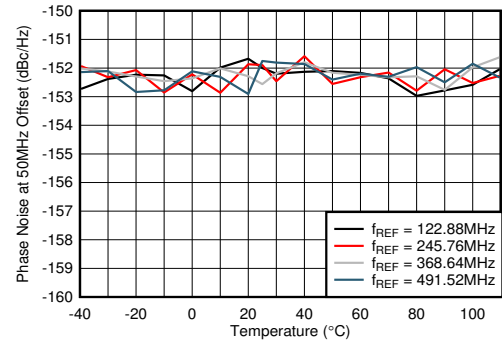
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 6-583. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



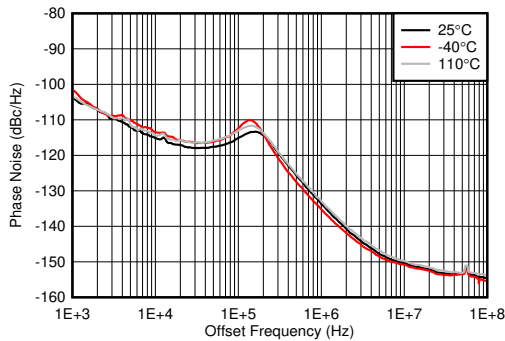
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 6-584. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



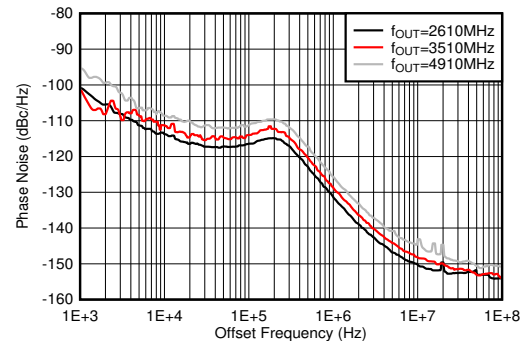
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**Figure 6-585. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



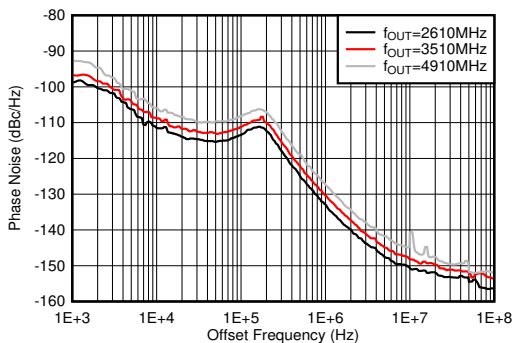
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-586. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**



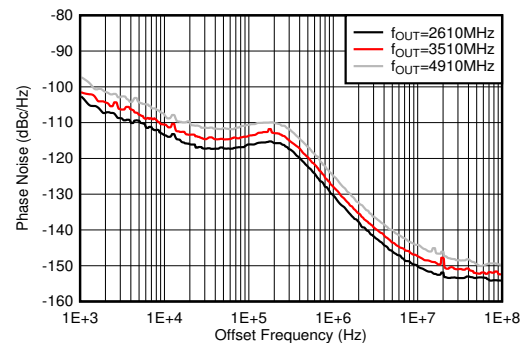
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-587. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 25°C**



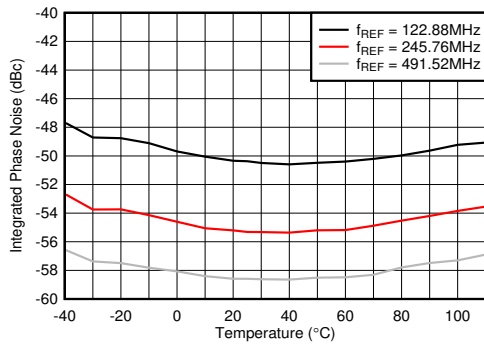
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-588. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at -40°C**



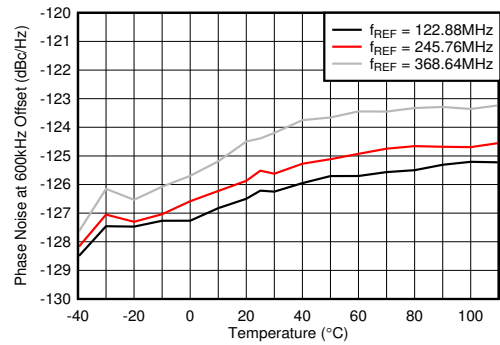
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-589. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 110°C**



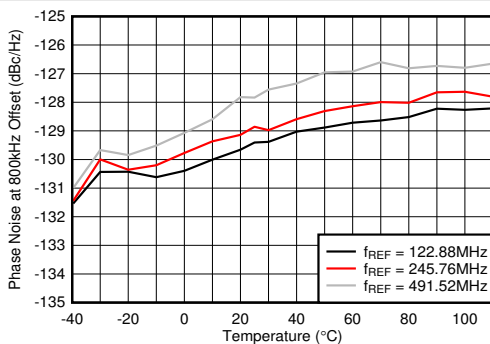
PLL enabled,  $f_{VCO} = 9830.4$  MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

**Figure 6-590. Integrated Phase Noise for 10-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



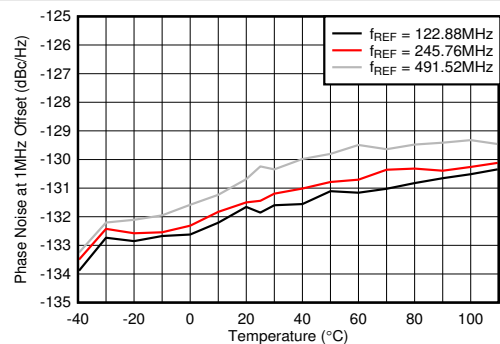
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 6-591. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



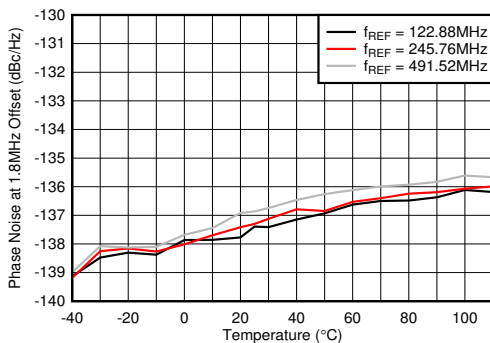
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 6-592. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



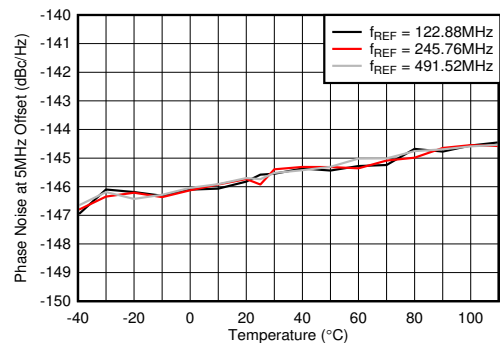
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 6-593. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



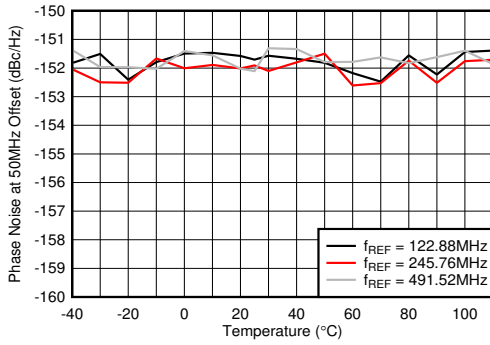
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 6-594. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



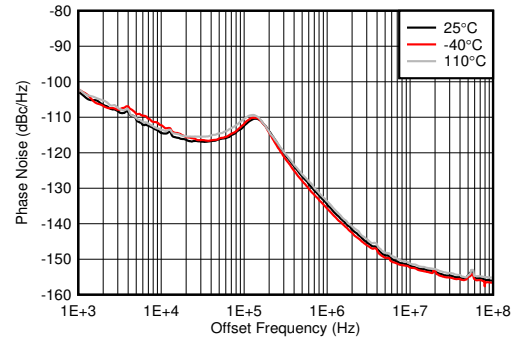
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 6-595. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



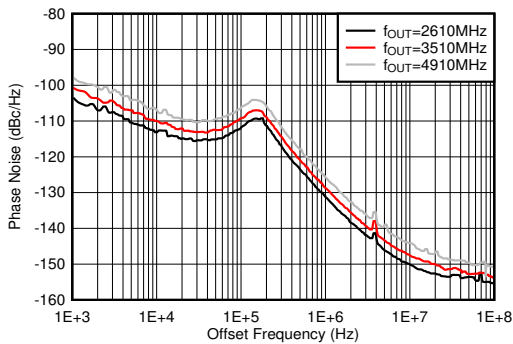
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**Figure 6-596. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



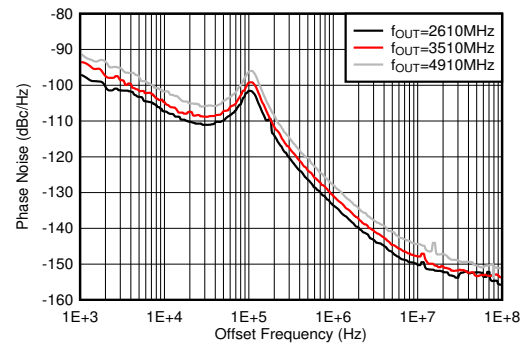
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-597. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**



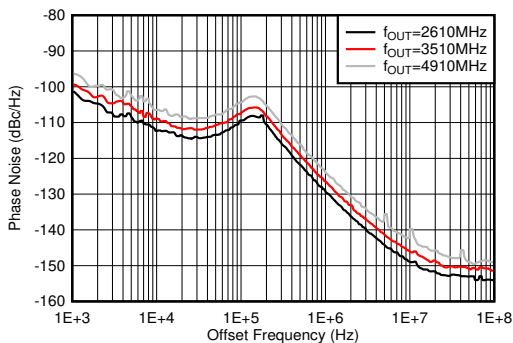
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-598. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 25°C**



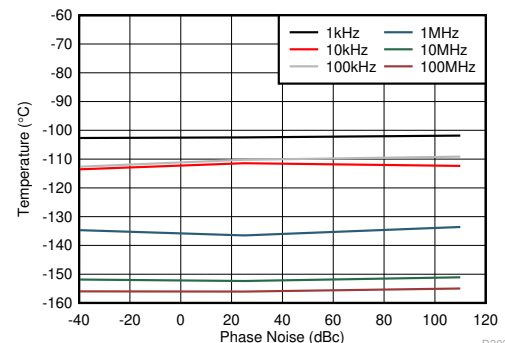
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-599. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at -40°C**



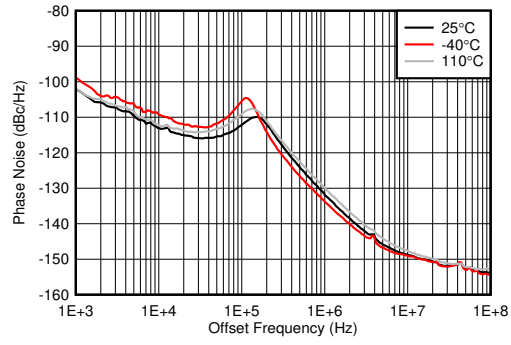
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-600. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 110°C**



PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, minimum LPF BW, measured at 2TXOUT

**Figure 6-601. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at  $f_{OUT} = 2.6$  GHz**



PLL enabled,  $f_{VCO} = 7864.32$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**Figure 6-602. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**

## 7 Device and Documentation Support

### 7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 7.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7900IABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7900I	<a href="#">Samples</a>
AFE7900IALK	ACTIVE	FCBGA	ALK	400	90	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7900 SNPB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

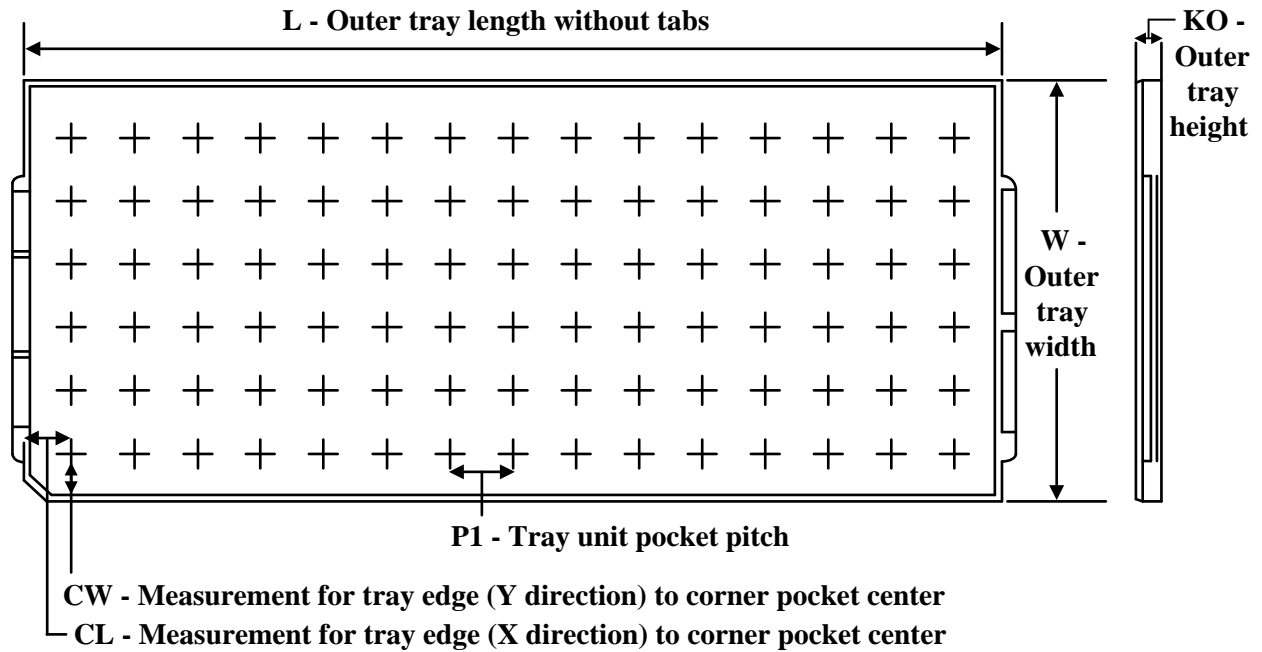
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





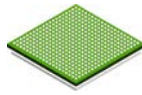
**TRAY**


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7900IABJ	ABJ	FCBGA	400	90	6 x 16	150	315	135.9	7620	19.5	21	19.2
AFE7900IALK	ALK	FCBGA	400	90	6 x 16	150	315	135.9	7620	19.5	21	19.2

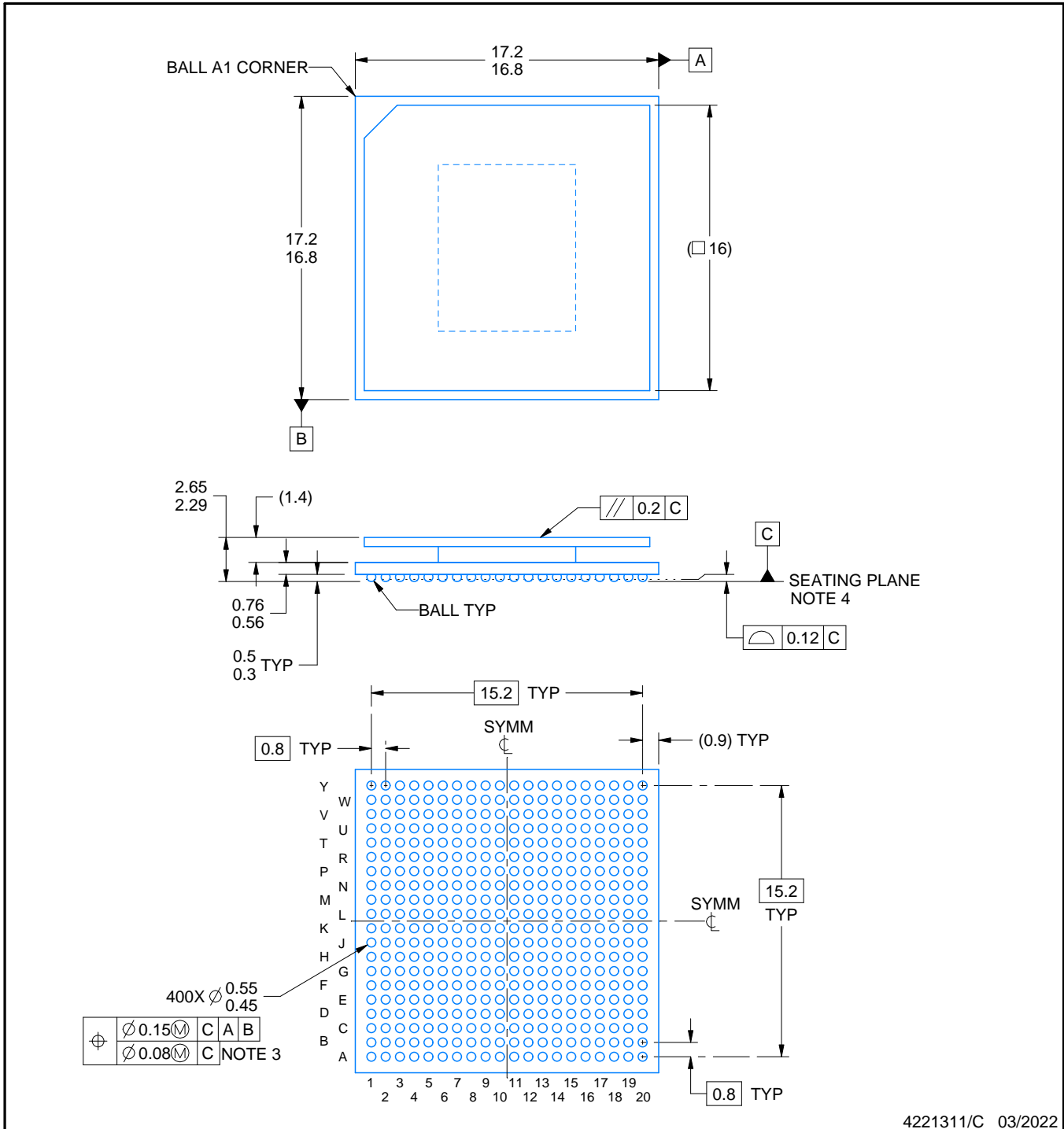
# ABJ0400A



# PACKAGE OUTLINE

FCBGA - 2.65 mm max height

BALL GRID ARRAY



4221311/C 03/2022

## NOTES:

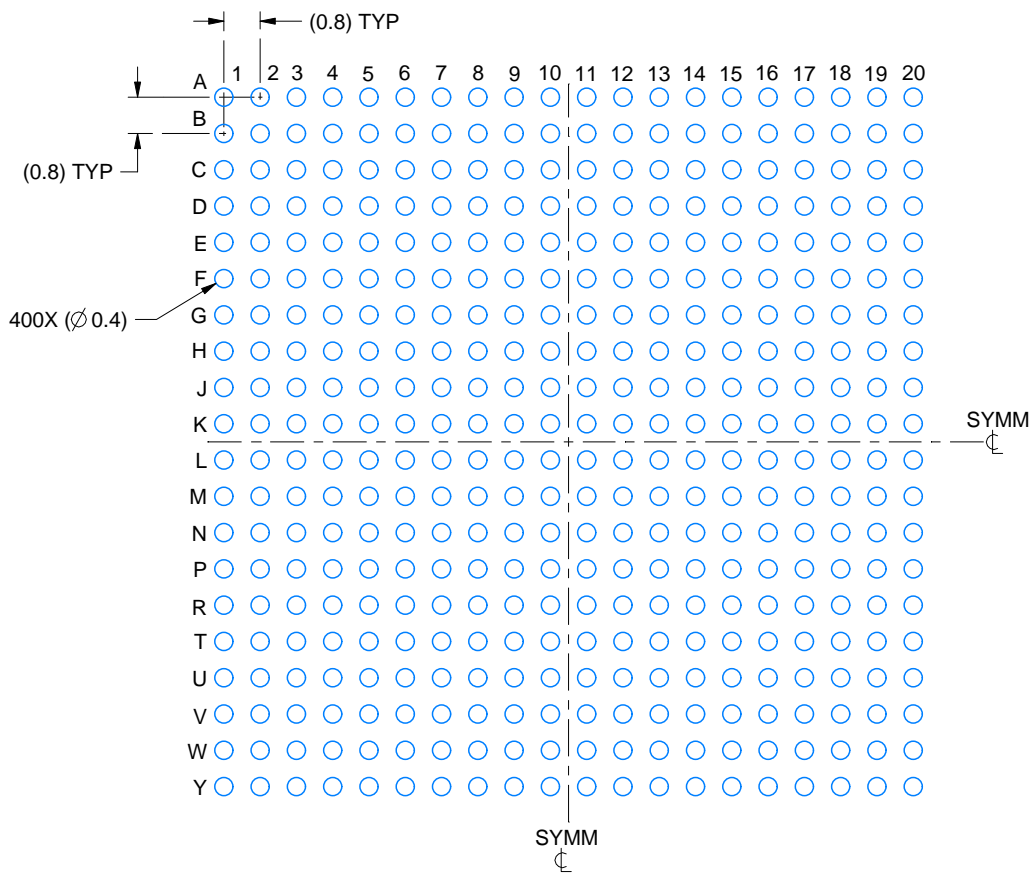
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
- Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

# EXAMPLE BOARD LAYOUT

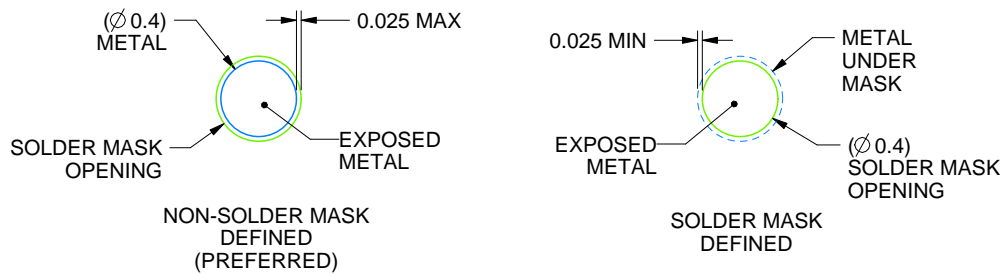
**ABJ0400A**

**FCBGA - 2.65 mm max height**

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

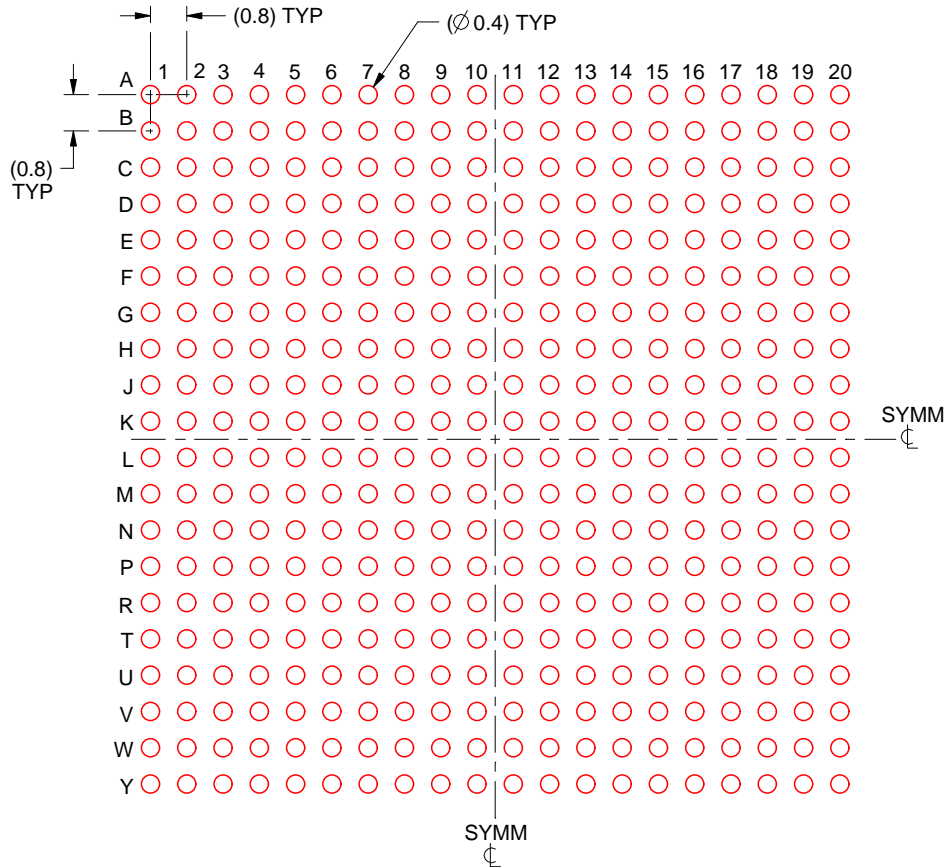
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

## ABJ0400A

## FCBGA - 2.65 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

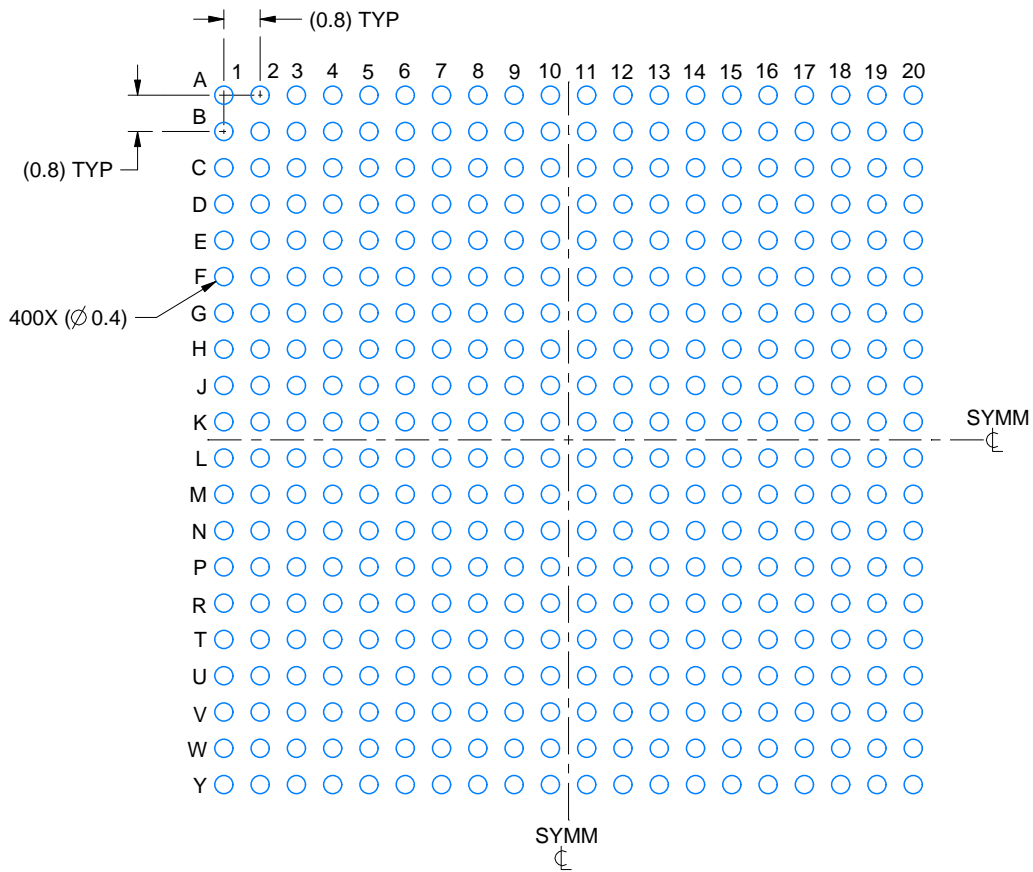


# EXAMPLE BOARD LAYOUT

ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

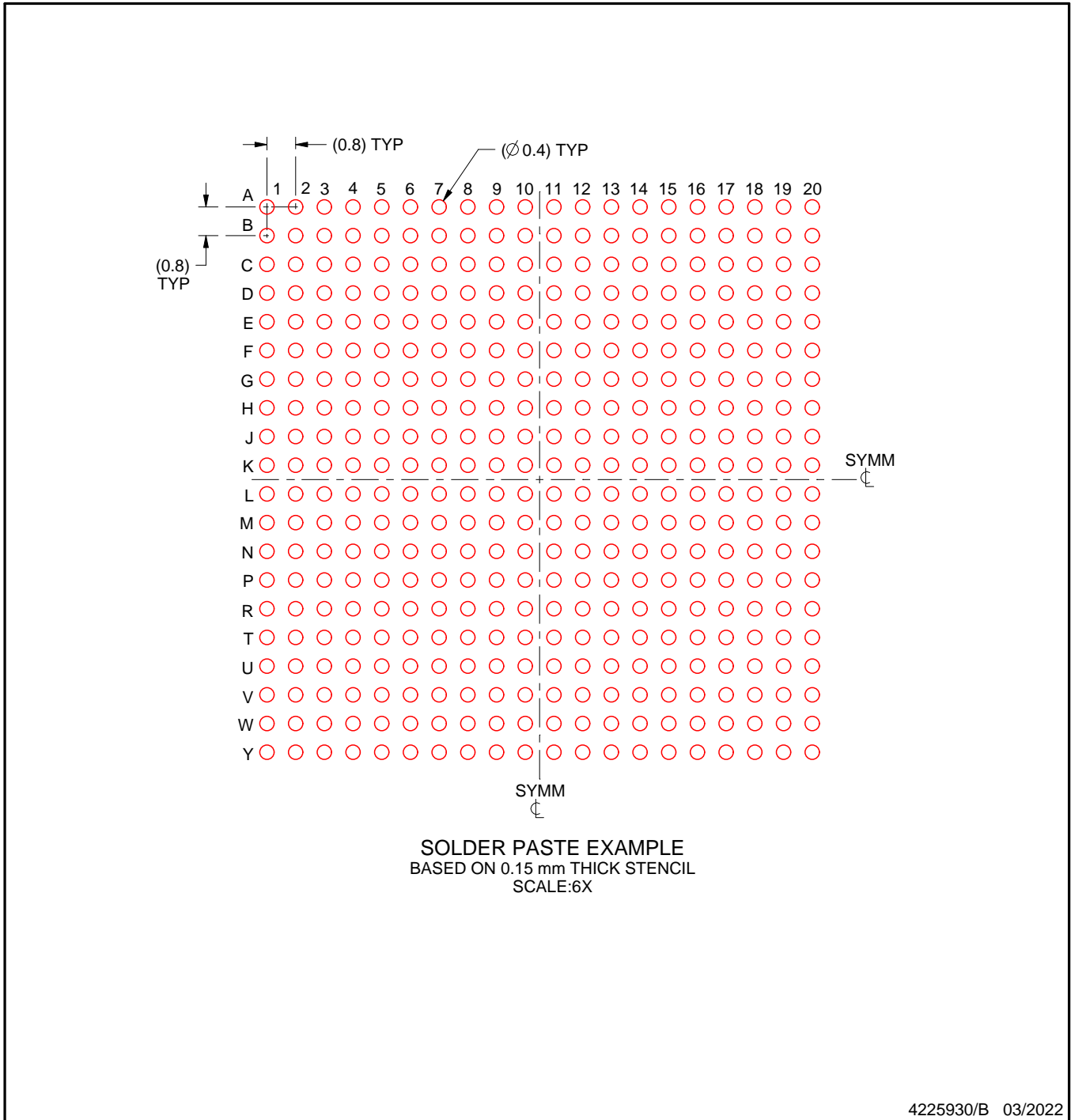
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

## ALK0400A

## FCBGA - 2.65 mm max height

BALL GRID ARRAY



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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