ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74HC299
Integrated Circuit
TTL – High Speed CMOS,
8–Bit Universal Shift Register with 3–State Output

Description:

The NTE74HC299 is an 8–bit shift/storage register with three–state bus interface capability in a 20–Lead DIP type package. The register has four synchronous–operating modes controlled by two select inputs as shown in the mode select (S0, S1) table. The mode select, the serial data (DS0, DS7) and the parallel data (I/O_0 – I/O_7) respond only to the low–to–high transition of the clock (CP) pulse. S0, S1 and data inputs must be stable one set–up time prior to the clock positive transaction.

The Master Reset ($\overline{MR}$) is an asynchronous active low input. When $\overline{MR}$ output is low, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The three–state input/output (I/O) port has three modes of operation:

1. Both output enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are low and S0 or S1 or both are low, the data in the register is presented at the eight outputs.
2. When both S0 and S1 are high, I/O terminals are in the high impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two output enable inputs being high will force I/O terminals to be in the off–state. It is noted that each I/O terminal is a three–state output and a CMOS buffer input.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- Buffered Inputs
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- Can be Cascaded for N–Bit Word Lengths
- I/O_0 – I/O_7 Bus Drive Capability and Three–State for Bus Oriented Applications
- Typical f_{MAX} = 50Mhz at V_{CC} = 5V, C_L = 15pF, T_A = +25°C
- Fanout (Over Temperature Range):
  Standard Outputs . . . 10 LS–TTL Loads
  Bus Driver Outputs . . 15 LS–TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} ..... −0.5 to +7.0V
Clamp Diode Current, I_{IK}, I_{OK} ..... ±20mA
DC Drain Current (Per Output), I_{OUT}
For Q Outputs ..... ±25mA
For I/O Outputs ..... ±35mA
DC Output Source or Sink Current (Per Output), I_{OUT} ..... ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} ..... ±50mA
Maximum Junction, T_J ..... +150°C
Storage Temperature Range, T_{stg} ..... −65°C to +150°C
Typical Thermal Resistance, Junction−to−Ambient, R_{thJA} ..... 69°C/W
Lead Temperature (During Soldering, 10sec), T_L ..... +300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	−	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	−	V_{CC}	V
Operating Temperature Range	T_A	−40	−	+85	°C
Input Rise or Fall Times	t_r, t_f				
V_{CC} = 2.0V		−	−	1000	ns
V_{CC} = 4.5V		−	−	500	ns
V_{CC} = 6.0V		−	−	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions		V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
					Typ	Guaranteed Limits		
Minimum HIGH Level Input Voltage	V_{IH}			2.0	−	1.5	1.5	V
				4.5	−	3.15	3.15	V
				6.0	−	4.2	4.2	V
Maximum LOW Level Input Voltage	V_{IL}			2.0	−	0.5	0.5	V
				4.5	−	1.35	1.35	V
				6.0	−	1.8	1.8	V
Minimum HIGH Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = −20μA	−	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V
			I_{OUT} = −6mA	4.5	−	3.98	3.84	V
			I_{OUT} = −7.8mA	6.0	−	5.48	5.34	V
Minimum LOW Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = 20μA	−	−	0.1	0.1	V
			I_{OUT} = 6mA	4.5	0.2	0.26	0.33	V
			I_{OUT} = 7.8mA	6.0	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	±0.1	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		6.0	−	8.0	80	μA
Three−State Leakage Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}		6.0	−	±0.5	±5.0	μA

Prerequisite for Switching Specifications:

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Maximum Clock Frequency	f_{MAX}		2.0	–	6	5	MHz
			4.5	–	30	25	MHz
			6.0	–	35	29	MHz
$\overline{MR}$ Pulse Width	t_W		2.0	–	50	65	ns
			4.5	–	10	13	ns
			6.0	–	9	11	ns
Clock Pulse Width	t_W		2.0	–	80	100	ns
			4.5	–	16	20	ns
			6.0	–	14	17	ns
Setup Time (DS0, DS7, I/On to Clock)	t_{SU}		2.0	–	100	125	ns
			4.5	–	20	25	ns
			6.0	–	17	21	ns
Hold Time (DS0, DS7, I/On, S0, S1 to Clock)	t_H		All	–	0	0	ns
Recovery Time ($\overline{MR}$ to Clock)	t_{REC}		All	–	5	5	ns
Setup Time (S1, S0 to Clock)	t_{SU}		2.0	–	120	150	ns
			4.5	–	24	30	ns
			6.0	–	20	26	ns

Switching Specifications: ($t_r = t_f$ = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Propagation Delay Time Clock to I/O Output Clock to Q0 and Q7 $\overline{MR}$ to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	200	250	ns
			4.5	–	40	50	ns
		C_L = 15pF	5.0	17	–	–	ns
		C_L = 50pF	6.0	–	34	43	ns
Output Enable and Disable Time	t_{PZL}	C_L = 15pF	5.0	10	–	–	ns
	t_{PZH}, t_{PZL}			13	–	–	ns
	t_{PZH}			15	–	–	ns
Output High−Z to High Level	t_{PZH}	C_L = 50pF	2.0	–	155	195	ns
			4.5	–	31	39	ns
			6.0	–	26	33	ns
Output High Level to High−Z	t_{PHZ}	C_L = 50pF	2.0	–	185	230	ns
			4.5	–	37	46	ns
			6.0	–	31	39	ns
Output Low Level to High−Z	t_{PLZ}	C_L = 50pF	2.0	–	155	195	ns
			4.5	–	31	39	ns
			6.0	–	26	33	ns
Output High−Z to Low Level	t_{PZL}	C_L = 50pF	2.0	–	130	165	ns
			4.5	–	26	33	ns
			6.0	–	22	28	ns
Output Transition Time, Q0, Q7	t_{TLH}, t_{THL}	C_L = 50pF	2.0	–	75	95	ns
			4.5	–	15	19	ns
			6.0	–	13	16	ns

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Output Transition Time, I/O_0 to I/O_7	t_{TLH}, t_{THL}	C_L = 50pF	2.0	–	60	75	ns
			4.5	–	12	15	ns
			6.0	–	10	13	ns
Maximum Input Capacitance	C_{IN}	C_L = 50pF	–	–	10	10	pF
Maximum Three−State Output Capacitance	C_{OUT}	C_L = 50pF	–	–	20	20	MHz
Power Dissipation Capacitance	C_{PD}	Note 3	5.0	150	–	–	pF

Note 3. C_{PD} is used to determine the dynamic power consumption, per channel.
$P_D = C_{PD} V_{CC}^2 f_i \Sigma (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Mode Select Function Table Three−State I/O Port Operating Mode:

Function	Inputs					Inputs/Outputs
	$\overline{OE1}$	$\overline{OE2}$	S0	S1	Qn (Register)	I/O0 – I/O7
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	Qn = I/On	I/On = Inputs
Disable I/O	H	X	X	X	X	Z
	X	H	X	X	X	Z

Truth Table:

Function	Inputs							Register Outputs				
	$\overline{MR}$	CP	S0	S1	DS0	DS7	I/On	Q0	Q1	– – –	Q6	Q7
Reset (Clear)	**L**	**X**	**X**	**X**	**X**	**X**	**X**	**L**	**L**	**– – –**	**L**	**L**
Shift Right	H	↑	h	l	l	X	X	L	q_1	– – –	q_1	q_6
	H	↑	h	l	h	X	X	H	q_1	– – –	q_1	Q_6
Shift Left	H	↑	l	h	X	l	X	q_1	q_1	– – –	q_1	L
	H	↑	l	h	X	h	X	q_1	q_1	– – –	q_1	H
Hold (Do Nothing)	H	↑	l	l	X	X	X	q_0	q_1	– – –	q_1	q_7
Parallel Load	H	↑	h	h	X	X	l	L	L	– – –	L	L
	H	↑	h	h	X	X	h	H	H	– – –	H	H

H = Input Voltage HIGH Level
h = Input Voltage HIGH one set−up timer prior to clock transition
L = Input Voltage LOW Level
l = Input Voltage LOW one set−up timer prior to clock transition
qn = Lower case letter indicates the state of reference output one set−up time prior to clock transition
X = Don't Care
Z = Output in high impedance state
↑ = Transition from LOW to HIGH Level

Pin Connection Diagram