

**General Description**

The DSC612NL3A-019A is a two-output low power MEMS clock generator.

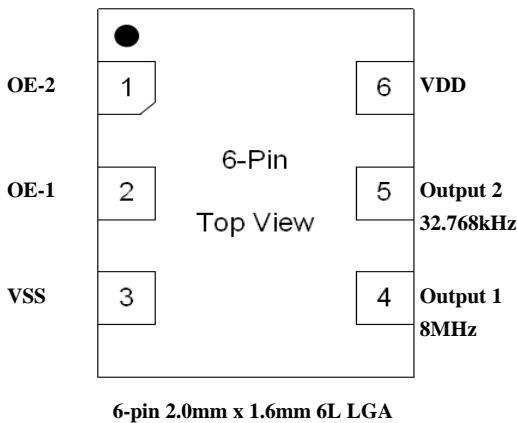
The MEMS based clock generator eliminates the need of external crystal or reference clock.

Refer to [DSC612 master data sheet](#) to read full descriptions.

**Features**

- Two LVCMOS clock outputs:  
8MHz, 32.768kHz
- Ultra-small package size: 2.0mm x 1.6mm 6L LGA
- High stability:  $\pm 20$ ppm
- Temperature range:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- Low power consumption
- Wide supply voltage range: 1.71V -3.63V VDD
- Excellent shock and vibration immunity
- High reliability
- Lead free and RoHS compliant

**Pin Configuration and Description**



Pin Number	Pin Name	Pin Type	Pin Description
1	OE-2	I	Output Enable H = Output Active L = Output Disabled (High Impedance)
2	OE-1	I	Output Enable H = Output Active L = Output Disabled (High Impedance)
3	VSS	Power	Power Supply Ground
4	Output 1	O	8MHz LVCMOS Clock Output Controlled by Pin 2 (OE-1)
5	Output 2	O	32.768kHz LVCMOS Clock Output Controlled by Pin 1 (OE-2)
6	VDD	Power	Power Supply

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## Ordering Information

Ordering Part Number	Temperature Range	High Stability	Shipping	Package
DSC612NL3A-019A	-40°C to +105°C	±20ppm	Bag	2.0mm x 1.6mm 6L LGA
DSC612NL3A-019AT	-40°C to +105°C	±20ppm	Tape and Reel	2.0mm x 1.6mm 6L LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

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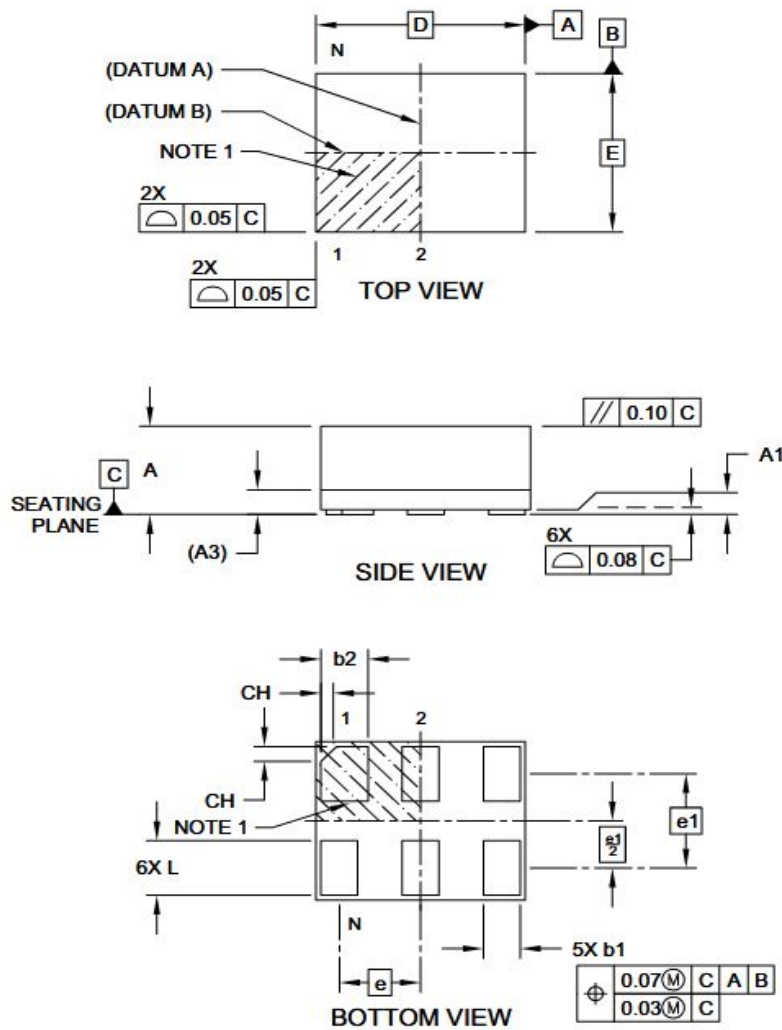
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6-Lead 2.0 mm x 1.6 mm VFLGA Package Outline and Recommended Land Pattern

6-Lead Very Thin Fine Pitch Land Grid Array (ATA) - 2.0x1.6 mm Body [VFLGA]

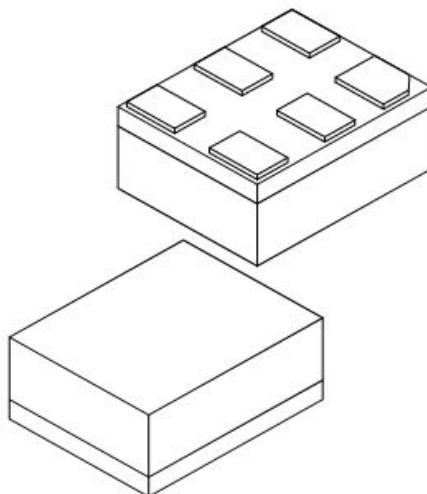
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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**6-Lead Very Thin Fine Pitch Land Grid Array (ATA) - 2.0x1.6 mm Body [VFLGA]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	6		
Terminal Pitch	e	0.775 BSC		
Terminal Pitch	e1	0.95 BSC		
Overall Height	A	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	1.60 BSC		
Terminal Width	b1	0.30	0.35	0.40
Terminal Width	b2	0.40	0.45	0.50
Terminal Length	L	0.50	0.55	0.60
Terminal 1 Index Chamfer	CH	-	0.15	-

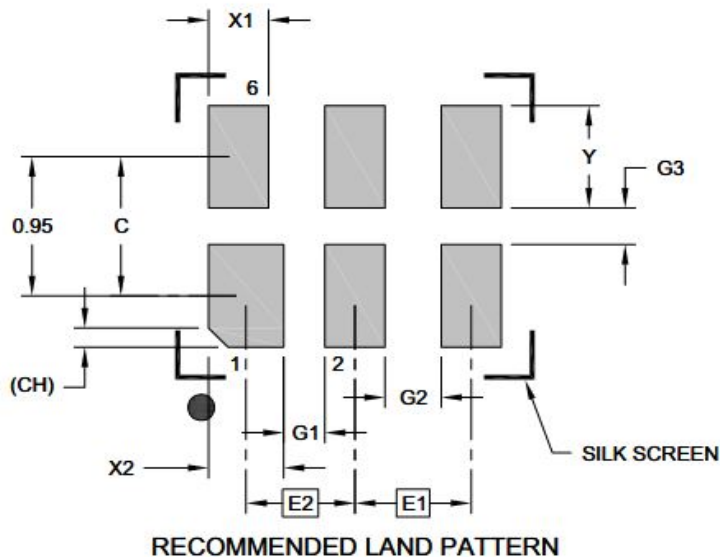
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

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**6-Lead Very Thin Fine Pitch Land Grid Array (ATA) - 2.0x1.6 mm Body [VFLGA]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E1		0.78 BSC	
Contact Pitch	E2		0.73 BSC	
Contact Spacing	C		0.95	
Contact Width (X4)	X1			0.40
Contact Width (X2)	X2			0.45
Contact Pad Length (X6)	Y			0.70
Space Between Contacts (X4)	G1	0.28		
Space Between Contacts (X3)	G2	0.38		
Space Between Contacts (X3)	G3	0.25		
Contact 1 Index Chamfer	CH	0.13 X 45° REF		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3201A