

### FEATURES

#### Isolated high-side and low-side outputs

High side or low side relative to input:  $\pm 700 V_{PEAK}$

High-side/low-side differential:  $700 V_{PEAK}$

#### 0.1 A peak output current

#### High frequency operation: 5 MHz maximum

#### High common-mode transient immunity: $>75 \text{ kV}/\mu\text{s}$

#### High temperature operation: $105^\circ\text{C}$

#### Wide body, 16-lead SOIC

#### Safety and regulatory approvals

##### UL recognition

2500 V rms for 1 minute per UL 1577

##### VDE certificate of conformity

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12

$V_{IORM} = 560 \text{ V peak}$

### APPLICATIONS

#### Isolated IGBT/MOSFET gate drives

#### Plasma displays

#### Industrial inverters

#### Switching power supplies

### GENERAL DESCRIPTION

The ADuM1233<sup>1</sup> is an isolated, half-bridge gate driver that uses the Analog Devices, Inc., *iCoupler*® technology to provide independent and isolated high-side and low-side outputs. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to optocoupler-based solutions.

By avoiding the use of LEDs and photodiodes, this *iCoupler* gate drive device is able to provide precision timing characteristics not possible with optocouplers. Furthermore, the reliability and performance stability problems associated with optocoupler LEDs are avoided.

In comparison to gate drivers that use high voltage level translation methodologies, the ADuM1233 offers the benefit of true, galvanic isolation between the input and each output. Each output can be operated up to  $\pm 700 V_{PEAK}$  relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high side and low side can be as high as  $700 V_{PEAK}$ .

As a result, the ADuM1233 provides reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

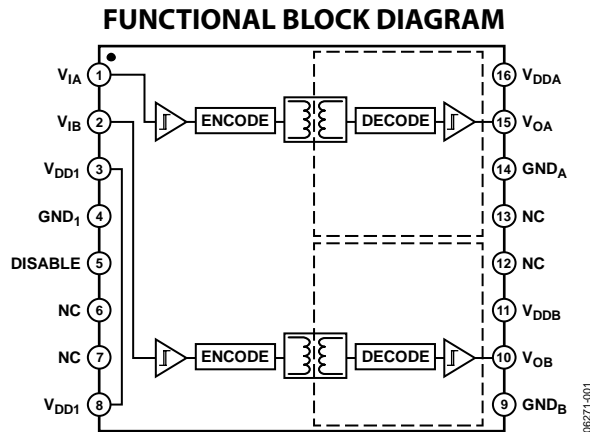


Figure 1.

<sup>1</sup> Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; 7,075,329.

#### Rev. C

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## REVISION HISTORY

### 8/12—Rev. B to Rev. C

Changes to Features Section.....	1
Created Hyperlink for Safety and Regulatory Approvals Entry in Features Section.....	1
Changed IC Junction-to-Ambient Thermal Resistance Parameter in Table 2.....	4
Changes to Table 3 and Table 4.....	4
Added DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics Section.....	5
Added Table 5 and Figure 2; Renumbered Sequentially .....	5
Updated Outline Dimensions .....	11

### 12/07—Rev. A to Rev. B

Changes to Note 1 .....	1
Change to Minimum Pulse Width.....	3

### 4/07—Rev. Sp0: Rev. A

Changes to Figure 1.....	1
Changes to Figure 7.....	7
Updated Outline Dimensions .....	10

### 7/06—Revision Sp0: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground.  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $12\text{ V} \leq V_{DDA} \leq 18\text{ V}$ , and  $12\text{ V} \leq V_{DDB} \leq 18\text{ V}$ . All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DDA} = 15\text{ V}$ , and  $V_{DDB} = 15\text{ V}$ .

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DC SPECIFICATIONS</b>						
Input Supply Current ( $V_{DD1}$ Pins)						
Quiescent	$I_{DD1(Q)}$		3.0	4.2	mA	
10 Mbps	$I_{DD1(10)}$		6.0	9.0	mA	
Output Supply Current ( $V_{DDA}$ and $V_{DDB}$ Pins)						
Quiescent	$I_{DDA(Q)}, I_{DDB(Q)}$		0.3	1.2	mA	
10 Mbps	$I_{DDA(10)}, I_{DDB(10)}$		16	22	mA	$C_L = 200\text{ pF}$
Input Currents	$I_{IA}, I_{IB}, I_{DISABLE}$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{IA}, V_{IB}, V_{DISABLE} \leq V_{DD1}$
Logic High Input Threshold	$V_{IH}$	2.0			V	
Logic Low Input Threshold	$V_{IL}$			0.8	V	
Logic High Output Voltages	$V_{OAH}, V_{OBH}$	$V_{DDA} - 0.1,$ $V_{DDB} - 0.1$	$V_{DDA}, V_{DDB}$		V	$I_{OA}, I_{OB} = -1\text{ mA}$
Logic Low Output Voltages	$V_{OAL}, V_{OBL}$			0.1	V	$I_{OA}, I_{OB} = +1\text{ mA}$
Output Short-Circuit Pulsed Current <sup>1</sup>	$I_{OA(SC)}, I_{OB(SC)}$	100			mA	
<b>SWITCHING SPECIFICATIONS</b>						
Minimum Pulse Width <sup>2</sup>	PW			80	ns	$C_L = 200\text{ pF}$
Maximum Switching Frequency <sup>3</sup>		10			Mbps	
Propagation Delay <sup>4</sup>	$t_{PHL}, t_{PLH}$	97	124	160	ns	
Change vs. Temperature			100		ps/ $^\circ\text{C}$	
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $	PWD			8	ns	
Channel-to-Channel Matching, Rising or Falling Edges <sup>5</sup>				5	ns	
Channel-to-Channel Matching, Rising vs. Falling Edges <sup>6</sup>				13	ns	
Part-to-Part Matching, Rising or Falling Edges <sup>7</sup>				55	ns	Input $t_R = 3\text{ ns}$
Part-to-Part Matching, Rising vs. Falling Edges <sup>8</sup>				63	ns	Input $t_R = 3\text{ ns}$
Output Rise/Fall Time (10% to 90%)	$t_R/t_F$			25	ns	

<sup>1</sup> Short-circuit duration less than one second.

<sup>2</sup> The minimum pulse width is the shortest pulse width at which the specified timing parameters are guaranteed.

<sup>3</sup> The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed.

<sup>4</sup>  $t_{PHL}$  propagation delay is measured from the 50% level of the falling edge of the  $V_{ix}$  signal to the 50% level of the falling edge of the  $V_{ox}$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level of the rising edge of the  $V_{ix}$  signal to the 50% level of the rising edge of the  $V_{ox}$  signal.

<sup>5</sup> Channel-to-channel matching, rising or falling edges is the magnitude of the propagation delay difference between two channels of the same part when the inputs are either both rising or falling edges. The supply voltages and the loads on each channel are equal.

<sup>6</sup> Channel-to-channel matching, rising vs. falling edges is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and the other input is a falling edge. The supply voltages and loads on each channel are equal.

<sup>7</sup> Part-to-part matching, rising or falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when the inputs are either both rising or falling edges. The supply voltages, temperatures, and loads of each part are equal.

<sup>8</sup> Part-to-part matching, rising vs. falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when one input is a rising edge and the other input is a falling edge. The supply voltages, temperatures, and loads of each part are equal.

## PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	f = 1 MHz
Capacitance (Input-to-Output) <sup>1</sup>	C <sub>I-O</sub>		2.0		pF	
Input Capacitance	C <sub>I</sub>		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ <sub>JA</sub>		45		°C/W	

<sup>1</sup> The device is considered a two-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

## REGULATORY INFORMATION

The ADuM1233 is approved by the organizations listed in Table 3.

Table 3.

UL	VDE
Recognized Under 1577 Component Recognition Program <sup>1</sup> Single/Basic 2500 V rms Isolation Voltage File E214100	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 <sup>2</sup> Reinforced insulation, 560 V peak File 2471900-4880-0001

<sup>1</sup> In accordance with UL 1577, each ADuM1233 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 μA).

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each ADuM1233 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (\*) marking branded on the component designates DIN V VDE V 0884-10 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	3.5 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	3.5 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

**DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS**

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (\*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 5.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V <sub>IORM</sub>	560	V peak
Input-to-Output Test Voltage, Method B1	V <sub>IORM</sub> × 1.875 = V <sub>pd(m)</sub> , 100% production test, t <sub>ini</sub> = t <sub>m</sub> = 1 sec, partial discharge < 5 pC	V <sub>pd(m)</sub>	1050	V peak
Input-to-Output Test Voltage, Method A After Environmental Tests Subgroup 1	V <sub>IORM</sub> × 1.5 = V <sub>pd(m)</sub> , t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec, partial discharge < 5 pC	V <sub>pd(m)</sub>	896	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	V <sub>IORM</sub> × 1.2 = V <sub>pd(m)</sub> , t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec, partial discharge < 5 pC	V <sub>pd(m)</sub>	672	V peak
Highest Allowable Overvoltage		V <sub>IOTM</sub>	4000	V peak
Surge Isolation Voltage		V <sub>IOSM</sub>	4000	V peak
Safety-Limiting Values	V peak = 10 kV, 1.2 μs rise time, 50 μs, 50% fall time Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T <sub>S</sub>	150	°C
Safety Total Dissipated Power		P <sub>S</sub>	1	W
Insulation Resistance at T <sub>S</sub>	V <sub>IO</sub> = 500 V	R <sub>S</sub>	>10 <sup>9</sup>	Ω

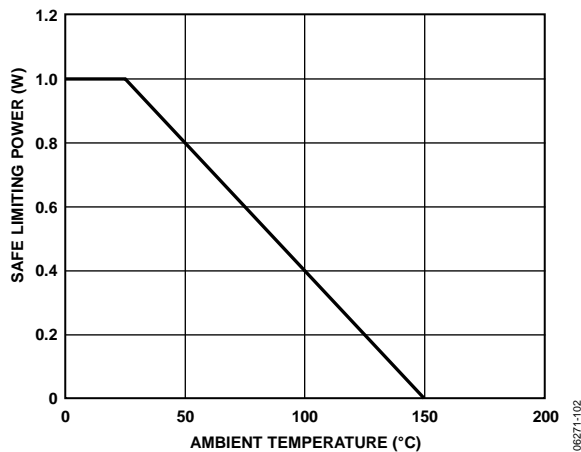


Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

**RECOMMENDED OPERATING CONDITIONS**

Table 6.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-40	+105	°C
Input Supply Voltage <sup>1</sup>	V <sub>DD1</sub>	4.5	5.5	V
Output Supply Voltages <sup>1</sup>	V <sub>DDA</sub> , V <sub>DDB</sub>	12	18	V
Input Signal Rise and Fall Times			100	ns
Common-Mode Transient Immunity				
Input-to-Output <sup>2</sup>		-75	+75	kV/μs
Between Outputs <sup>2</sup>		-75	+75	kV/μs
Transient Immunity, Supply Voltages <sup>2</sup>		-75	+75	kV/μs

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> See the Common-Mode Transient Immunity section for more information.

## ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Storage Temperature ( $T_{ST}$ )	-55°C to +150°C
Ambient Operating Temperature ( $T_A$ )	-40°C to +105°C
Input Supply Voltage <sup>1</sup> ( $V_{DD1}$ )	-0.5 V to +7.0 V
Output Supply Voltage <sup>1</sup> ( $V_{DDA}$ , $V_{ddb}$ )	-0.5 V to +27 V
Input Voltage <sup>1</sup> ( $V_{IA}$ , $V_{IB}$ )	-0.5 V to $V_{DD1} + 0.5$ V
Output Voltage <sup>1</sup>	
$V_{OA}$	-0.5 V to $V_{DDA} + 0.5$ V
$V_{OB}$	-0.5 V to $V_{ddb} + 0.5$ V
Input-to-Output Voltage <sup>2</sup>	-700 $V_{PEAK}$ to +700 $V_{PEAK}$
Output Differential Voltage <sup>3</sup>	+700 $V_{PEAK}$
Output DC Current ( $I_{OA}$ , $I_{OB}$ )	-20 mA to +20 mA
Common-Mode Transients <sup>4</sup>	-100 kV/ $\mu$ s to +100 kV/ $\mu$ s

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> Input-to-output voltage is defined as  $GND_A - GND_1$  or  $GND_B - GND_1$ .

<sup>3</sup> Output differential voltage is defined as  $GND_A - GND_B$ .

<sup>4</sup> Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

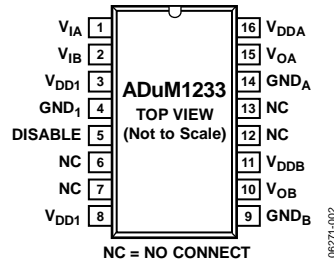


Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>IA</sub>	Logic Input A.
2	V <sub>IB</sub>	Logic Input B.
3, 8 <sup>1</sup>	V <sub>DD1</sub>	Input Supply Voltage, 4.5 V to 5.5 V.
4	GND <sub>1</sub>	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. Disables the isolator inputs and refresh circuits. Outputs take on default low state.
6, 7, 12, 13 <sup>2</sup>	NC	No Connect.
9	GND <sub>B</sub>	Ground Reference for Output B.
10	V <sub>OB</sub>	Output B.
11	V <sub>DDB</sub>	Output B Supply Voltage, 12 V to 18 V.
14	GND <sub>A</sub>	Ground Reference for Output A.
15	V <sub>OA</sub>	Output A.
16	V <sub>DDA</sub>	Output A Supply Voltage, 12 V to 18 V.

<sup>1</sup> Pin 3 and Pin 8 are internally connected. Connecting both pins to V<sub>DD1</sub> is recommended.

<sup>2</sup> Pin 12 and Pin 13 are floating and should be left unconnected.

Table 9. Truth Table (Positive Logic)

V <sub>IA</sub> /V <sub>IB</sub> Input	V <sub>DD1</sub> State	DISABLE	V <sub>OA</sub> /V <sub>OB</sub> Output	Notes
High	Powered	Low	High	Output returns to input state within 1 μs of V <sub>DD1</sub> power restoration.
Low	Powered	Low	Low	
X <sup>1</sup>	Unpowered	X <sup>1</sup>	Low	
X <sup>1</sup>	Powered	High	Low	

<sup>1</sup> X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

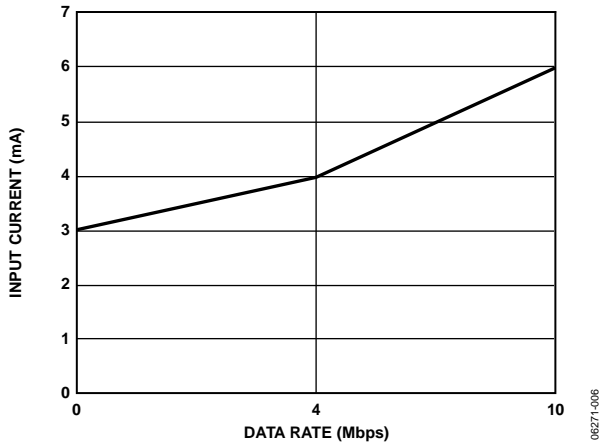


Figure 4. Typical Input Supply Current Variation with Data Rate

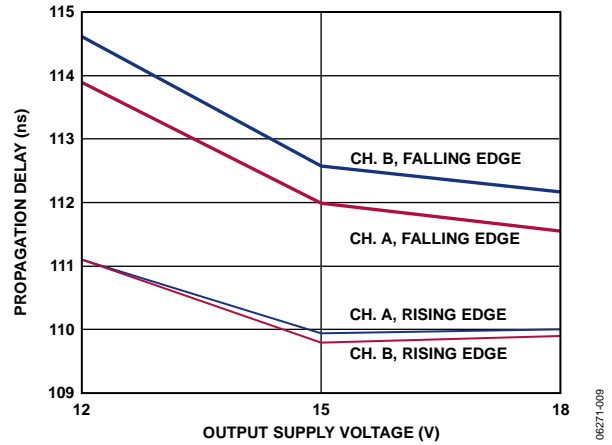


Figure 7. Typical Propagation Delay Variation with Output Supply Voltage (Input Supply Voltage = 5.0 V)

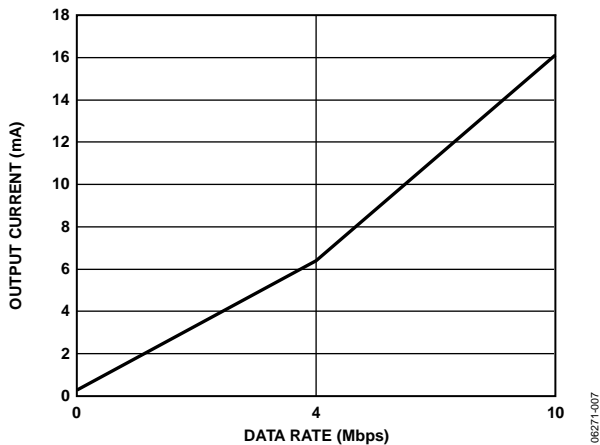


Figure 5. Typical Output Supply Current Variation with Data Rate

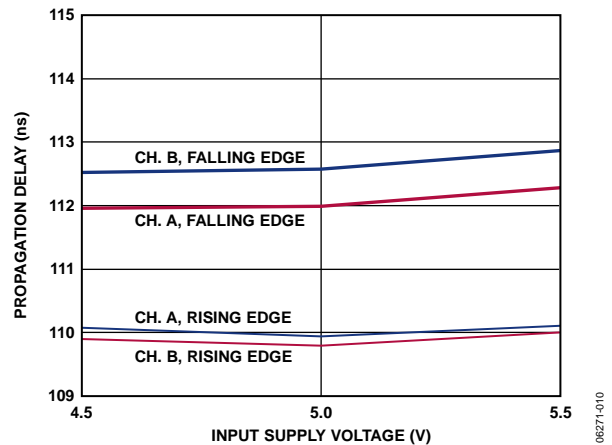


Figure 8. Typical Propagation Delay Variation with Input Supply Voltage (Output Supply Voltage = 15.0 V)

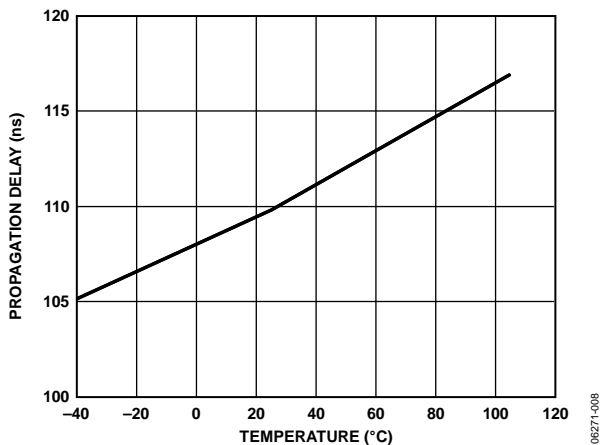


Figure 6. Typical Propagation Delay Variation with Temperature



# APPLICATIONS INFORMATION

## COMMON-MODE TRANSIENT IMMUNITY

In general, common-mode transients consist of linear and sinusoidal components. The linear component of a common-mode transient is given by

$$V_{CM, linear} = (\Delta V/\Delta t) t$$

where  $\Delta V/\Delta t$  is the slope of the transient shown in Figure 12 and Figure 13.

The transient of the linear component is given by

$$dV_{CM}/dt = \Delta V/\Delta t$$

The ability of the ADuM1233 to operate correctly in the presence of linear transients is characterized by the data in Figure 9. The data is based on design simulation and is the maximum linear transient magnitude that the ADuM1233 can tolerate without an operational error. This data shows a higher level of robustness than what is listed in Table 6 because the transient immunity values obtained in Table 6 use measured data and apply allowances for measurement error and margin.

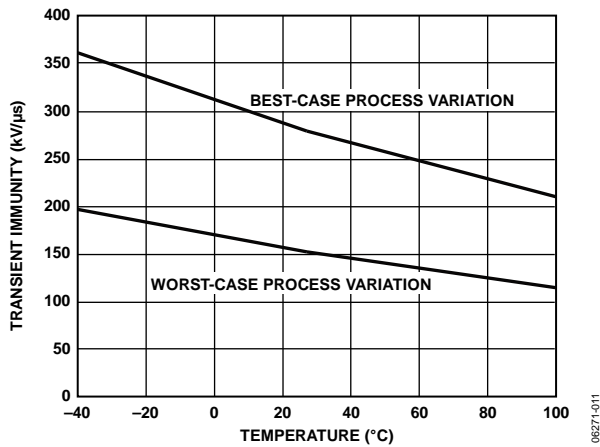


Figure 9. Transient Immunity (Linear Transients) vs. Temperature

The sinusoidal component (at a given frequency) is given by

$$V_{CM, sinusoidal} = V_o \sin(2\pi ft)$$

where:

$V_o$  is the magnitude of the sinusoidal.

$f$  is the frequency of the sinusoidal.

The transient magnitude of the sinusoidal component is given by

$$dV_{CM}/dt = 2\pi f V_o$$

The ability of the ADuM1233 to operate correctly in the presence of sinusoidal transients is characterized by the data in Figure 10 and Figure 11. The data is based on design simulation and is the maximum sinusoidal transient magnitude ( $2\pi f V_o$ ) that the ADuM1233 can tolerate without an operational error. Values for immunity against sinusoidal transients are not included in Table 6 because measurements to obtain such values have not been possible.

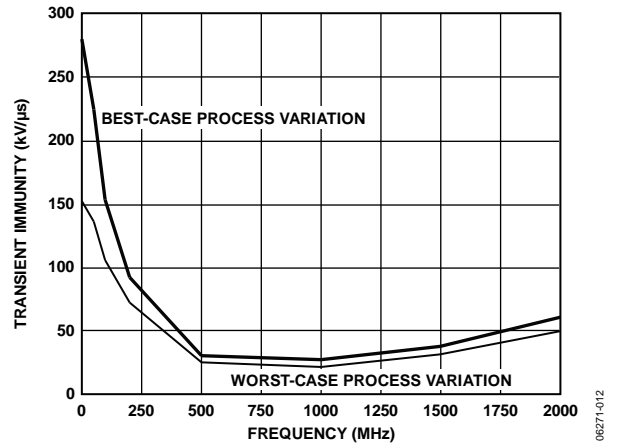


Figure 10. Transient Immunity (Sinusoidal Transients), 27°C Ambient Temperature

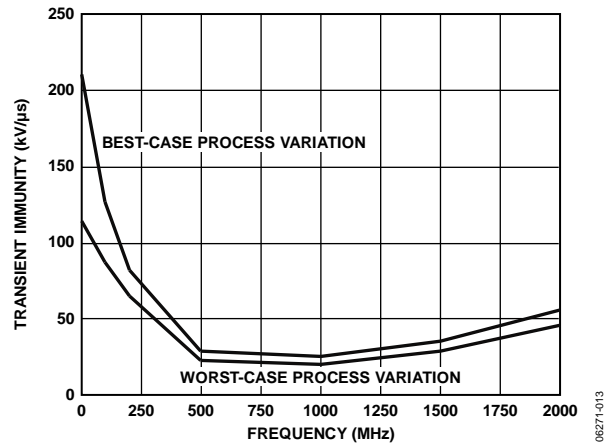


Figure 11. Transient Immunity (Sinusoidal Transients), 100°C Ambient Temperature

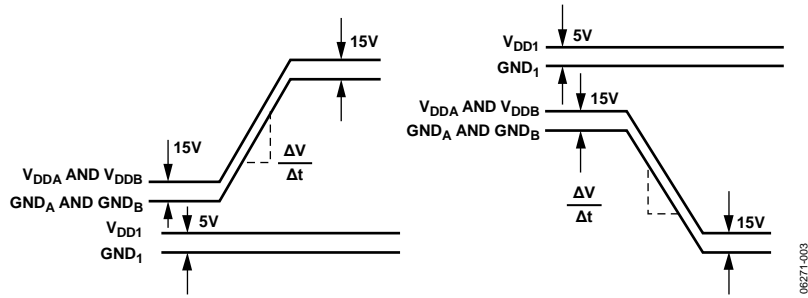


Figure 12. Common-Mode Transient Immunity Waveforms—Input to Output

06271-003

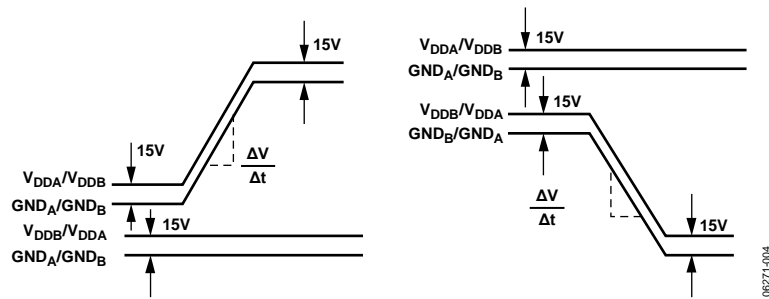


Figure 13. Common-Mode Transient Immunity Waveforms—Between Outputs

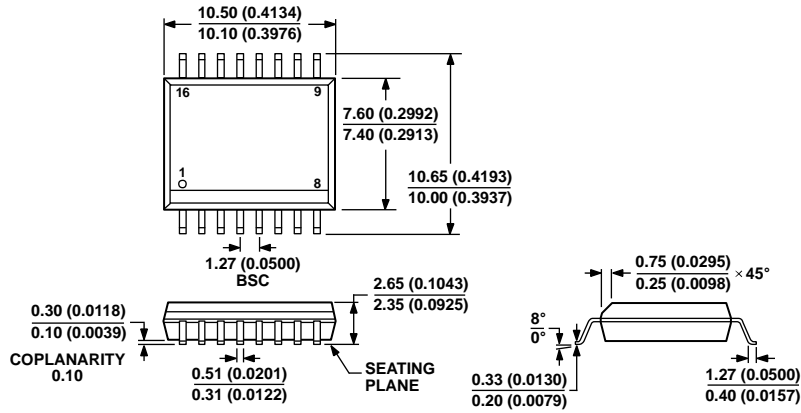
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Figure 14. Transient Immunity Waveforms—Output Supplies

06271-005

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 15. 16-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body  
 (RW-16)  
 Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model <sup>1</sup>	No. of Channels	Output Peak Current (A)	Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM1233BRWZ	2	0.1	15	-40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1233BRWZ-RL	2	0.1	15	-40°C to +105°C	16-Lead SOIC_W, 13-Inch Tape and Reel Option (1,000 Units)	RW-16

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**