



Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

| | |
|---|---|
| PCN #: TB1812-01 DATE: January 8, 2019 Product Affected: F2270NLGK F2270NLGK8 Date Effective: April 8, 2019 | MEANS OF DISTINGUISHING CHANGED DEVICES: <input type="checkbox"/> Product Mark <input type="checkbox"/> Back Mark <input type="checkbox"/> Date Code <input checked="" type="checkbox"/> Other Shipment after PCN Effective |
|---|---|

| | |
|---|---|
| Contact: IDT PCN DESK E-mail: pcndesk@idt.com | Attachment: <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No Samples: Contact your local sales representative for sample and datasheet requests. |
|---|---|

DESCRIPTION AND PURPOSE OF CHANGE:

| | |
|--|--|
| <input type="checkbox"/> Die Technology <input type="checkbox"/> Wafer Fabrication Process <input type="checkbox"/> Assembly Process <input type="checkbox"/> Equipment <input type="checkbox"/> Material <input type="checkbox"/> Testing <input type="checkbox"/> Manufacturing Site <input checked="" type="checkbox"/> Data Sheet <input checked="" type="checkbox"/> Other - ATE limits | <p>This notice is to advise our customers that Data Sheet limits and ATE limits are being changed as the process variation for Control Pin Leakage Current that was used to calculate the original ATE limits does not accurately represent the variation observed in production test measurements.</p> <p>Refer to Attachment I for details of the changes.</p> |
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RELIABILITY/QUALIFICATION SUMMARY:

There is no expected change in quality or reliability.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

IDT reserves the right to ship either version manufactured after the process change effective date.

| | |
|------------------|---|
| Customer: _____ | <input type="checkbox"/> <i>Approval for shipments prior to effective date.</i> |
| Name/Date: _____ | E-Mail Address: _____ |
| Title: _____ | Phone# /Fax# : _____ |

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____



PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT I - PCN # : TB1812-01

PCN Type: Data Sheet & ATE Limits

Data Sheet Change: Yes

Details Of Change:

This notice is to advise our customers that Data Sheet limits and ATE limits are being changed as the process variation for Control Pin Leakage Current that was used to calculate the original ATE limits does not accurately represent the variation observed in production test measurements.

Table 1: Datasheet Limits Changes

From:

(i) V_{MODE} Current and V_{CTRL} Current

Table 4. Electrical Characteristics (General)

Refer to the application circuit in Figure 60 for the required circuit and use $L1 = L2 = 0\Omega$. The specifications in this table apply at $V_{DD} = +5.0V$, $T_{SP} = +25^\circ C$, $f_{RF} = 500MHz$, $Z_s = Z_L = 75\Omega$, signal applied to RF1, minimum attenuation, $P_{IN} = 0dBm$ for small signal parameters, $P_{IN} = +20dBm$ per tone for two tone tests, V_{MODE} is LOW or HIGH, and Evaluation Board (EVBkit) trace and connector losses are de-embedded, unless otherwise noted.

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|---|----------------------|---|-------------|---------|----------------|---------|
| V_{MODE} Logic Input HIGH | V_{IH} | $3.9V \leq V_{DD} \leq 5.5V$ | 1.07 | | 3.6 | V |
| | | $V_{DD} < 3.9V$ | 1.07 | | $V_{DD} - 0.3$ | |
| V_{MODE} Logic Input LOW | V_{IL} | | 0 | | 0.63 | V |
| V_{DD} Current | I_{DD} | | | 1.4 | 2.5 | μA |
| V_{MODE} Current | I_{MODE} | | -40 | | 40 | μA |
| V_{CTRL} Current | I_{CTRL} | | -50 | | 50 | μA |
| Attenuation Slope | ATT _{SLOPE} | $V_{MODE} = LOW$ | | 10 | | dB/V |
| | | $V_{MODE} = HIGH$ | | -10 | | |
| Attenuation Variation over Temperature (reference to +25°C) | ATT _{VAR} | $f_{RF} = 50MHz$ (-40°C to 105°C, over full signal range of V_{CTRL}) | | ± 1 | | dB |
| Settling Time | t _{SETTLE} | Any 1dB step in the 0dB to 33dB control range, 50% of V_{CTRL} signal to RF settled to within $\pm 0.1dB$ | | 25 | | μs |

[a] Specifications in the minimum/maximum columns that are shown in **bold italics** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

To:

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|---|----------------------|---|-------------|-----------|----------------|---------|
| V_{MODE} Logic Input HIGH | V_{IH} | $3.9V \leq V_{DD} \leq 5.5V$ | 1.07 | | 3.6 | V |
| | | $V_{DD} < 3.9V$ | 1.07 | | $V_{DD} - 0.3$ | |
| V_{MODE} Logic Input LOW | V_{IL} | | 0 | | 0.63 | V |
| V_{DD} Current | I_{DD} | | | 1.4 | 2.5 | μA |
| V_{MODE} Current | I_{MODE} | | | 25 | | μA |
| V_{CTRL} Current | I_{CTRL} | | | 50 | | μA |
| Attenuation Slope | ATT _{SLOPE} | $V_{MODE} = LOW$ | | 10 | | dB/V |
| | | $V_{MODE} = HIGH$ | | -10 | | |
| Attenuation Variation over Temperature (reference to +25°C) | ATT _{VAR} | $f_{RF} = 50MHz$ (-40°C to 105°C, over full signal range of V_{CTRL}) | | ± 1 | | dB |
| Settling Time | t _{SETTLE} | Any 1dB step in the 0dB to 33dB control range, 50% of V_{CTRL} signal to RF settled to within $\pm 0.1dB$ | | 25 | | μs |

[a] Specifications in the minimum/maximum columns that are shown in **bold italics** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.



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Table 2: ATE Limits Changes

(ii) Deleted 3.6v logic current tests

| From | To |
|--|--|
| Test 301 Ictrl @ 3.6v Min 25uA Max 32uA | - |
| Test 302 Ictrl @ 3.6v Min 8uA Max 30uA | - |
| Test 303 Ictrl @ 5.5v Min 40uA Max 50uA | Test 303 Ictrl @ 5.5v Min 40uA Max 63uA |
| Test 401 Ictrl @ 3.6v Min -6uA Max -0.1uA | - |
| Test 402 Imode @ 3.6v Min -0.9uA Max 0.9uA | - |