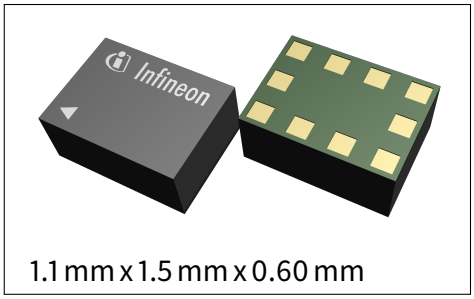
BGSX22G6U10

DPDT cross switch with GPIO control interface

Features

- High linearity up to 39 dBm peak power
- Low current consumption
- Low insertion loss and high port to port isolation up to 7.125 GHz
- Fast switching speed to enable 5G-SRS applications
- General Purpose Input-Output (GPIO) Interface
- No decoupling capacitors required for typical applications
- Ultra low profile lead-less plastic package (MSL-1, 260 °C per IPC/JEDEC J-STD-20)
- RoHS and WEEE compliant package
- Small form factor 1.1mm x 1.5mm



1.1 mm x 1.5 mm x 0.60 mm

RoHS Halogen-Free Lead-Free Green

Potential applications

- RF path routing/swapping for cellular mobile devices
- GSM, WCDMA, LTE and 5G applications

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

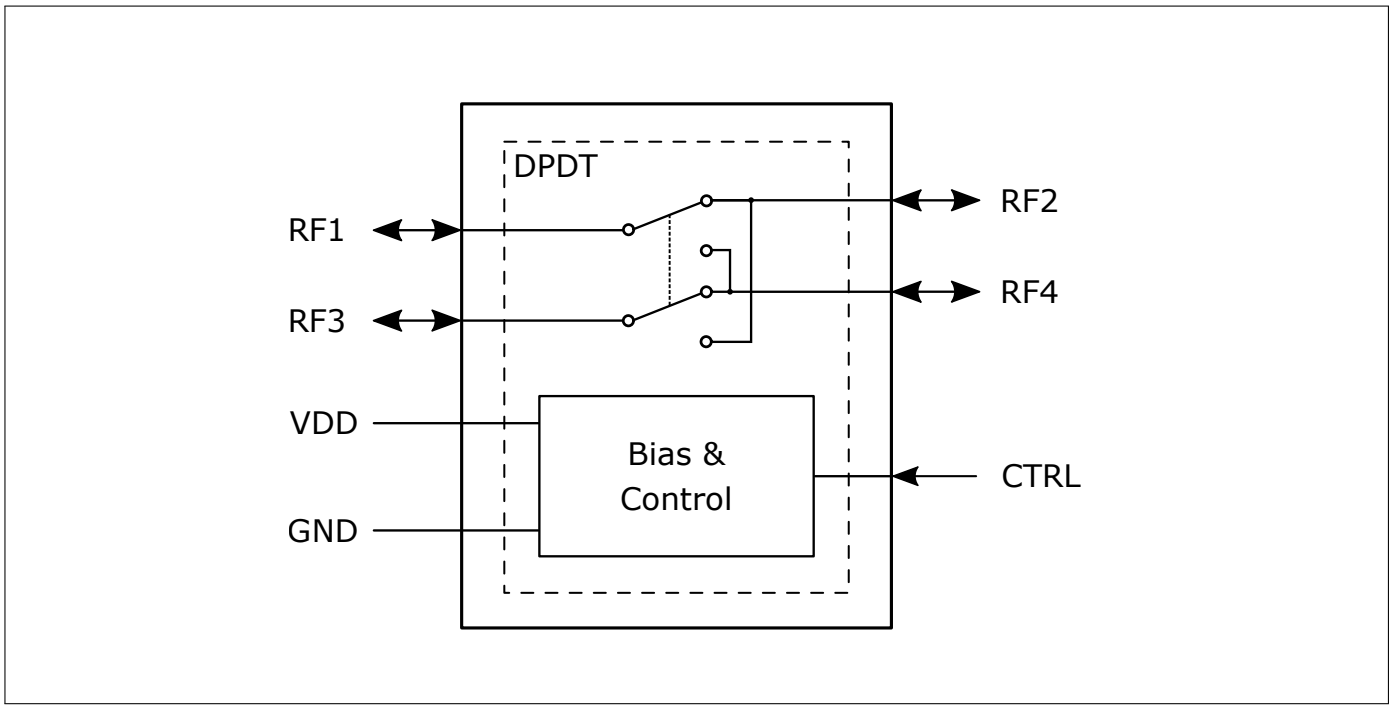
Description

The BGSX22G6U10 RF CMOS switch is specifically designed for GSM, WCDMA, LTE and 5G applications. This DPDT offers low insertion loss even at high frequencies of up to 7.125 GHz, low harmonic generation along with high isolation between RF ports. In addition, the fast switching speed enables 5G-SRS applications.
The switch is controlled via a GPIO interface. The on-chip controller allows power-supply voltages from 1.6V to 3.6V.
The switch features direct-connect-to-battery functionality and DC-free RF ports. Unlike GaAs technology, external DC blocking capacitors at the RF Ports are only required if DC voltage is applied externally. The device has a very small size of only 1.1mm x 1.5mm and a thickness of 0.60mm.

Table 1: Ordering information

Product type	Marking	Package
BGSX22G6U10	X6	PG-ULGA-10-1

Block diagram



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1 Absolute maximum ratings

Table 2: Maximum Ratings Table at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	-0.3	–	3.9	V	–
Abs-Max RF input power	$P_{RF,max}$	–	–	39	dBm	Duty cycle 25 %, frequency 0.4–7.125 GHz, VSWR 1:1
ESD robustness, CDM[1)]	V_{ESD_CDM}	-1	–	+1	kV	
ESD robustness, HBM[2)]	V_{ESD_HBM}	-2	–	+2	kV	
Maximum DC voltage on RF ports and RF ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF ports
GPIO control voltage levels	V_{Ctrlx}	-0.7	–	V_{DD}+0.7 (max. 3.9V)	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–

[1)] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[2)] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

2 Operation ranges

Table 3: Operation ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Max RF input power	$P_{RF,max}$	–	–	39	dBm	Peak envelope power of a 5G NR signal[1], frequency 0.4-7.125 GHz, VSWR 1:1
		–	–	37	dBm	Pulsed RF input power, duty cycle of 25 % with T_{period} = 4615 µs, through-path, frequency 0.4–7.125 GHz, VSWR 1:1
Supply voltage	V_{DD}	1.6	–	3.6	V	–
Control voltage Low	$V_{Ctrl,L}$	-0.3	–	0.45	V	–
Control voltage High	$V_{Ctrl,H}$	1.2	–	V_{DD}	V	–
Supply current	I_{DD}	–	25	35	µA	P_{RF} = 0 dBm
Control current	I_{Ctrl}	–	2	10	nA	–
Ambient temperature	T_A	-40	25	85	°C	–

[1] MCS 27 (256 QAM) OFDM, 60 kHz sub carrier spacing, 100 MHz bandwidth, RMS power is 9 dB below peak power.

3 RF characteristics

Table 4: RF characteristics at T_A = 25 °C, P_{RF} = 0 dBm, V_{DD} = 1.8V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion loss[1]						
All RF ports	*IL*	–	0.29	0.35	dB	400 to 960MHz
		–	0.34	0.42	dB	1710 to 2200MHz
		–	0.37	0.45	dB	2300 to 2690MHz
		–	0.44	0.56	dB	3300 to 4200MHz
		–	0.50	0.63	dB	4400 to 5000MHz
		–	0.55	0.72	dB	5150 to 5925MHz
		–	0.64	0.85	dB	5925 to 7125MHz

[1] Measured on application board without any external matching components.

Table 5: RF Characteristics at T_A = −40 °C...85 °C, P_{RF} = 0 dBm, V_{DD} = 1.6V ... 3.6V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion loss[1]						
All RF ports	*IL*	–	0.29	0.40	dB	400 to 960MHz
		–	0.34	0.48	dB	1710 to 2200MHz
		–	0.37	0.51	dB	2300 to 2690MHz
		–	0.44	0.63	dB	3300 to 4200MHz
		–	0.50	0.71	dB	4400 to 5000MHz
		–	0.55	0.80	dB	5150 to 5925MHz
		–	0.64	0.95	dB	5925 to 7125MHz
Return loss[1]						
All RF ports	*RL*	27	34	–	dB	400 to 960MHz
		22	33	–	dB	1710 to 2200MHz
		20	32	–	dB	2300 to 2690MHz
		17	28	–	dB	3300 to 4200MHz
		16	24	–	dB	4400 to 5000MHz
		14	22	–	dB	5150 to 5925MHz
		12	18	–	dB	5925 to 7125MHz

[1] Measured on application board without any external matching components.

Table 6: RF characteristics at T_A = −40 °C...85 °C, P_{RF} = 0 dBm, V_{DD} = 1.6V ... 3.6V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Isolation[1]						
		33	37	–	dB	400 to 960MHz
State 1 & State 2:		26	29	–	dB	1710 to 2200MHz
RF1 to RF3		24	27	–	dB	2300 to 2690MHz
RF2 to RF4	*ISO*	21	24	–	dB	3300 to 4200MHz
		19	22	–	dB	4400 to 5000MHz
		18	21	–	dB	5150 to 5925MHz
		17	20	–	dB	5925 to 7125MHz
Isolation[1]						
		33	38	–	dB	400 to 960MHz
State 1:		26	30	–	dB	1710 to 2200MHz
RF1 to RF4, RF2 to RF3		24	28	–	dB	2300 to 2690MHz
	ISO	21	25	–	dB	3300 to 4200MHz
State 2:		20	23	–	dB	4400 to 5000MHz
RF1 to RF2, RF3 to RF4		19	22	–	dB	5150 to 5925MHz
		18	21	–	dB	5925 to 7125MHz

[1] Measured on application board without any external matching components.

Table 7: RF characteristics at T_A = −40 °C...85 °C, V_{DD} = 1.6V ... 3.6V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Harmonic generation[1] at CW, VSWR 1:1 / 50 Ω						
2nd Harmonic	P_{H2}	–	-84	-78	dBm	LTE LB, 663–915 MHz, P_{RF} = 26 dBm
		–	-80	-76	dBm	LTE MB, 1710–2020 MHz, P_{RF} = 26 dBm
		–	-78	-73	dBm	LTE HB, 2300–2690 MHz, P_{RF} = 26 dBm
		–	-75	-67	dBm	N77 NR, 3300–4200 MHz, P_{RF} = 26 dBm
		–	-72	-67	dBm	N79 NR, 4400–5000 MHz, P_{RF} = 26 dBm
3rd Harmonic	P_{H3}	–	-86	-80	dBm	LTE LB, 663–915 MHz, P_{RF} = 26 dBm
		–	-86	-76	dBm	LTE MB, 1710–2020 MHz, P_{RF} = 26 dBm
		–	-86	-76	dBm	LTE HB, 2300–2690 MHz, P_{RF} = 26 dBm
		–	-86	-72	dBm	N77 NR, 3300–4200 MHz, P_{RF} = 26 dBm
		–	-86	-77	dBm	N79 NR, 4400–5000 MHz, P_{RF} = 26 dBm
Harmonic generation[1] at 25 % duty cycle, VSWR 1:1 / 50 Ω						
2nd Harmonic	P_{H2}	–	-66	-60	dBm	GSM LB, 824–915 MHz, P_{RF} = 35 dBm
		–	-67	-62	dBm	GSM HB, 1710–1910 MHz, P_{RF} = 33 dBm
3rd Harmonic	P_{H3}	–	-60	-55	dBm	GSM LB, 824–915 MHz, P_{RF} = 35 dBm
		–	-66	-60	dBm	GSM HB, 1710–1910 MHz, P_{RF} = 33 dBm
Intermodulation distortion IMD2[1]						
IMD2 low & IMD2 high	*IMD2*	–	-120	-104	dBm	Test conditions, see Tab. 8
IMD2 ULCA		–	-98	-92	dBm	
IMD2 ENDC		–	-100	-92	dBm	
Intermodulation distortion IMD3[1]						
IMD3 mid & IMD3 high	*IMD3*	–	-125	-115	dBm	Test conditions, see Tab. 9
IMD3 ULCA		–	-95	-90	dBm	
IMD3 ENDC		–	-110	-100	dBm	

[1] Measured on application board without any external matching components.

Table 8: IMD2 testcases[1]

Band	Symbol	In-Band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD2,high}$	2140	1950	20	4090	-15
	$B1_{IMD2,low}$	2140	1950	20	190	-15
Band 5	$B5_{IMD2,high}$	881.5	836.5	20	1718	-15
	$B5_{IMD2,low}$	881.5	836.5	20	45	-15
Band 7	$B7_{IMD2,high}$	2655	2535	20	5190	-15
	$B7_{IMD2,low}$	2655	2535	20	120	-15
Band 3 + Band 5 ULCA	$B3B5_{IMD2,ULCA}$	881.5	836.5	23	1718	10
Band 3 + N77 ENDC	$B3N77_{IMD2,ENDC}$	1842.5	1747.5	23	3590	10

[1] Both blockers applied to same RF path.

Table 9: IMD3 testcases[1)]

Band	Symbol	In-Band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD3,high}$	2140	1950	20	6040	-15
	$B1_{IMD3,mid}$	2140	1950	20	1760	-15
Band 5	$B5_{IMD3,high}$	881.5	836.5	20	2554.5	-15
	$B5_{IMD3,mid}$	881.5	836.5	20	791.5	-15
Band 7	$B7_{IMD3,high}$	2655	2535	20	7725	-15
	$B7_{IMD3,mid}$	2655	2535	20	2415	-15
Band 1 + Band 3 ULCA	$B1B3_{IMD3,ULCA}$	2140	1950	23	1760	10
Band 5 + N78 ENDC	$B5N78_{IMD3,ENDC}$	2122	3780	26	829	10

[1)] Both blockers applied to same RF path.

Table 10: Switching time at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, V_{DD} = 1.6V ... 3.6V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching time[1)]						
Switching time	t_{ST}	–	1.3	1.8	µs	Time between RF states in active mode $V_{Ctrl,H}$ Min. or $V_{Ctrl,L}$ Max. level to 90% RF-signal
RF rise time	t_{RT}	–	0.65	0.9	µs	Time between 10% to 90% RF Signal
Power up settling time	t_{PUP}	–	10	25	µs	Time from V_{DD} Min. power level to 90% RF-signal

[1)] Measured on application board without any external matching components.

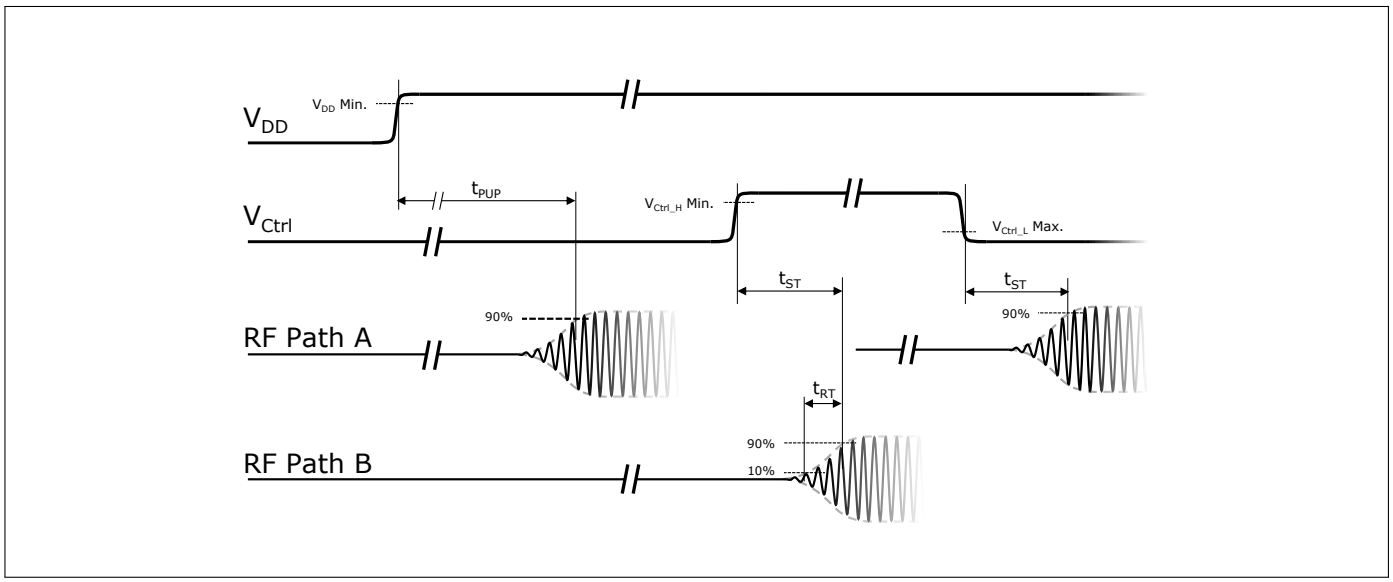

Figure 1: CTRL to RF time

4 Modes of operation

Table 11: Modes of operation (truth table)

		Control input
State	**Mode**	**CTRL**
1	RF1 - RF2	0
	RF3 - RF4	
2	RF1 - RF4	1
	RF3 - RF2	

5 Application Information

Pin Configuration and Function

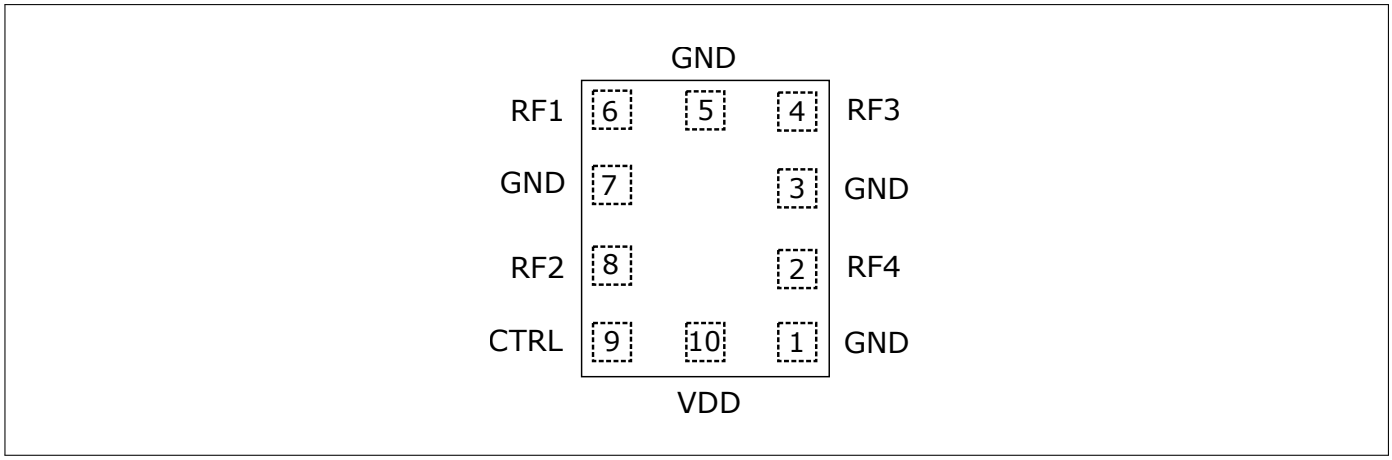

Figure 2: BGSX22G6U10 Pin Configuration (top view)

Table 12: Pin Definition and Function

Pin No.	Name	Function
1	GND	DC ground
2	RF4	RF port 4
3	GND	RF ground
4	RF3	RF port 3
5	GND	RF ground
6	RF1	RF port 1
7	GND	RF ground
8	RF2	RF port 2
9	CTRL	GPIO control pin
10	VDD	Power supply

6 Package information

Table 13: Mechanical data

Parameter	Symbol	Value	Unit
X-Dimension	*X*	1.1 ± 0.05	mm
Y-Dimension	*Y*	1.5 ± 0.05	mm
Size	*Size*	1.65	mm^2
Height	*H*	0.60 ± 0.05	mm

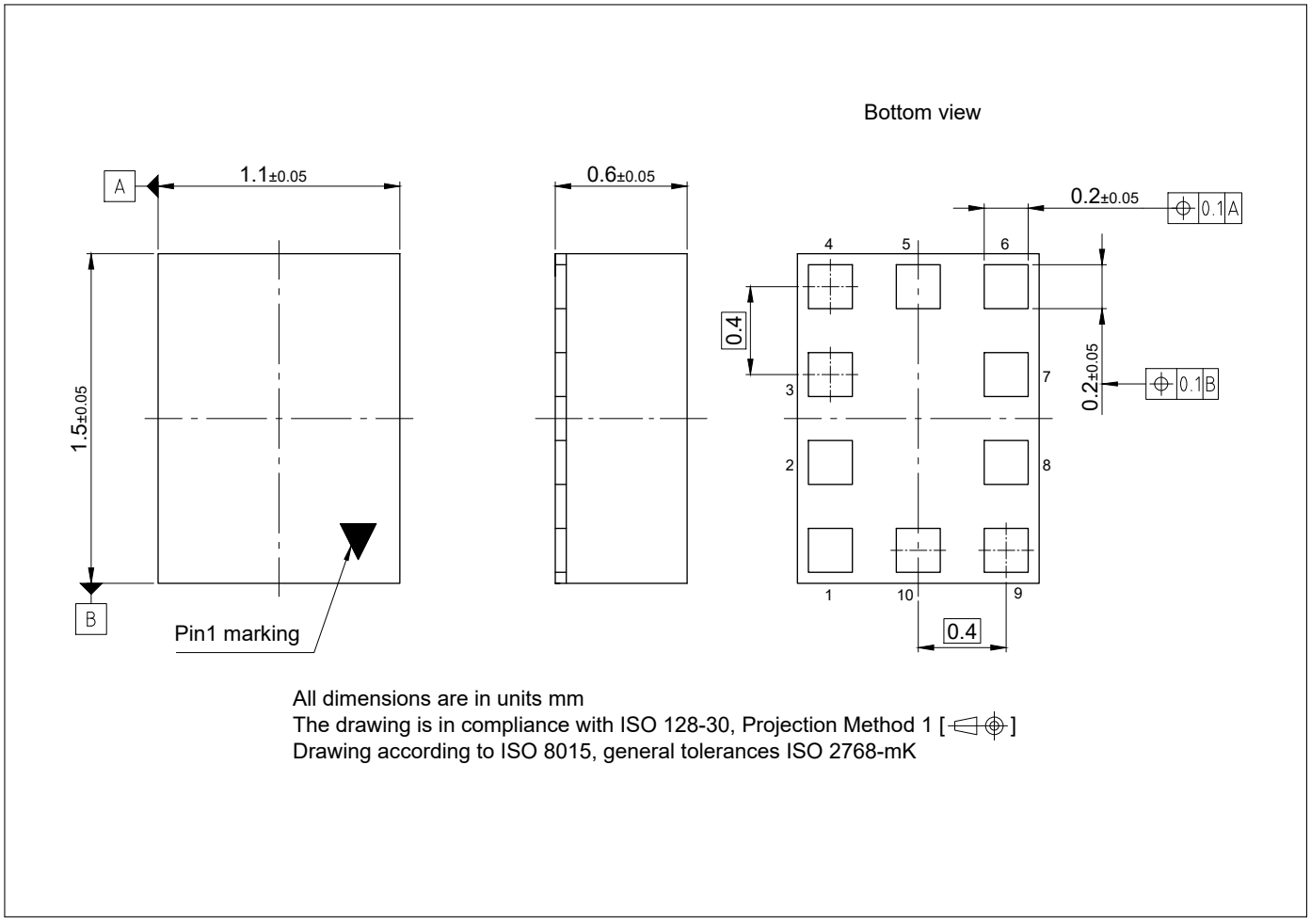

Figure 3: Package outline (top, side and bottom views)

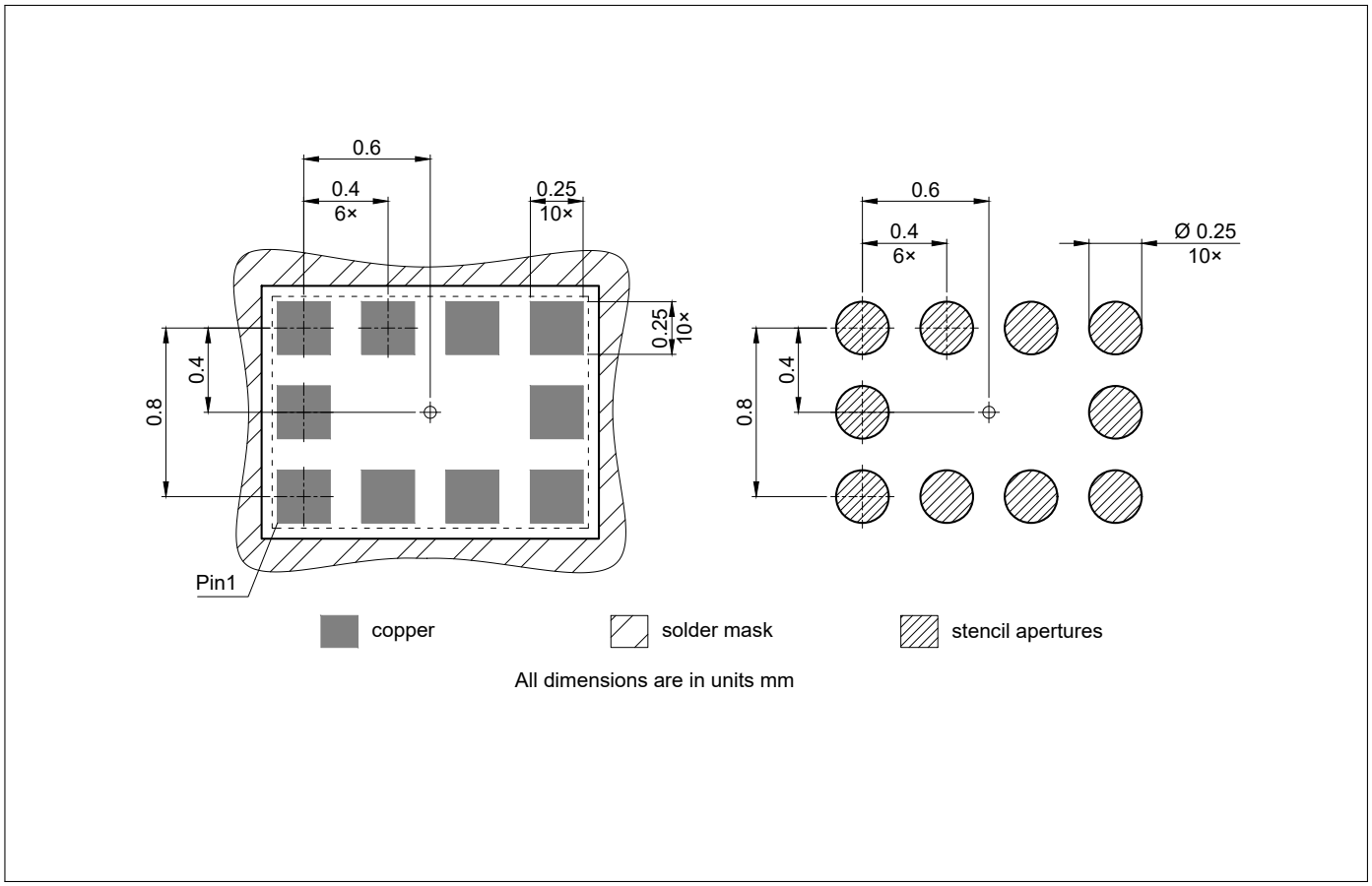

Figure 4: Footprint recommendation

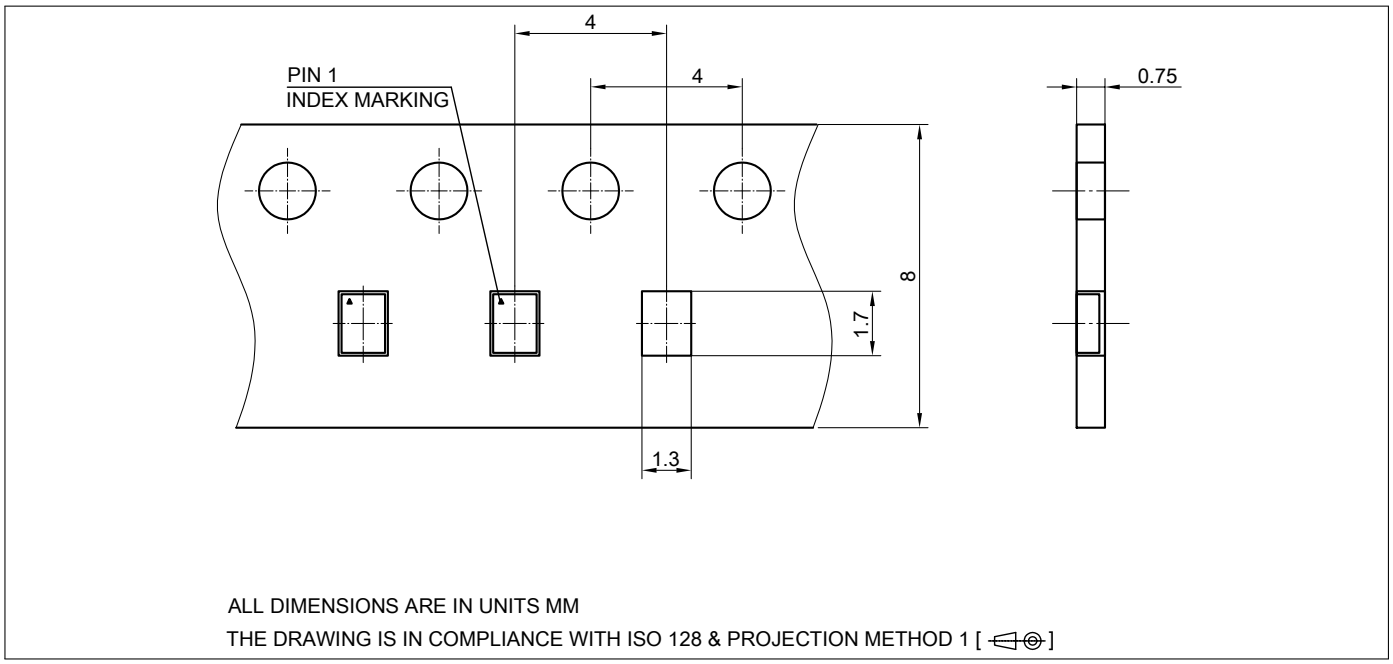

Figure 5: Carrier tape

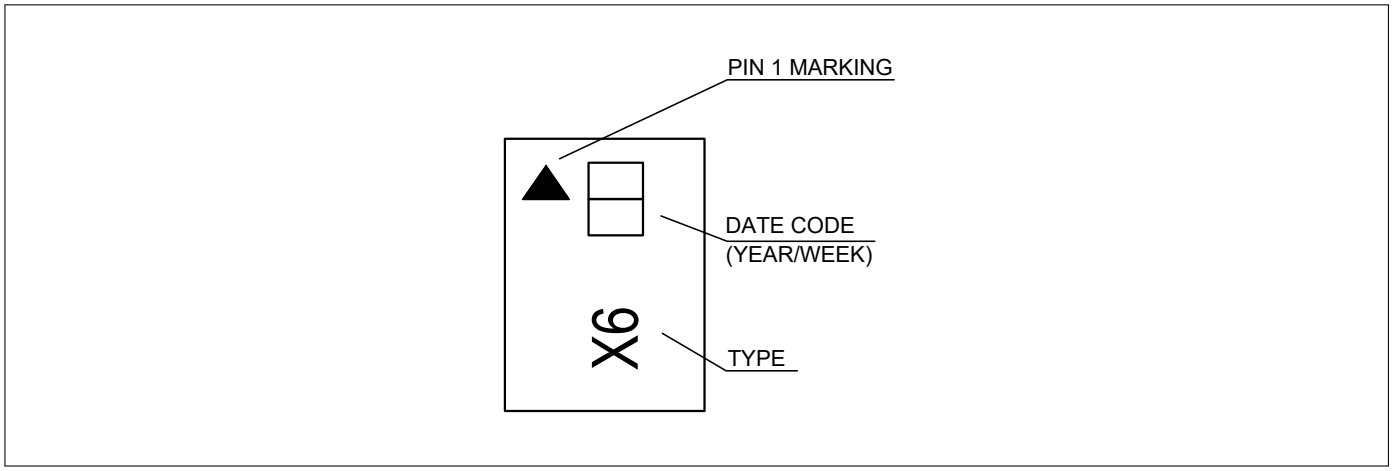

Figure 6: Marking specification (top view): date code digits Y and W defined in tables 14 and 15

Table 14: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"
2020	0	2030	0
2021	1	2031	1
2022	2	2032	2
2023	3	2033	3
2024	4	2034	4
2025	5	2035	5
2026	6	2036	6
2027	7	2037	7
2028	8	2038	8
2029	9	2039	9

Table 15: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
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	Initial version

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