ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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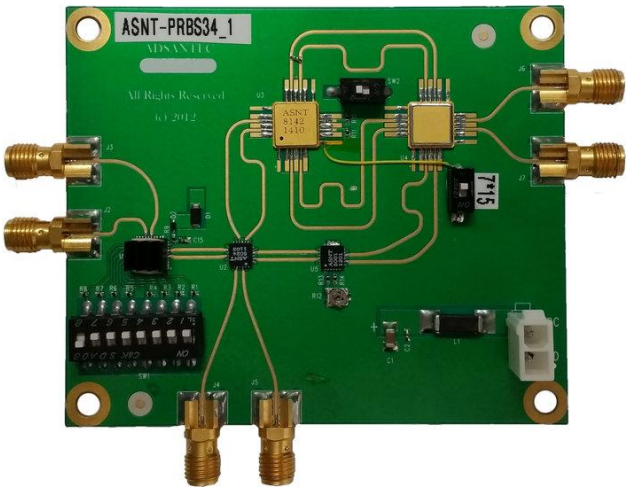
ASNT_PRBS34_1
8*Gbps*-34*Gbps* PRBS7/PRBS15 Generator with Sync Output



- Broadband frequency range from 8*Gbps* – 34*Gbps*
- On board data rate multiplexer to reduce the input clock frequency rate
- Adjustable phase shift for multiplexer clock input
- 1-256 divide sync output
- Differential inputs and outputs
- Minimal insertion jitter
- Fast rise and fall times
- 50% duty cycle sync output on all divide ratios
- Single +3.3*V* supply

DESCRIPTION

The ASNT_PRBS34_1 is a broadband 2^7-1 or 2^{15}-1 PRBS generator intended for test, prototyping, microwave, and communication applications. A single-ended or differential clock from 4*GHz* to 17*GHz* can be used. A differential Sync Output divides the input clock from 1 to 256 allowing a PRBS7 pattern view on an oscilloscope by using a divide ratio 127 or 254. The PRBS7/PRBS15 data output is multiplexed to double the data rate, giving a maximum data rate of 34*Gbps*. An on-board trim potentiometer allows to phase adjust the multiplexer clock input for all input clock frequencies in a specified range to ensure the best output is achieved. An on-board PRBS reset switch presets the generator to avoid the all zero state lock-up.

The ASNT_PRBS34_1 board contains six Emerson SMA connectors MFG PN: 142-0761-881, 50*Ohm* transmission lines to the device, and power supply decoupling networks on the evaluation board. Power is supplied through a two-pin MOLEX connector P/N: 39-28-1023

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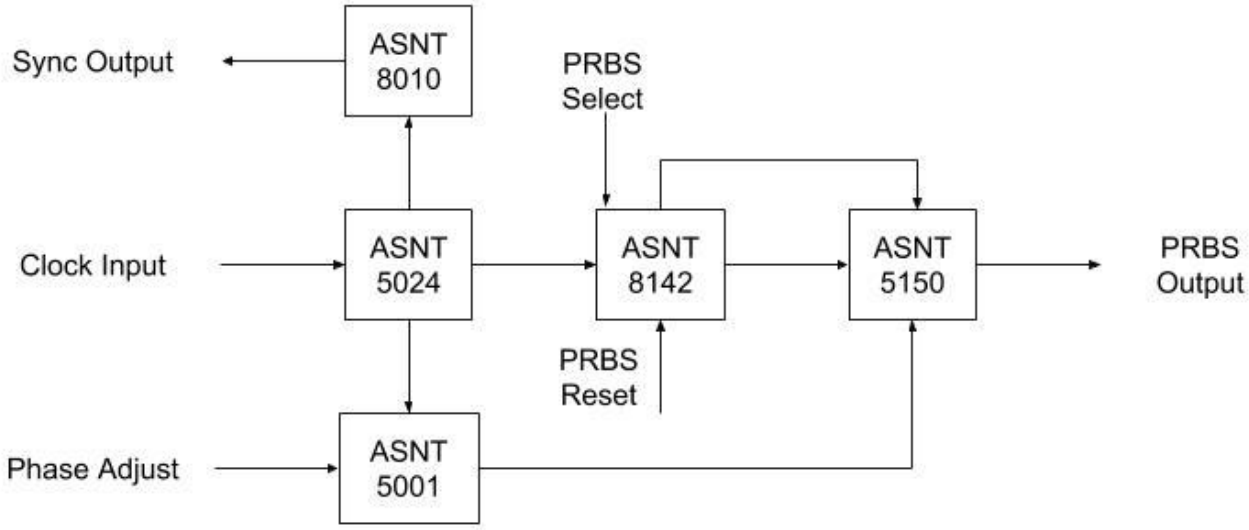
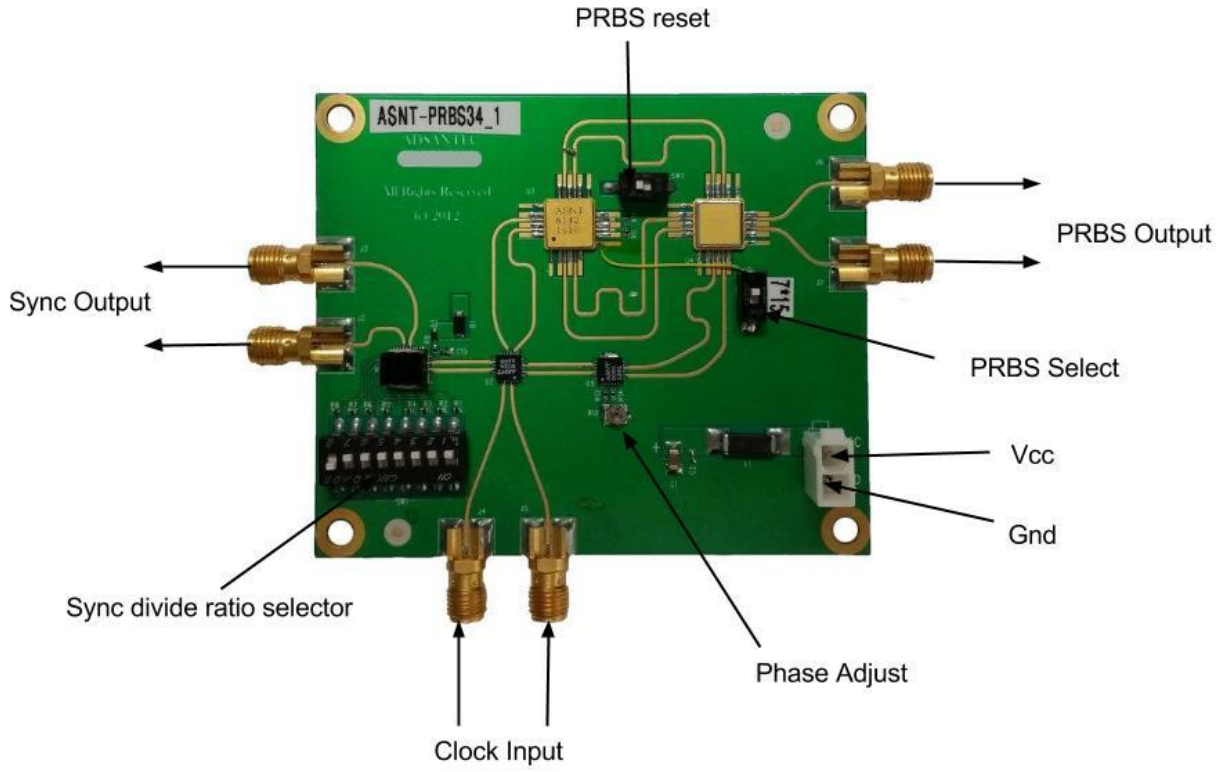
FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS



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PRBS Select

Move the switch to the ON position for PRBS15 data. Move the switch to the OFF position for PRBS7 data output. The PRBS Reset may need to be toggled to the ON position then OFF before a PRBS pattern is observed on the data output.

Sync Output

The Sync Output can be configured to output any divide ratio from 1 to 256 of the clock input. It contains eight switches that represent 8 bits. The LSB starts at SW1 and the MSB ends at SW8. The binary value of zero gives a decimal n value of 256. Increasing binary values increases the decimal value n as shown in Table 1.

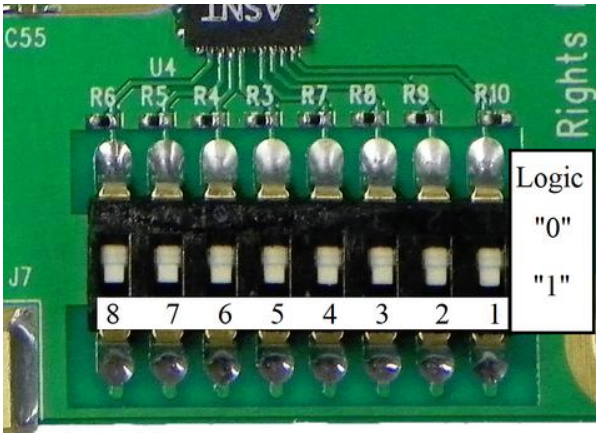

Table 1. Divide ratio

DIP SW # 8 7 6 5 4 3 2 1	n Divide Ratio	
0 0 0 0 0 0 0 1	1	
0 0 0 0 0 0 1 0	2	
0 0 0 1 0 0 0 0	16	Eye diagram
.		
0 1 1 1 1 1 1 1	127	pattern
1 1 1 1 1 1 1 0	254	pattern
0 0 0 0 0 0 0 0	256	

OPERATION

1. Measure 50*Ohms* on all SMA connectors referenced to vcc.
2. Set the PRBS Reset switch to the OFF position.
3. Set the power supply to 0*V* and current limit it to 1.8*A*.
4. Connect the power supply to the board and slowly increase to +3.3*V*.
5. Apply an AC coupled single-ended/differential clock signal to the Clock Input.
6. Connect PRBS Output to a 50*Ohm* terminated AC coupled oscilloscope single-ended/differentially.
7. Connect Sync Output AC coupled to trigger single-ended/differentially.

   Note: If using single-ended input/output only, apply an AC coupled 50*Ohm* termination to the unused input/output. This will reduce any noise present.

7. Set the PRBS Reset switch to the ON position then to the OFF position. Set the PRBS Select switch to the ON position to select PRBS15, or to the OFF position to select PRBS7.

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8. Use a divide by 127 for the Sync Output to view the PRBS7 pattern on the oscilloscope.
9. Scroll/Delay the 127 bit PRBS7 pattern on the oscilloscope until you observe a sequence of data close to 7 one's followed by 6 zero's. You may find a pattern shown below in **Figure 1**, which is incorrect.

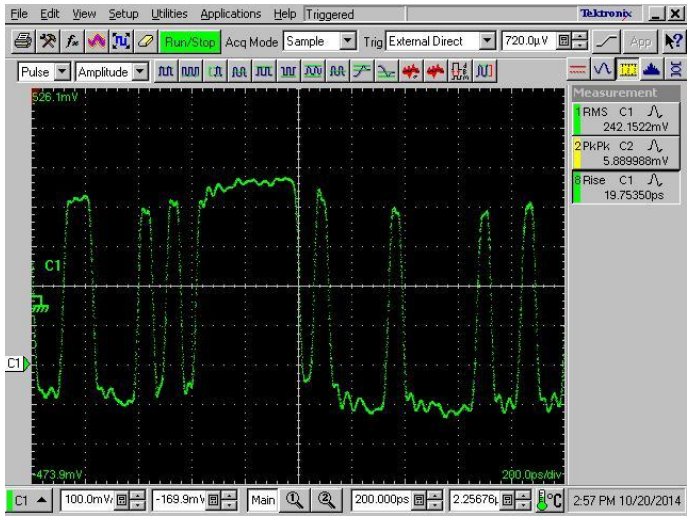

Figure 1. Incorrect PRBS7 pattern

10. Adjust the Phase Adjust potentiometer in order to get the correct PRBS7 pattern as shown in **Figure 2**.

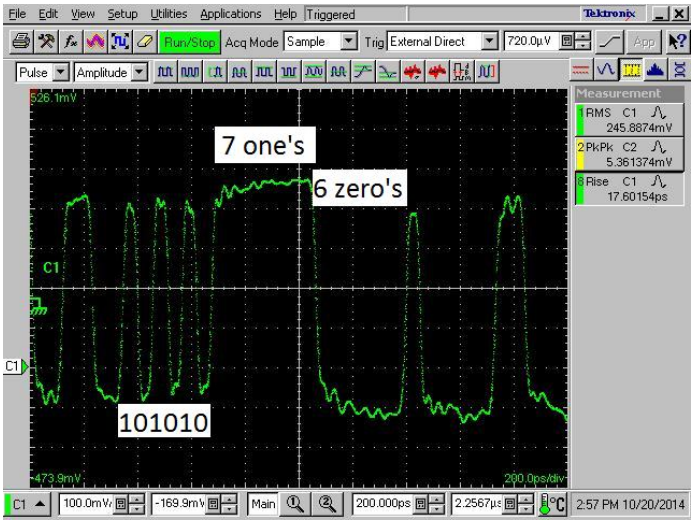

Figure 2. Correct PRBS7 pattern

Alternatively, an error detector can be used instead of an oscilloscope to find the correct PRBS7 pattern.
Note: After adjusting the data output using PRBS7, PRBS15 may be selected and will give the correct PRBS15 pattern.

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If the clock input rate is changed, repeat steps 7 and 9.

MEASURED RESULTS

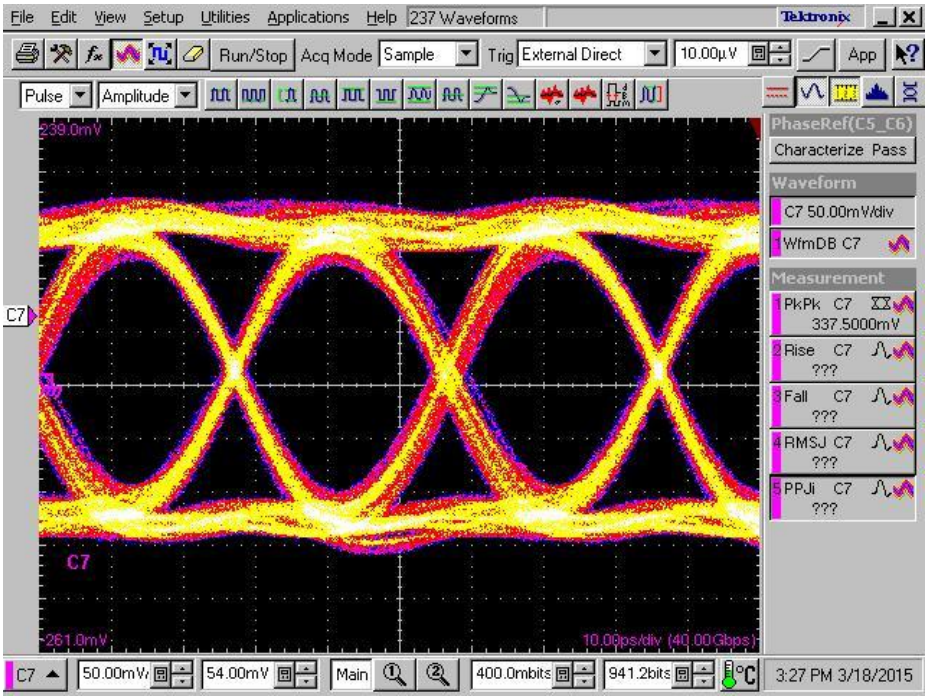

Fig. 3. 34Gbps eye diagram

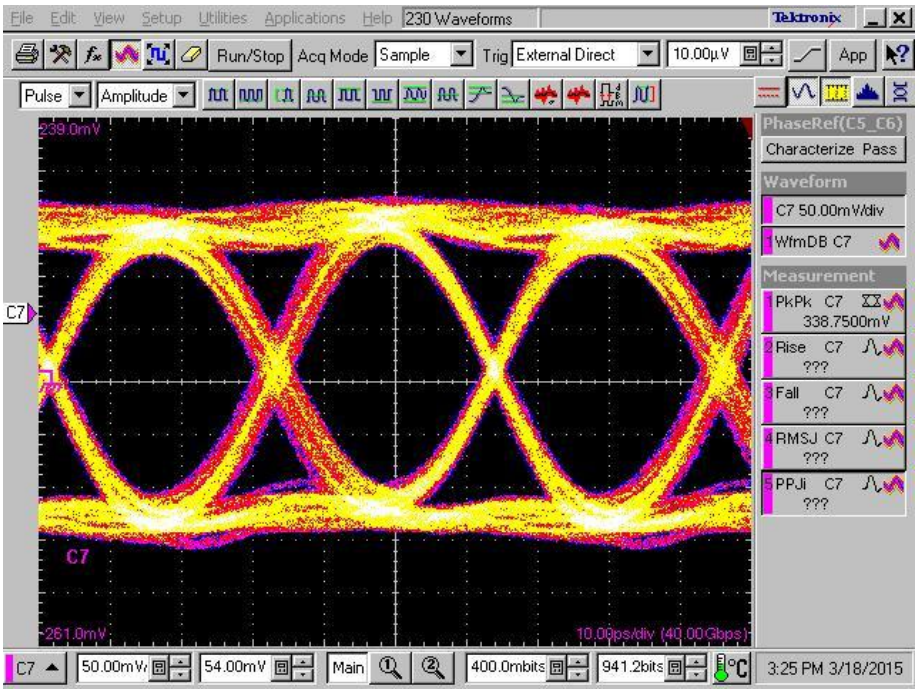

Fig. 4. 32Gbps eye diagram

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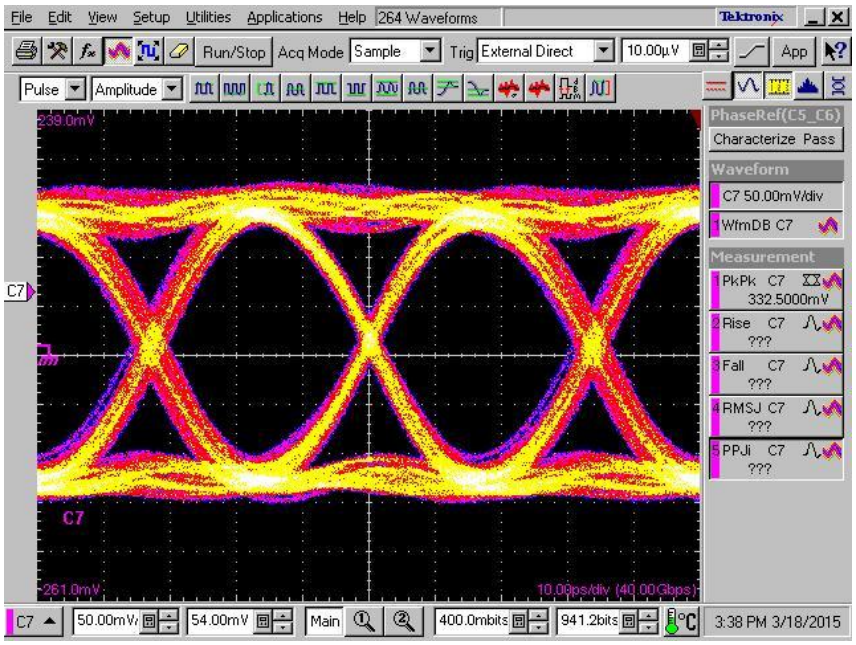

Fig. 5. 30Gbps eye diagram

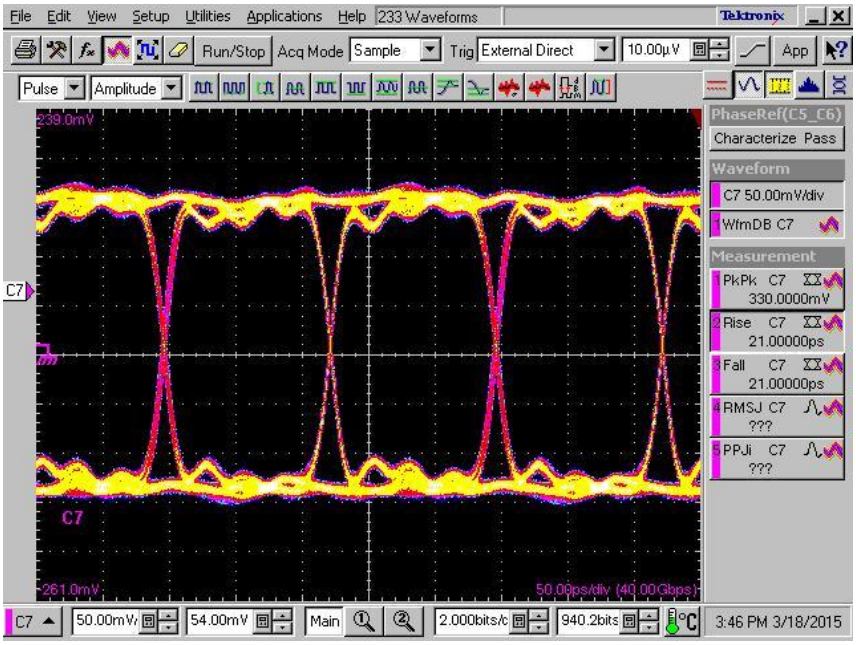

Fig. 6. 8Gbps eye diagram

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ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Comments
vee		0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	
I_{VCC}	1.36	1.7	2.04	*A*	
Power		5.6		*W*	
Operating Temperature	-25	50	85	*°C*	
Clock Input					
Frequency	4		17	*GHz*	
Single-Ended Swing	50	400	1000	*mV*	Peak-to-Peak
Common mode level	vcc -0.8	vcc -0.2	vcc	*V*	
Duty Cycle	40%	50%	60%		Range of input tolerance
Sync Output					
Frequency	0.007		17	*GHz*	
Single-Ended Swing	570	600	630	*mV*	Peak-to-Peak
Common-Mode Level	vcc - (Single-Ended Swing)/2				
Rise/Fall Times	15	17	19	*ps*	20% to 80%
Duty Cycle	45%	50%	55%		For clock signal
PRBS Output					
Data rate	8		34	*Gbps*	
Single-Ended Voltage Level		330		*mV*	Peak-to-Peak
Common Mode Level	vcc - (Single-Ended Swing)/2			*V*	
Duty Cycle	40%	50%	60%		
Rise/Fall Time		21		*ps*	20% to 80%

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REVISION HISTORY

Revision	Date	Changes
1.3.2	07-2019	Updated Letterhead
1.3.1	04-2019	Added P/N of connectors to board description
1.2.1	06-2017	Revised Electrical Characteristics
1.1.1	04-2015	Updated pictures Added PRBS Select section Updated Operation section Revised Electrical Characteristics
1.0.1	04-2015	Initial release