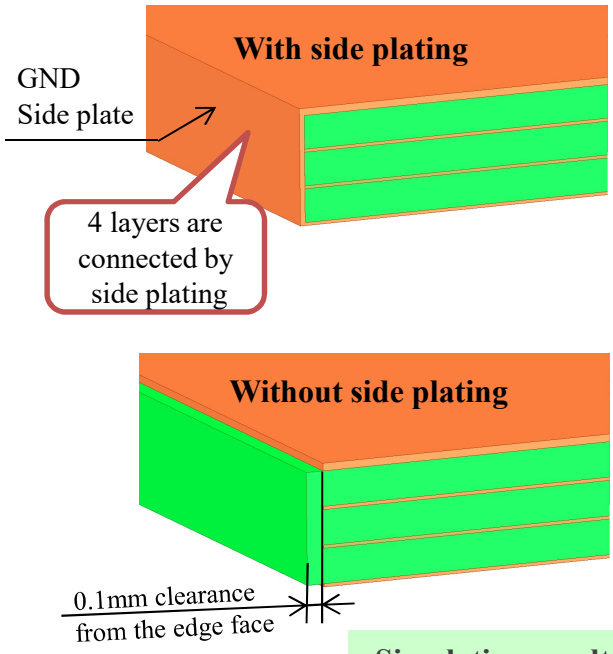
PCB board design tips

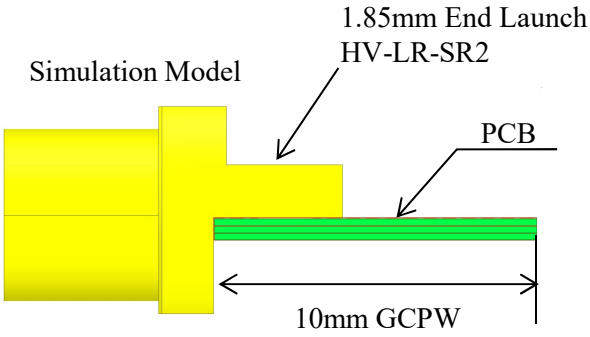
As the needs for high frequency measurement is increasing due to the high speed transmission inside equipment, the level of difficulty for designing is getting higher. When designing RF board, engineers should consider different factors including power dissipation, board size and noises etc.

The following board guidance shows the points to keep in mind when using our End Launch connector. Hirose highly recommends to optimize PCB pattern and the ground via position to match the specific connectors you will be using. In the case you need to optimize PCB with Hirose, please visit our website for more details at https://www.hirose.com/product/en/pr/mmwave/ and contact us.

Side plating effects

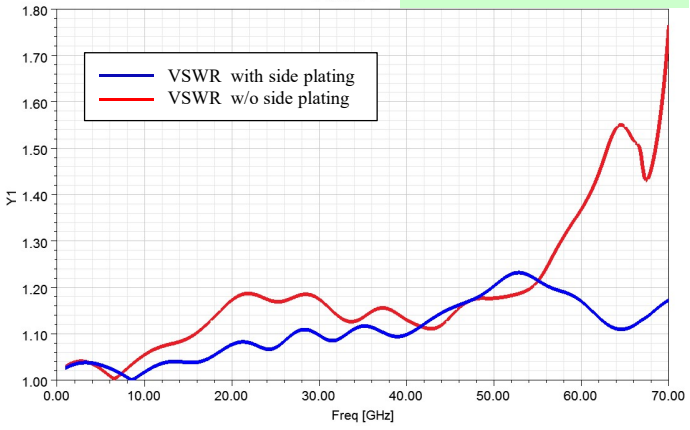
◆ As the frequency increases, more stable characteristics can be achieved by side plating.





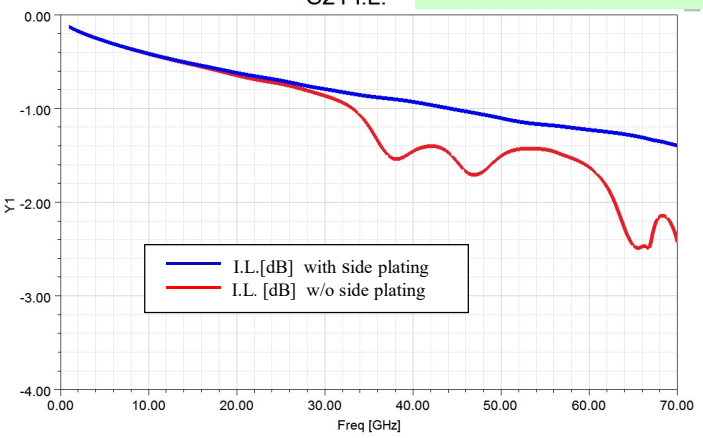
Simulation result

VSWR



Simulation result

S21 I.L.

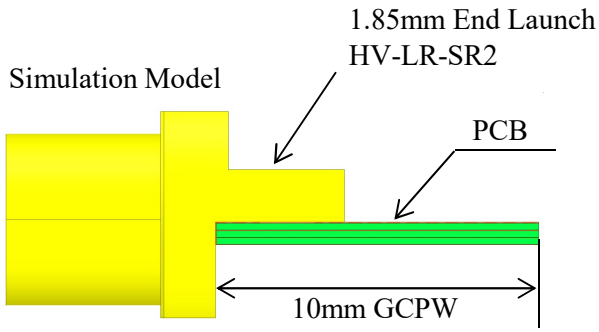


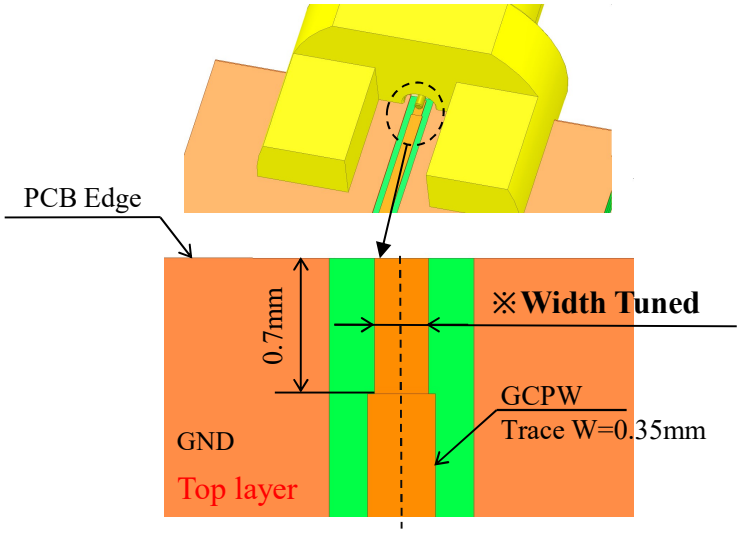
Trace width optimization

◆ According to the trace design of a connector mounted position, RF characteristic and TDR Impedance can be optimized by ※the trace width change of the edge of the board.

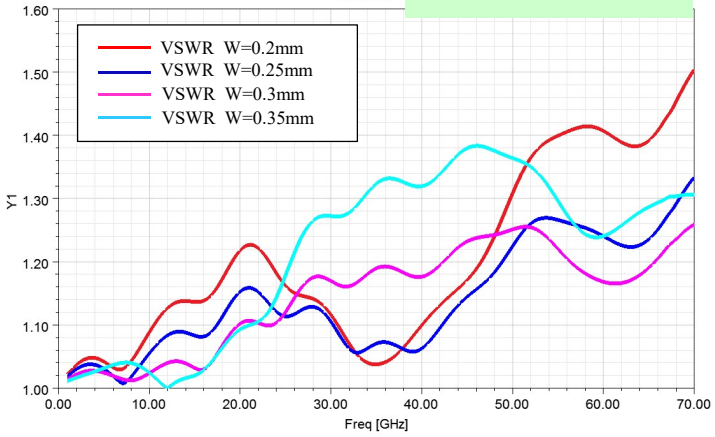
Simulation PCB layer

Top	43 micron (Copper foil + Plating)
	200 micron (Meg.6 R-5775K εr=3.62)
2nd	18 micron (Copper foil)
	200 micron (Meg.6 R-5670KG εr=3.62)
3rd	18 micron (Copper foil)
	200 micron (Meg.6 R-5775K εr=3.62)
4th	43 micron (Copper foil + Plating)

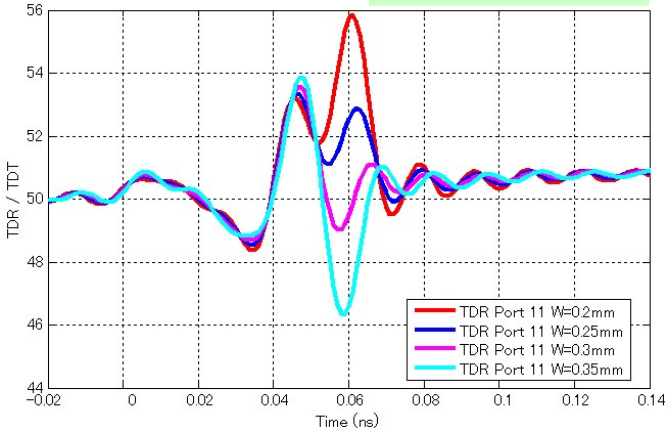




Simulation result



Simulation result

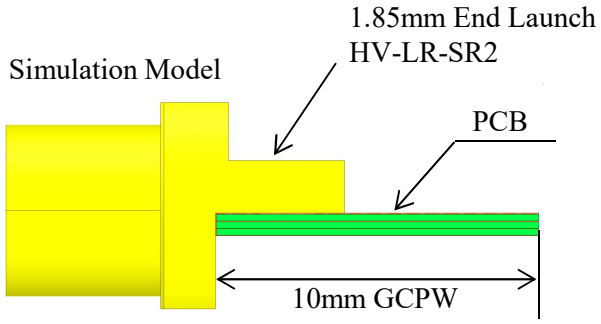


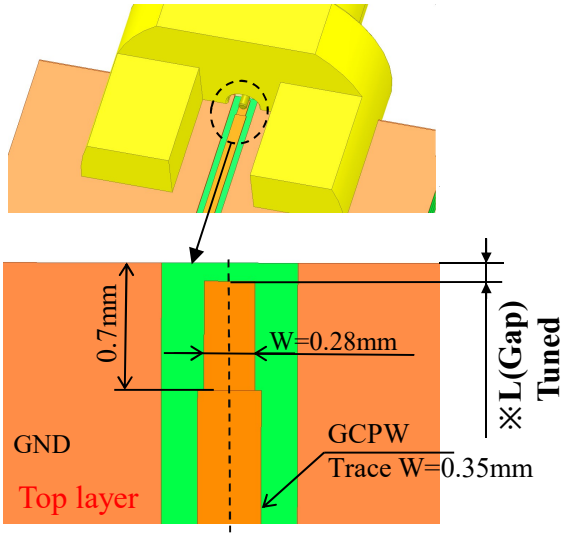
Trace gap optimization

◆ According to the trace design of a connector mounted position , RF characteristic and TDR Impedance can be optimized by ※the length (Gap) change of the edge of the board.

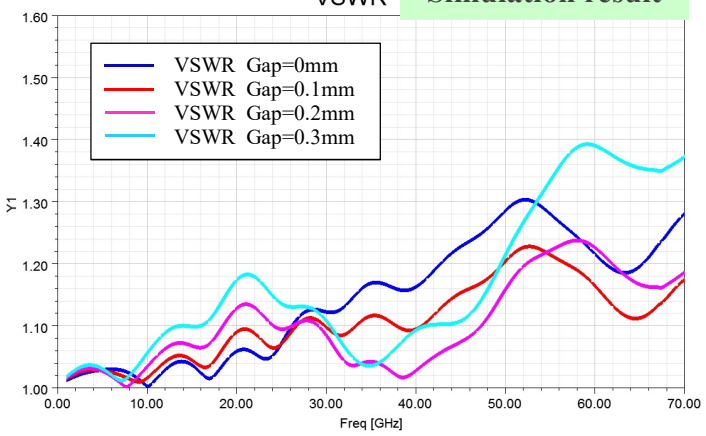
Simulation PCB layer

Top	43 micron (Copper foil + Plating)
	200 micron (Meg.6 R-5775K εr=3.62)
2nd	18 micron (Copper foil)
	200 micron (Meg.6 R-5670KG εr=3.62)
3rd	18 micron (Copper foil)
	200 micron (Meg.6 R-5775K εr=3.62)
4th	43 micron (Copper foil + Plating)

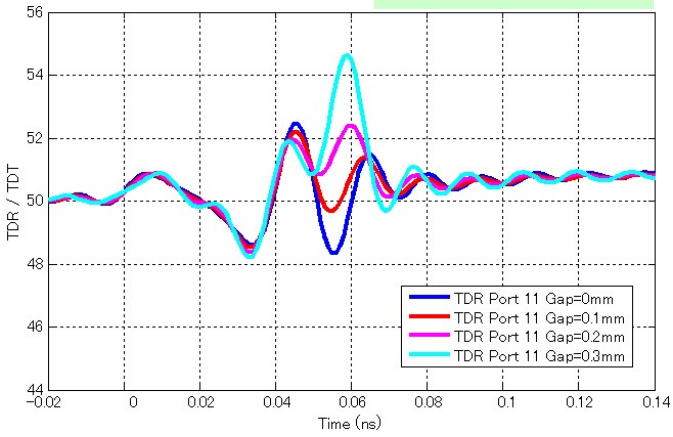




Simulation result



Simulation result



CPWG recommended stitching via pitch

◆ In order to prevent resonance in the structure of the coplanar line, we recommend a stitching via of less than ¼ wavelength on both sides of the ground as shown below.

Simulation PCB layer

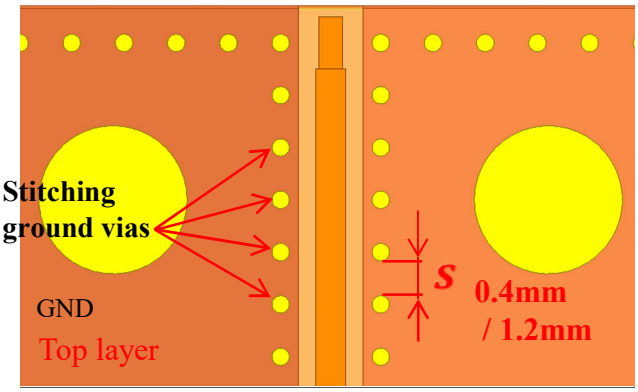
Top	43 micron (Copper foil + Plating)
	200 micron (Meg.6 R-5775K εr=3.62)
2nd	18 micron (Copper foil)
	200 micron (Meg.6 R-5670KG εr=3.62)
3rd	18 micron (Copper foil)
	200 micron (Meg.6 R-5775K εr=3.62)
4th	43 micron (Copper foil + Plating)

$$s < \frac{\lambda_0}{4\sqrt{\varepsilon_{eff}}}$$

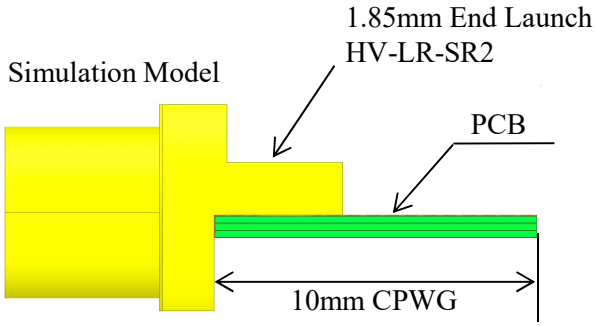
S : Via pitch interval

λ_0 : Electric wavelength

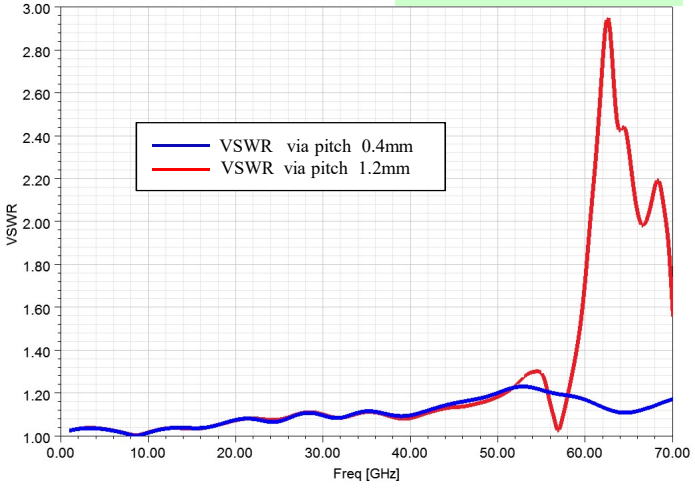
ε_{eff} : Effective dielectric constant



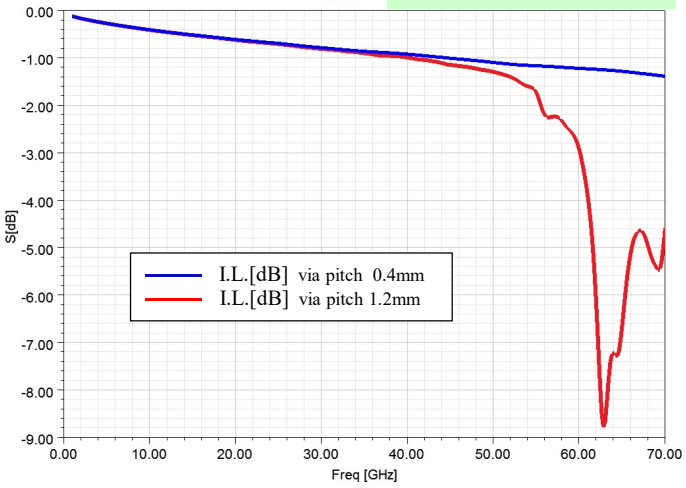
Trace



VSWR **Simulation result**



S21 **Simulation result**



CPWG recommended stitching via intervals

◆ For the interval of the stitching via on the side of the signal line, width of more than three times of the signal trace width or less than one-half wavelength is recommended. If the via is too close to signal trace, there is an opportunity that impedance might be affected. When the via is too far from the signal trace, unintended propagation modes may occur and there is a risk of affecting the RF characteristics.

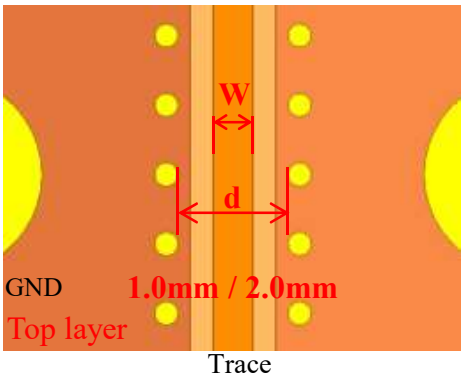
Simulation PCB layer

Top	43 micron (Copper foil + Plating)
	200 micron (Meg.6 R-5775K εr=3.62)
2nd	18 micron (Copper foil)
	200 micron (Meg.6 R-5670KG εr=3.62)
3rd	18 micron (Copper foil)
	200 micron (Meg.6 R-5775K εr=3.62)
4th	43 micron (Copper foil + Plating)

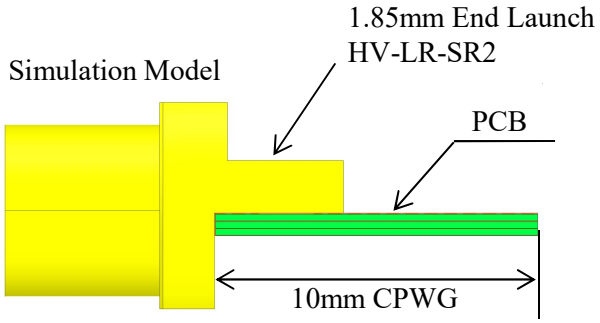
$$d > 3w$$

$$d < \frac{\lambda_0}{2\sqrt{\varepsilon_{eff}}}$$

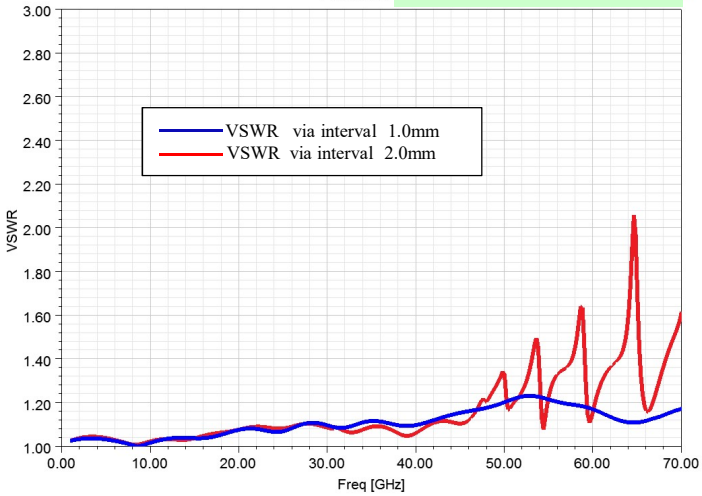
d : Via interval
w : Signal linewidth
λ_0 : Electric wavelength
ε_{eff} : Effective dielectric constant



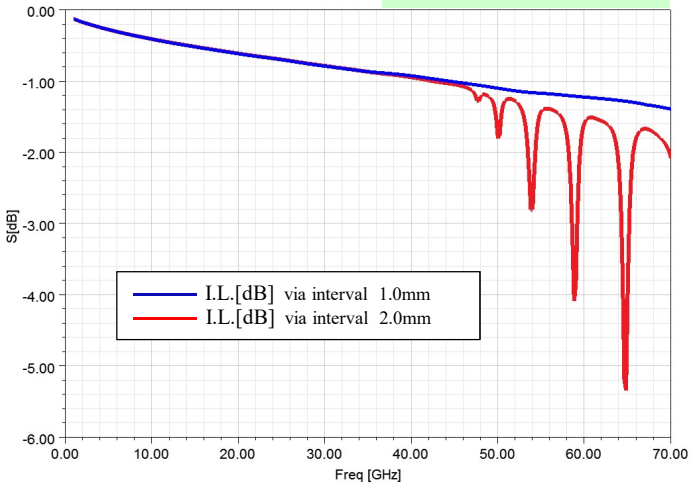
Trace



VSWR **Simulation result**



S21 **Simulation result**



Others

The introduced design information herein are generally depends on the board permittivity, thickness and layer structure. The higher frequency used, the more difficult the design is. Depending on whether the connector and the mounting areas are optimized or not, there will be a significant difference in performance.

If you have any questions about designing high-frequency circuit board, please contact us.

https://www.hirose.com/

To optimize the performance of the board, we can provide electromagnetic field simulation models of connectors and various kinds of information. Please see below.

https://www.hirose.com/product/en/pr/mmwave/board_test/