

DDR4 SDRAM UDIMM Addendum

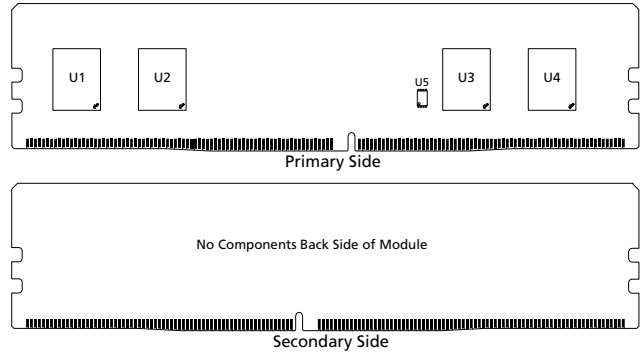
MTA4ATF1G64AZ – 8GB

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR4 UDIMM Core data sheet.

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 UDIMM core data sheet
- 288-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rate: PC4-3200, PC4-2666
- 8GB (1 Gig x 64)
- Data bus inversion (DBI) for data bus
- Single-rank
- On-board I²C serial presence-detect (SPD) EEPROM
- 8 internal banks; 2 groups of 4 banks each

Figure 1: 288-Pin UDIMM (R/C C0)



Options

- Operating temperature
 - Commercial (0°C ≤ T_{OPER} ≤ 95°C)
- Package
 - 288-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)
 - 0.75ns @ CL = 19 (DDR4-2666)

Marking

- None
- Z
- 3G2
- 2G6

Table 1: Addressing

Parameter	8GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	2 BG0
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (1 Gig x 16), 8 banks
Module rank address	CS0_n



Table 2: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT40A1G16,¹ 16Gb DDR4 SDRAM

Part Number²	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL_{-n}RCD_{-n}RP)
MTA4ATF1G64AZ-3G2__	8GB	1 Gig x 64	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA4ATF1G64AZ-2G6__	8GB	1 Gig x 64	21.3 GB/s	0.75ns/2666 MT/s	19-19-19

- Notes: 1. The data sheet for the base device can be found on micron.com.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA4ATF1G64AZ-3G2F1.



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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	00	3	157	U2	00	19	179
	01	1	150		01	17	172
	02	2	12		02	18	34
	03	0	5		03	16	27
	04	7	155		04	23	177
	05	5	148		05	21	170
	06	6	10		06	22	32
	07	4	3		07	20	25
	08	11	168		08	27	190
	09	8	16		09	24	38
	10	10	23		10	26	45
	11	9	161		11	25	183
	12	14	21		12	30	43
	13	13	159		13	29	181
	14	15	166		14	31	188
	15	12	14	15	28	36	
U3	00	35	249	U4	00	51	271
	01	33	242		01	49	264
	02	34	104		02	50	126
	03	32	97		03	48	119
	04	39	247		04	55	269
	05	37	240		05	53	262
	06	38	102		06	54	124
	07	36	95		07	52	117
	08	43	260		08	59	282
	09	40	108		09	56	130
	10	42	115		10	58	137
	11	41	253		11	57	275
	12	46	113		12	62	135
	13	45	251		13	61	273
	14	47	257		14	63	280
15	44	106	15	60	128		



I_{DD} Specifications

Table 4: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 8GB (Die Revision E)

Values are for the MT40A1G16 DDR4 SDRAM only and are computed from values specified in the 16Gb (1 Gig x 16) component data sheet

Parameter	Symbol	3200	2666	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	280	272	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I _{pp} current	I _{PP0}	16	16	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	336	328	mA
Precharge standby current	I _{DD2N}	180	172	mA
Precharge standby ODT current	I _{DD2NT}	232	224	mA
Precharge power-down current	I _{DD2P}	152	152	mA
Precharge quiet standby current	I _{DD2Q}	168	168	mA
Active standby current	I _{DD3N}	248	240	mA
Active standby I _{pp} current	I _{PP3N}	8	8	mA
Active power-down current	I _{DD3P}	204	196	mA
Burst read current	I _{DD4R}	1196	1052	mA
Burst write current	I _{DD4W}	944	852	mA
Burst refresh current (1x REF)	I _{DD5R}	272	272	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R}	16	16	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N}	212	212	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E}	452	452	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R}	80	80	mA
Auto self refresh current (25°C)	I _{DD6A}	44	44	mA
Auto self refresh current (45°C)	I _{DD6A}	80	80	mA
Auto self refresh current (75°C)	I _{DD6A}	204	204	mA
Auto self refresh current (95°C)	I _{DD6A}	452	452	mA
Auto self refresh I _{pp} current	I _{PP6X}	24	24	mA
Bank interleave read current	I _{DD7}	980	944	mA
Bank interleave read I _{pp} current	I _{PP7}	36	36	mA
Maximum power-down current	I _{DD8}	144	144	mA

Notes: 1. When T_C > 85°C, the I_{DD} and I_{pp} values must be derated. Refer to the base device data sheet I_{DD} and I_{pp} specification tables for derating values for the applicable die-revision.



8GB (x64, SR) 288-Pin DDR4 UDIMM I_{DD} Specifications

Table 5: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 8GB (Die Revision B)

Values are for the MT40A1G16 DDR4 SDRAM only and are computed from values specified in the 16Gb (1 Gig x 16) component data sheet

Parameter	Symbol	3200	2666	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	312	304	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I _{pp} current	I _{PP0}	20	20	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	396	388	mA
Precharge standby current	I _{DD2N}	208	200	mA
Precharge standby ODT current	I _{DD2NT}	260	252	mA
Precharge power-down current	I _{DD2P}	172	172	mA
Precharge quiet standby current	I _{DD2Q}	188	188	mA
Active standby current	I _{DD3N}	324	316	mA
Active standby I _{pp} current	I _{PP3N}	12	12	mA
Active power-down current	I _{DD3P}	288	280	mA
Burst read current	I _{DD4R}	1304	1136	mA
Burst write current	I _{DD4W}	1096	960	mA
Burst refresh current (1x REF)	I _{DD5R}	316	308	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R}	20	20	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N}	268	268	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E}	484	484	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R}	116	116	mA
Auto self refresh current (25°C)	I _{DD6A}	40	40	mA
Auto self refresh current (45°C)	I _{DD6A}	116	116	mA
Auto self refresh current (75°C)	I _{DD6A}	244	244	mA
Auto self refresh current (95°C)	I _{DD6A}	484	484	mA
Auto self refresh I _{pp} current	I _{PP6X}	44	44	mA
Bank interleave read current	I _{DD7}	1072	1040	mA
Bank interleave read I _{pp} current	I _{PP7}	44	44	mA
Maximum power-down current	I _{DD8}	160	160	mA

Notes: 1. When T_C > 85°C, the I_{DD} and I_{pp} values must be derated. Refer to the base device data sheet I_{DD} and I_{pp} specification tables for derating values for the applicable die-revision.



8GB (x64, SR) 288-Pin DDR4 UDIMM I_{DD} Specifications

Table 6: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 8GB (Die Revision F)

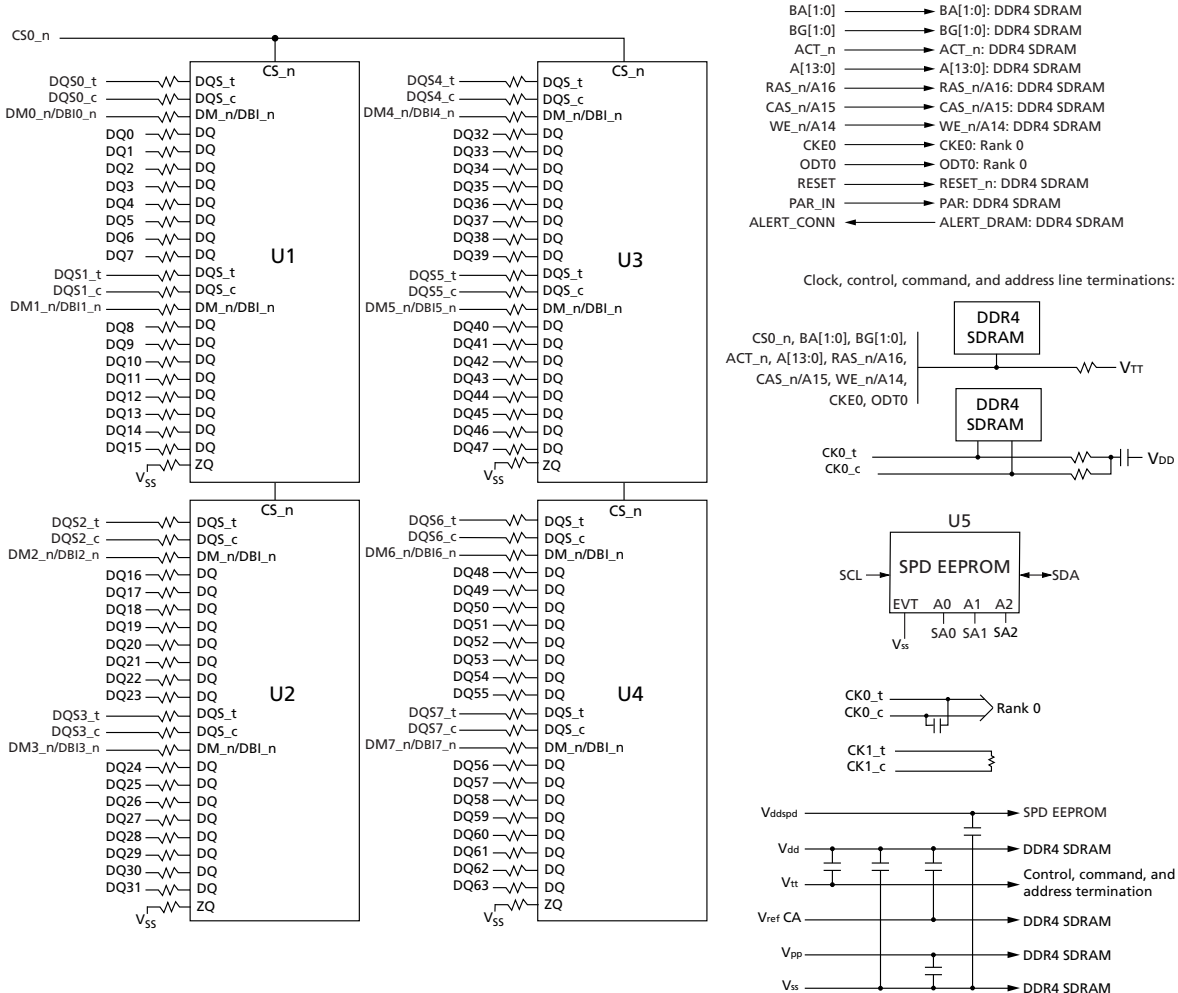
Values are for the MT40A1G16 DDR4 SDRAM only and are computed from values specified in the 16Gb (1 Gig x 16) component data sheet

Parameter	Symbol	3200	2666	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	280	272	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I _{pp} current	I _{PP0}	16	16	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	336	328	mA
Precharge standby current	I _{DD2N}	180	172	mA
Precharge standby ODT current	I _{DD2NT}	232	224	mA
Precharge power-down current	I _{DD2P}	152	152	mA
Precharge quiet standby current	I _{DD2Q}	168	168	mA
Active standby current	I _{DD3N}	248	240	mA
Active standby I _{pp} current	I _{PP3N}	8	8	mA
Active power-down current	I _{DD3P}	204	196	mA
Burst read current	I _{DD4R}	772	668	mA
Burst write current	I _{DD4W}	564	484	mA
Burst refresh current (1x REF)	I _{DD5R}	272	272	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R}	16	16	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N}	212	212	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E}	360	360	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R}	80	80	mA
Auto self refresh current (25°C)	I _{DD6A}	44	44	mA
Auto self refresh current (45°C)	I _{DD6A}	80	80	mA
Auto self refresh current (75°C)	I _{DD6A}	204	204	mA
Auto self refresh current (95°C)	I _{DD6A}	360	360	mA
Auto self refresh I _{pp} current	I _{PP6X}	24	24	mA
Bank interleave read current	I _{DD7}	800	760	mA
Bank interleave read I _{pp} current	I _{PP7}	52	52	mA
Maximum power-down current	I _{DD8}	144	144	mA

Notes: 1. When T_C > 85°C, the I_{DD} and I_{pp} values must be derated. Refer to the base device data sheet I_{DD} and I_{pp} specification tables for derating values for the applicable die-revision.

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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