Thermal Management of NV612X *GaNFast™* Power ICs

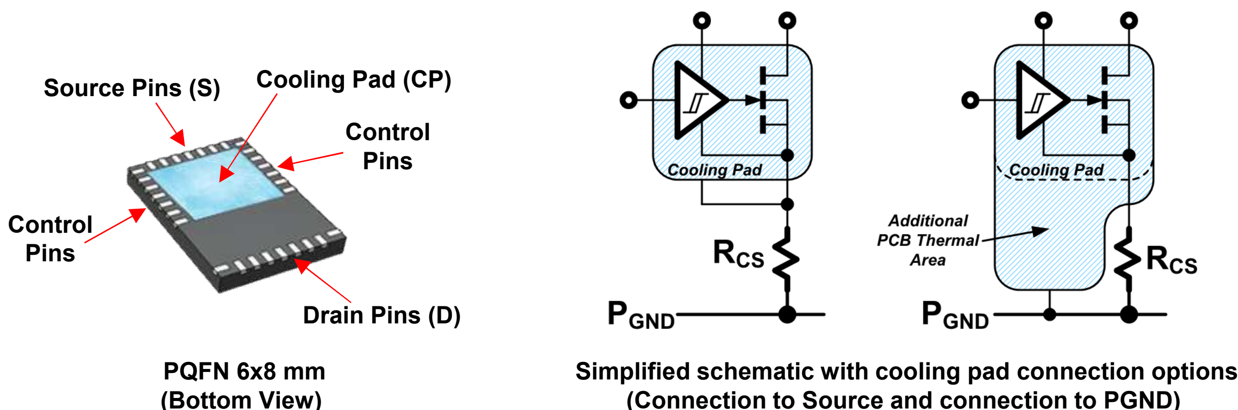
Introduction

The latest family of Navitas *GaNFast™* Power ICs include NV6123/25/27 which are available in a 6x8 mm PQFN package. This thermally enhanced package includes a large cooling pad for a low package thermal resistance and increased thermal performance. This package enables the design of high-density power supplies, especially for fully enclosed chargers and adapters with no air flow. In order to take full advantage of these thermal benefits, the PCB layout, thermal interfacing, and heatsinking, must all be designed properly.

This application note includes PCB layout guidelines and examples to help designers to design for correct thermal management for NV6123/25/27. These guidelines are intended to extract maximum efficiency and power density when using GaN Power ICs.

Overview

The popular NV6113/15/17 5x6 mm GaN ICs have been designed into a variety of high density power supplies. For designs with a more challenging thermal environment, this larger 6x8 mm product enables more efficient heat removal. The IC pinout of the new 6x8 mm PQFN package includes (see Figure 1) Drain pins (D), Source pins (S), control pins, and a large cooling pad (CP). The control pins manage the gate drive supply and on/off control of the GaN power FET, and most of the switching currents of the external power conversion circuit flow from the Drain pins, through the GaN power FET, and to the Source pins. A fraction of the switching current does flow through the silicon substrate of the die and out through CP. Inside the package the IC is mounted directly on the cooling pad. So the heat generated from the power losses of the GaN power FET ***must be*** taken out through the cooling pad (CP), through the solder, and to the PCB. It is helpful to use as much copper as possible to connect to the CP on the layer to which the package is soldered. Thermal vias are then used to transfer the heat to the opposite side of the PCB and/or to inner layers that have large copper planes where it can then be spread and cooled. The cooling pad is connected to the chip substrate, which can float +/-10V relative to the source. For applications where current sensing resistors are used, the cooling pad can be connected (Figure 1) to the Source pin (at the top of the current sensing resistor R_{CS}), or can be connected to PGND to gain additional PCB thermal area for cooling.



PQFN 6x8 mm (Bottom View)

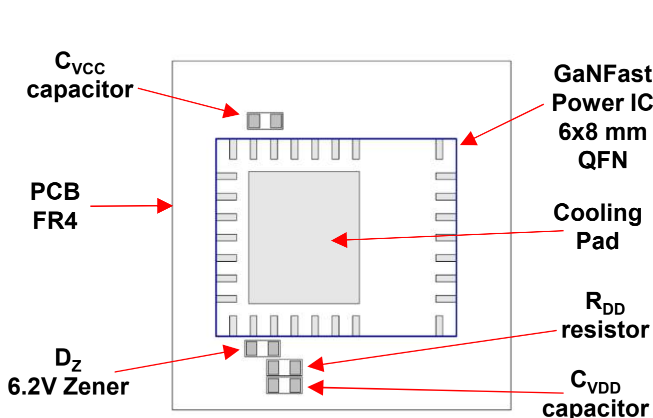
Simplified schematic with cooling pad connection options (Connection to Source and connection to PGND)

Fig 1. 6x8 mm PQFN package and simplified schematic with cooling pad

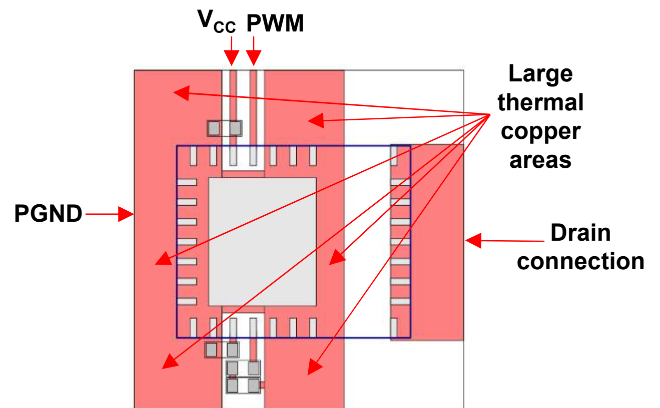
PCB Guidelines (without CS resistor)

When designing the PCB layout for the GaNFast Power ICs, several guidelines must be followed in order to achieve acceptable device temperatures. Thermal vias must be used to conduct the heat from the top layer IC Source landing pad to the bottom layer and large copper areas are used for PCB heatsinking. The following layout steps and instructions illustrate best layout practices for optimal IC thermal performance.

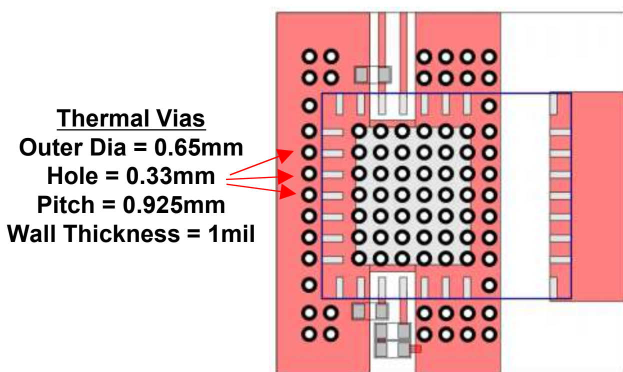
1) Place the GaNFast IC 6x8 mm PQFN footprint on the PCB top layer.
2) Place the additional SMD components required for the control pins on the top layer (C_{VCC}, C_{VDD}, R_{DD}, D_Z). ***Place the SMD components as close as possible to the IC pins!***
3) Route the connections for the SMD components, control pins, Drain pins, Source pins, and cooling pad all on the top layer.
4) Place large copper areas on the top layer at cooling pad and sides.
5) Place thermal vias inside the cooling pad and at sides.
6) Place large copper areas on all other layers (bottom, mid1, mid2, etc.).



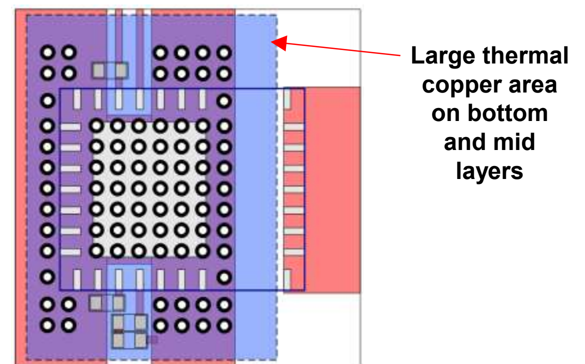
(a) Place GaNFast IC and SMD components on top layer



(b) Route Drain pins, Source pins, CP pad, SMD components, and place large copper areas on top layer



(c) Place thermal vias inside cooling pad and sides



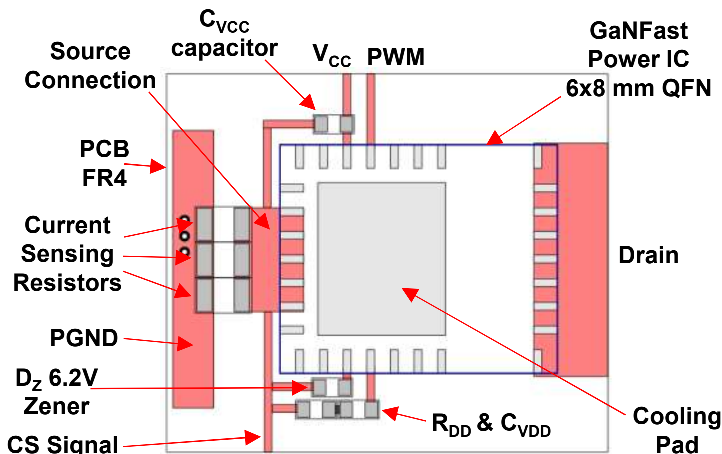
(d) Place large copper areas on bottom and mid layers

Fig 2. GaNFast IC PCB layout steps (without CS resistors)

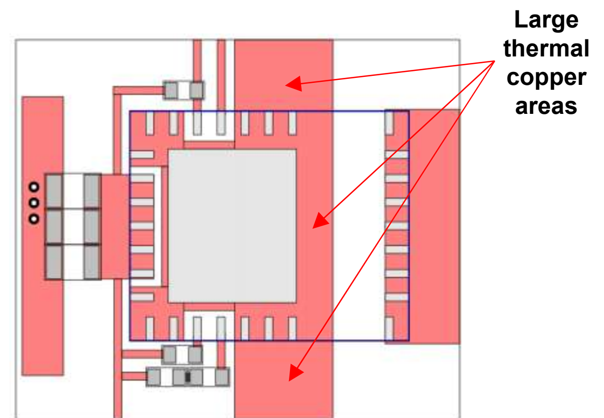
PCB Guidelines (with CS resistor)

When using a current sensing resistor placed in between the source and PGND, the floating cooling pad allows for the PCB copper area to be stretched across the current sensing resistors and connected directly to PGND. When designing a PCB with CS resistors the following steps should be followed:

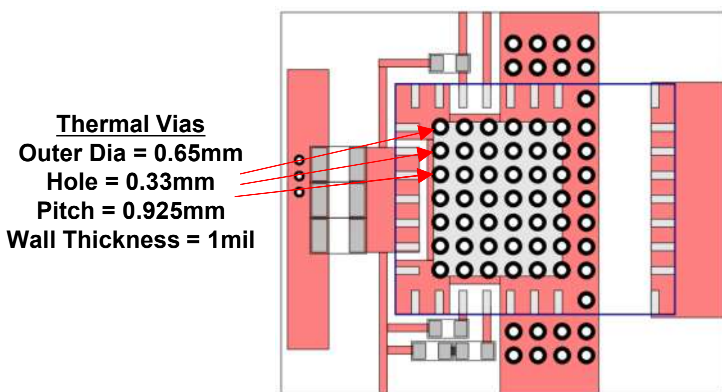
1) Place the GaNFast IC 6x8 mm PQFN footprint on the PCB top layer.
2) Place the additional SMD components required for the control pins on the top layer (CV_{CC}, CV_{DD}, R_{DD}, D_Z). ***Place the SMD components as close as possible to the IC pins!***
3) Route the connections for the SMD components, control pins, and Drain pins, and Source pins all on the top layer.
4) Place large copper areas on the top layer at cooling pad and sides.
5) Place thermal vias inside the cooling pad and at sides.
6) Place large copper areas on all other layers (bottom, mid1, mid2, etc.).
7) Connect cooling pad copper area potential to PGND with vias.



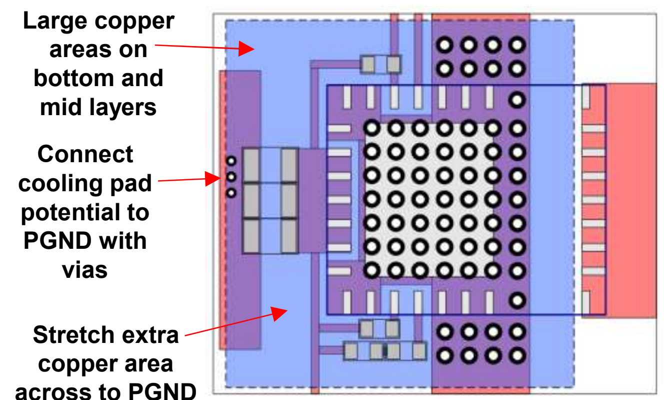
(a) Place and route GaN IC and SMD on top layer



(b) Place large copper area at cooling pad and sides



(c) Place thermal vias inside cooling pad and sides

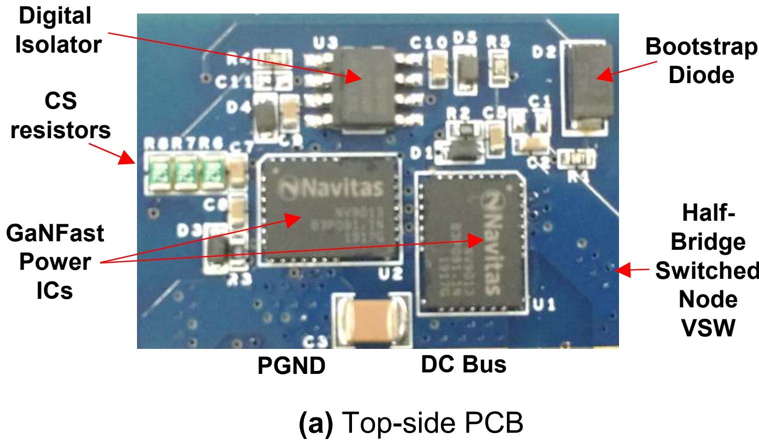


(d) Place large copper areas on bottom and mid layers. Connect cooling pad potential to PGND.

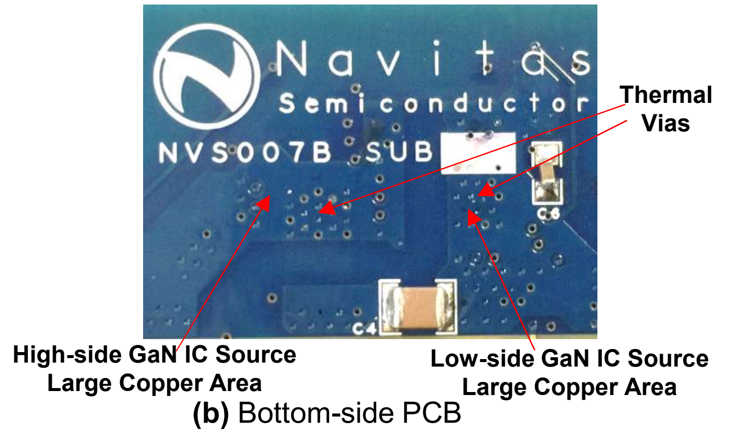
Fig 3. GaNFast IC PCB layout steps (with CS resistors)

PCB Layout Example (Half-Bridge Configuration)

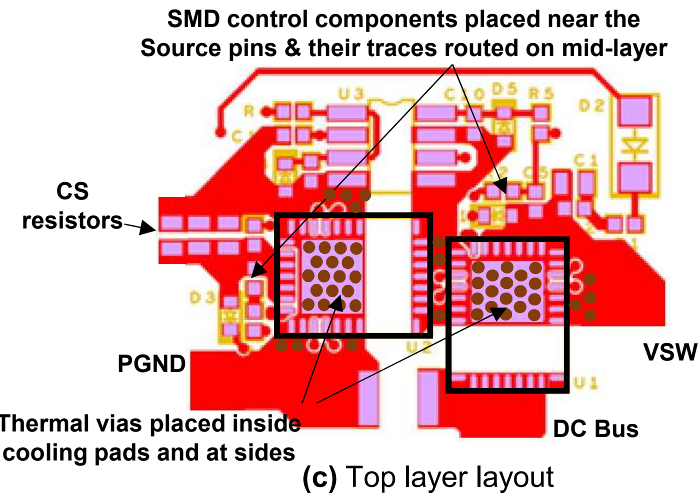
The following example (Figure 4) shows correct layout practices for half-bridge configuration. Almost all components are realized on top layer allowing all other layers to be used for large copper area and thermal vias. If 4-layers are used, then additional copper area can be gained at the sides of the GaNFast ICs by placing the SMD control components near the Source pins and routing to their pins on the mid-layers.



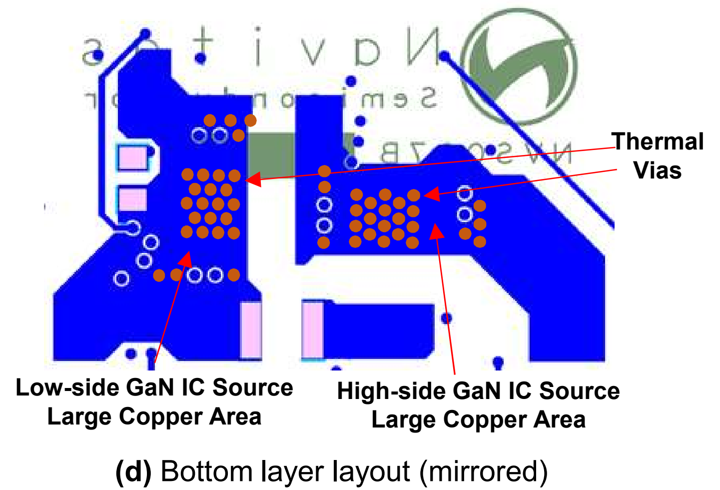
(a) Top-side PCB



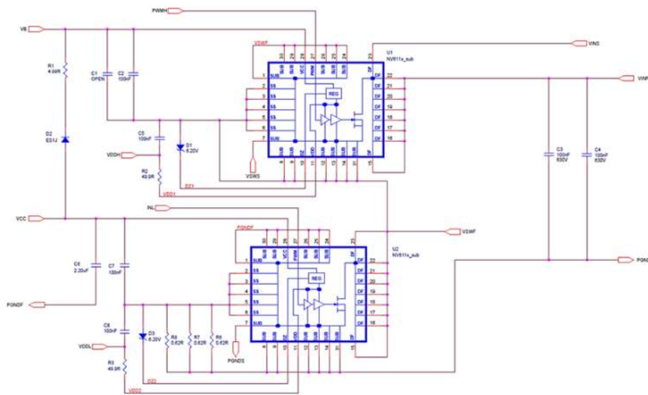
(b) Bottom-side PCB



(c) Top layer layout



(d) Bottom layer layout (mirrored)

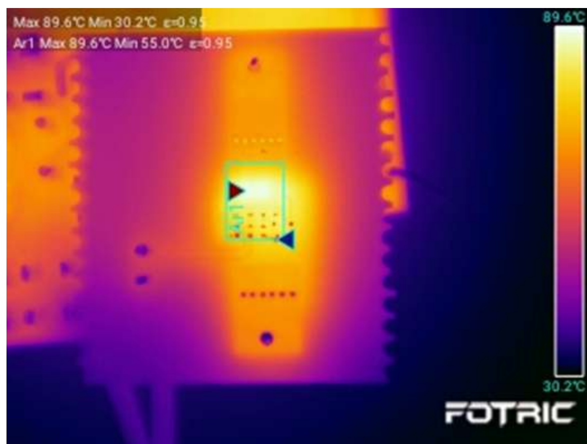


(e) Circuit schematic

Fig 4. PCB and layout for GaN Power ICs in half-bridge configuration.
(a) Top side PCB, (b) Bottom side PCB, (c) Top layout, (d) Bottom/Mid layout, (e) Circuit schematic

NV6125 vs NV6115 Thermal Comparison

The NV6125 (6x8 mm) and NV6115 (5x6 mm) were tested and compared for thermal performance inside a 65W HFQR (High Frequency Quasi-Resonant Flyback) demoboard. Both parts were tested at similar AC input, DC output, and efficiency conditions. PCB layouts were optimized for both ICs by following recommended PCB layout guidelines. The results show at 9.4degC decrease in case temperature for the NV6125 at low-line 90 VAC input and full-load conditions.



a) NV6115 (90 VAC, 100% Load)

a) NV6125 (90 VAC, 100% Load)

Fig 5. NV6125 and NV6115 Thermal Measurements (65 W HFQR, Ta = 25 C)

VAC Input	*NV6115*		*NV6125*		*dT_{CASE} $T_{NV6125} - T_{NV6115}$*
	EFF	*Temp*	*EFF*	*Temp*	
90 VAC	92.9 %	89.6 C	93.0 %	80.2 C	**-9.4 C**

Fig 6. NV6125 vs NV6115 Thermal Comparison (65 W HFQR, Ta = 25 C)

45 W HFQR Planar USB-C PD Charger Example

When placing the power supply PCB board into a housing, additional thermal management is required to properly conduct the heat from the PCB to the case. This is necessary to avoid high component temperatures and reduced efficiency. The following 45 W HFQR (High Frequency Quasi-Resonant Flyback) USB-C PD charger example (Figure 7) uses thermal glue placed on top of the power components, followed by isolation tape and an aluminum sheet for heat spreading. A thermal pad is then used to conduct the heat from aluminum sheet to the plastic case.

Planar daughter card
Output capacitor
USB-C PD output
DC bus capacitors
AC Input

(a) 45 W charger top side PCBA

NV6125
Input Bridge Rectifier
Plastic housing

(b) 45 W charger bottom side PCBA

Thermal Glue

(c) Place local thermal glue over power devices

Aluminum Sheet
Isolation Tape

(d) Add isolation tape (yellow) and aluminum sheet

Thermal Pad

(e) Add thermal pad

GaNFast™

(f) Add AC plug and cover

Fig 7. 45 W USB-C PD charger thermal management steps
(a) Top side PCBA, (b) Bottom side PCBA, (c) Thermal glue, (d) Isolation tape & aluminum sheet, (e) Thermal pad, (f) Plastic housing

Product Selection Guide

The following table (Figure 8) shows Navitas part recommendations (typical only) for different circuit topologies and power levels.

Topology	30W	45W	65W	150W	300W
QR	NV6113	NV6115 or NV6123	NV6125	N/A	N/A
ACF	NV6113(HS) NV6113(LS)	NV6113(HS) NV6115(LS) or NV6252	NV6113(HS) NV6125(LS)	N/A	N/A
PFC (CrCM)	N/A	N/A	N/A	NV6127	2x NV6127
LLC	N/A	N/A	N/A	NV6113(HS) NV6113(LS)	NV6115(HS) NV6115(LS)

Fig 8. Product selection guide for different topologies and power levels

References (www.navitassemi.com)

1) Navitas *GaNFast*™ NV6123, NV6125, NV6127 datasheets, Navitas Semiconductor, 2019
2) Thermal Management of *GaNFast*™ Power ICs, AN010, Navitas Semiconductor, 2019

Additional Information

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