**ADSANTEC**

Ultra High-Speed Mixed Signal ASICs

ASNT1121-KMM
DC-50*Gbps* Broadband Digital 4:1 Multiplexer

- High speed broadband 4:1 Multiplexer (MUX)

- Exhibits low jitter and limited temperature variation over industrial temperature range

- Differential CML I/O data and clock buffers

- Quarter-rate clock output

- Single +3.3*V* or -3.3*V* power supply

- Power consumption: 960m*W*

- Fabricated in SiGe for high performance, yield, and reliability
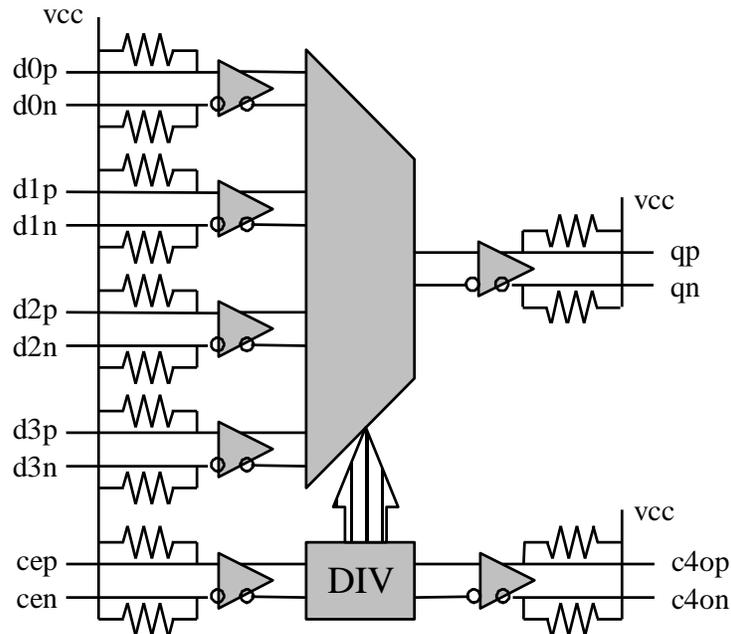
- Custom CQFP 44-pin package
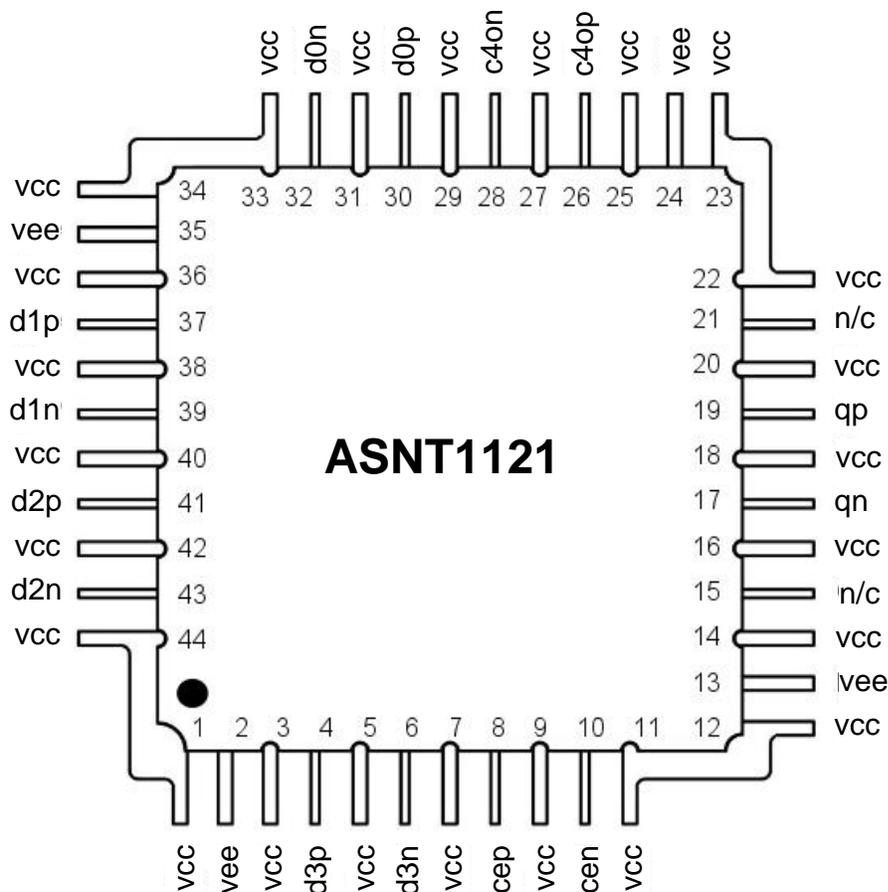
DESCRIPTION

Fig. 1. Functional Block Diagram

The ASNT1121-KMM SiGe IC is a low power and high-speed digital 4-to-1 serializer-multiplexer (MUX) that functions seamlessly over data rates (f_{bit}) ranging from DC to its maximum frequency.

The main function of the part shown in Fig. 1 is to multiplex 4 parallel differential CML data signals d0p/d0n, d1p/d1n, d2p/d2n, d3p/d3n running at a bit rate of $f_{bit}/4$ into a high speed serial bit stream qp/qn running at a bit rate of f_{bit}. Differential or single-ended full-rate clock cep/cen must be provided by an external source for the part to function properly.

The serialized data words qp/qn and the clock divided-by-4 signal c4op/c4on are transmitted through CML output interfaces. The clock and data outputs are phase-matched to each other resulting in a very little relative skew over the operating temperature range of the device.

The part's I/O's support the CML logic interface with on chip $50Ohm$ termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0V = ground and vee = −3.3V), or positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with $50Ohm$ termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.1	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Case Temperature		+100	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
Low-Speed I/Os			
d0p	30	CML	Differential quarter-rate data inputs with internal SE $50Ohm$
d0n	32	input	termination to vcc
d1p	37	CML	Differential quarter-rate data inputs with internal SE $50Ohm$
d1n	39	input	termination to vcc
d2p	41	CML	Differential quarter-rate data inputs with internal SE $50Ohm$
d2n	43	input	termination to vcc
d3p	4	CML	Differential quarter-rate data inputs with internal SE $50Ohm$
d3n	6	input	termination to vcc
c4op	26	CML	Differential quater-rate clock outputs with internal SE $50Ohm$
c4on	28	output	termination to vcc. Require external SE $50Ohm$ termination to vcc
High-Speed I/Os			
cep	8	CML	Differential full-rate clock input signals with internal $50Ohm$
cen	10	input	termination to vcc
qp	19	CML	Differential full-rate data outputs with internal SE $50Ohm$
qn	17	output	termination to vcc. Require external SE $50Ohm$ termination to vcc

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply ($+3.3V$ or 0)	1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vee	Negative power supply ($0V$ or $-3.3V$)	2, 13, 24, 35
n/c	Not connected pins	15, 21

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		290		*mA*	
Power consumption		960		*mW*	
Junction temperature	-40	25	125	*°C*	
LS Input Data (d0p/d0n, d1p/d1n, d2p/d2n, d3p/d3n)					
Data Rate	DC	10	12.5	*Gbps*	
Swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cep/cen)					
Frequency	DC	40	50	*GHz*	
Swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty Cycle	40	50	60	*%*	
HS Output Data (qp/qn)					
Data Rate	DC	40	50	*Gb/s*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.6		*V*	With external 50*Ohm* DC termination
Output Jitter		3		*ps*	Peak-to-peak at 40*Gb/s*
LS Output Clock (c4op/c4on)					
Frequency	DC	10	12.5	*GHz*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.6		*V*	With external 50*Ohm* DC termination
Duty Cycle		50		*%*	
Output Jitter		2		*ps*	Peak-to-peak at 10*GHz*

PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT1121-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.
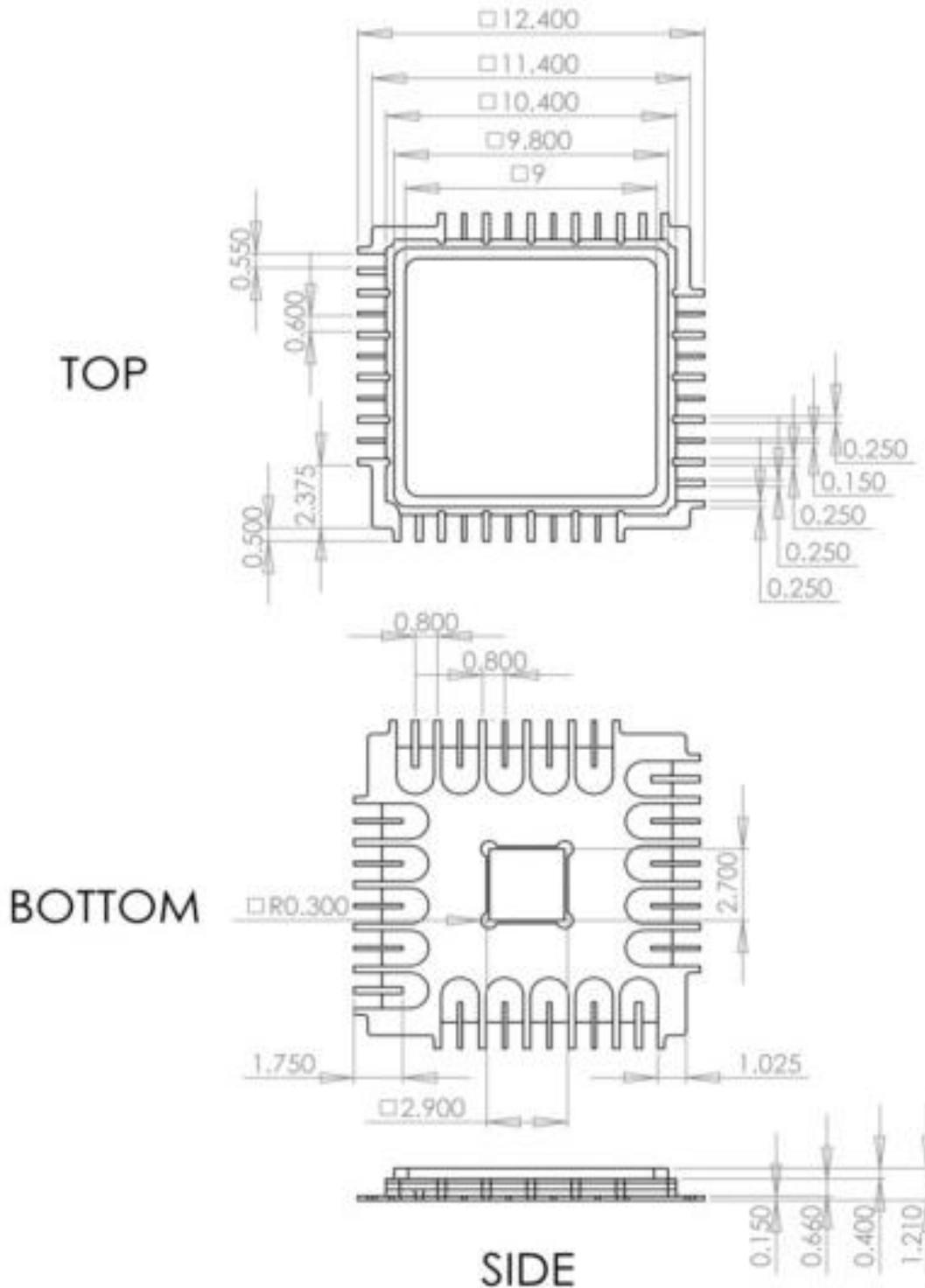

Fig. 2. CQFP 44-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.8.2	01-2020	Updated Package Information
1.7.2	07-2019	Updated Letterhead
1.7.1	05-2019	Corrected cep/cen description in Terminal Function table
1.6.1	05-2015	Updated Package Information section
1.5.1	02-2013	Title correction Corrected description Corrected Terminal Functions table Corrected Electrical Characteristics Updated Package Information
1.4.1	01-2013	Corrected block diagram Updated Package Information Updated Description
1.3.1	12-2011	Format Correction
1.3	11-2011	Corrected Terminal Functions table
1.2	05-2011	Added Absolute Maximums Rating table Added packaging information
1.1	01-2011	Added RoHS compliancy Added revision history table
1.0	12-2010	First release