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Description

The AP3432 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized by peak-current mode architecture with built-in synchronous power MOSFET switchers.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use of small surface mount inductors and capacitors for portable product implementations. Additional features including Soft Start (SS), Under Voltage Lock Out (UVLO), Thermal Shutdown Detection (TSD) and short circuit protection are integrated to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 0.8V to V_{IN} when input voltage range is from 2.7V to 5.5V, and is able to deliver up to 2.5A.

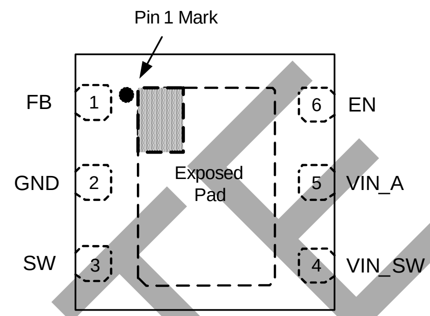
The AP3432 is available in DFN-3×3-6 package.

Features

- High Efficiency Buck Power Converter
- Low $R_{DS(ON)}$ Internal Switches: 100mΩ
- Output Current: 2.5A
- Adjustable Output Voltage from 0.8V to V_{IN}
- Wide Operating Voltage Range: 2.7V to 5.5V
- Built-in Power Switchers for Synchronous Rectification with High Efficiency
- Feedback Voltage Allows Output: 800mV
- 1.5MHz Switching Frequency
- Thermal Shutdown Protection
- Low Drop-out Operation at 100% Duty Cycle
- No Schottky Diode Required
- Input Over Voltage Protection
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Pin Assignments

(Top View)



DFN-3×3-6

Applications

- LCD TV
- Set Top Box
- Post DC-DC Voltage Regulation
- PDA and Notebook Computer

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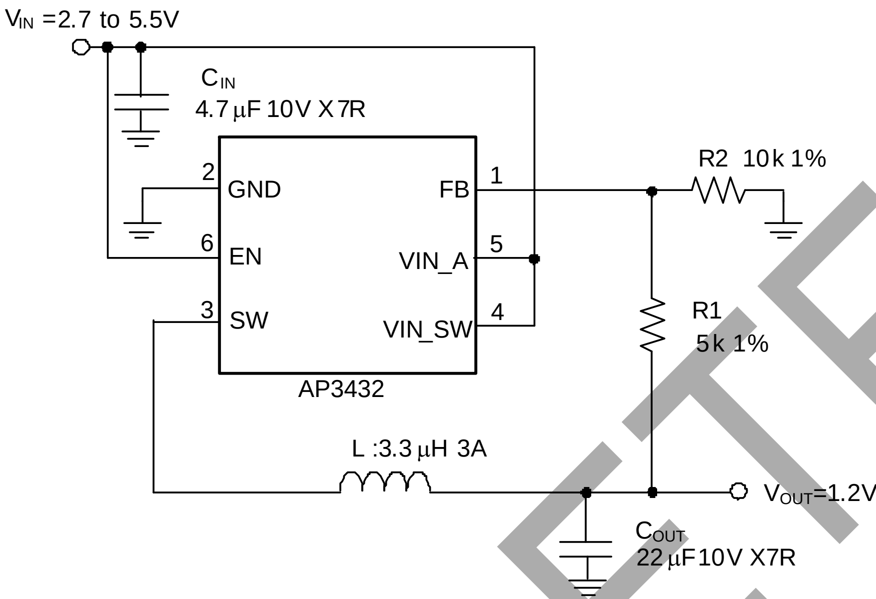
Typical Applications Circuit (Note 1)



Note 1: $$V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2})$$

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)
3.3	31.25	10	3.3
2.5	21.5	10	3.3
1.8	12.5	10	3.3
1.2	5	10	3.3
1.0	3	10	3.3

Table 1. Component Guide

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Pin Descriptions

Pin Number	Pin Name	Function
1	FB	Output voltage feedback pin
2	GND	Ground pin
3	SW	Switch output pin
4	VIN_SW	Power supply input for the MOSFET switch
5	VIN_A	Supply input for the analog circuit
6	EN	Enable pin, active high

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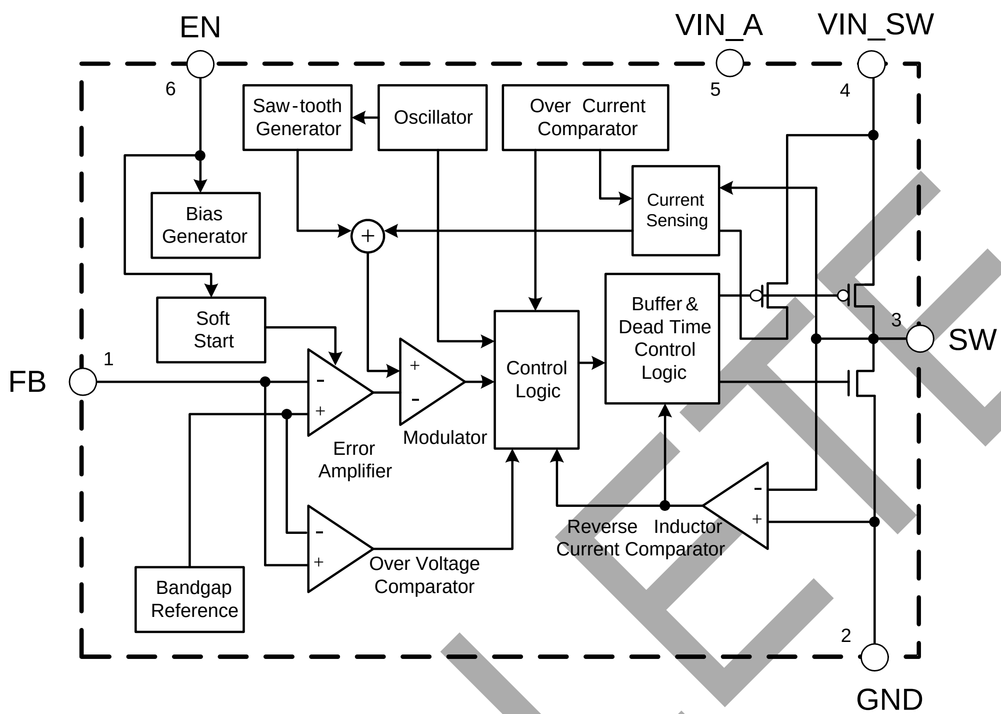
Functional Block Diagram



Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Value	Unit
V_{IN_SW}	Supply Input Voltage (pin VIN_SW)	0 to 6.5	V
V_{IN_A}	Supply Input Voltage (pin VIN_A)	0 to 6.5	V
V_{SW}	SW Pin Switch Voltage	-0.3 to V_{IN_SW}+0.3	V
V_{EN}	Enable Voltage	-0.3 to V_{IN_A}+0.3	V
I_{SW}	SW Pin Switch Current	3.5	A
P_D	Power Dissipation (On PCB, T_A=25°C)	2.49	W
θ_{JA}	Thermal Resistance (Junction to Ambient, Simulation)	40.11	°C/W
T_J	Operating Junction Temperature	+150	°C
T_{OP}	Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
V_{HBM}	ESD (Human Body Model)	2000	V
V_{MM}	ESD (Machine Model)	200	V

Note 2: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

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Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Input Voltage	2.7	5.5	V
T_J	Junction Temperature Range	-40	+125	°C
T_A	Ambient Temperature Range	-40	+80	°C

Electrical Characteristics

($V_{IN\_SW}=V_{IN\_A}=V_{EN}=5V$, $V_{OUT}=1.2V$, $V_{FB}=0.8V$, $L=3.3\mu H$, $C_{IN}=4.7\mu F$, $C_{OUT}=22\mu F$, $T_A=+25°C$, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	—	2.7	—	5.5	V
I_{OFF}	Shutdown Current	$V_{EN}=0V$	—	—	1	μA
I_{ON}	Active Current	$V_{FB}=0.95V$	—	310	—	μA
V_{FB}	Regulated Feedback Voltage	For Adjustable Output Voltage	0.784	0.8	0.816	V
$\Delta V_{OUT}/V_{OUT}$	Regulated Output Voltage Accuracy	$V_{IN}=2.7V$ to 5.5V, $I_{OUT}=10mA$ to 2.5A	-3	—	3	%
I_{PK}	Peak Inductor Current	—	3.0	3.5	—	A
f_{OSC}	Oscillator Frequency	—	1.2	1.5	1.8	MHz
$R_{ON(P)}$	PMOSFET R_{ON}	$I_{SW}=0.75A$	—	100	—	mΩ
$R_{ON(N)}$	NMOSFET R_{ON}	$I_{SW}=0.75A$	—	100	—	mΩ
V_{EN_H}	EN High-level Input Voltage	—	1.5	—	—	V
V_{EN_L}	EN Low-level Input Voltage	—	—	—	0.4	V
I_{EN}	EN Input Current	—	—	—	1	μA
t_{SS}	Soft-start time	—	—	400	—	μS
D_{MAX}	Maximum Duty Cycle	—	100	—	—	%
V_{UVLO}	Under Voltage Lock Out	Rising	—	2.4	—	V
		Falling	—	2.3	—	
—	Hysteresis	Hysteresis	—	0.1	—	V
V_{OVP}	OVP Threshold	—	5.8	5.9	6.0	V
—	Hysteresis on OVP	—	300	400	500	mV
T_{SD}	Thermal Shutdown	Hysteresis=+30°C	—	+150	—	°C

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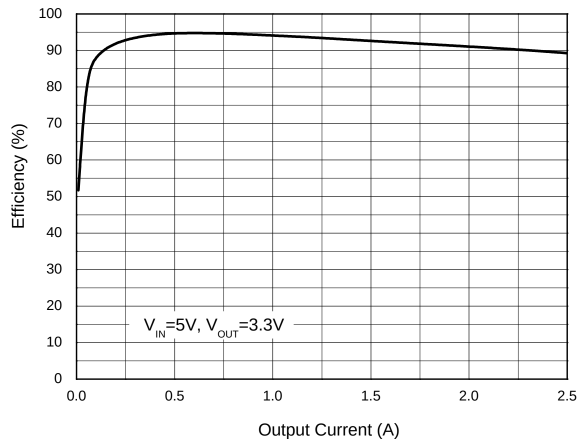
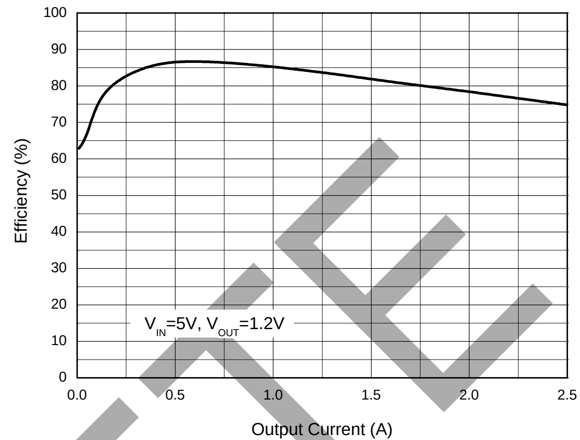
Performance Characteristics

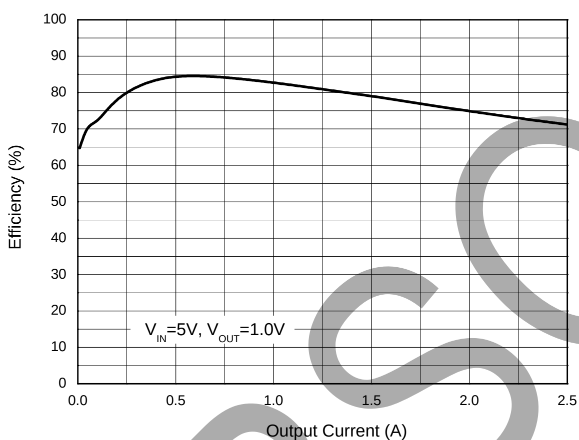
Efficiency vs. Output Current



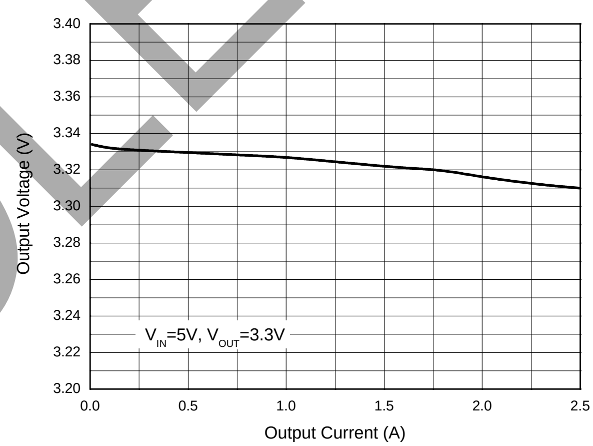
Efficiency vs. Output Current



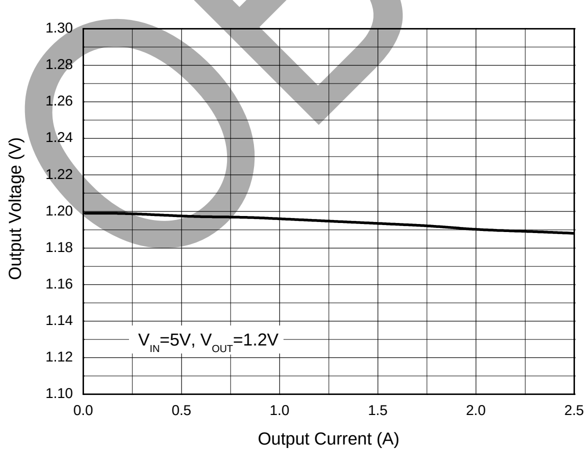
Efficiency vs. Output Current



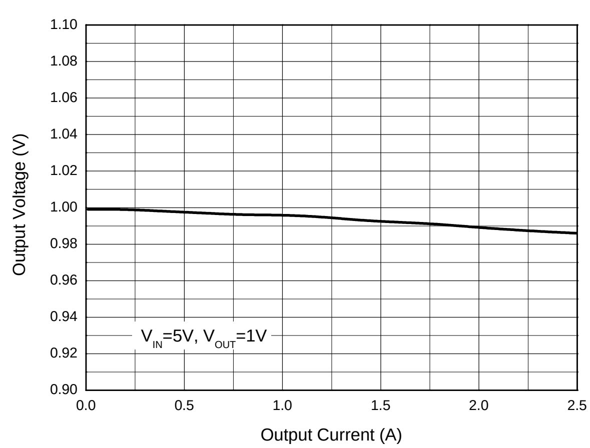
3.3V Load Regulation



1.2V Load Regulation



1.0V Load Regulation



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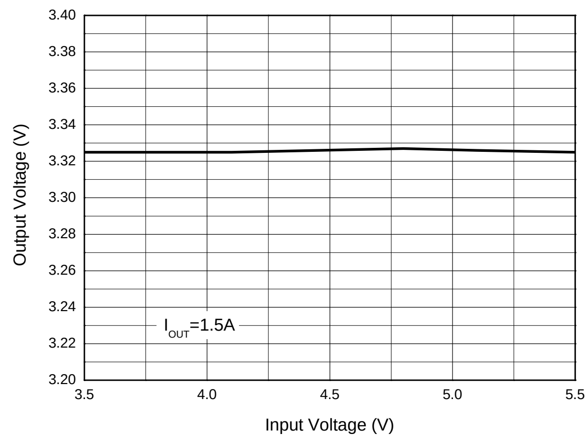
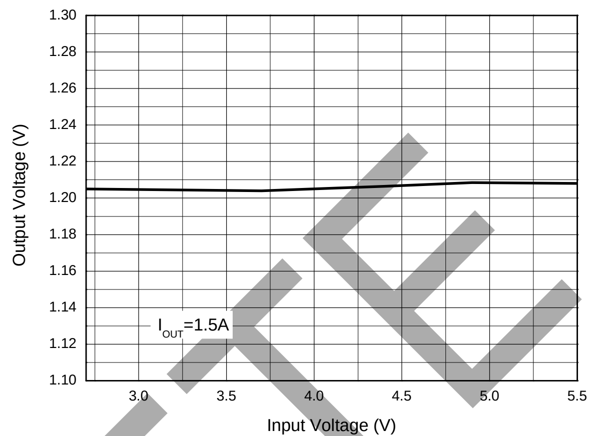
Performance Characteristics (Cont.)

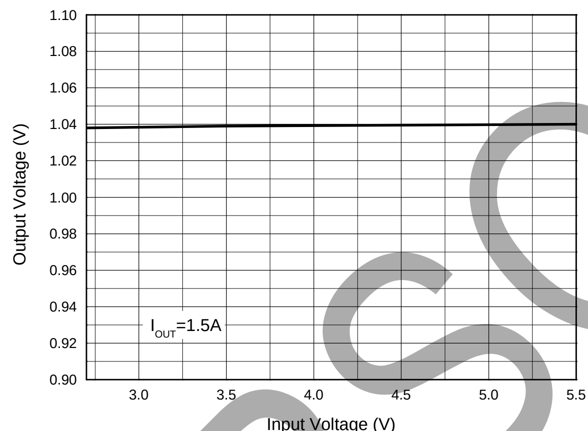
3.3V Line Regulation



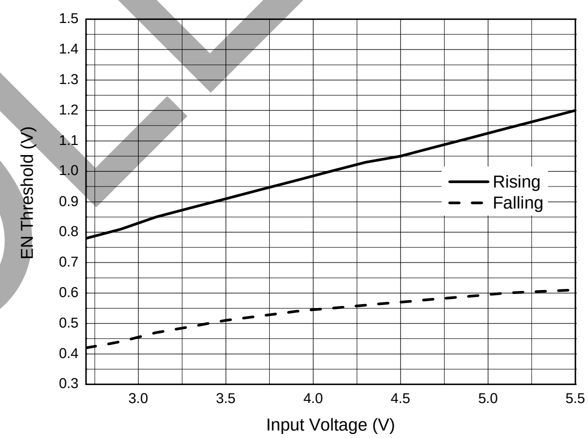
1.2V Line Regulation



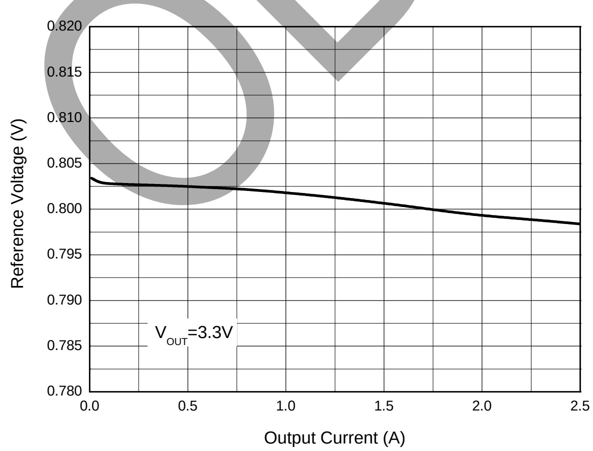
1.0V Line Regulation



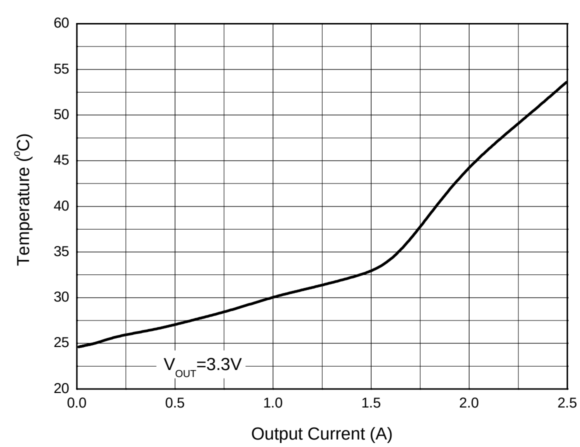
EN Threshold vs. Input Voltage



Reference Voltage vs. Output Current



Temperature vs. Output Current



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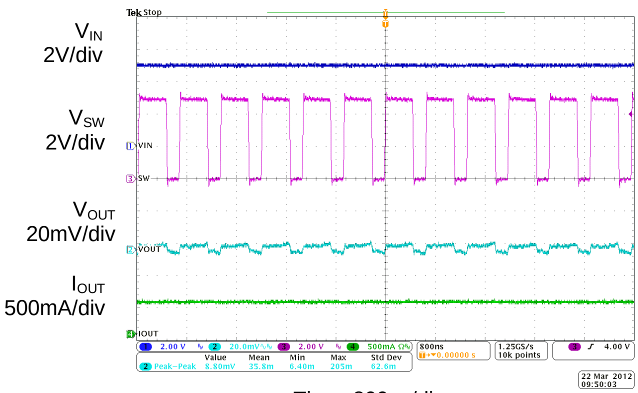
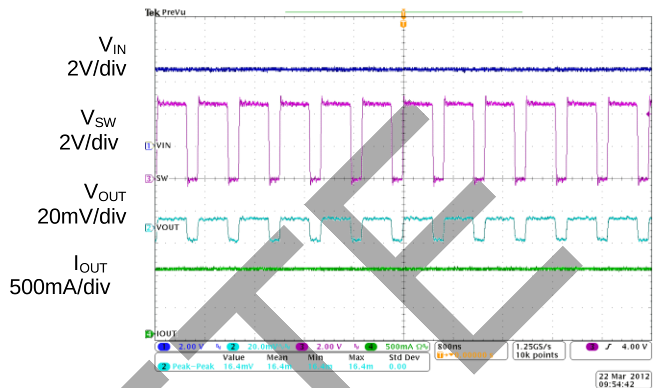
Performance Characteristics (Cont.)

V_{OUT} Ripple
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=500mA)



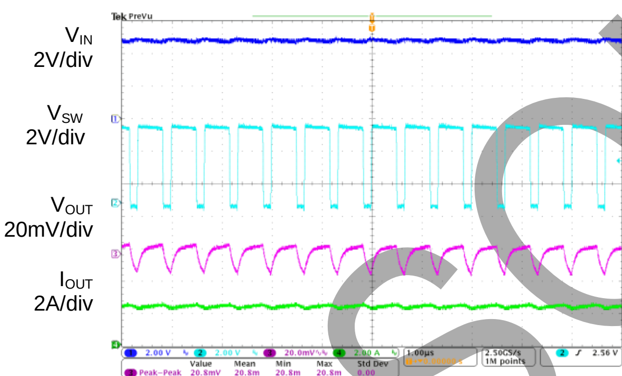
Time 800ns/div

V_{OUT} Ripple
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1000mA)



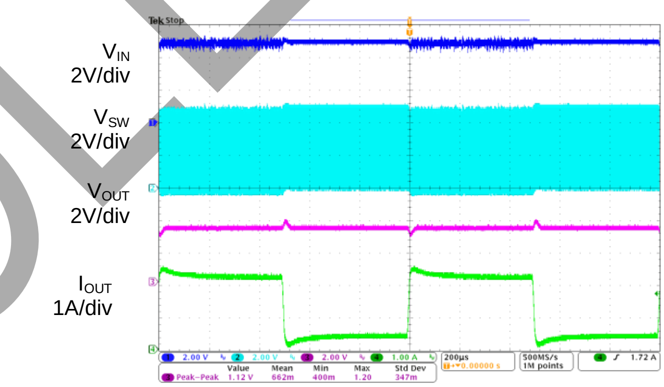
Time 800ns/div

V_{OUT} Ripple
(I_{OUT}=2500mA)



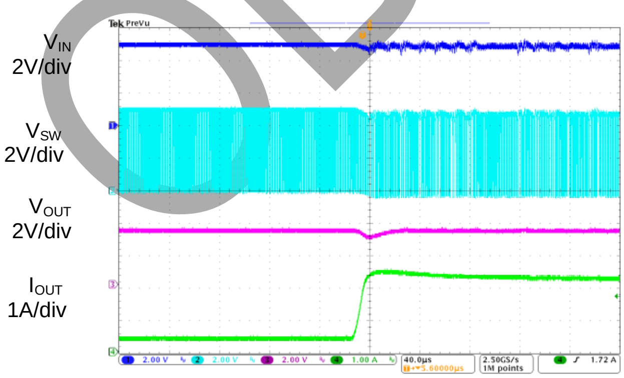
Time 1µs/div

Dynamic Mode
(I_{OUT}=500mA to 2500mA)



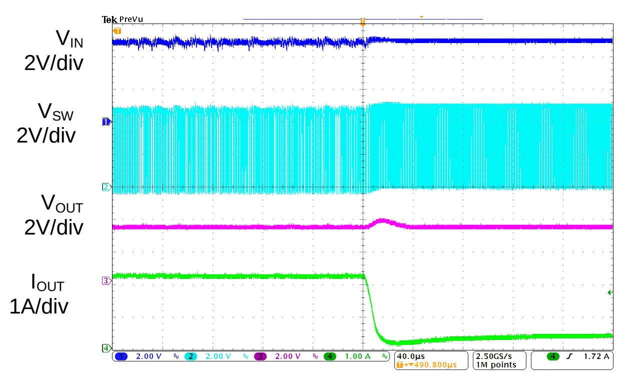
Time 200µs/div

Dynamic Mode (Rising)



Time 40µs/div

Dynamic Mode (Falling)



Time 40µs/div

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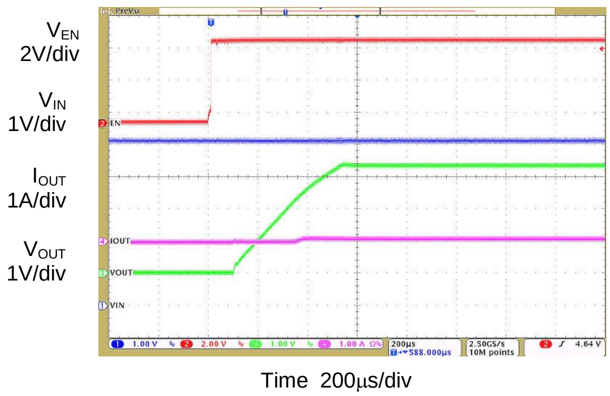
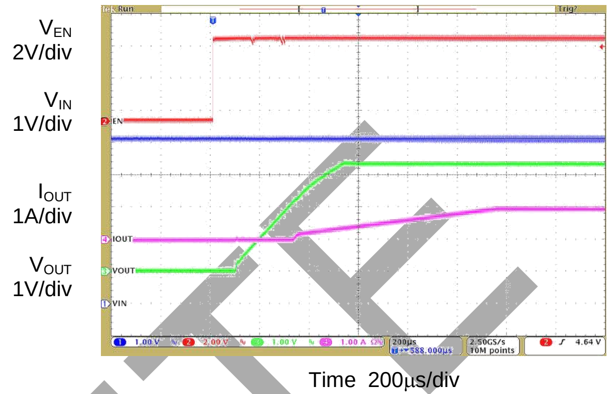
Performance Characteristics (Cont.)

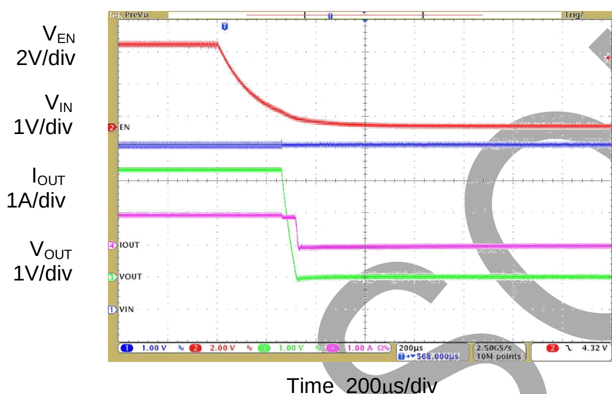
EN Pin L to H
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=100mA)



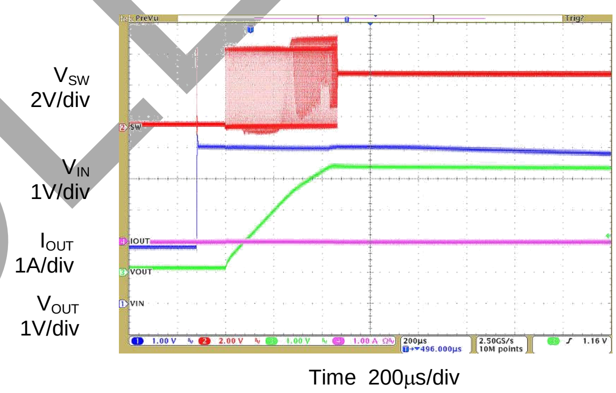
EN Pin L to H
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1000mA)



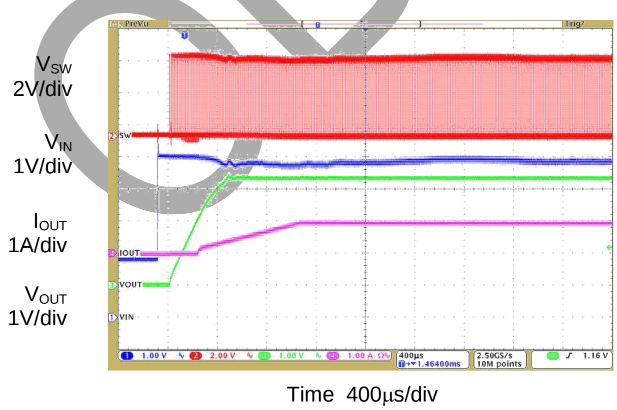
EN Pin H to L
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A)



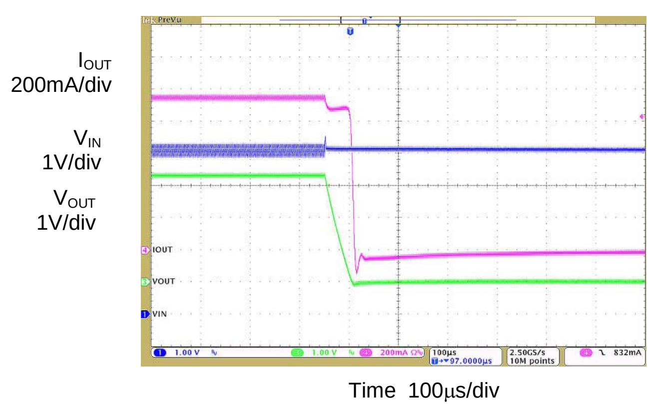
Soft Start Function
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A)



Soft Start Function
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A)



OTP Function



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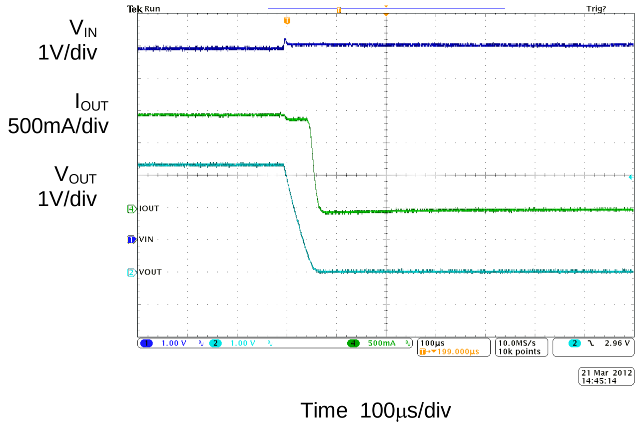
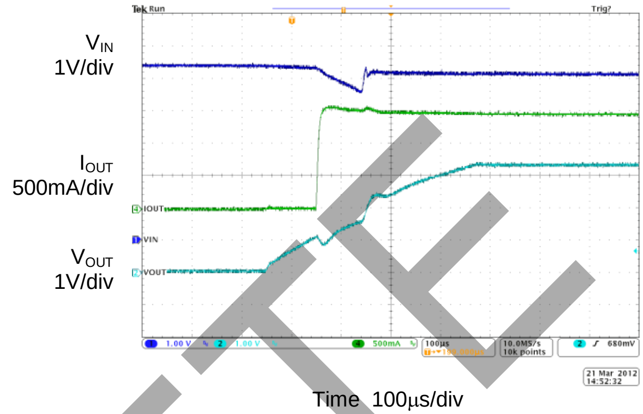
Performance Characteristics (Cont.)

OVP Function
(V_{IN}=5V to 6V)



Leave OVP Function
(V_{IN}=6V to 5V)



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Application Information

5. Short Circuit Protection

When AP3432 output node is shorted to GND, as V_{FB} drops under 0.4V, the chip will enter soft-start to protect itself; when short circuit is removed, and V_{FB} rises over 0.4V, the chip will enter normal operation again. If AP3432 reaches OCP threshold while short circuit, it will enter soft-start cycle and last until the current drops under OCP threshold.

6. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…..

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very light load currents and the I^2R loss dominates the efficiency loss at medium to heavy load currents.

6.1 The V_{IN} quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge, dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the internal DC bias current. In continuous mode,

$$I_{GATE} = f \times (Q_P + Q_N)$$

Where Q_P and Q_N are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the V_{IN} and this effect will be more serious at higher input voltages.

6.2 I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance R_L. In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the SW pin is a function of both PMOSFET $R_{DS(ON)P}$ and NMOSFET $R_{DS(ON)N}$ resistance and the duty cycle (D):

$$R_{SW} = R_{DS(ON)P} \times D + R_{DS(ON)N} \times (1 - D)$$

Therefore, to obtain the I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of total additional loss.

7. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high $R_{DS(ON)}$ resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

8. Input Over Voltage Protection

When the input voltage of AP3432 exceeds V_{OVP}, the IC would enter the mode of Input Over Voltage Protection. It will be shutdown and there will be no output voltage. As the input voltage goes down below 5.5V, the IC would leave input OVP mode and the output voltage will be recovered.

9. PC Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to optimize the

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Application Information (Continued)

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performance of AP3432.

1. The power traces, including the GND trace, the SW trace and the VIN trace should be kept direct, short and wide.

2. Put the input capacitor as close as possible to the VIN_SW, VIN_A and GND pins.

3. The FB pin should be connected directly to the feedback resistor divider.

4. Keep the switching node SW away from the sensitive FB pin and the node should be kept small area.

The following is an example of 2-layer PCB layout as shown in Figure 32 and Figure 33 for reference.

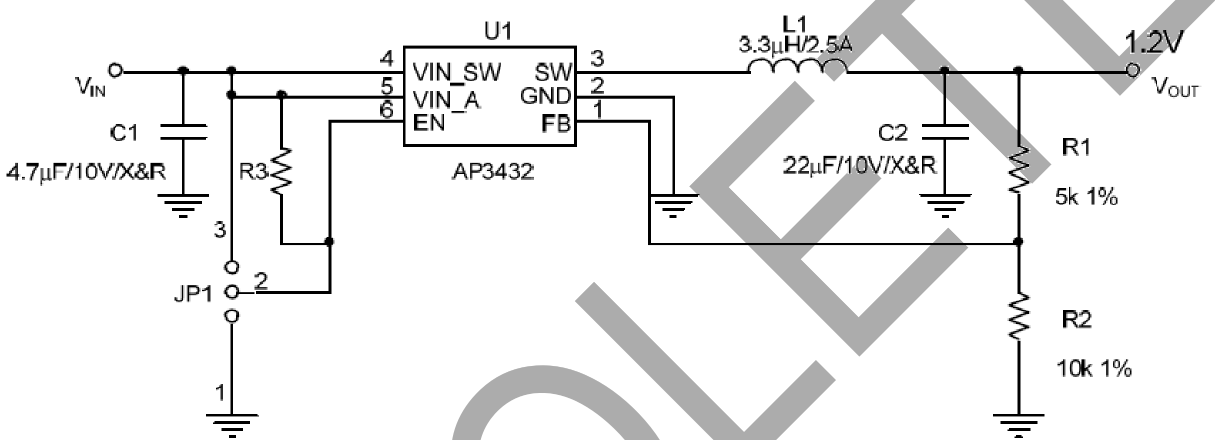

Figure 31. The Evaluation Board Schematic

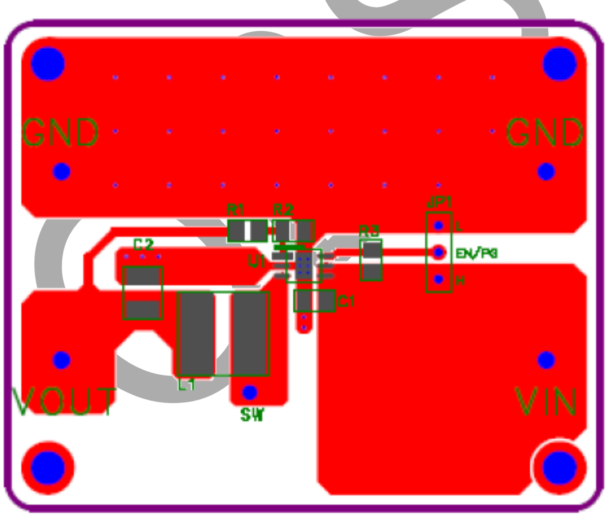

Figure 32. Top Layer for Demo Board

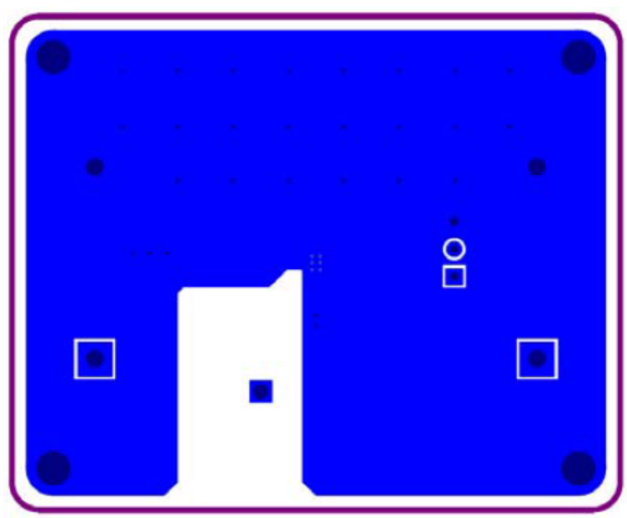

Figure 33. Bottom Layer for Demo Board

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Ordering Information

AP3432 XX XX - XX

Product Name	Package	Packing	RoHS/Green
	DN : DFN-3x3-6	TR : Tape & Reel	G1 : Green

Package	Temperature Range	Part Number	Marking ID	Packing
DFN-3×3-6	-40 to +80°C	AP3432DNTR-G1	BQA	Tape & Reel

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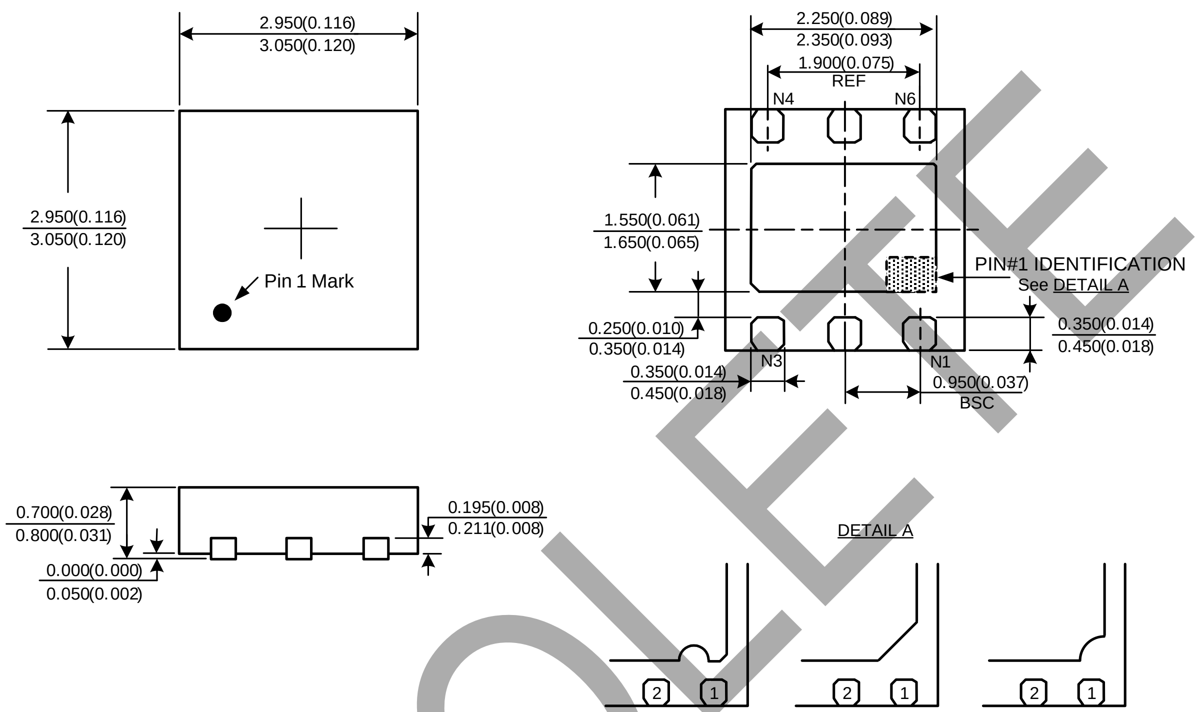
Package Outline Dimensions (All dimensions in mm(inch).)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: DFN-3×3-6



Pin 1 options

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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