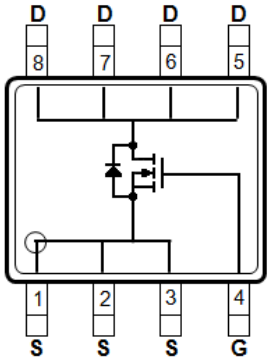
PJL9452A

100V N-Channel Enhancement Mode MOSFET

Voltage	100 V	Current	3.3 A

SOP-8



Features

- $R_{DS(ON)}$, V_{GS}@10V, ID@3.3A<115mΩ
- $R_{DS(ON)}$, V_{GS}@4.5V, ID@1.5A<120mΩ
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOP-8 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Marking: L9452A

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	3.3	A
	T_A=70°C		2.6	
Pulsed Drain Current (Note 1)		I_{DM}	13.2	A
Power Dissipation	T_A=25°C	P_D	2.5	W
	T_A=70°C		1.6	
Single Pulse Avalanche Energy (Note 5)		E_{AS}	3.2	mJ
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient, t≦10s (Note 5)		$R_{\theta JA}$	50	°C/W

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1.0	1.76	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=3.3A	-	92	115	mΩ
		V_{GS}=4.5V,I_D=1.5A	-	95	120	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1.0	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	V_{DS}=50V, I_D=2A, V_{GS}=10V (Note 1,2)	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	3.2	-	
Gate-Drain Charge	Q_{gd}		-	3.6	-	
Input Capacitance	Ciss	V_{DS}=25V, V_{GS}=0V, f=1.0MHZ	-	1413	-	pF
Output Capacitance	Coss		-	60	-	
Reverse Transfer Capacitance	Crss		-	34	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=50V, I_D=1A, V_{GS}=10V, R_G=3.3Ω (Note 1,2)	-	18	-	ns
Turn-On Rise Time	tr		-	4.3	-	
Turn-Off Delay Time	$td_{(off)}$		-	41	-	
Turn-Off Fall Time	tf		-	4.2	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	3.3	A
Diode Forward Voltage	V_{SD}	I_S=1.0A, V_{GS}=0V	-	0.73	1.0	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial TJ=25°C.
4. The maximum current rating is package limited.
5. The test condition is L=0.1mH, I_{AS}=8A, V_{DD}=25V, V_{GS}=10V
6. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
7. Guaranteed by design, not subject to production testing.

PJL9452A

TYPICAL CHARACTERISTIC CURVES

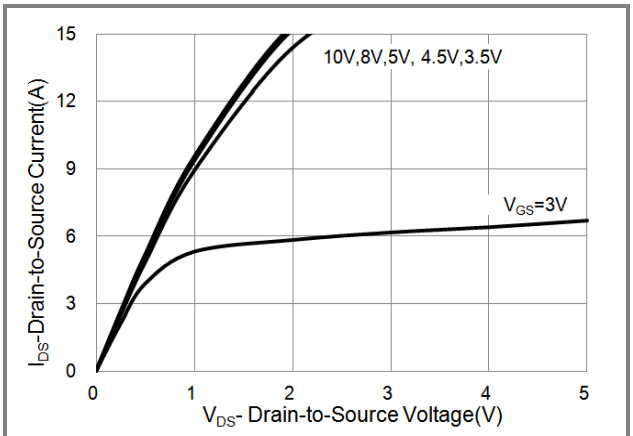

Fig.1 On-Region Characteristics

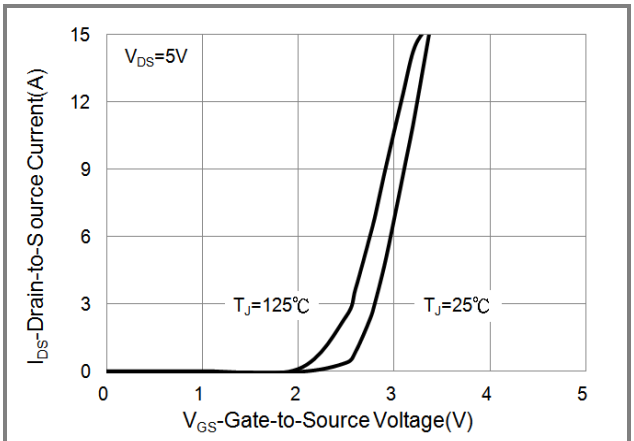

Fig.2 Transfer Characteristics

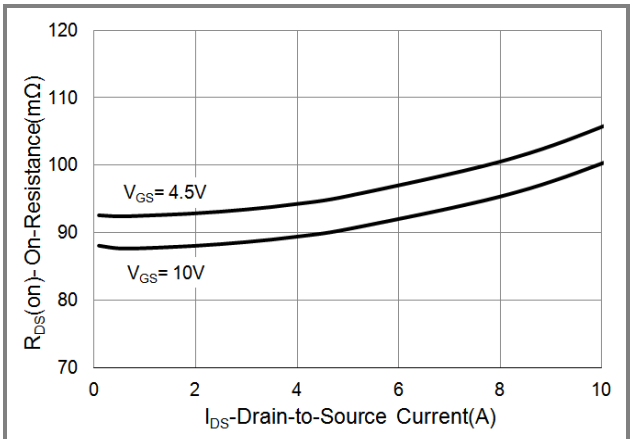

Fig.3 On-Resistance vs. Drain Current

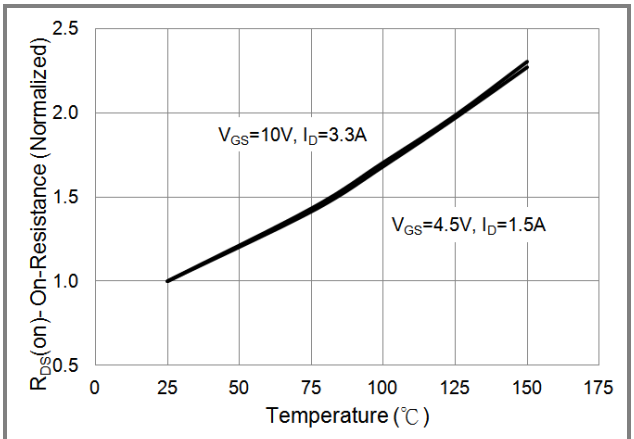

Fig.4 On-Resistance vs. Junction temperature

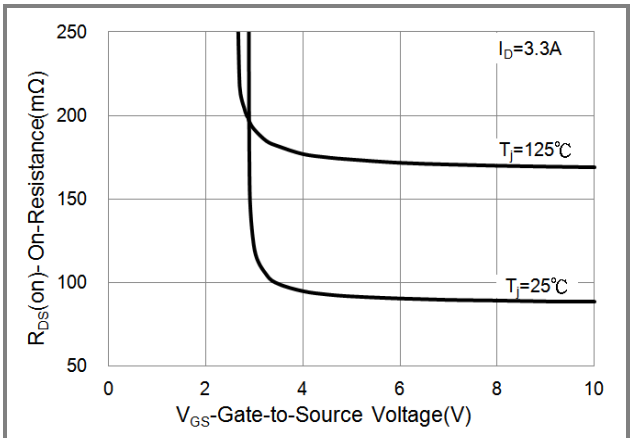

Fig.5 On-Resistance Variation with VGS.

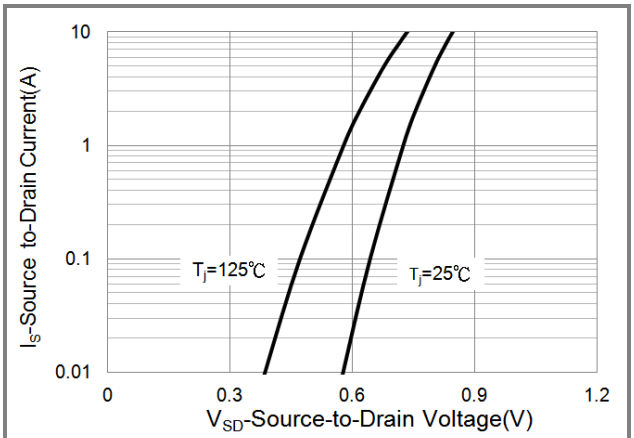

Fig.6 Body Diode Characteristics

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TYPICAL CHARACTERISTIC CURVES

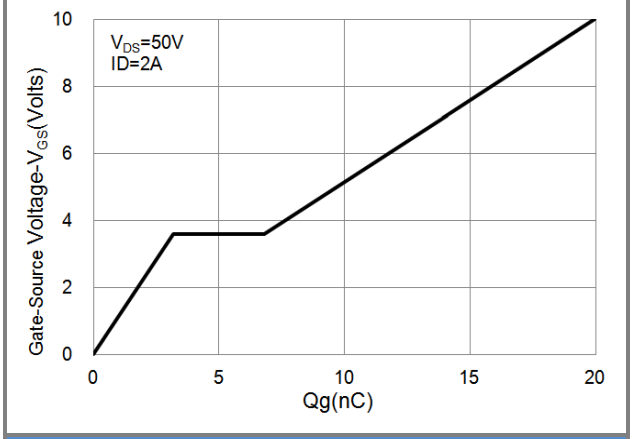

Fig.7 Gate-Charge Characteristics

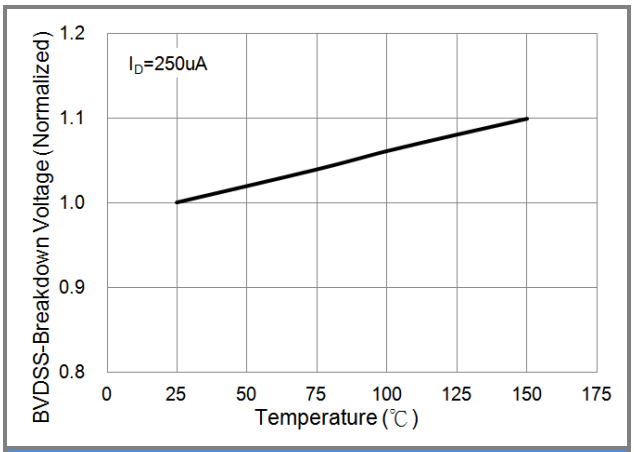

Fig.8 Breakdown Voltage Variation vs. Temperature

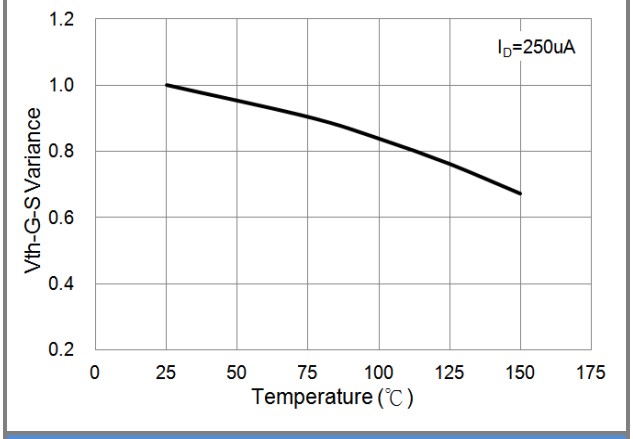

Fig.9 Threshold Voltage Variation with Temperature.

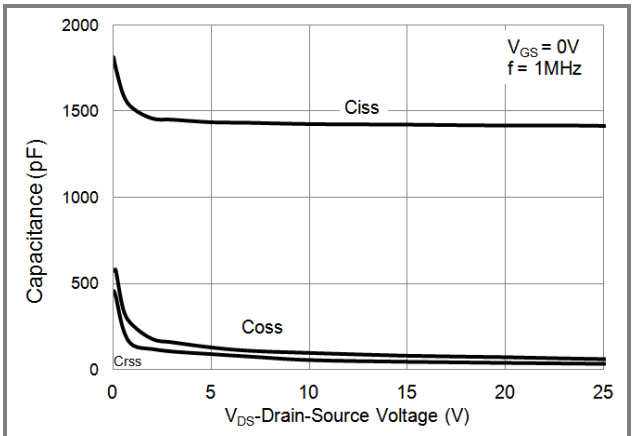

Fig.10 Capacitance vs. Drain-Source Voltage.

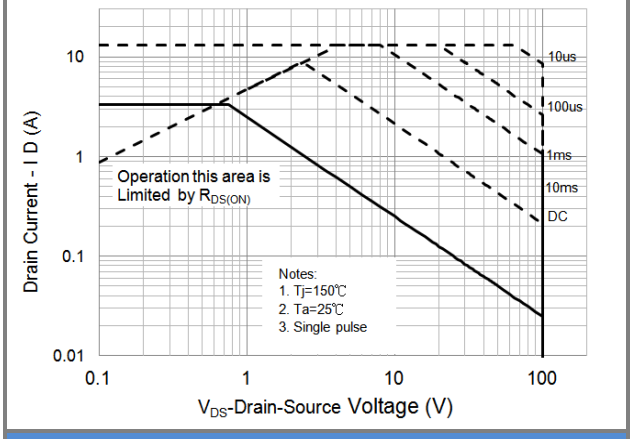

Fig.11 Maximum Safe Operating Area

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TYPICAL CHARACTERISTIC CURVES

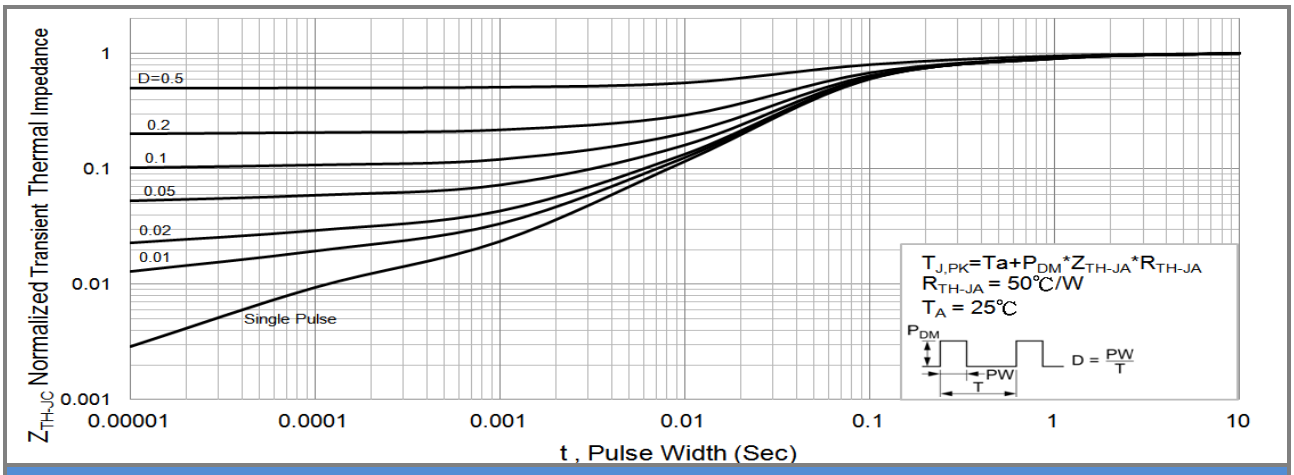


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

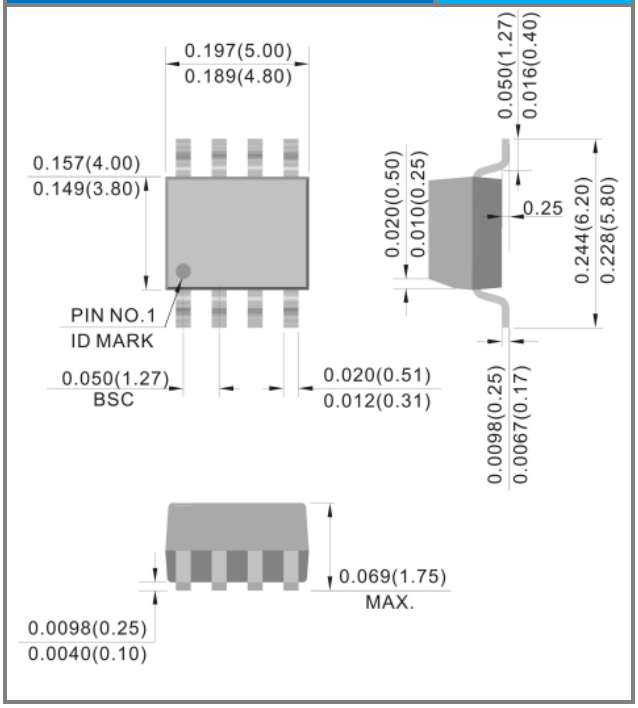
PJL9452A

PART NO PACKING CODE VERSION

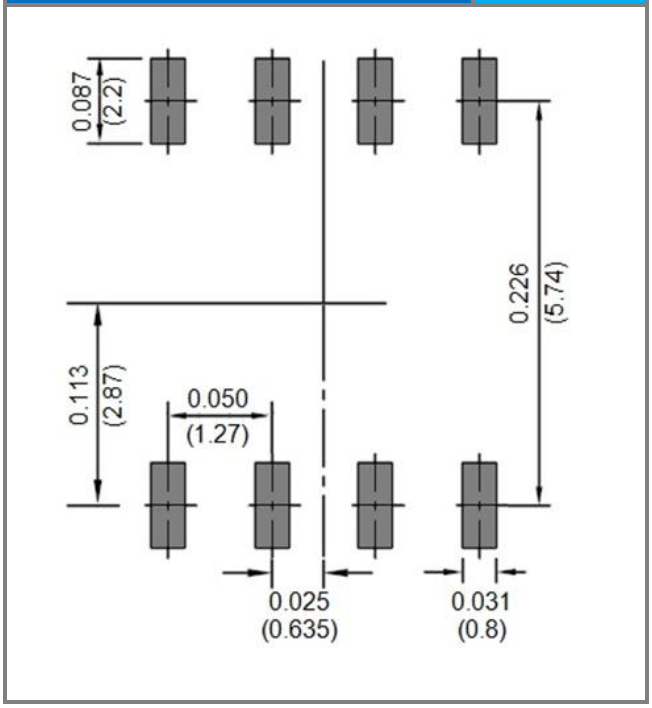
Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9452A_R2_00001	SOP-8	2.5K pcs / 13” reel	L9452A	Halogen free

Packaging Information & Mounting Pad Layout

SOP-8 Dimension — Unit: mm



SOP-8 PAD LAYOUT — Unit: mm



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