Click here to ask an associate for production status of specific part numbers.

0.7% Accuracy, Single Window Voltage Monitor with BIST

MAX16138

General Description

The MAX16138 is a low-voltage, ±0.7% accurate supervisory circuit that monitors a single system supply voltage for undervoltage and overvoltage faults within a factory set threshold window. When the monitored supply voltage drops below the undervoltage threshold or goes above the overvoltage threshold, the reset output asserts low. The reset output deasserts after the reset timeout period when the supply voltage returns within the undervoltage and overvoltage threshold window.

The reset output is active low available in either the push-pull or open-drain options. The MAX16138 offers factory-trimmed nominal input voltage options from 0.51V to 5.01V in approximately 20mV increment. A variety of factory-trimmed undervoltage/overvoltage thresholds from ±2% to ±9% are available to accommodate different supply voltages and tolerances.

The MAX16138 features a unique Built-In-Self-Test (BIST) diagnostic capability that monitors the health of the internal reset circuit during power-up. If the built-in-self-test fails, the MAX16138 asserts BIST low. During normal operation, the MAX16138 performs an on-demand BIST when the CLR/BIST is pulled low for more than 150µs. See the *Built-In Self-Test* section for more details.

The MAX16138 is available in a small, 2mm x 2mm, 8-pin TDFN side-wettable package and operates over the automotive temperature range of -40°C to +125°C.

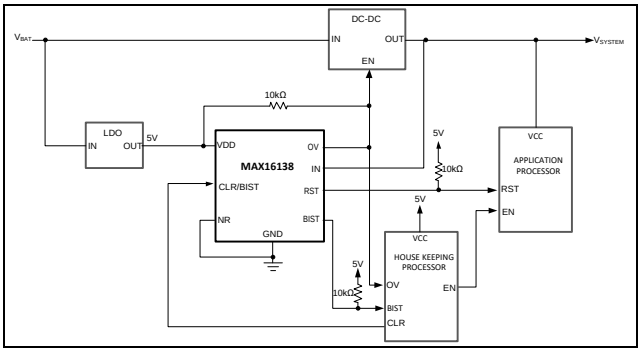
Applications

- Advanced Driver-Assistance Systems (ADAS)
- Multivoltage ASICs
- Servers
- Storage Equipment

Benefits and Features

- ±0.7% Allow Precision Supply Monitoring
- BIST Enhances System Safety
- Enables ASIL Compliance at System Level
- Factory-Set Threshold 0.51V to 5.01V with 20mV Increment
- Factory-Set Input Tolerance ±2% to ±9% UV/OV Threshold Window
- Factory-Set Reset Timeout
- Latched Overvoltage Fault Output
- 5µs Overvoltage Fault Response
- Open-Drain/Push-Pull Reset Output
- 2mm x 2mm TDFN-8 Side-Wettable Package
- -40°C to +125°C Temperature Range
- AEC-Q100 Qualified

Typical Application Circuit



***Ordering Information* appears at end of data sheet.**

19-101422; Rev 0; 4/22

Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to 6V

IN, RST Open-Drain Output, CLR/BISTB, OV, BIST, NR to GND ..... -0.3V to 6V

RST Push-Pull Output to GND .....-0.3V to (V_{DD} +0.3)V

Input/Output Continuous Current, RST, CLR/BISTB, OV, BIST, NR..... 20mA

Continuous Power Dissipation (T_A = +70°C, TDFN-8, derate 6.2mW/°C above +70°C) 496mW

Operating Temperature Range.....-40°C to +125°C

Junction Temperature..... +150°C

Soldering Temperature (Reflow) .....+26C°C

Storage Temperature Range .....-65°C to +150°C

Lead Temperature (Soldering, 10s) ..... 300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	T822CY+2C
Outline Number	*21-100341*
Land Pattern Number	*90-100117*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	162(°C/W)
Junction-to-Case Thermal Resistance (θ_{JC})	20(°C/W)

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages.* Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial.*

Electrical Characteristics

((V_{DD} = 1.71V to 5.50V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) TYP is at 3.3V. 10kΩ pullup resistor for all the open drain outputs.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{DD}	Comparators Functional	1.71		5.5	V
Minimum Supply Voltage		RST is guaranteed to be at a known logic	1.1			V
Supply Current	I_{DD}	RST, OV, BIST not asserted		12	25.5	µA
Undervoltage Lockout Threshold	V_{UVLO}	V_{DD} Rising	1.3	1.5	1.68	V
Undervoltage Lockout Threshold Hysteresis		V_{DD} falling		47		mV
Input Threshold Voltage Programming Range	V_{IN_TH}		0.51		5.01	V
Input Voltage Programming Step				20		mV
Undervoltage/ Overvoltage Window Threshold Programming Range	TOL	Reset occurs when V_{IN} falls outside of V_{IN_TH} (1 ±TOL)	±2		±9	%
Window Threshold Programming Resolution	TOL_{RES}			1		%
INPUT THRESHOLD ACCURACY						
Undervoltage Threshold Accuracy	V_{UVTH_A}	All V_{IN_TH} setting, V_{IN} falling, V_{UVTH} = V_{IN_TH}(1 - TOL%)	-0.7		+0.7	%
Overvoltage Threshold Accuracy	V_{OVTH_A}	All V_{IN_TH} settling, V_{IN} rising, V_{OVTH}=V_{IN_TH}(1 + TOL%)	-0.7		+0.7	%
Undervoltage/Overvoltage Hysteresis	V_{HYS}	Option A		0.25		%VT
		Option B		0.50		
Input Current	I_{IN}			1.3	5	µA
Overvoltage Fault-to-OV Assert Delay	$t_{OV\ DLY}$	(V_{OVTH} - 1%) to (V_{OVTH} + 1%)		5		µs
OV Fault Glitch Immunity	V_{OVTH} + 5%			0.2		µs
CLEAR/BUILT-IN SELF-TEST INPUT (CLRB/BIST**)**						
CLRB/BIST Input Glitch Immunity			50			ns
CLRB/BIST Input Pulse Width to Clear OV Latch	t_{CLR}	From falling edge of CLRB/BIST to OV rising edge	0.4			µs
CLRB/BIST Pulse Width to Initiate BIST	t_{BIST}	From falling edge of CLRB/BIST to start of BIST (*Note 2*)	150			µs
CLRB/BIST Internal Pull Up Resistance				50		kΩ
On-Demand CLRB/BIST to BIST Assert Delay		From the falling edge of CLRB/BIST to BIST asserting			380	µs
RESET OUTPUT(RST**)**						
Reset Timeout Period Accuracy	t_{RP}	From the time when V_{IN} enters overvoltage/undervoltage threshold-window to the time RST goes high, V_{DD} = 3.3V	-20		+20	%

((V_{DD} = 1.71V to 5.50V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) TYP is at 3.3V. 10kΩ pullup resistor for all the open drain outputs.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN-to-RST Propagation Delay	t_{DOV}	(V_{OVTH} - 1%) to (V_{OVTH} + 1%)		5		µs
	t_{DUV}	(V_{UVTH} + 1%) to (V_{UVTH} - 1%)		12		
RST Leakage Current		V_{RST} = V_{OV} = 5.5V		0.01	1	µA
INPUT VOLTAGE (CLR/BIST**, NR)**						
Input Voltage Low	V_{IL}				0.3 x VDD	V
Input Voltage High	V_{IH}		0.7 x VDD			V
Leakage Current		$V_{CLRB/BIST}$ = V_{NR} = V_{DD},	-0.1		+0.1	µA
OUTPUT VOLTAGE (RST**,** OV**,** BIST**)**						
Output Voltage Low	V_{OL}	RST, OV, BIST, V_{DD} = 5V, I_{SINK} = 3mA		0.1	0.3	V
		RST, OV, BIST, V_{DD} = 1.71V, I_{SINK} = 3mA		0.1	0.3	
		RST, V_{DD} = 1.71V, I_{SINK} = 8µA		0.1	0.3	
Reset Output Voltage High (Push-Pull Option)	V_{OH}	V_{DD} = 1.71V, I_{SOURCE} = 200µA	0.8 x V_{DD}			V
Reset Output Voltage High (Push-Pull Option	V_{OH}	V_{DD} = 4.5V, I_{SOURCE} = 800µA	0.8 x V_{DD}			V

Note 1: Outputs are guaranteed to be in correct state down to V_{DD} = 1.1V.

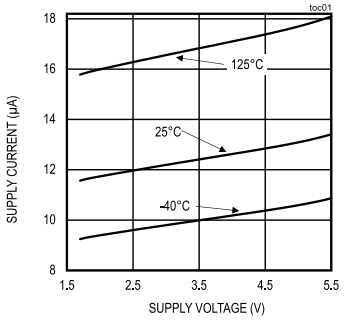
Note 2: Minimum pulse required to clear OV latch state. No overvoltage fault present and RST = high.

Note 3: Use <100kΩ pullup resistor for RST pin, otherwise BIST error is reported.

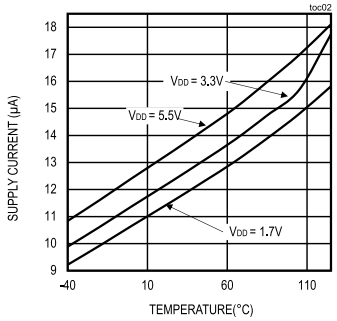
Typical Operating Characteristics

(V_{DD} = 1.71V to 5.50V, T_A = -40°C to 125°C. Typical values are at V_{DD} = 3.3V, unless otherwise specified.)

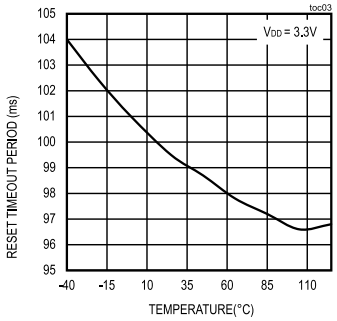
SUPPLY CURRENT vs. SUPPLY VOLTAGE



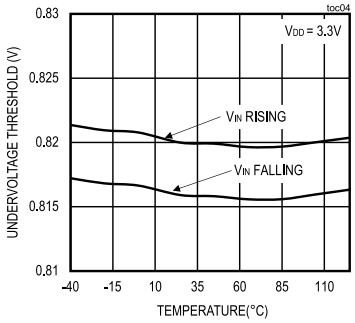
SUPPLY CURRENT vs. TEMPERATURE



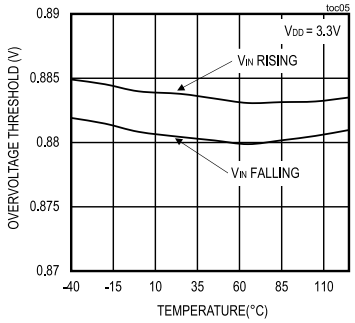
RESET TIMEOUT PERIOD vs. TEMPERATURE



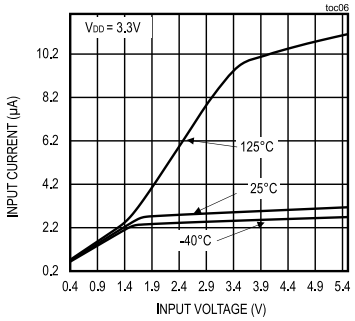
UNDERVOLTAGE THRESHOLD vs. TEMPERATURE



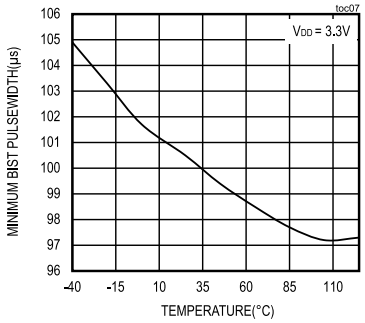
OVERVOLTAGE THRESHOLD vs. TEMPERATURE



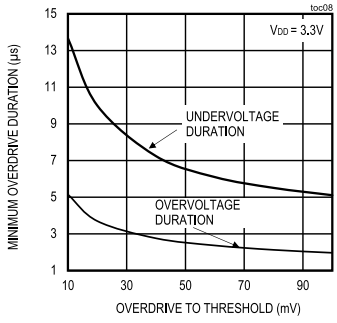
INPUT CURRENT vs. INPUT VOLTAGE



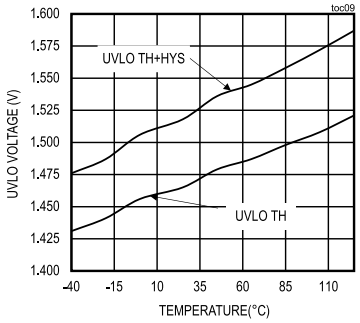
MINIMUM BIST PULSEWIDTH vs. TEMPERATURE



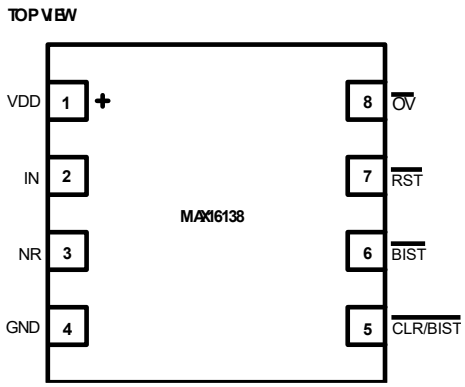
MINIMUM OVERDRIVE DURATION vs. OVERDRIVE TO THRESHOLD



UVLO VOLTAGE vs. TEMPERATURE



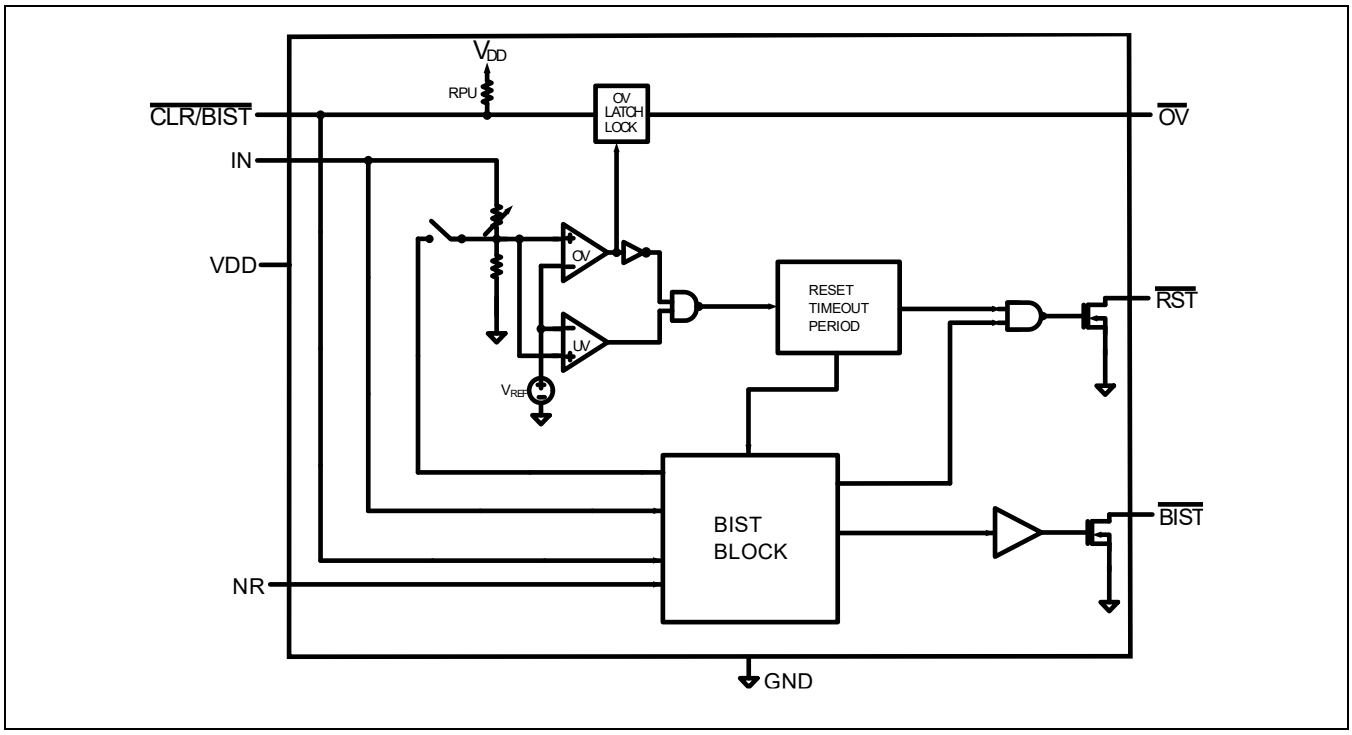
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	VDD	Supply Input. Bypass V_{DD} to ground with a 0.1µF capacitor.
2	IN	Monitoring Input IN (Factory-Set Threshold Monitoring Input). When V_{IN} falls outside the factory selected undervoltage/overvoltage threshold window, RST asserts and stays asserted for a selected reset timeout period after V_{IN} falls within the undervoltage/overvoltage threshold window. When V_{IN} exceeds the overvoltage threshold, OV asserts and indicates an overvoltage fault.
3	NR	No Reset BIST Logic Input. Setting NR to a logic low and driving CLRB/BIST low for more than 150µs initiates BIST and asserts the reset output and BIST if BIST fails. Setting NR to a logic high and driving CLRB/BIST low for more than 150µs initiates BIST and asserts BIST only if BIST fails.
4	GND	Ground
5	CLR/BIST	Overvoltage Clear/Built-In-Self-Test Input. CLRB/BIST is a multiplexed function input. A falling edge on CLRB/BIST clears OV latch. Drving CLRB/BIST for more than 150µs initiates BIST.
6	BIST	Active-Low, Open-Drain Output. BIST asserts low if BIST fails. Pull BIST to V_{DD} with a pullup resistor.
7	RST	Open-Drain Reset Output. RST asserts low when V_{IN} falls outside of the undervoltage/overvoltage threshold window. The reset output deasserts after the reset timeout period when V_{IN} enters the undervoltage/overvoltage threshold window
8	OV	Open-Drain, Active-Low Overvoltage Latched Fault Output. OV latches low when the voltage at IN exceeds the overvoltage threshold setting. OV latch is cleared on the falling edge of CLRB/BIST.

Functional Diagram



Detailed Description

The MAX16138 is a high-accuracy single-channel supervisory reset circuit that monitors the system supply for undervoltage and overvoltage faults within factory-programmable window thresholds. The MAX16138's Built-In Self-Test (BIST) diagnostic capability and overvoltage fault output optimizes system safety in ADAS applications. A reset output (RST) asserts when the input voltage falls outside of the threshold window. The reset output deasserts after the reset timeout period when the supply voltage returns to its nominal voltage level.

Input Voltage Threshold

The MAX16138 offers a wide range of nominal input voltages from 0.51V to 5.01V, in approximately 20mV increments. Each selected nominal input voltage is factory-trimmed halfway between the undervoltage and overvoltage threshold window. See the *Undervoltage/Overvoltage Thresholds* section for more details. Contact Analog Devices for options not listed in the *Ordering Information* table.

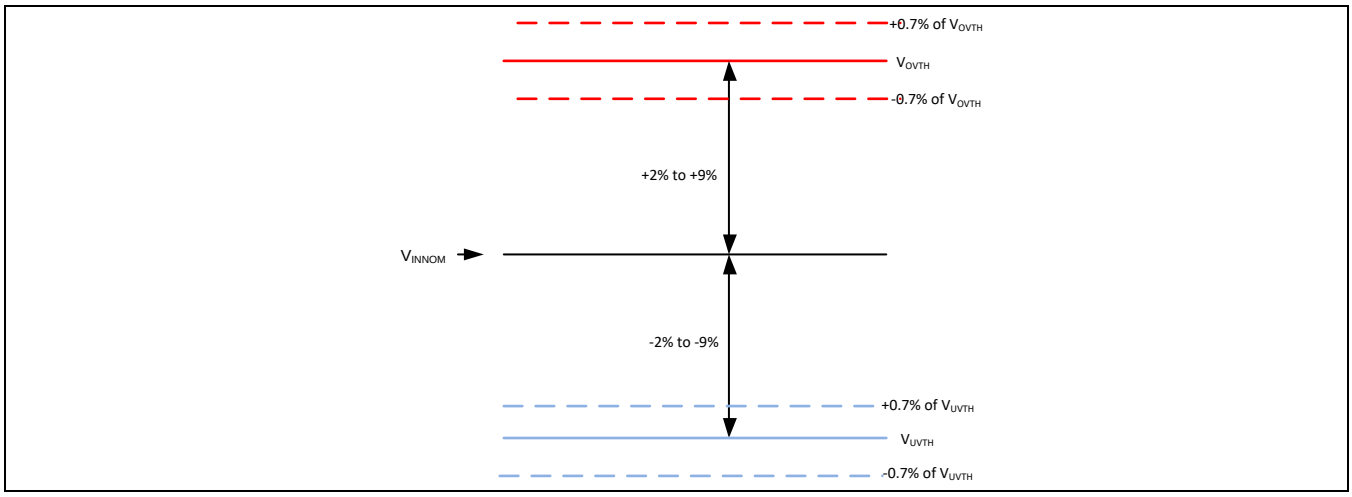


Figure 1. Undervoltage/Overvoltage Threshold Tolerance and Accuracy

Undervoltage/Overvoltage Threshold

The MAX16138 monitors supply voltage for undervoltage/overvoltage faults with respect to the nominal input voltage within ±0.7% accuracy over the operating temperature and supply ranges. The undervoltage and overvoltage thresholds are factory-trimmed from ±2% to ±9%, in ±1% increments. Contact Analog Devices for a threshold not listed in the *Ordering Information* table.

Undervoltage/Overvoltage Threshold Hysteresis

The monitoring input (IN) features undervoltage/overvoltage threshold hysteresis that provides immunity to short input transients. The input hysteresis is factory-set to either 0.25% or 0.5% and is applicable to both the undervoltage and overvoltage thresholds. Contact Analog Devices for a hysteresis option not listed in the *Ordering Information* table.

Overvoltage Fault Output

OV is an open-drain, active-low latched output that latches low 5µs after V_{IN} exceeds the overvoltage threshold level. OV latch is cleared on the falling edge of CLR/BIST after the overvoltage fault is removed. See the *Electrical Characteristics* table and *Figure 2* for more details.

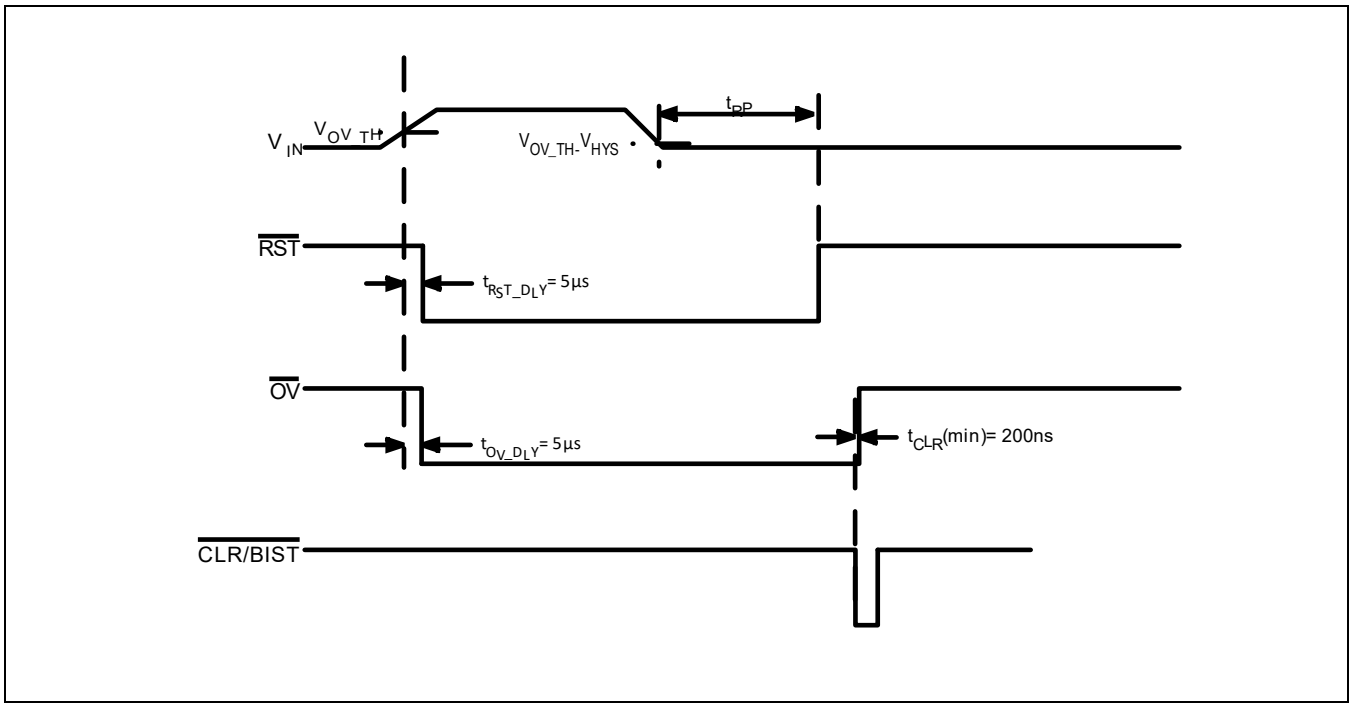


Figure 2. Clear Input Timing Diagram

Built-In Self-Test

Built-in Self-Test (BIST) is a diagnostic feature that monitors the health of the MAX16138. BIST is initiated during power-up and completes after the expiration of the reset timeout period. During power-up, the MAX16138 monitors the state of the reset output. A high-logic reset output status during power-up indicates a fault either inside or outside the MAX16138, and BIST is pulled low. See the following *Figure 3* at T1. After the expiration of the reset timeout period, the MAX16138 generates internally fictitious undervoltage and overvoltage fault scenarios, and RST deasserts. If the MAX16138 internal circuit does not respond properly to the internally generated undervoltage and overvoltage faults, BIST and RST are pulled low. See the *Figure 3* at T2 and T3. Then the MAX16138 monitors the state of the reset output again. A low-logic reset output status indicates a fault either inside or outside the MAX16138 and BIST is pulled low. See T4 in *Figure 3*.

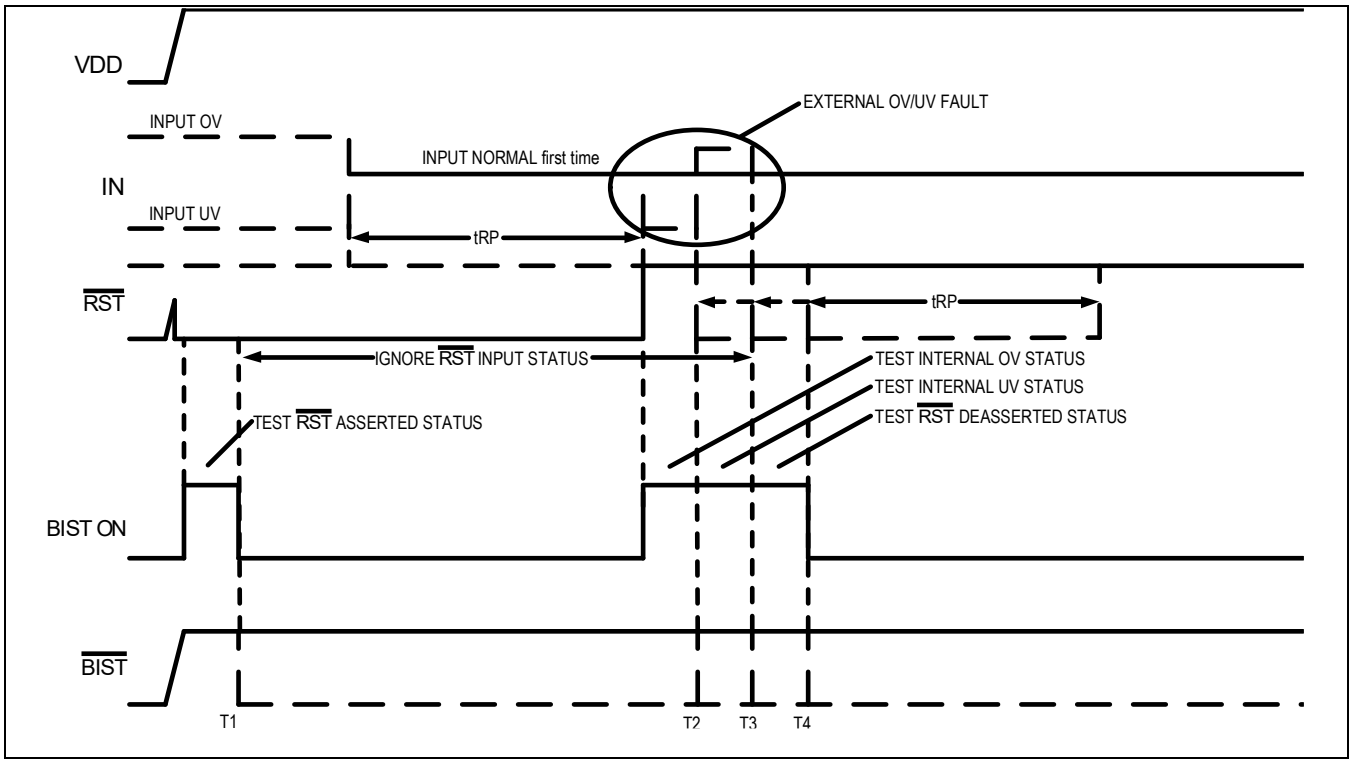


Figure 3. MAX16138 BIST Timing Relationship

On-Demand BIST

On-demand BIST allows the MAX16138 to initiate BIST during normal operation. On-demand BIST is initiated when CLR/BIST is pulled low for more than t_{BIST}. See the *Electrical Characteristics* table for more details. If CLR/BIST is pulled low for less than t_{BIST} or if the input is overvoltage or undervoltage before the expiration of t_{BIST}, on-demand BIST is ignored.

With NR at logic low and CLR/BIST pulled low for more than t_{BIST}, the on-demand BIST operation is similar to that of power-up; the MAX16138 pulls the reset output low during the internal OV and UV testing while keeping the system in reset (*Figure 4)*. When NR is at logic high and CLR/BIST is pulled low for more than t_{BIST}, the on-demand BIST operation is carried out without pulling the reset output low. See *Figure 5* for more details.

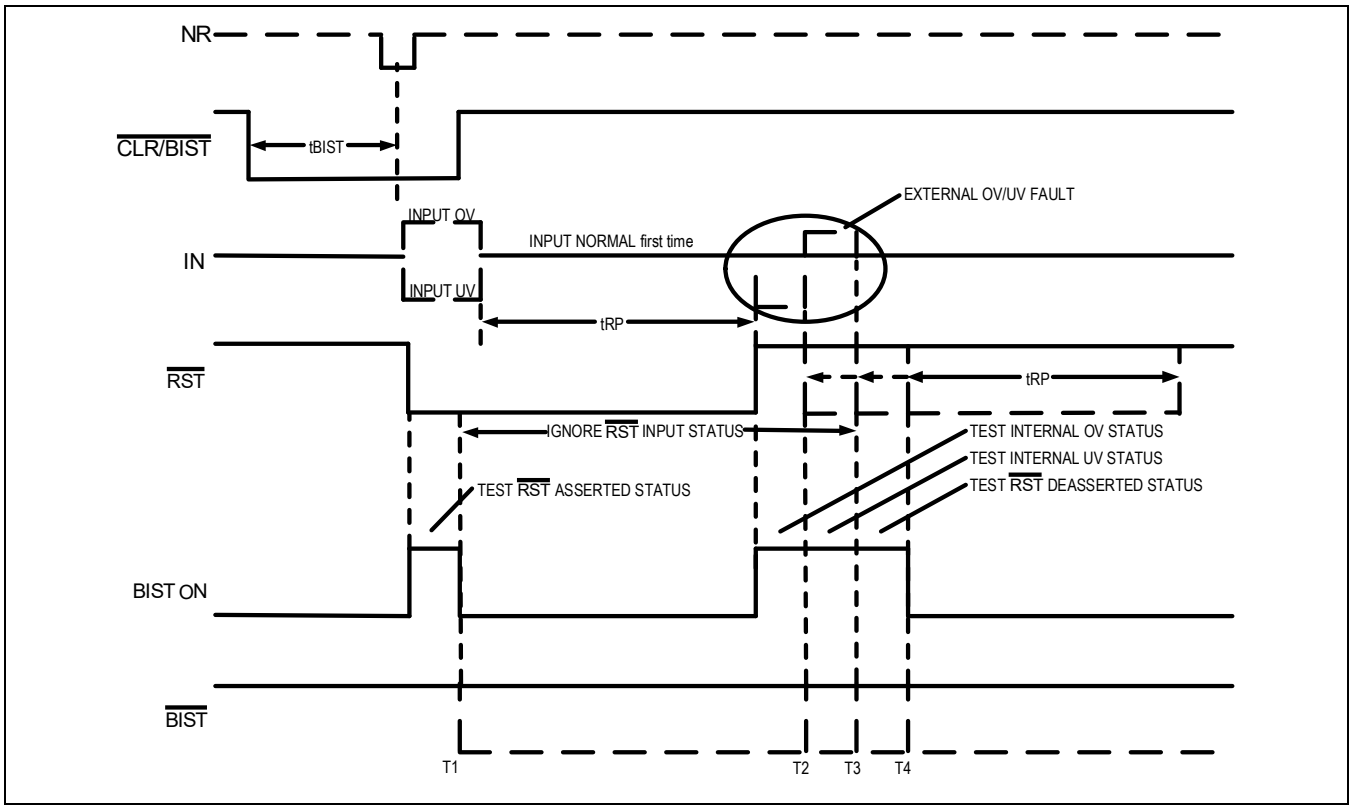


Figure 4. MAX16138 On-Demand BIST with NR = Low

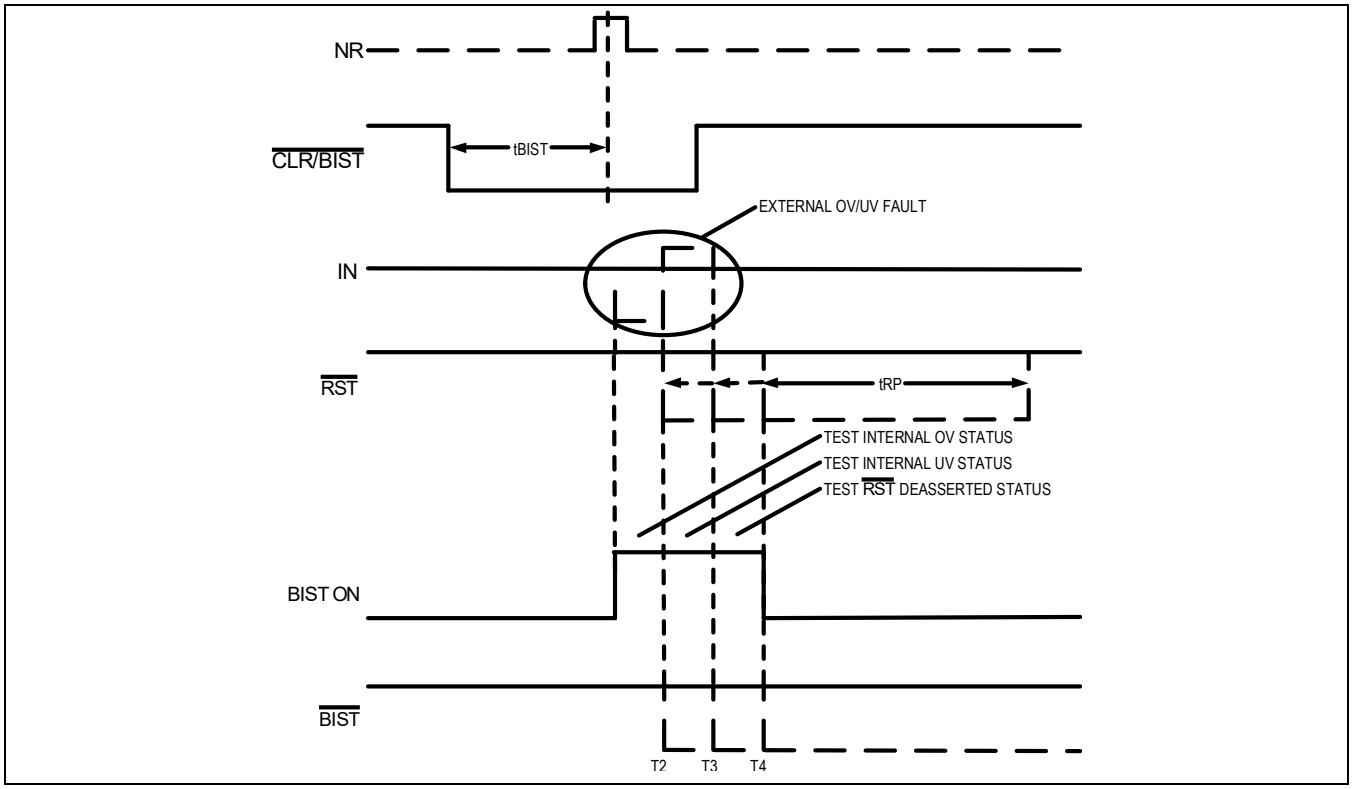


Figure 5. MAX16138 On-Demand BIST with NR = High

Reset Timeout Period

The active-low, open-drain reset output (RST) asserts low when the input voltage falls outside the set undervoltage and overvoltage window threshold. The reset output deasserts after the reset timeout period when the input voltage falls within the set window threshold. At power-up, the resets stay asserted for the reset timeout period once V_{DD} is above the UVLO. The reset output requires a pullup resistor to V_{DD}. The MAX16138 offers 16 factory-set reset timeout periods. The MAX16138 is also available in push-pull option. Contact Analog Devices for availability. See *Table 1* for available options and *Figure 6* for more details.

Table 1. Reset Timeout Options

MIN RESET TIMEOUT PERIOD
1ms
5ms
10ms
15ms
20ms
50ms
100ms
150ms
200ms
250ms
300ms
500ms
750ms
1000ms
15000ms

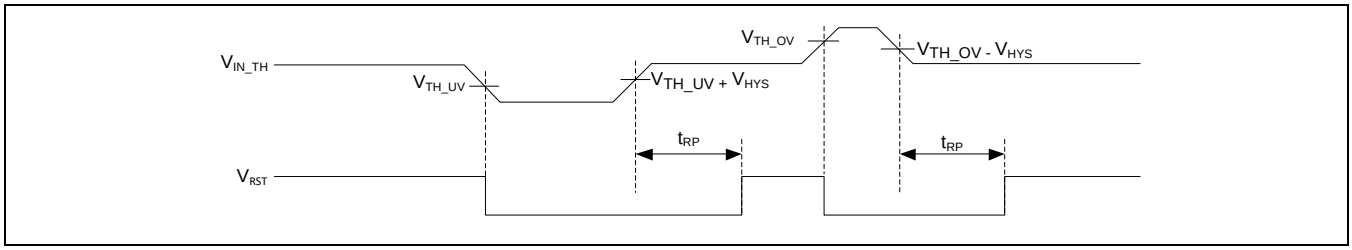


Figure 6. Reset Output Timing Diagram

Applications Information

Setting Input Thresholds Tolerance and Hysteresis

The MAX16138 monitors a system supply voltage for undervoltage/overvoltage window threshold. Depending on the system supply tolerance requirement, the undervoltage/overvoltage thresholds can be factory-trimmed from ±2% to ±9%. The tolerance setting is symmetrical with respect to the selected nominal input threshold voltage (V_{IN_NOM}). A detailed calculation of how to determine the undervoltage/overvoltage threshold levels with ±0.7% threshold accuracy for 3.31V ±5% supply voltage is as follows:

V_{IN_NOM} = 3.31V

TOL = ± 5%

$V_{UVTH} = V_{IN\_NOM} (1 - 5\%) = 3.31V (1 - 0.05) = 3.1445V$

$V_{OVTH} = V_{IN\_NOM} (1 + 5\%) = 3.31V (1 + 0.05) = 3.4755V$

where:

V_{IN_NOM} is the selected nominal input threshold voltage

TOL is the input tolerance

V_{UVTH} is undervoltage threshold voltage

V_{OVTH} is the overvoltage threshold voltage

The MAX16138 monitors the supply voltage with ±0.7% accuracy over the operating temperature and supply range. The accuracy range for the 3.3V ±5% is as follows:

$V_{UVTH\_A} = V_{UVTH} (1 \pm 0.7\%) = 3.1445V (1 \pm 0.007) = 3.1445V \pm 0.0220115V$

$V_{OVTH\_A} = V_{OVTH} (1 \pm 0.7\%) = 3.4775V (1 \pm 0.007) = 3.4775V \pm 0.0243425V$

where V_{UVTH_A} is the undervoltage threshold accuracy range and V_{OVTH_A} is the overvoltage threshold accuracy range. See *Figure 7* for details.

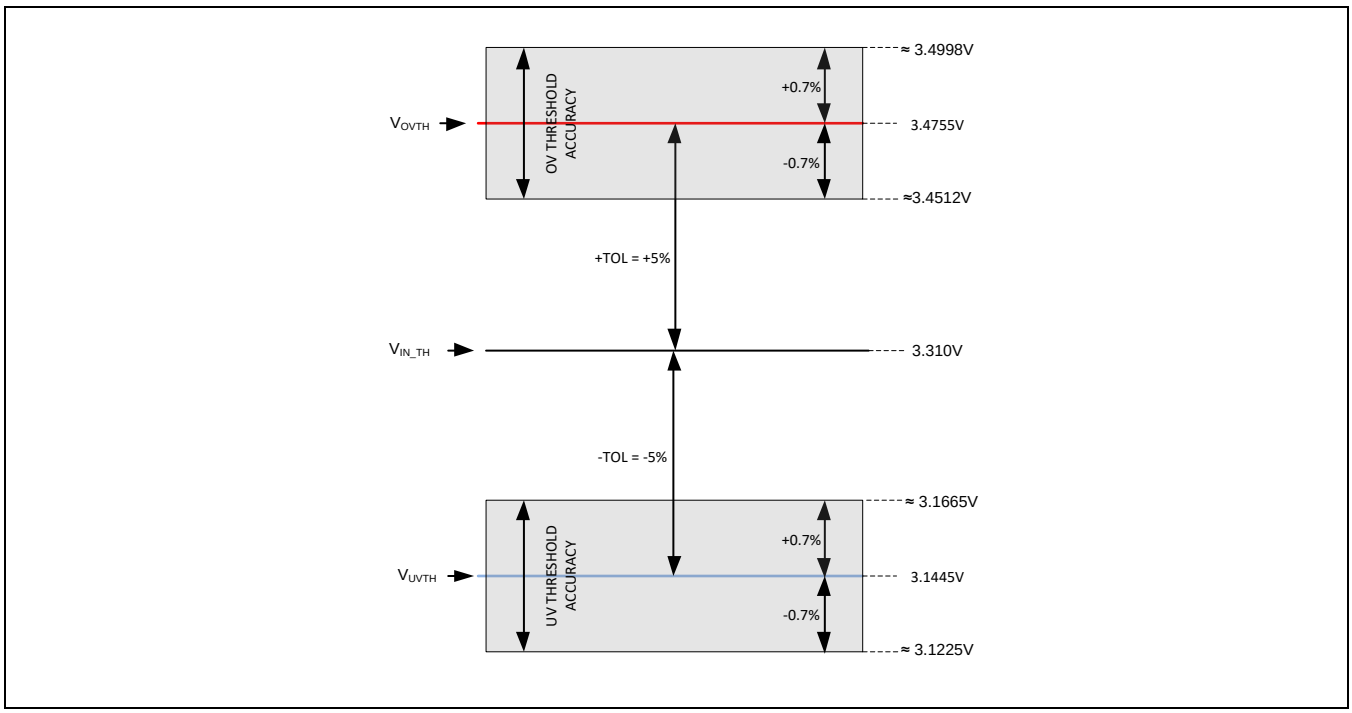


Figure 7. Undervoltage/Overvoltage Threshold Accuracy

Hysteresis adds noise immunity to the voltage monitors and prevents oscillation due to repeated triggering when the monitored voltage is near the threshold trip voltage.

A detailed calculation to get the threshold hysteresis is as follows:

V_{IN_TH} = 3.31V

Hysteresis = 0.5%

V_{HYST} = 3.31V x 0.5% = 0.01655V

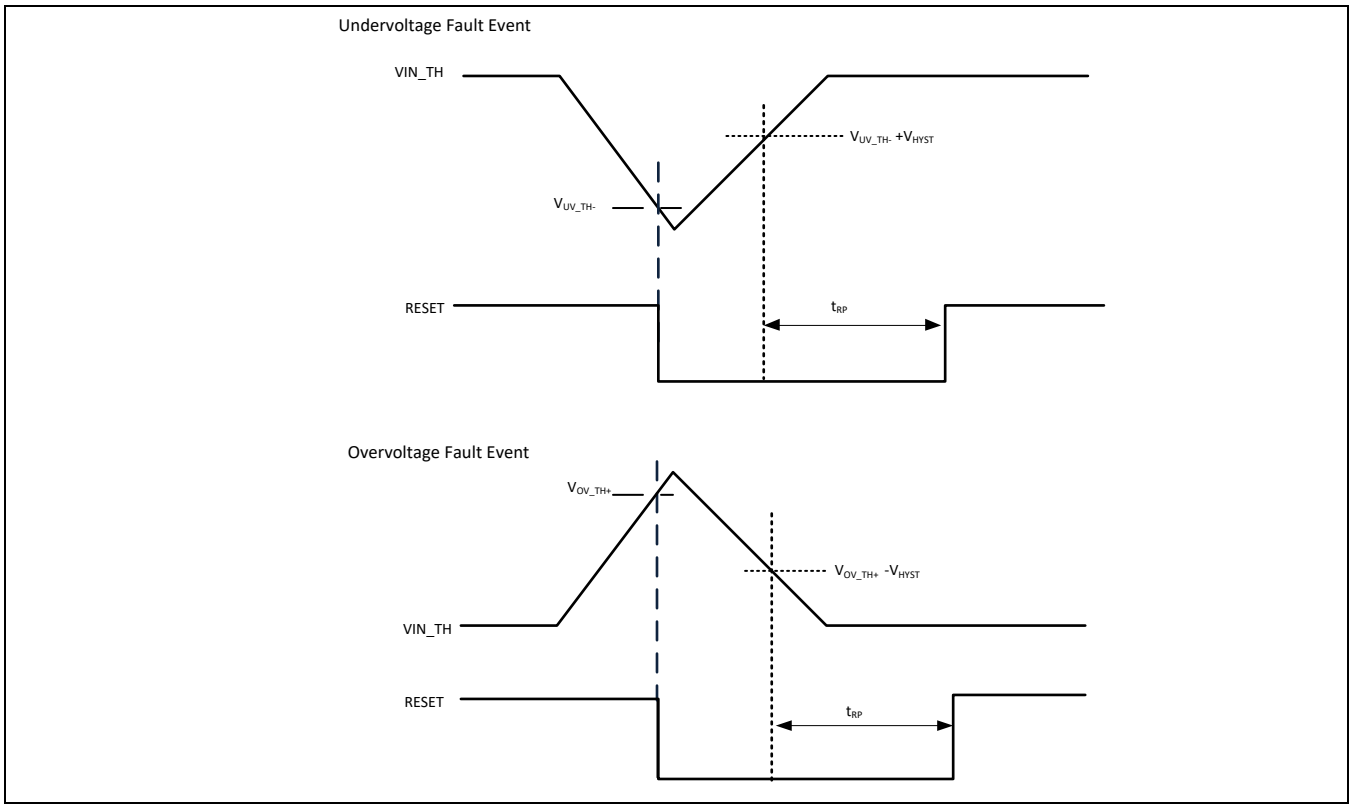


Figure 8. Undervoltage/Overvoltage Threshold Hysteresis

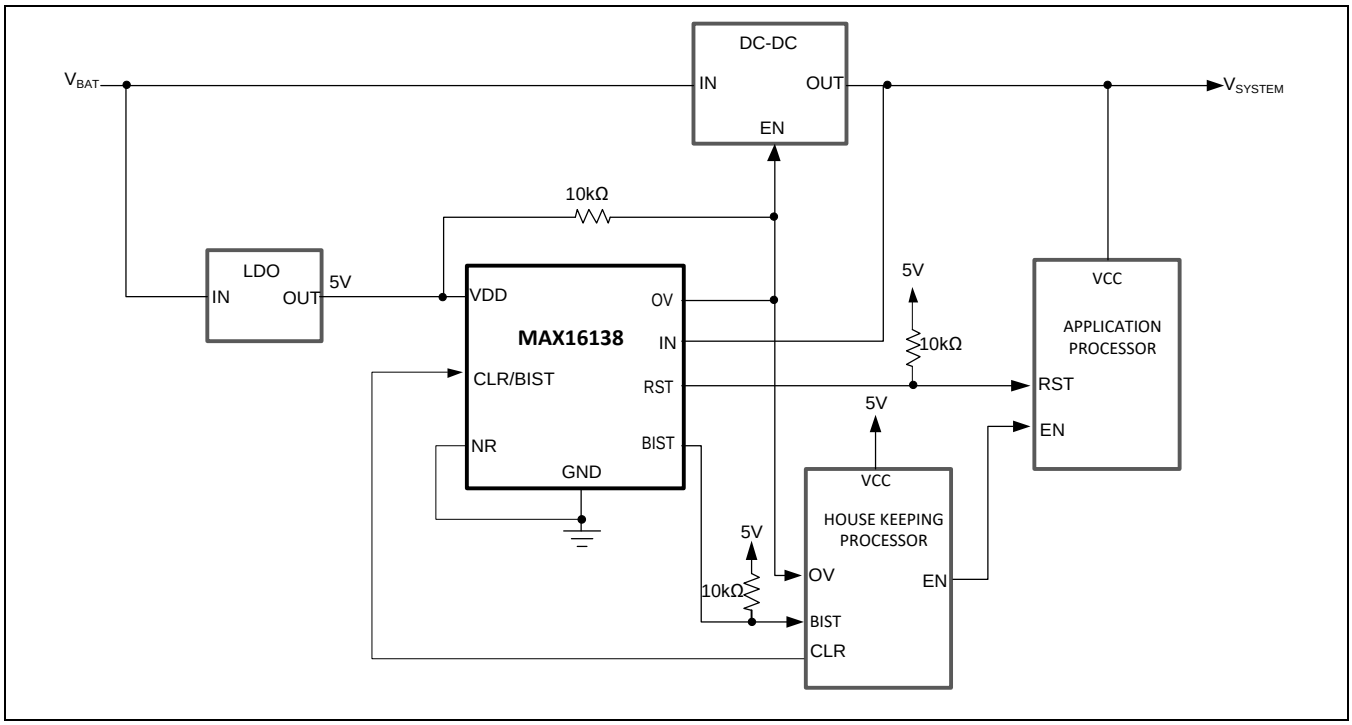
Power-Supply Bypassing/Noise Immunity

The MAX16138 operates from a 1.71V to 5.50V supply. Bypass V_{DD} to ground with a 0.1µF capacitor as close to the device as possible. An additional capacitor improves transient immunity.

Selector Guide Table

PART NUMBER	THRESHOLD VOLTAGE	TOLERANCE	HYSTERESIS	RESET TIMEOUT
MAX16138ATA01/VY+	0.85V	±4%	±0.5%	100ms

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX16138ATA01/VY+	-40°C to 125°C	8-TDFN

/V denotes an automotive qualified part.

Y =Side-wettable package.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/22	Release for Market Intro	—