CML Microcircuits

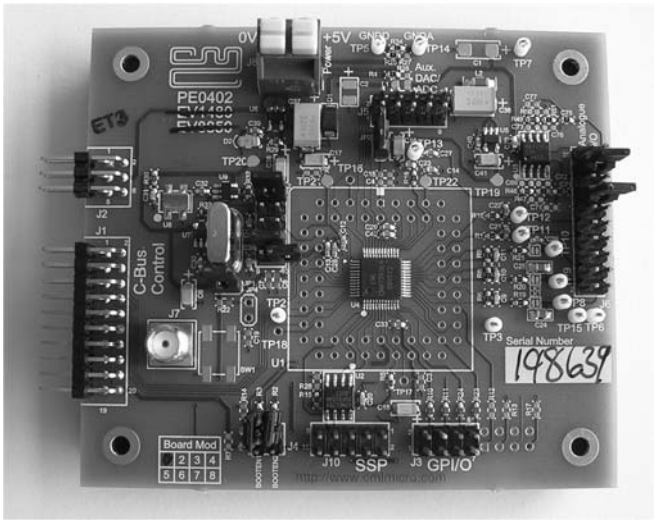
COMMUNICATION SEMICONDUCTORS

PE0402
Evaluation Kit
User Manual

UM0402/2 December 2010

Features

- **CMX704x/CMX714x *FirmASIC*® product range evaluation**
- **Serial Flash Option for Function Image™ with In-circuit Programming**
- **On-board supply regulators operate from a single 5 volt supply**
- **Command and control by PC via the PE0002 interface card or user's µC development application or emulator**
- **19.2MHz oscillator, 6.144MHz crystal or external clock input to CMX7040**
- **On-board access to all CMX7040 signals, commands and data**



1 Brief Description

The PE0402 Platform Evaluation Kit is designed to assist in the evaluation and application development of the CMX704x/CMX714x range of *FirmASIC*® products. The kit is in the form of a populated PCB comprising a CMX7040 IC and appropriate supporting components and circuitry.

The board also incorporates all of the necessary power-supply regulation facilities for operation from a single 5 volt supply.

The board is fitted with a C-BUS connector allowing the PE0402 to be operated by connection to either of the two C-BUS ports on a CML PE0002 Interface Card, and used with the associated PC GUI software, or by direct connection between the CMX7040 C-BUS and the user's µC development application or emulation system.

The CMX704x Function Image™ (FI) can be loaded, on power-up, directly into the on-board target IC (CMX7040) using the PE0002 interface or the user's system. Alternatively, it can be automatically loaded from the on-board serial memory, on power-up. In this case, the on-board serial memory has to be pre-loaded with the FI by using a suitable third party programmer or by using the 'Program Serial Memory' tab on the PE0002 GUI software. This software is available from the CML website.

Function images suitable for the CMX704x/CMX714x range of products can be downloaded from the CML Technical Portal.

CONTENTS

Section Page

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
2	Covers two types of serial memory used – dependant upon mod state and serial numbers.	9th Dec '10
1	Original document.	28th Aug '09

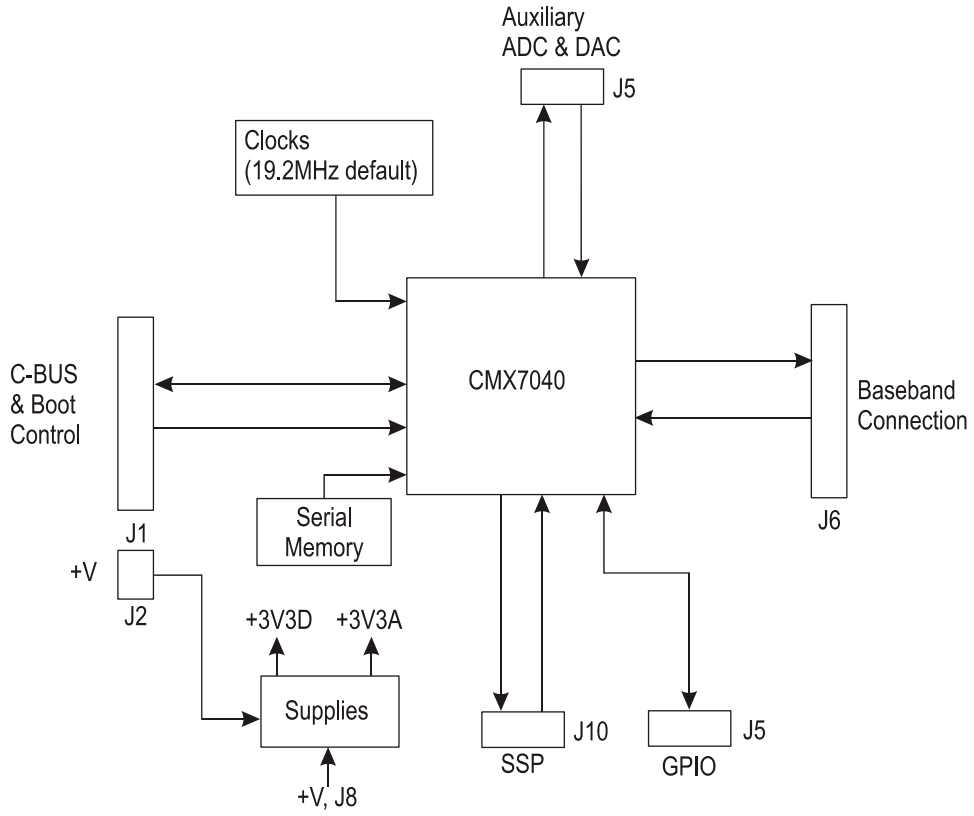


Figure 1 – Block Diagram

2 Preliminary Information

The PE0402 is designed to support the CMX704x/CMX714x range of *FirmASIC*® devices using their respective Function Image™.

The CMX7040 IC fitted to the PE0402 is a special evaluation IC with the architecture of all CMX704x/CMX714x series ICs. The functionality of this evaluation IC is obtained from the relevant Function Image™ (FI); evaluation FIs are downloaded from the CML Technical Portal. Each Function Image™ can represent a different set of features.

2.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

A 5 Volt dc regulated power supply.

If the PE0402 is being used with the PE0002 Interface Card, the following items will also be required:

1. An IBM compatible PC with the following requirements:
   - One of the following Windows operating systems installed: 2000sp4 or XPsp2.
   - USB port.
   - Minimum screen resolution 800 x 600. Recommended resolution 1024 x 768.
2. A USB type A male to mini B male cable.
3. Software application **`ES000230.exe`**, or later version, installed on the PC.

2.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

2.2.1 Static Protection

This product uses low power CMOS circuits that can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.2.2 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK0402) and notify CML within 7 working days if the delivery is incomplete.

2.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product.

3 Quick Start

This section is divided into two sub-sections. The first is for those users who are using the PE0402 with a PE0002 controller card and its Windows PC GUI software. The second is for users who are using the PE0402 by itself, without a PE0002.

3.1 With PE0002

Note that the C-BUS connector J1 and the power connector J2 are both right angle headers and are designed to plug directly into sockets J5 (C-BUS 1 port) and J9 respectively, or sockets J3 (C-BUS 2 port) and J7 respectively, of a PE0002.

3.1.1 Setting-Up

- Refer to the PE0002 user manual, and follow the instructions given in the quick start section.
- Ensure the jumpers on J4 are open circuit. The BootEn1 and BootEn2 signals are driven from the PE0002.

The basic arrangement, when used with the PE0002 is shown below:

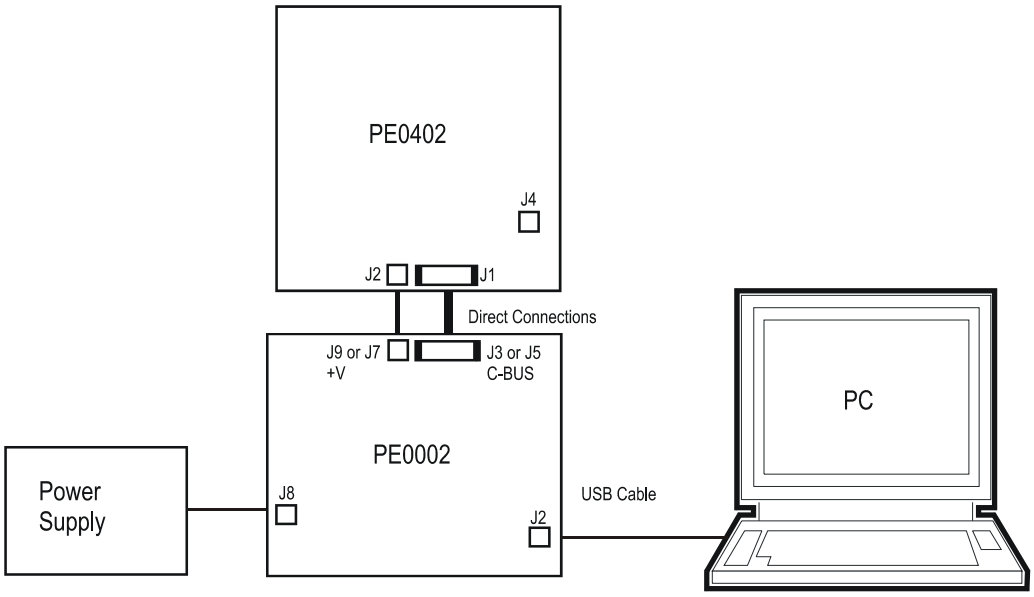


Figure 2 – PE0402 used with PE0002

3.1.2 Operation

The Function Image™ (FI) must now be loaded into the CMX7040 device. A FI is provided as a 'C' type header file and must be obtained from the CML Project Resource Portal. There are two methods available for loading the FI:

1. Directly from a file on the PE0002 host PC to the CMX7040.

2. From the on-board PE0402 serial memory. To use this method the serial memory must first be programmed with the FI by using the 'Program Serial Memory' tab on the PE0002 GUI software.

The PE0402 should now be ready for evaluation of the CMX7040 with the chosen FI.

3.2 Without PE0002

As an alternative to using the PE0002 controller kit, users may control the CMX7040 target device with a user-supplied host controller card. C-BUS connections are made via connector J1.

The power-up, or boot state of the CMX7040 BOOTEN1 and BOOTEN2 pins may be set using jumpers on header, J4. Consult the relevant CMX704x/CMX714x documentation for valid modes. A jumper in-circuit on header, J4, corresponds to a '0' state on the boot pins. Alternatively the state of these pins may be set via the connector, J1, pins 13 and 14. By default, 47kΩ pullup resistors on the PE0402 board provide a '1' state on each of the two BOOTEN pins.

A FI for the CMX7040 device must be either included in the customer's host system and loaded into the CMX7040 device on power-up or programmed into the on-board serial memory following the guidelines in the application note: 'Writing a Function Image™ to Serial Memory'.

4 Signal Lists

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1	1, 3, 5, 7, 9, 15 to18	N/C	-	
	2	CSN	I/P	Chip select. Connects to host μC.
	4	CDATA	I/P	Serial Data input. Connects to host μC.
	6	SCLK	I/P	Serial clock input. Connects to host μC.
	8	RDATA	O/P	Serial data output. Connects to host μC.
	10	IRQN	O/P	Interrupt request. Connects to host μC.
	11, 12	GNDD	PWR	Digital supply ground.
	13	BOOTEN1	I/P	CMX7040 Hardware Boot Control.
	14	BOOTEN2	I/P	CMX7040 Hardware Boot Control.
	19, 20	+3V3D	PWR	3.3V dc digital supply rail.
J2	1, 2	GNDD	PWR	Digital supply ground.
	3 to 6	+V	PWR	External supply voltage – Daisy chained from PE0002.
J3	1	GPIO1	BI	General purpose I/O pin.
	3	GPIO2	BI	General purpose I/O pin.
	5	GPIOA	BI	General purpose I/O pin.
	7	GPIOB	BI	General purpose I/O pin.
	2, 4, 6, 8	GNDD	PWR	Digital supply ground.
J5	1	AUXADC4	I/P	Auxiliary ADC input.
	2	AUXDAC1	O/P	Auxiliary DAC output.
	3	AUXADC3	I/P	Auxiliary ADC input.
	4	AUXDAC2	O/P	Auxiliary DAC output.
	5	AUXADC2	I/P	Auxiliary ADC input.
	6	AUXDAC3	O/P	Auxiliary DAC output.
	7	AUXADC1	I/P	Auxiliary ADC input.
	8	AUXDAC4	O/P	Auxiliary DAC output.
	9, 10	GNDA	PWR	Analogue supply ground.

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J6	1	IP1	I/P	Channel 1 inverting input.
	3	IP2	I/P	Channel 2 inverting input.
	5	IP3	I/P	Channel 3 inverting input.
	7	MOD1	O/P	Channel 1 output.
	9	MOD2	O/P	Channel 2 output.
	11	AUDIO	O/P	Channel 3 output.
	13	BUF1IN	I/P	High impedance buffered input.
	15	BUF1OUT	O/P	Buffered output.
	17	BUF2IN	I/P	High impedance buffered input.
	19	BUF2OUT	O/P	Buffered output.
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20	GNDA	PWR	Analogue supply ground.
J7		CLK EXT	I/P	External input option for CMX7040 clock.
J8		+V	PWR	External supply voltage.
		0V	PWR	External supply ground.
J10	1	SSOUT/ FSO	BI	SSP Frame sync.
	3	MOSI	O/P	SSP Master output, slave input.
	5	MISO	I/P	SSP Master input, slave output.
	7	SSPCLK	BI	SSP Clock.
	2, 4, 6, 8	N/C	-	
	9, 10	GNDD	PWR	Digital supply ground.

Table 1 – Signal List

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP2	0V	Loop – CMX7040 system clock 2 output.
TP3	0V	Loop – CMX7040 system clock 1 output.
TP5	0V	Loop – GNDD, digital ground.
TP6	0V	Loop – GNDA, analogue ground.
TP7	0V	Loop – GNDA, analogue ground.
TP8	-	Loop – IP1 - Channel 1 inverting input.
TP9	-	Loop – IP2 - Channel 2 inverting input.
TP10	-	Loop – IP3 - Channel 3 inverting input.
TP11	HiZ	Loop – MOD1 - Channel 1 output.
TP12	HiZ	Loop – MOD2 - Channel 2 output.
TP13	HiZ	Loop – Audio - Channel 3 output.
TP14	0V	Loop – GNDA, analogue ground.
TP15	0V	Loop – GNDA, analogue ground.
TP19	3.3V	Pad – Output from on-board regulator. DC supply voltage for analogue rail.
TP20	3.3V	Pad – Output from on-board regulator. DC supply voltage for digital rail.
TP21	2.5V	Pad – CMX7040 internally generated voltage.
TP22	0V	Pad – CMX7040 VBIAS.

Table 2 – Test Points

JUMPERS			
Link Ref.	**Positions**	**Default Position**	**Description**
JP1	1-2	Short	Isolates digital supply rail from CMX7040.
JP2	1-2	Short	Isolates analogue supply rail from CMX7040.
J4	1-2	Open	Manual BootEn1 control (short = LO).
	3-4	Open	Manual BootEn2 control (short = LO).
J9	1-2	Short	19.2MHz oscillator clock source.
	3-4	Open	External clock source.
	5-6	Open	Crystal clock source – if components fitted by customer.
	7-8	Short	Ground external clock input.
	9-10	Open	Crystal clock source – if components fitted by customer.
J6	13-14	Short	Ground input to uncommitted buffer1.
	17-18	Short	Ground input to uncommitted buffer2.

Table 3 – Jumpers

LEDs	
LED Ref.	**Description**
D2	Indicates that the digital supply voltage is present.

Table 4 – LEDs

Notes:
BI = Bidirectional
HiZ = High impedance
I/P = Input
N/C = Not connected
O/P = Output
PWR = Power supply connection

5 Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as separate high-resolution files. These can be obtained via the CML website.

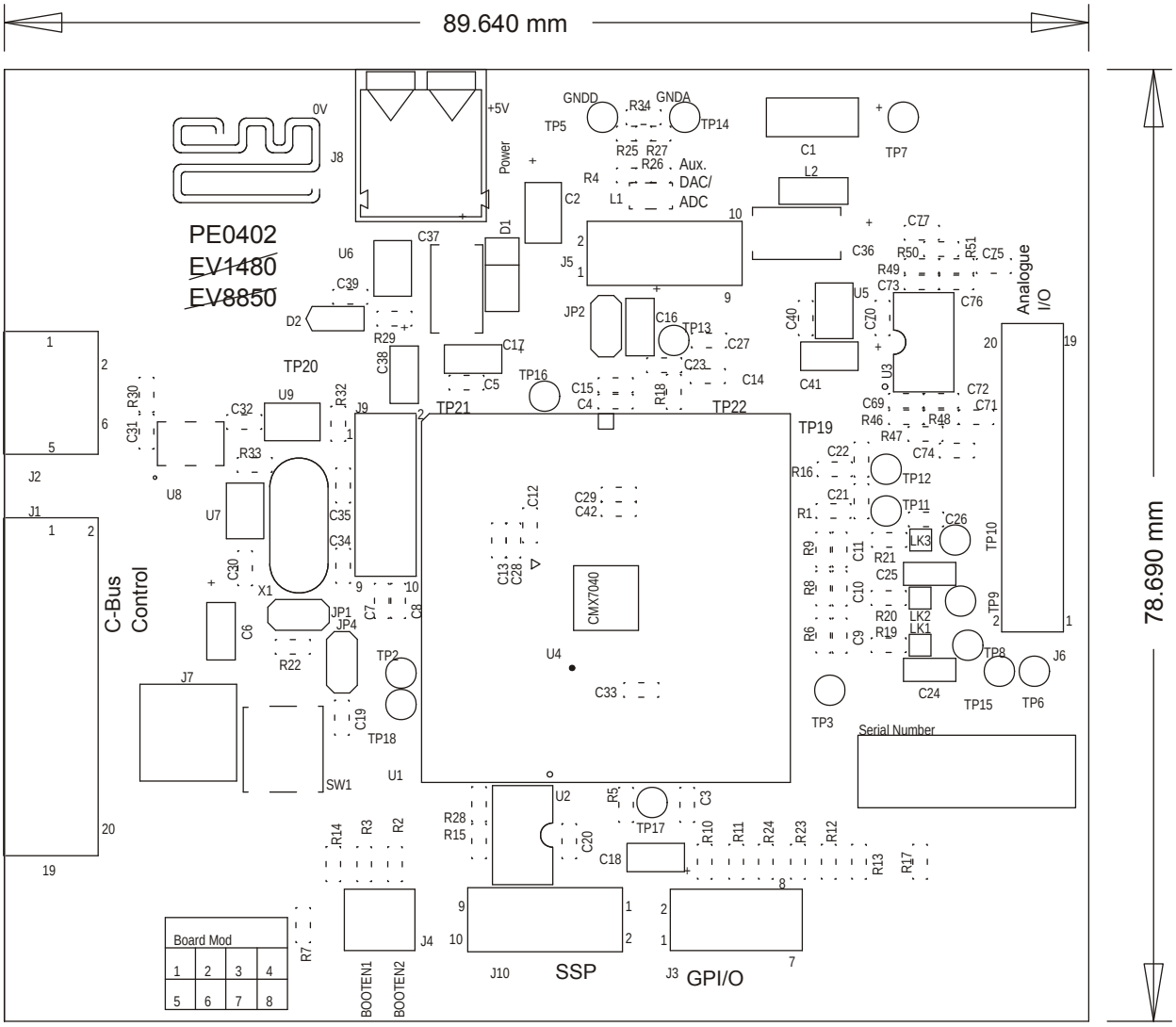


Figure 3 – PCB Layout: Top

6 Detailed Description

6.1 Hardware Description

The PE0402 as shipped may not have the optimum configuration or component values for all function images. Check the PE0402 schematic against recommendations in the specific CMX704x/CMX714x datasheet.

6.1.1 Power Supplies

The board is fitted with two voltage regulators. U5 and U6 provide the analogue and digital supply rails respectively. The input to these two regulators should be provided by an external 5V dc regulated power supply, which can be daisy chained from the PE0002 or connected to the board via connector J8, a push type connector.

The analogue and digital supply voltage levels can be monitored on test points TP19 and TP20 respectively.

LED illumination confirms the on-board presence of the +3.3V dc digital voltage supply.

6.1.2 Clock Options

The PCB is designed to provide three CMX7040 device clock options. The board is supplied with a 19.2MHz oscillator module fitted. This option allows convenient RF synthesiser configuration to typical channel spacings.

Other options are an external clock source at J7 or a 6.144MHz quartz crystal oscillator circuit (C34, C35 and X1).

Header J9 is used with jumper sockets to select the required option as shown in the table below. Shaded cells illustrate locations where a jumper socket should be fitted.

J4 Jumper Position	**Clock Option**		
	19.2MHz TCXO (default)	External	Quartz crystal
1-2	■		
3-4		■	
5-6			■
7-8	■		■
9-10			■

Table 5 – Clock Select Jumper Positions

6.1.3 Control Interface

The C-BUS and CMX7040 boot control signals are brought out on connector J1. This is a right angle male header designed to plug directly into the PE0002 interface card that has a matching female header.

Alternatively, if not using the PE0002, the CMX7040 boot control signals can be manually set with jumpers on header J4.

6.1.4 Serial Memory

The serial memory, U2, can be used for non-volatile storage of a Function Image™. The PE0402 is shipped with a blank serial memory.

6.1.5 Baseband Interfacing

Connector J5 provides access to Auxiliary ADCs 1 to 4 and Auxiliary DACs 1 to 4 of the CMX7040 device.

The CMX7040 device baseband input amplifiers for IP1, IP2 and IP3 are configured as ac coupled, unity gain, inverting amplifiers. The inputs to these circuits are fed from connector J6.

The CMX7040 device baseband outputs, MOD1, MOD2 and AUDIO, are fed through an RC network to connector J6.

A dual op amp IC is fitted to the board, with both amplifiers configured as unity-gain buffers. It is possible to set up other op amp based configurations with the addition of passive components to the PCB footprints provided. It is recommended that 0603 sized surface mount components be used. Access to the input and output of each of these uncommitted amplifiers is also from connector J6.

6.1.6 Digital Interfacing

Connector J3 provides access to four general purpose I/O lines.

Connector J10 provides access to a synchronous serial port.

Use of these signals is Function Image™ dependant. In some cases they will have no function. See relevant CMX704x/CMX714x documentation.

6.2 Adjustments and Controls

The boot state of the CMX7040 device can be set manually, using jumpers on header, J4. If using with the PE0002, the jumpers should be left open circuit.

6.3 Function Image™

There are two methods by which a FI may be loaded into the CMX7040 device.

Whenever power is removed from the PE0402 the FI data will be erased from the CMX7040 device. Therefore, whenever power is applied a FI must be loaded, either from the serial memory or via the C-BUS interface.

If the PE0402 is used with the PE0002 PC interface, function images can be loaded as described in sections 6.3.1, 6.3.2 and 6.3.3.

6.3.1 Load Function Image™ via C-BUS

Use the Function Image™ Load tab. Select Function Image™ Source: 'C-BUS'.

- Enter the name of the file containing the Function Image™, or navigate to the required file using the 'Browse' button.
- Enter the activation code in the lower edit box. Alternatively select one of two previously used codes in the drop down list.
- Select Target Board.
- Click the "Load" button. The progress of the download is shown visually on the progress bar and when the download has completed a message box will be displayed indicating if the result of the download operation was successful or not.

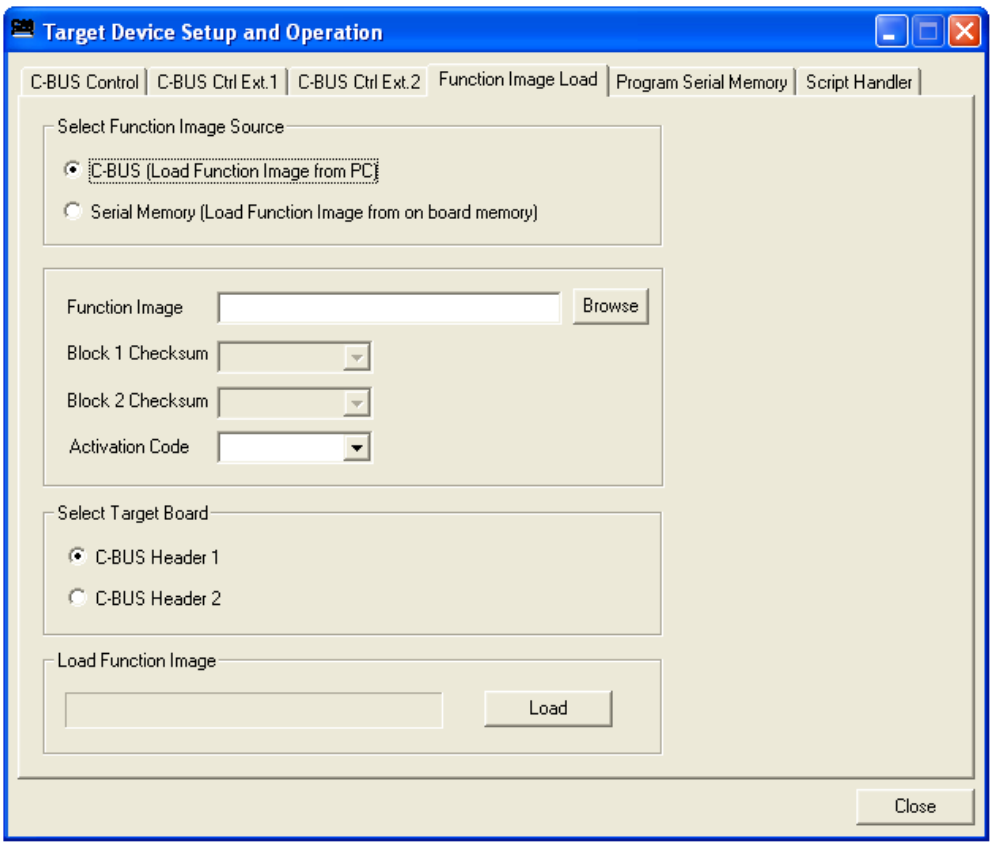


Figure 4 – Function Image™ Load Tab – via C-BUS

6.3.2 Load Function Image™ from Serial Memory Device

It is assumed that the serial memory has been programmed with the Function Image™ prior to using this load method. This can be carried out with the serial memory in circuit using the ES0002xx 'Program Serial Memory' tab.

Use the Function Image™ Load tab. Select Function Image™ Source: 'Serial Memory'.

- Enter the block 1 and block 2 checksum values in the edit boxes. Alternatively select one of two previously used values in the drop down list for each block.
- Enter the activation code in the lower edit box. Alternatively select one of two previously used codes in the drop down list.
- Select Target Board.
- Click the 'Load' button. The progress of the download is shown visually on the progress bar and when the download has completed a message box will be displayed indicating if the result of the download operation was successful or not.

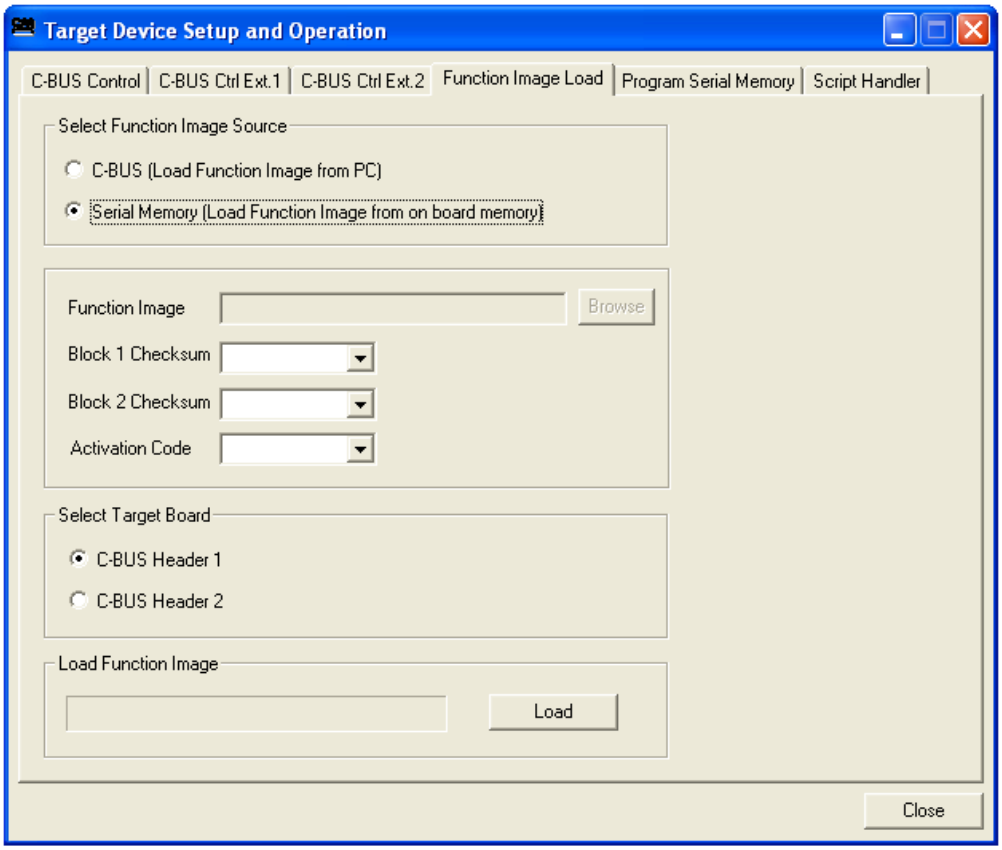


Figure 5 – Function Image™ Load Tab – from Serial Memory

6.3.3 Program Serial Memory

The specific serial memory device fitted to the PE0402 and the appropriate "thick stub" application software are shown below. The "thick stub" application software is available from the CML Technical Portal.

Revision	Serial numbers	Memory type	Thick Stub
Up to Rev B Mod 2*	Up to 198841	Atmel AT25F512A	**FI_FLASH_xx.h**
From Rev B Mod 3*		ST M25P10A or equivalent.	**EF0402_M25P10A_xx.h**

Table 6 – Serial Memory Types

* For correct identification of mod state (modification state) see section 6.5.1

Use the 'Program Serial Memory' tab:

- Enter the name of the file containing the thick stub, or navigate to the required file using the 'Browse' button. This file is in the same 'C' language header format as the Function Image™.
- Enter the name of the file containing the Function Image™, or navigate to the required file using the 'Browse' button.
- Enter, in units of MHz, the crystal/clock input frequency of the CMX7040 device. The default is 19.2MHz. The 'Clk. Divide Setting' is dependent on the entered frequency value and is calculated by the software, requiring no intervention from the user.
- Select Target Board.
- Click the 'Load' button.

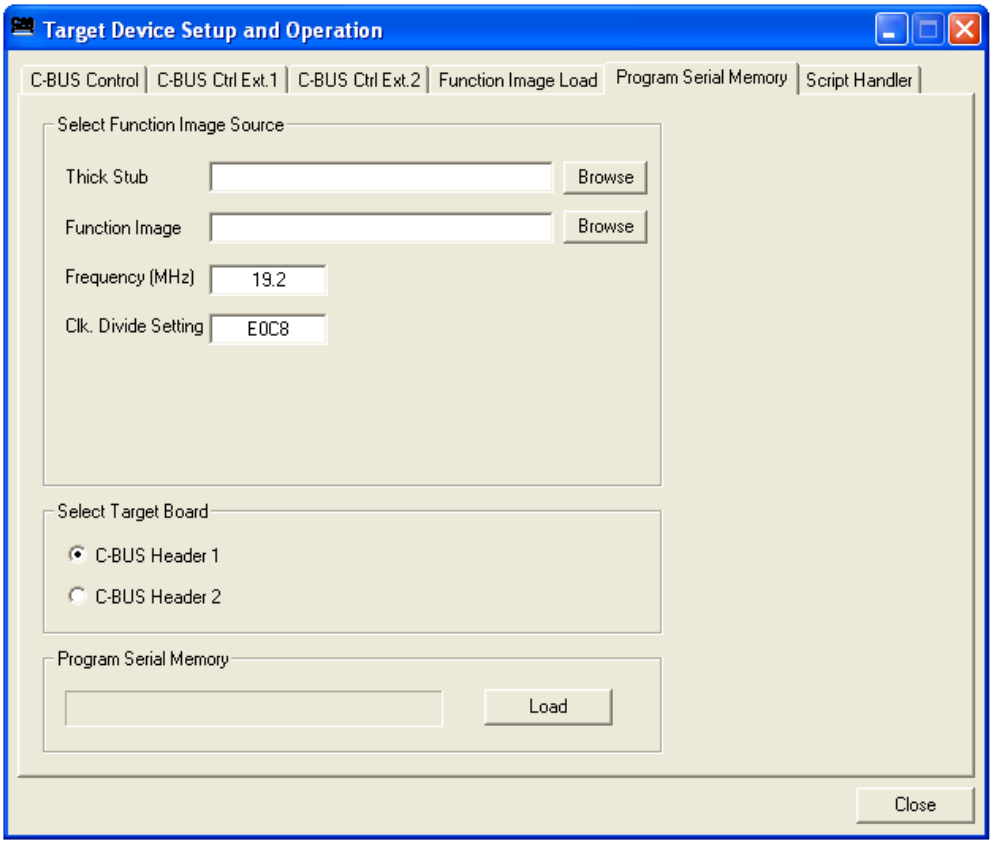


Figure 6 – Program Serial Memory Tab

Shortly after pressing the Load button, a message box will confirm that the application has loaded the Thick Stub.

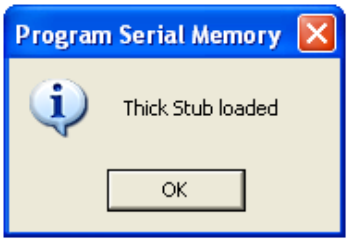


Figure 7 – Thick Stub Loaded Message Box

Click on the message box OK button and the application will proceed to programme the Function Image™ into the serial memory on the PE0402 card. Progress is shown visually on the progress bar. When programming is complete a message box will be displayed indicating if the operation was successful or not.

Figure 8 – Program Serial Memory Complete Message Box

6.4 Evaluation Tests

Before a Function Image™ is loaded into the CMX7040 device; there is a limited functionality that can be demonstrated directly by programming the C-BUS registers. The following examples can be used to verify control of the CMX7040 via the C-BUS interface. These registers can be programmed using the 'C-BUS Control' tab in the PE0002 software.

6.4.1 Write to and Read from a Register

- Write any 16-bit number to register $C0.
  The data transferred to the device on the Command Data pin looks like this:
  { C0 } { <ms byte> } { <ls byte> } ..... Command Data

- The value written to this register (the Powerdown Control register) can be read back from register $C4 by issuing a single command byte, then reading two data bytes from the Reply Data pin, as follows:
  { C4 } ..... Command Data
  { <ms byte> } { <ls byte> } ..... Reply Data

Note that the power consumption of the device will increase once this register has been written to, since some parts of the device will no longer be powersaved.

6.4.2 Check Analogue Path and Set Input Gain

Configure the CMX7040 with the C-BUS register data given in Table 7.

	C-BUS Register	
Write Data	Address	Name
$5061	$C0	Powerdown Control
$770F	$B0	Analogue Gain
$0830	$B1	Input Gain and Signal Routing
$0008	$CF	Test Mode

Table 7 – CMX7040 Register Settings - Analogue Path and Input Gain

Apply a 1kHz, audio signal to the input, IP3 (J6 pin 5 or TP10), at a level of -10dBm (the maximum signal level before distortion is about +1dBm).

Check the audio signal coming out of the AUDIO OUT pin (TP13). The level should be nominally 6.4dB, above the level of the input signal.

6.4.3 Check Analogue Path and Set Output Gain

Configure the CMX7040 with the C-BUS register data given in Table 8.

	C-BUS Register	
Write Data	Address	Name
$A3E1	$C0	Powerdown Control
$650C	$B0	Analogue Gain
$0001	$CF	Test Mode

Table 8 – CMX7040 Register Settings - Analogue Path and Output Gain

Apply a differential 1kHz, audio signal across the inputs, IP1 (J6, pin 1 or TP8) and IP2 (J6, pin 2 or TP9), at a level of 0dBm between them.

Check the audio signal coming out of the AUDIO OUT pin (TP13).
The level should be –9.2dBm.

Check the audio signal coming out of the MOD1 pin (J6, pin 7 or TP11). The level should be -8.0dBm.

Check the audio signal coming out of the MOD2 pin (J6, pin 9 or TP12). The level should be -10.0dBm.

The MOD1 and MOD2 outputs should have a DC bias level of approximately 1.65 volts.

6.4.4 Generate Two External Digital Clocks

Configure the CMX7040 with the C-BUS register data given in Table 9.

	C-BUS Register	
Write Data	Address	Name
$0021	$C0	Powerdown Control
$1900	$AB	System Clock 1 PLL Configuration
$E0C8	$AC	System Clock 1 Reference and Source Configuration
$0E00	$AD	System Clock 2 PLL Configuration
$E6C8	$AE	System Clock 2 Reference and Source Configuration

Table 9 – CMX7040 Register Settings - External Digital Clocks

With the default 19,2MHz clock input, a digital clock frequency of 4.096MHz should be observed at the system clock 1 output (TP3) and a frequency of 16.384MHz should be observed at the system clock 2 output (TP2).

Now write 0xC0C8 to either $AC or $AE registers, to turn off the system clock 1 or system clock 2 outputs, respectively.

6.5 Troubleshooting

After loading a Function Image™ the ES0002xx application writes the activation code that has been typed into the Activation Code edit box to the CMX7040 device. If this code is incorrect for the Function Image™ that has just been loaded the CMX7040 device will lock up and will not respond to further input from the ES0002xx application. It is recoverable only by closing the ES0002xx application, power cycling the PE0402 and PE0002 cards, and then restarting the application. Keep the power off for at least 10 seconds during this process.

6.5.1 Modification State

The modification state (mod state) of the PE0402 can be determined from the 'Board Mod' box printed on the PCB silkscreen. The highest number in the box that is blacked out gives the mod state. The following examples indicate a mod state of 3.

Figure 9 – Examples of Mod State Identification

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (+V – 0V)	-0.3	9.0	V
Voltage on any connector pin to V_{SS}	-0.3	3.6	V
Current into or out of +V and V_{SS} pins	0	+0.45	A
Current into or out of any other connector pin	-20	+20	mA

7.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (+V – 0V)		4.5	5.5	V
External Clock Frequency		3.0	24.576	MHz

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Evaluation Device Clock Frequency = 19.2MHz, +V = 5.0V, Tamb = +25°C.

For CMX7040 parameters, see relevant CMX704x/CMX714x data sheet.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1, 2	-	15	-	mA
+3V3A		3.15	3.3	3.45	V
+3V3D		3.15	3.3	3.45	V
Analogue Parameters					
Output Impedances					
Mod1, Mod2 and Audio	3	-	100	-	kΩ
Buf1out and Buf2out	4	-	0.1	-	Ω
Input Impedances					
IP1, IP2 and IP3		-	50	-	kΩ
Buf1in and Buf2in	4	1	-	-	MΩ
External Clock Input					
'High' pulse width		21	-	-	ns
'Low' pulse width		21	-	-	ns
Input impedance		10	-	-	MΩ

Notes:
1. PCB current consumption, not current consumption of the CMX7040.
2. Not including any current drawn from pins by external circuitry.
3. Small signal impedance.
4. When configured, as supplied, as unity gain buffers.

7.1.4 Operating Characteristics - Timing Diagrams

Please refer to relevant CMX704x/CMX714x Datasheet for details.

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New function images may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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