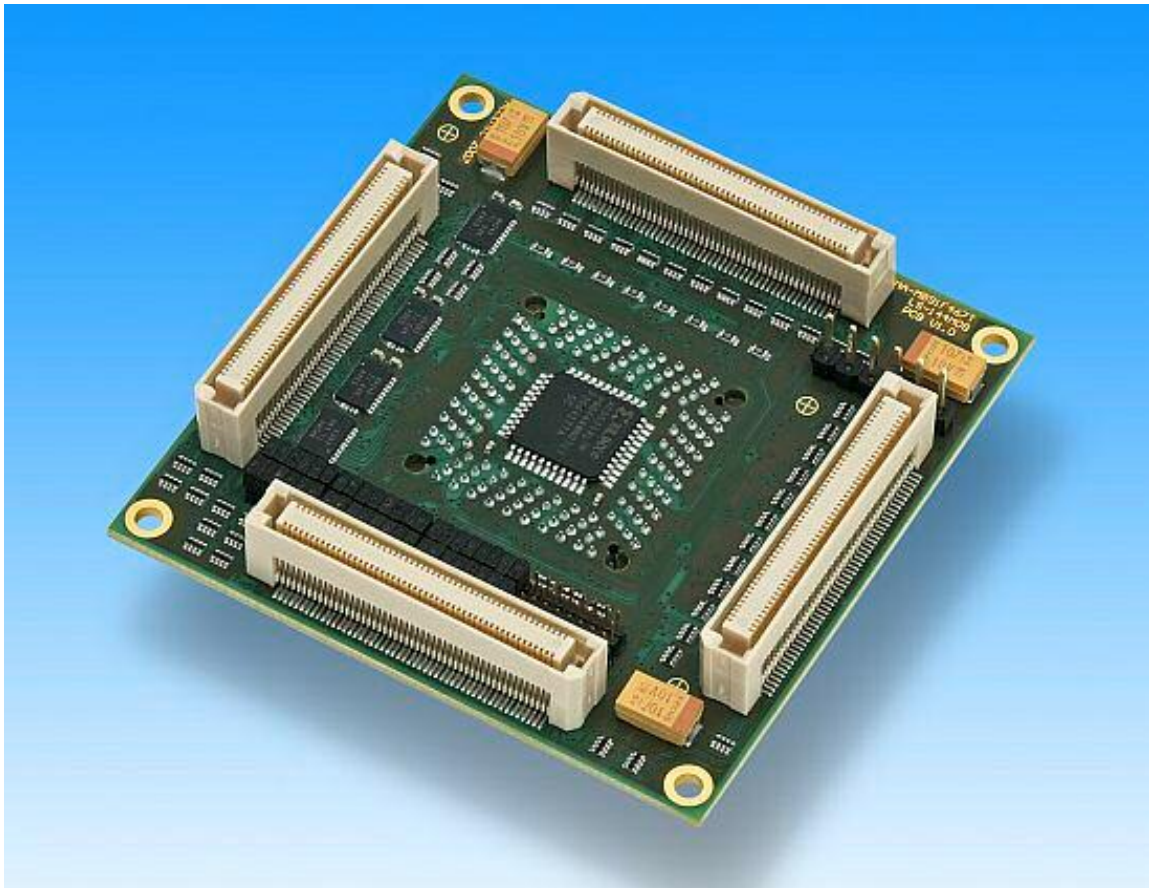# FR60 FAMILY
SOCKET ADAPTER BOARD
EMA-MB91F467T-LS-144M08

USER GUIDE

Revision History

Date	Issue
12.09.2007	V1.0, MB,AW,RH First creation
02.10.2007	V1.1, Amendments to tables 3.4.1 to 3.4.3; table 3.4.4 deleted
25.10.2007	V1.2, Removing of headlines
19.01.2009	V1.3, CEy Description for EMA-MB91FV460B-001 added, updated CPLD code

Schematic version: 1.1

PCB version: 1.0

CPLD version: 1.3

This document contains 21 pages.

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0 Contents

1   Overview

1.1   Abstract

The EMA-MB91F467T-LS-144M08 in combination with the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 is a development system for the Fujitsu FR60 MB91V460 Flash microcontroller.

The EMA-MB91F467T-LS-144M08 is an adapter board with level shifters to support the MB91V460A external bus interface at 3.3V levels.

The development system allows the designer immediately to start with the software development before MB91V460 based silicon samples are available.

This board must only be used for test applications in an evaluation laboratory environment.

Before using the EMA-MB91F467T-LS-144M08 adapter board, make sure that the following packed components have been delivered:

- o   1 pcs. EMA-MB91F467T-LS-144M08 socket adapter board
- o   1 pcs. YQPACK144SD
- o   5 pcs. Screw M2x12
- o   5 pcs. Washer M2, Nylon
- o   20 pcs. 1.27mm mini jumper
- o   1 pcs. User Guide

1.2   General Description

The EMA-MB91F467T-LS-144M08 in combination with the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 replaces a MB91F467T microcontroller. For further details of the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 board please refer to the User Guide of the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001.

1.3   Functional Restrictions

1.3.1 Valid for EMA-MB91V460A-002B/-80/003 and EMA-MB91FV460B-001

This probe cable can only be used for the following Microcontroller configuration:

1. VDD5 = 5V, VDD35 = 3.3V, External bus enabled by software

The following Microcontroller configurations (2 & 3) are applicable with this probe cable, but it is recommended to use the appropriate MCU "NLS" probe cable!

2. VDD5 = 5V, VDD35 = 5V, External bus enabled by software

3. VDD5 = 3.3V, VDD35 = 3.3V, External bus enabled by software

While using this probe cable, the GPIO functionality on the external bus interface (VDD35 voltage domain) is restricted!

Unused external bus function pins (e.g. address lines) cannot be configured as general purpose in- or output randomly!

The following ports can be configured as permanent general purpose input OR output.

1. P07[0..7]

2. P06[0..7]

3. P05[0..7]

It is only possible to configure the whole port as input OR output!

Configuring each pin of these ports separately as input or output is not applicable!

For details on how to configure the port input and output direction please see chapter 3.4 Level-shifter direction control jumper!

2 Installation

Remove carefully the EMA-MB91F467T-LS-144M08 board from the shipping carton and check if there are any damages.

Please refer to the attached document "NQPACK/ YQPACK/ HQPACK Technical Information" for installation the socket adapter.
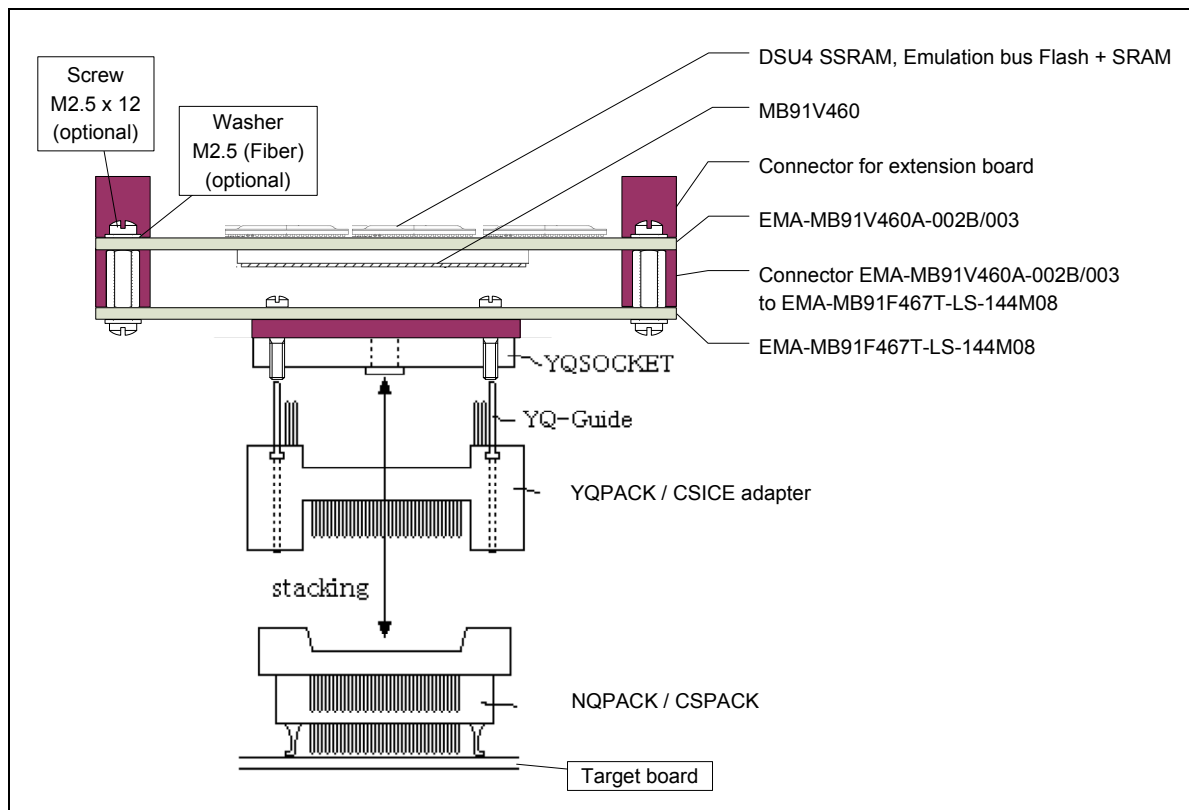

Figure 2-1: Installation

3 Switches and Jumpers

This chapter describes all switches and jumpers that can be modified or accessed on the EMA-MB91F467T-LS-144M08 board. The default setting is shown with a grey shaded area.

3.1 Level Shifter Switches and Jumpers overview

Jumper	Description/ Function	Type	Default
S400-1	DIR_U406	DIP-Switch	OFF
S400-2	DIR_U407	DIP-Switch	OFF
S400-3	DIR_U408	DIP-Switch	OFF
S400-4	P09_0 ⇐ CS0#	DIP-Switch	OFF
S400-5	P09_1 ⇐ CS1#	DIP-Switch	OFF
S400-6	P09_2 ⇐ CS2#	DIP-Switch	OFF
S400-7	P10_0 ⇐ SYSCLK	DIP-Switch	OFF
S400-8	P10_1 ⇐ AS#	DIP-Switch	OFF
S400-9	P10_3 ⇐ WE#	DIP-Switch	OFF
S400-10	P08_0 ⇐ WR0#	DIP-Switch	OFF
S401-1	CS select	DIP-Switch	OFF
S401-2		DIP-Switch	OFF
S401-3	reserved	DIP-Switch	OFF
S401-4		DIP-Switch	OFF
S401-5		DIP-Switch	OFF
S401-6		DIP-Switch	OFF
S401-7		DIP-Switch	OFF
S401-8	P08_7 ⇨ RDY	DIP-Switch	OFF
S401-9	P08_4 ⇐ RD#	DIP-Switch	OFF
S401-10	P08_1 ⇐ WR1	DIP-Switch	OFF
R400	P09_0 ⇨ CS0#	0603	Closed
R401	P09_1 ⇨ CS1#	0603	Closed
R402	P09_2 ⇨ CS2#	0603	Closed
R403	P10_0 ⇨ SYSCLK	0603	Closed
R404	P10_1 ⇨ AS#	0603	Closed
R405	P10_3 ⇨ WE#	0603	Closed
R406	P08_0 ⇨ WR0#	0603	Closed
R407	P08_1 ⇨ WR1#	0603	Closed
R408	P08_4 ⇨ RD#	0603	Closed
R410	P08_7 ⇐ RDY	0603	Closed

3.2 Level-shifter direction control jumper

Jumper	Setting	Description
S400-1 (Direction U406)	ON	Target board A[0..7] ⇨ MB91V460 A[0..7]
	OFF	Target board A[0..7] ⇦ MB91V460 A[0..7]
S400-2 (Direction U407)	ON	Target board A[8..15] ⇨ MB91V460 A[8..15]
	OFF	Target board A[8..15] ⇦ MB91V460 A[8..15]
S400-3 (Direction U408)	ON	Target board A[16..23] ⇨ MB91V460 A[16..23]
	OFF	Target board A[16..23] ⇦ MB91V460 A[16..23]

Default: S400-1, S400-2, S400-3: OFF

3.3 Bus control jumpers

3.3.1 WR0# (P08_0)

R406	S400-10	Description
Closed	OFF	P08_0 ⇨ WR0#
Open	ON	P08_0 ⇦ WR0#
Closed	ON	Prohibited

Default: R406: Closed, S400-10: OFF

3.3.2 WR1# (P08_1)

R407	S401-10	Description
Closed	OFF	P08_1 ⇨ WR1#
Open	ON	P08_1 ⇦ WR1#
Closed	ON	Prohibited

Default: R407: Closed, S401-10: OFF

3.3.3 RD# (P08_4)

R408	S401-9	Description
Closed	OFF	P08_4 ⇨ RD#
Open	ON	P08_4 ⇦ RD#
Closed	ON	Prohibited

Default: R408: Closed, S401-9: OFF

3.3.4 RDY (P08_7)

R410	S401-8	Description
Closed	OFF	P08_7 ⇦ RDY
Open	ON	P08_7 ⇨ RDY
Closed	ON	Prohibited

Default: R410: Closed, S401-8: OFF

3.3.5 CS0# (P09_0)

R400	S400-4	Description
Closed	OFF	P09_0 ⇨ CS0#
Open	ON	P09_0 ⇦ CS0#
Closed	ON	Prohibited

Default: R400: Closed, S400-4: OFF

3.3.6 CS1# (P09_1)

R401	S400-5	Description
Closed	OFF	P09_1 ⇨ CS1#
Open	ON	P09_1 ⇦ CS1#
Closed	ON	Prohibited

Default: R401: Closed, S400-5: OFF

3.3.7 CS2# (P09_2)

R402	S400-6	Description
Closed	OFF	P09_2 ⇨ CS2#
Open	ON	P09_2 ⇦ CS2#
Closed	ON	Prohibited

Default: R402: Closed, S400-6: OFF

3.3.8 SYSCLK (P10_0)

R403	S400-7	Description
Closed	OFF	P10_0 ⇨ SYSCLK
Open	ON	P10_0 ⇦ SYSCLK
Closed	ON	Prohibited

Default: R403: Closed, S400-7: OFF

3.3.9 AS# (P10_1)

R404	S400-8	Description
Closed	OFF	P10_1 ⇨ AS#
Open	ON	P10_1 ⇦ AS#
Closed	ON	Prohibited

Default: R404: Closed, S400-8: OFF

3.3.10 WE# (P10_3)

R405	S400-9	Description
Closed	OFF	P10_3 ⇨ WE#
Open	ON	P10_3 ⇦ WE#
Closed	ON	Prohibited

Default: R405: Closed, S400-9: OFF

3.3.11 CS select (CPLD)

S401_2	S401_1	Description
OFF	OFF	CS0# is selected
OFF	ON	CS1# is selected
ON	OFF	CS2# is selected
ON	ON	Do not set

Default: S401_1, S401_2: OFF

3.4 Port Jumpers

3.4.1 P35 ⇨ P29

Jumper	U100 pin	P 1-2 [PPMUX.PS5=1]	P 2-3 [PPMUX.PS5=0]	P 3-4 [PPMUX.PS5=1]
J238	110	P35_0	P29_0	P29_0 pulldown
J239	111	P35_1	P29_1	P29_1 pulldown
J240	112	P35_2	P29_2	P29_2 pulldown
J241	113	P35_3	P29_3	P29_3 pulldown
J242	114	P35_4	P29_4	P29_4 pulldown
J243	115	P35_5	P29_5	P29_5 pulldown

Default: all 1-2 and 3-4

3.4.2 P24 ⇨ P28

Jumper	U100 pin	P 1-2 [PPMUX.PS2=0] and [PPMUX.PR0=0]	P 2-3 [PPMUX.PS2=1] and [PPMUX.PR0=1]	P 3-4 [PPMUX.PS2=0] and [PPMUX.PR0=0]
J244	118	P24_0	P28_0	P28_0 pulldown
J245	119	P24_1	P28_1	P28_1 pulldown
J246	120	P24_2	P28_2	P28_2 pulldown
J247	121	P24_3	P28_3	P28_3 pulldown
J248	122	P24_4	P28_4	P28_4 pulldown
J249	123	P24_5	P28_5	P28_5 pulldown
J250	124	P24_6	P28_6	P28_6 pulldown
J251	125	P24_7	P28_7	P28_7 pulldown

Default: all 1-2 and 3-4

3.4.3 P16/P20 ⇨ P27

Jumper	U100 pin	P 1-2 [PPMUX.PS1=0] and NOT [PPMUX.PR(11..17)=1] and [PPMUX.PRPS0=1]	P 2-3 [PPMUX.PS1=1] and NOT [PPMUX.PR(11..17)=1] and [PPMUX.PRPS0=1]	P 3-4 [PPMUX.PS1=0] and NOT [PPMUX.PR(11..17)=1] and [PPMUX.PRPS0=1]
J252	128	P16_0	P27_0	P27_0 pulldown
J253	129	P16_1	P27_1	P27_1 pulldown
J254	130	P20_0	P27_2	P27_2 pulldown
J255	131	P20_1	P27_3	P27_3 pulldown
J256	132	P20_2	P27_4	P27_4 pulldown
J257	133	P20_4	P27_5	P27_5 pulldown
J258	134	P20_5	P27_6	P27_6 pulldown
J259	135	P20_6	P27_7	P27_7 pulldown

Default: all 1-2 and 3-4

3.5 Default Jumper Setting

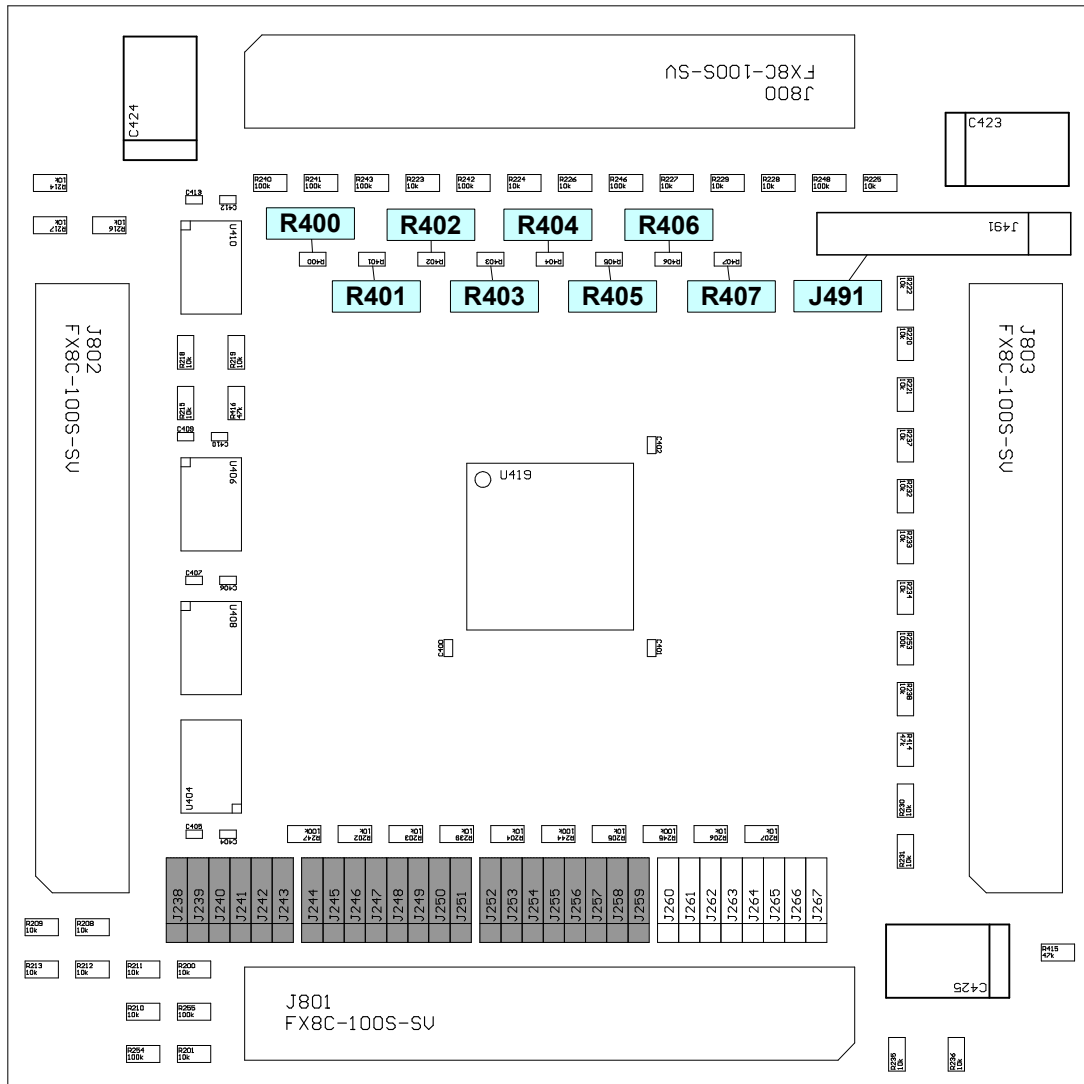The following jumper setting is the default setting.
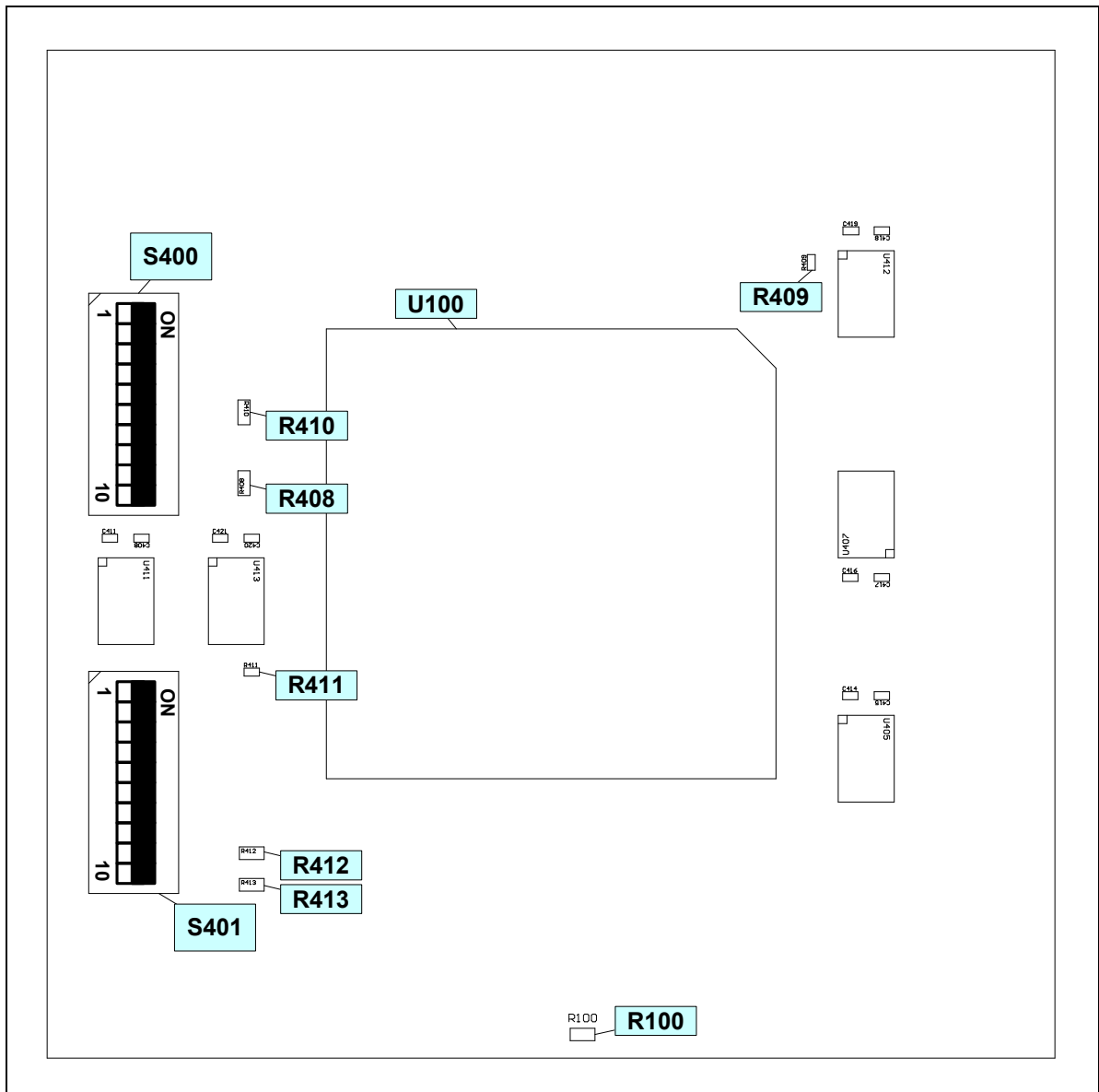

Figure 3-1: Jumper default setting, top

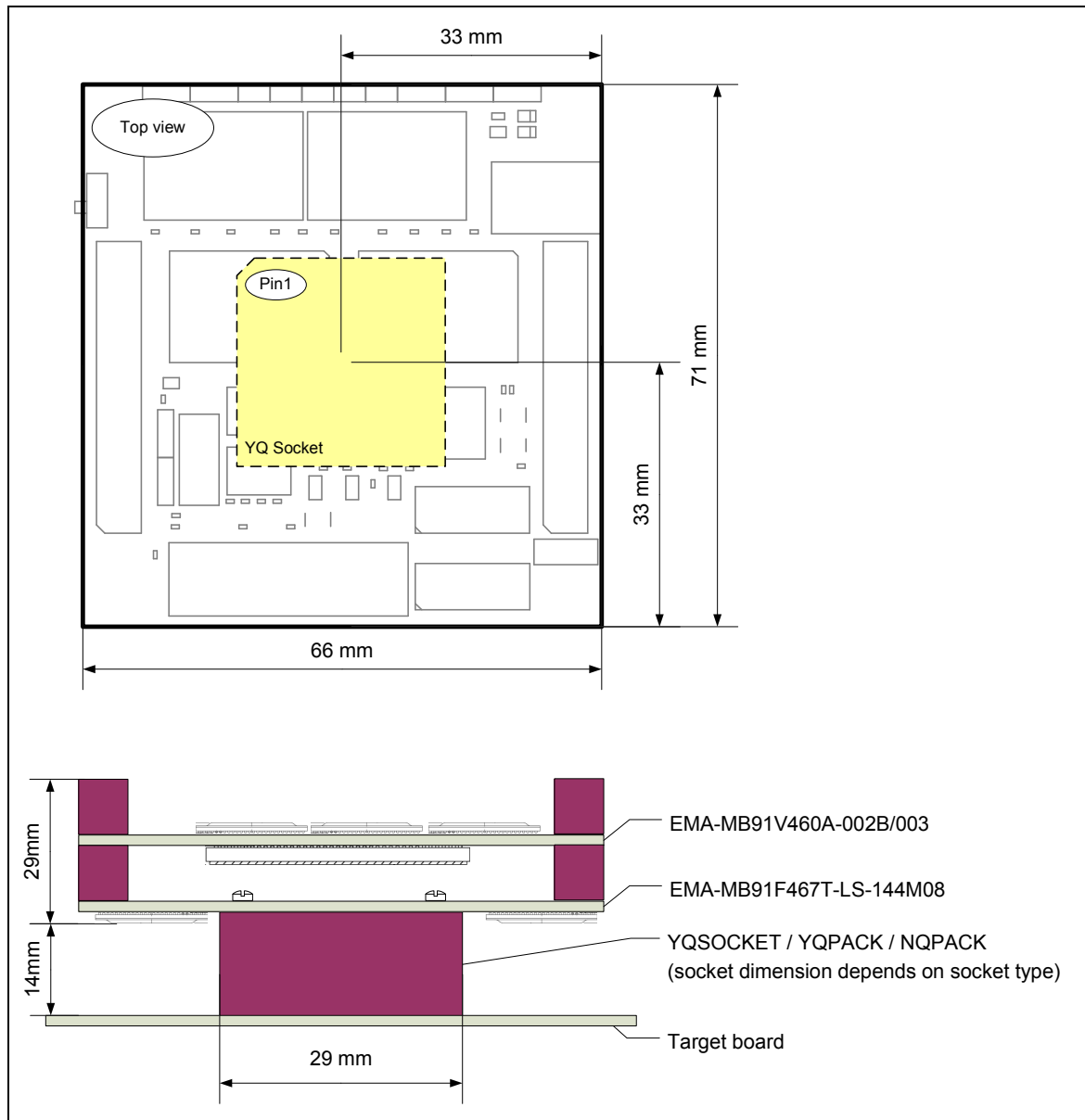Figure 3-2: Jumper location, bottom

4 Mechanical dimensions

Figure 4-1: Mechanical Dimensions

5 CPLD

The CPLD Xilinx XC9536XL-5VQL44C controls the direction of the data bus.

5.1 CPLD Verilog Code

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////
// Company:        Accemic GmbH & Co. KG
// Engineer:       RH / AW
//
// Create Date:    03/08/2007
// Design Name:    EMA-MB91F467T-LS-144M08
// Module Name:    F467T
// Project Name:
// Target Devices: XC9536XL-5VQ44
// Tool versions:  ISE 9.1
// Description:
//
// Dependencies:
//
// Revision:
// Revision              1.3
// Additional Comments:  none
//
// USERCODE:   7T13
//              ||||____ Subversion
//                |||_____ Version
//              ||_____ Target 467T
//                              **
//
//////////////////////////////////////////////////////////////////////////////

module EMA_MB91F467T_LS_144M08_V11_cpld_7T13(
ECSx,
CSx,                      // P09_7..P09_0
WRx,                      // P08_3..P08_0
RDx,                      // P08_4
ASx,                      // P10_1
BAAx,                     // P10_2
WEx,                      // P10_3
IORDx,                    // P11_0
IOWRx,                    // P11_1
S401,
DIR_U400,
DIR_U401,
DIR_U404,
DIR_U405,
OEx_U400_U401,
OEx_U404_U405);
```

```
input ECSx;
input[7:0] CSx;
input[3:0] WRx;
input RDx;
input ASx;
input BAAx;
input WEx;
input IORDx;
input IOWRx;
input[7:1] S401;
output DIR_U400;
output DIR_U401;
output DIR_U404;
output DIR_U405;
output OEx_U400_U401;
output OEx_U404_U405;

reg OEx_U400_U401, OEx_U404_U405;
reg DIR_U400, DIR_U401, DIR_U404, DIR_U405;

always @*
begin
      case (S401[2:1] ) // CS_MASK
            2'b11: // CS0
                        OEx_U404_U405 = !ECSx | (CSx[1] & CSx[2]);
            2'b10: // CS1
                        OEx_U404_U405 = !ECSx | (CSx[0] & CSx[2]);
            2'b01: // CS2
                        OEx_U404_U405 = !ECSx | (CSx[0] & CSx[1]);
            2'b00: // none masked
                        OEx_U404_U405 = !ECSx | (CSx[0] & CSx[1] & CSx[2]);
      endcase

      OEx_U400_U401 = 1;

      // check schematic for DIR level (different on LS boards)
      DIR_U400 = 1;
      DIR_U401 = 1;
      DIR_U404 = !RDx;
      DIR_U405 = !RDx;
end

endmodule
```

5.2   CPLD programming jumper (J491)

The CPLD is re-configurable by programming via J491. Please refer to www.xilinx.com for details and tools for Xilinx CPLD configuration.

J491 pin	Name
1	GND
2	TDO
3	TCK
4	TMS
5	TDI
6	VREF

6 Information in the WWW

Information about FUJITSU MICROELECTRONICS Products
can be found on the following Internet pages:

Microcontrollers (8-, 16- and 32bit), Graphics Controllers
Datasheets and Hardware Manuals, Support Tools (Hard- and Software)

> **http://www.fme.gsdc.de/gsdc.htm**

Linear Products: Power Management, A/D and D/A Converters

> **http://www.fujitsu.com/emea/services/microelectronics**

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> **http://www.fujitsu.com/emea/services/microelectronics/saw**

For more information about FUJITUS MICROELECTRONICS

> **http://www.fujitsu.com/emea/services/microelectronics**

7 Recycling

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Gemäß der Europäischen WEEE-Richtlinie und deren Umsetzung in landesspezifische Gesetze nehmen wir dieses Gerät wieder zurück.

Zur Entsorgung schicken Sie das Gerät bitte an die folgende Adresse:

Fujitsu Microelectronics Europe GmbH

Warehouse/Disposal

Monzastraße 4a

63225 Langen

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Fujitsu Microelectronics Europe GmbH

Warehouse/Disposal

Monzastraße 4a

63225 Langen