# MOSFET - Power, Single N-Channel, Source Down, WDFN9

## 25 V, 0.85 mΩ, 264 A

## NTTFSS1D1N02P1E

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 25 V | 0.85 mΩ @ 10 V | 264 A |
| | 1.05 mΩ @ 4.5 V | |

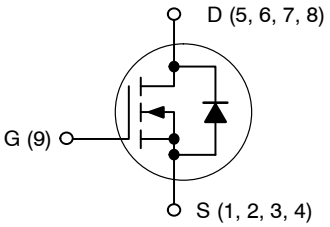
### Features

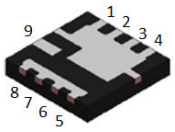
- Advanced Source−Down Package Technology (3.3x3.3mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Low $Q_G$ and Capacitance to Minimize Driving and Switching Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- DC−DC Switching Applications
- ORing Applications
- Power Load Switch
- Battery Management and Protection

NMOS




WDFN9
CASE 511EB

MARKING DIAGRAM


1D1N2 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

### MAXIMUM RATINGS ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 25 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±16 | V |
| Continuous Drain Current $R_{\theta JC}$ (Note 2) | Steady State | $T_C$ = 25°C | $I_D$ | 264 | A |
| | | $T_C$ = 85°C | | 189 | |
| Power Dissipation $R_{\theta JC}$ (Note 2) | | $T_C$ = 25°C | $P_D$ | 89 | W |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A$ = 25°C | $I_D$ | 39 | A |
| | | $T_A$ = 85°C | | 28 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | | $T_A$ = 25°C | $P_D$ | 2 | W |
| Pulsed Drain Current | $T_A$ = 25°C, $t_p$ = 10 μs | | $I_{DM}$ | 900 | A |
| Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 63 A, L = 0.1 mH) | | | $E_{AS}$ | 173 | mJ |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 1 $in^2$ pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are valid for the particular conditions noted.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

## THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction−to−Case − Steady State (Note 1) | $R_{\theta JC}$ | 1.4 | °C/W |
| Junction−to−Ambient − Steady State (Note 1, 2) | $R_{\theta JA}$ | 60 | |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 25 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D$ = 250 μA, ref to 25°C | | | 12.8 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 20 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 125°C | | | 100 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = 16 V | | | | 100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 934 μA | | 1.2 | | 2.0 | V |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | $I_D$ = 934 μA, ref to 25°C | | | −4.9 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 27 A | | 0.70 | 0.85 | mΩ |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 27 A | | 0.83 | 1.05 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 3 V, $I_D$ = 27 A | | | 146 | | S |
| Gate Resistance | $R_G$ | $T_A$ = 25°C | | | 0.8 | | Ω |
| **CHARGES & CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 13 V, f = 1 MHz | | | 4360 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 1150 | | |
| Reverse Capacitance | $C_{RSS}$ | | | | 80 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 13 V; $I_D$ = 27 A | | | 60 | | nC |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 13 V; $I_D$ = 27 A | | | 26.3 | | |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 6.2 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 4.0 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 10.8 | | |
| **SWITCHING CHARACTERISTICS, $V_{GS}$ = 10 V** (Note 3) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 10 V, $V_{DD}$ = 13 V, $I_D$ = 30 A, $R_G$ = 3 Ω | | | 10.8 | | ns |
| Rise Time | $t_r$ | | | | 3.4 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 34.7 | | |
| Fall Time | $t_f$ | | | | 5.1 | | |
| **SOURCE−TO−DRAIN DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 27 A | $T_J$ = 25°C | | 0.76 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.63 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, dI/dt = 100 A/μs, $I_S$ = 27 A | | | 45 | | ns |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 40 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

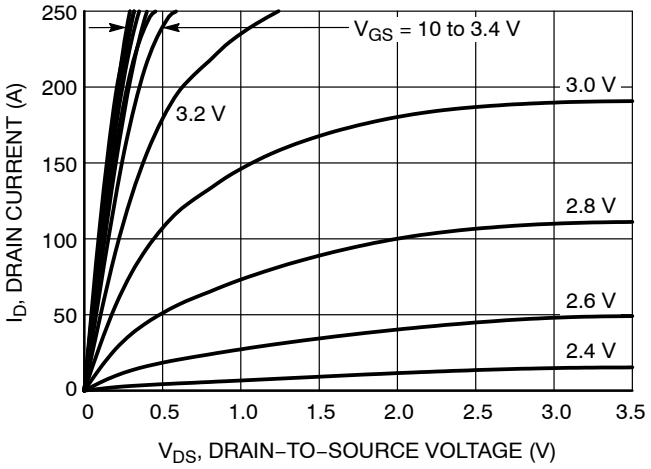



**Figure 1. On−Region Characteristics**

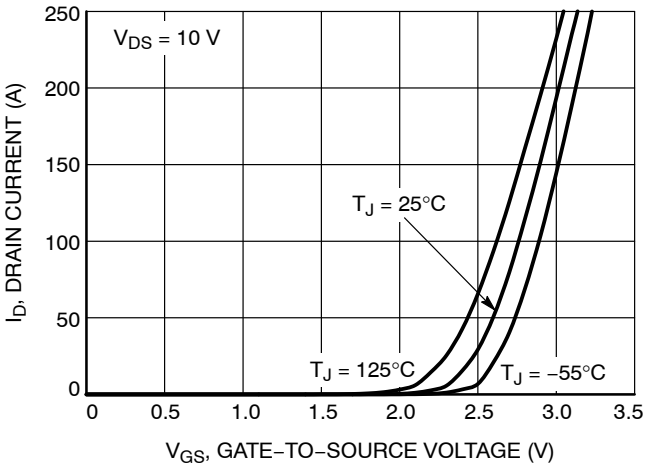



**Figure 2. Transfer Characteristics**

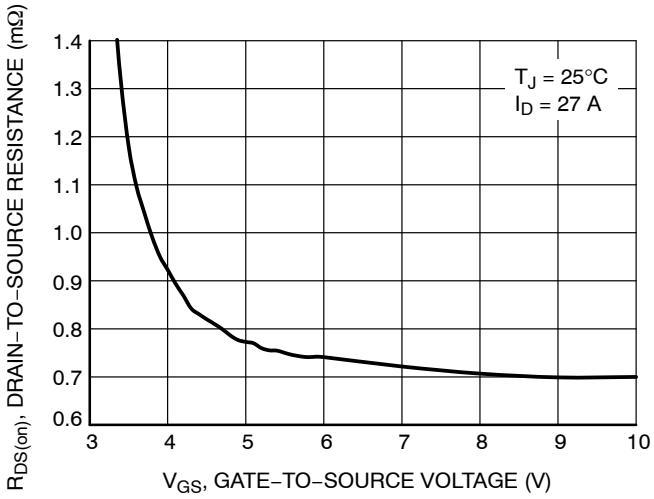



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

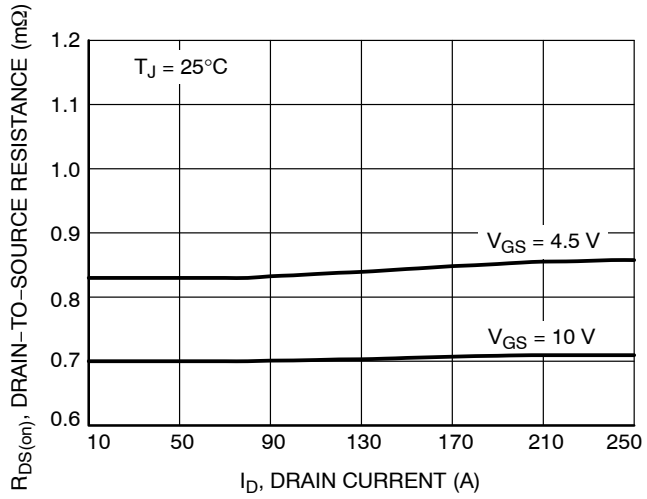



**Figure 4. On−Resistance vs. Drain Current**

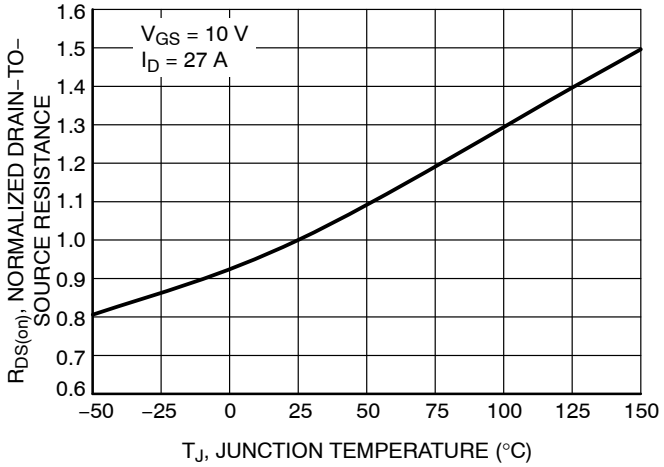



**Figure 5. On−Resistance Variation with Temperature**

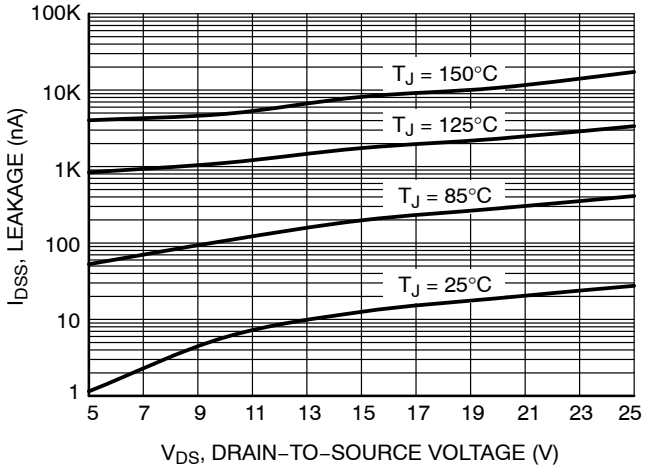



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS

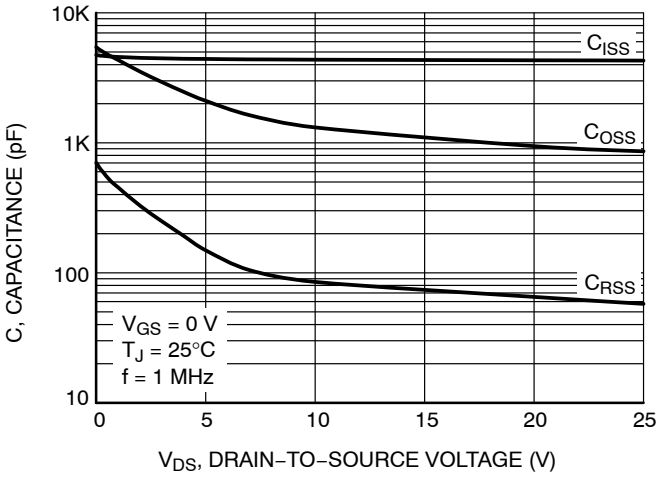



**Figure 7. Capacitance Variation**

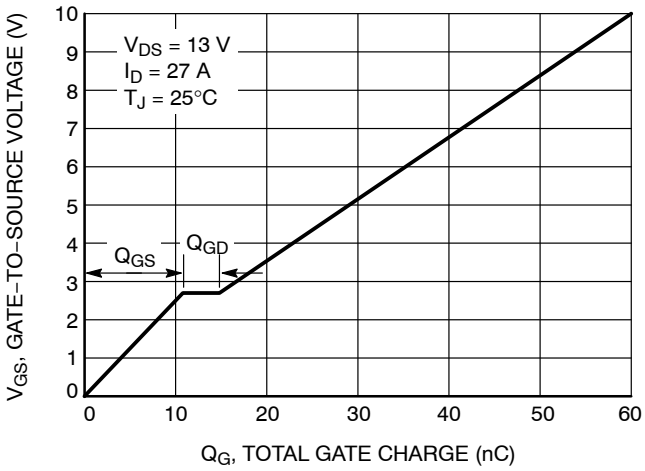



**Figure 8. Gate−to−Source Voltage vs. Total Charge**

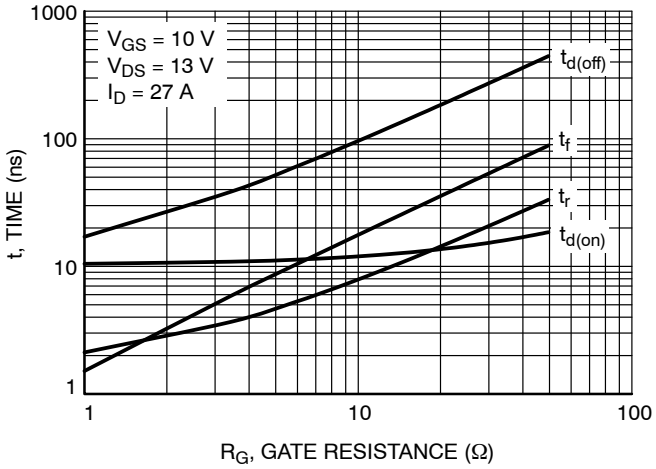



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

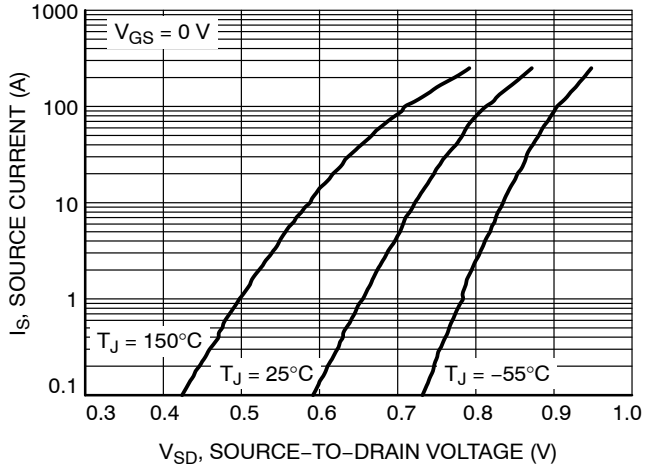



**Figure 10. Diode Forward Voltage vs. Current**

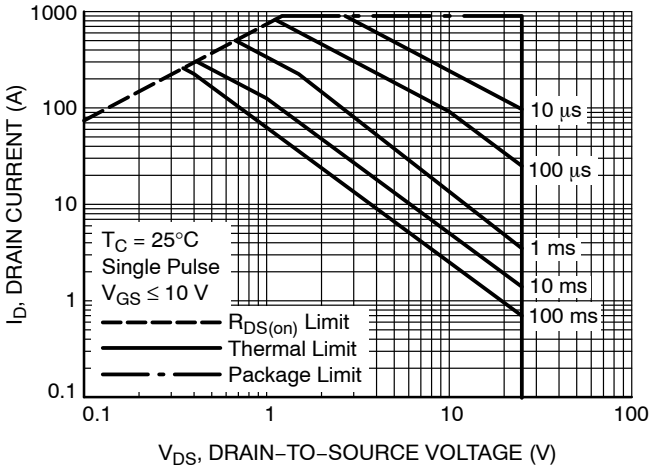



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

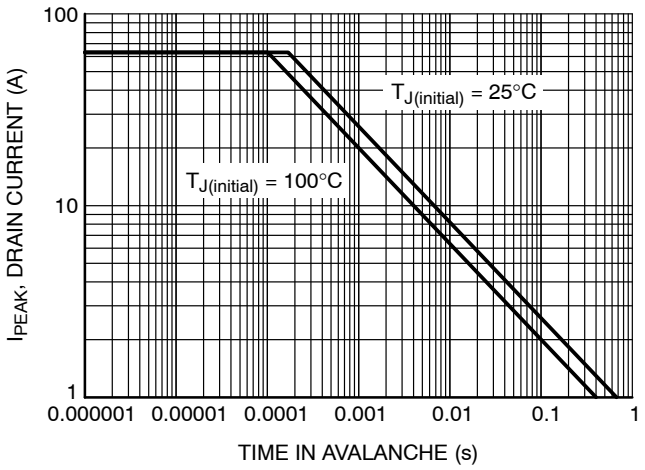



**Figure 12. Maximum Drain Current vs. Time in Avalanche**

## TYPICAL CHARACTERISTICS

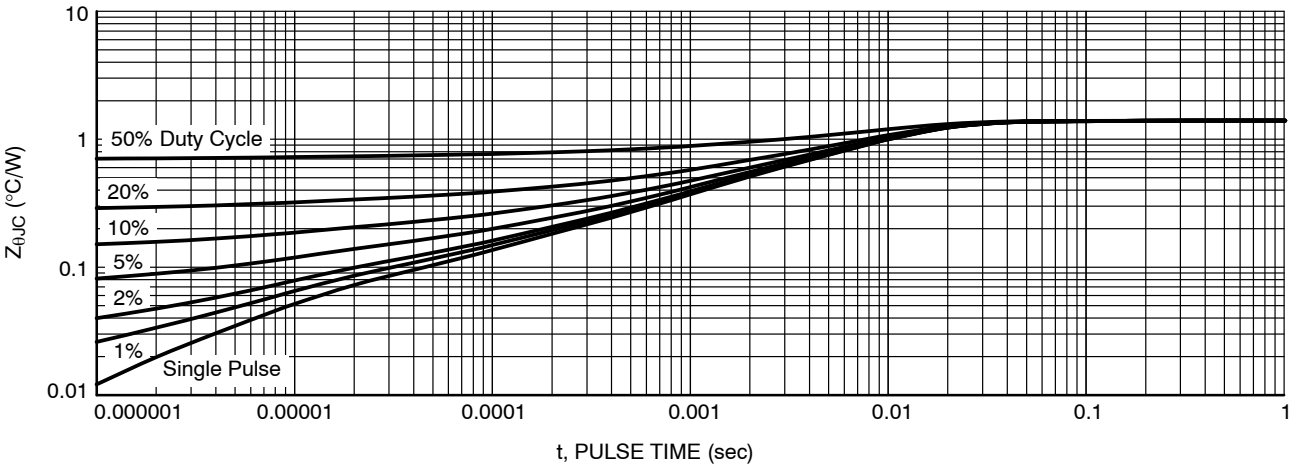



**Figure 13. Junction−to−Case Transient Thermal Response**

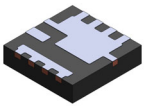
### ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| NTTFSS1D1N02P1E | 1D1N2 | WDFN9<br>(Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

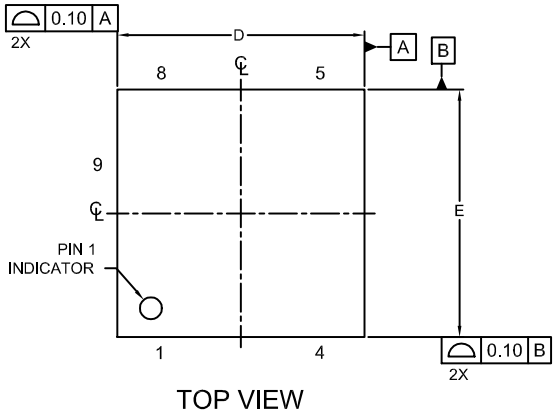
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

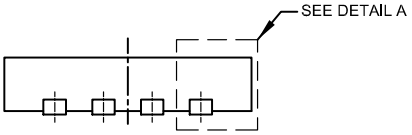


**WDFN9 3.3x3.3, 0.65P**
CASE 511EB
ISSUE B

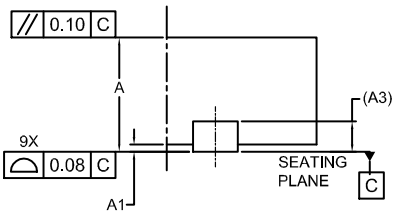
DATE 21 JUL 2021




TOP VIEW



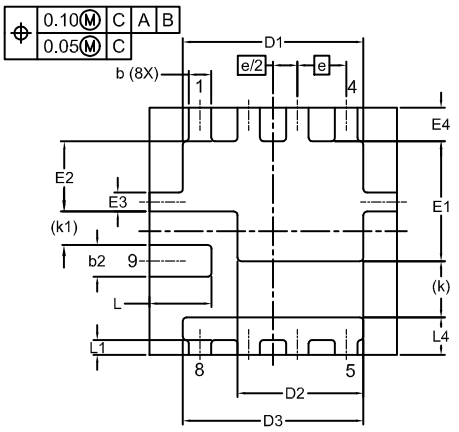

FRONT VIEW



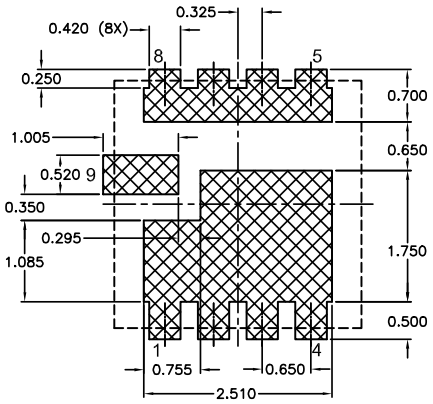

DETAIL A
SCALE: 2:1

NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

| UNIT IN MILLIMETER | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.25 | 0.30 | 0.35 |
| b2 | 0.37 | 0.42 | 0.47 |
| D | 3.20 | 3.30 | 3.40 |
| D1 | 2.31 | 2.41 | 2.51 |
| D2 | 1.58 | 1.68 | 1.78 |
| D3 | 2.31 | 2.41 | 2.51 |
| E | 3.20 | 3.30 | 3.40 |
| E1 | 1.50 | 1.60 | 1.70 |
| E2 | 0.84 | 0.94 | 1.04 |
| E3 | 0.20 | 0.25 | 0.30 |
| E4 | 0.35 | 0.45 | 0.55 |
| e | | 0.650 BSC | |
| e/2 | | 0.325 BSC | |
| k | | 0.75 REF | |
| k1 | | 0.45 REF | |
| L | 0.73 | 0.83 | 0.93 |
| L1 | 0.10 | 0.20 | 0.30 |
| L4 | 0.40 | 0.50 | 0.60 |




BOTTOM VIEW




LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **WDFN9 3.3x3.3, 0.65P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
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