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APPLICATION NOTE 1748

VFD Grid/Anode Supply Using MAX6850-MAX6853 PUMP Output

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Abstract: This note describes how to use the PUMP clock output of the MAX6850, MAX6851, MAX6852, or MAX6853 vacuum fluorescent display controllers to construct a low-cost boost converter. The dc-dc converter generates the high-voltage grid supply anode supply for the VFD tube from the 3.3V supply used by the MAX6850-3 display controller.

This application note discusses how to use the MAX6850, MAX6851, MAX6852, and MAX6853 vacuum fluorescent display (VFD) controllers' PUMP clock output to build a minimal cost boost converter to generate the high voltage grid/anode driver supply from a convenient lower voltage.

The PUMP output is one of five general logic outputs available on the MAX6850–MAX6853 VFD controllers. All these logic outputs have additional special functions; in the case of PUMP, the output can be configured as a nominally 80kHz clock output. The PUMP clock frequency is actually OSC/50, where OSC is the multiplex clock frequency set up using the MAX6850–MAX6853 OSC1 and OSC2 pins. OSC may be set up using an internal RC oscillator, or an external clock may be used. Either way, the allowed range is 2MHz to 8MHz. The nominal OSC frequency is 4MHz, setting the PUMP frequency to 80kHz.

The converter topology discussed here is a discontinuous boost with fixed on time and 'bang-bang' regulation. The circuit works by ramping up the current through an inductor L1 for the first half cycle of each PUMP clock, when PUMP is high, and dumping the stored energy into the output capacitor C2 during the second half cycle of PUMP, when PUMP is low (**Figures 1** and **2**).
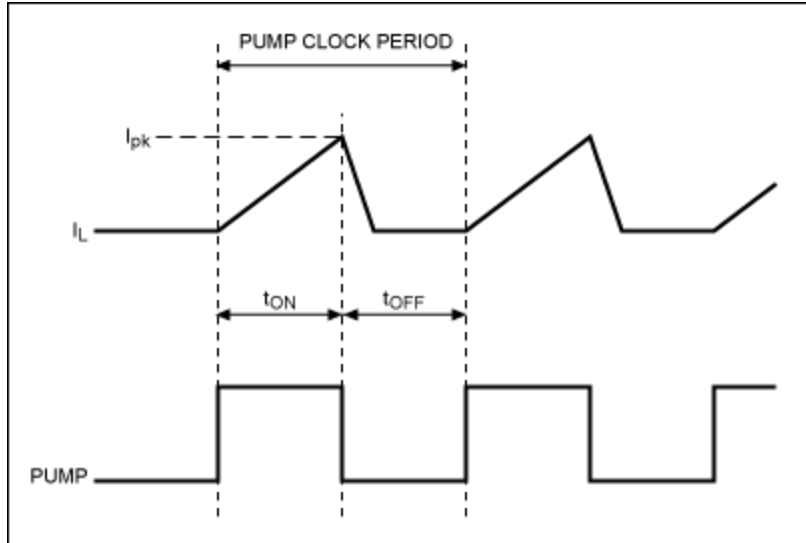
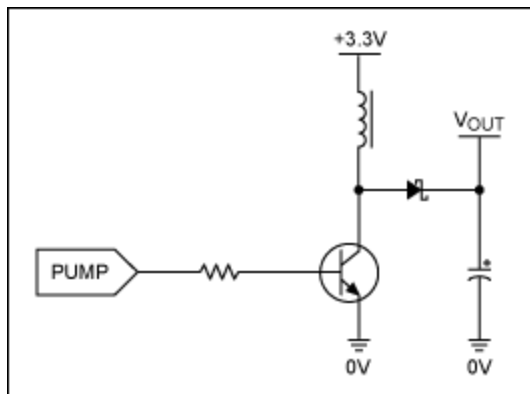Figure 1. Using PUMP output as boost switch driver.

Figure 2. Basic boost converter topology.

Without any feedback, the output voltage of the basic boost circuit shown in Figure 2 will vary with both input voltage and load. With the output unloaded, the output voltage would keep rising with every power cycle, because the inductor stored energy is always being dumped into the output capacitor. A simple regulation technique can detect that the output is above a desired voltage. Further power cycles are then prevented until the converter output voltage, held up by the output capacitor, drops. This is often called bang-bang regulation, and involves gating the conversion clock (PUMP in this case) to allow conversion cycles only when the output is out of regulation.

Figure 3 shows an implementation of a low cost boost converter with feedback. To understand the circuit operation, first consider the start of the cycle when PUMP is rising. Presume for the moment that the circuit is out of regulation and Q2 is off. As PUMP rises, Q1 turns on as a switch, and current starts to ramp up through L1. Half a PUMP clock cycle later, PUMP falls and Q1 turns off. L1 current has meanwhile ramped up to a value I_{pk}, and this current now flows through diode D1 into the output capacitor C2 and any load that is present. If the output voltage is high enough to turn on zener diode D2, then current will flow through D2 and R2. As the output voltage rises above this threshold, eventually Q2 will turn on, clamping the base-emitter of Q1, preventing Q1 from turning on when PUMP next goes high. Otherwise, R3 ensures Q2 stays off, Q1 turns on again and the conversion repeats. C4 provides a small delay to the detection to reduce the chatter as the Q2 switches on and off to maintain regulation.
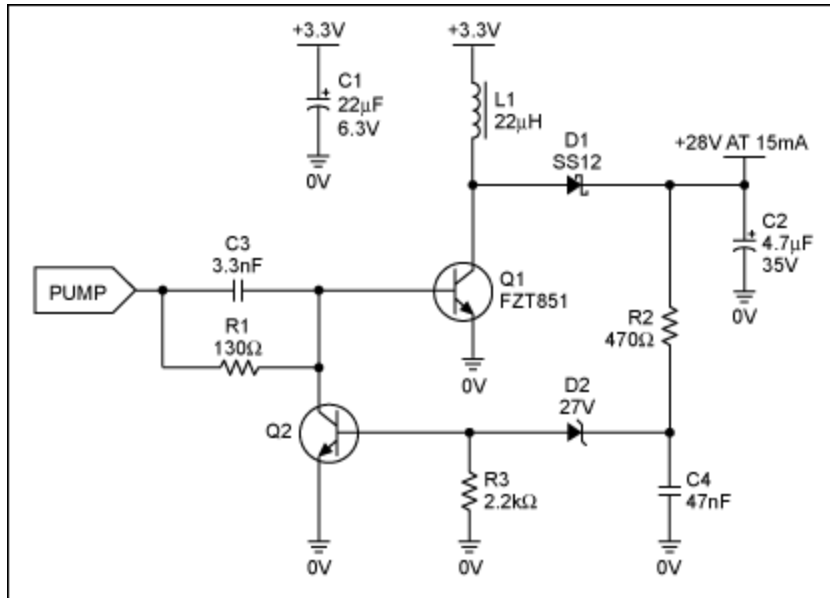
Figure 3. One transistor feedback control.

The simple circuit of Figure 3 can be improved by adding hysteresis to the output voltage detection. Hysteresis ensures that Q2 is always hard on or off. Without hysteresis, Q2 can turn partly on at the regulation threshold, bleeding some of the base current from Q1. When this happens Q1 may not saturate as hard, reducing efficiency. Hysteresis can be achieved by adding a two transistor Schmitt trigger, as shown in **Figure 4**. The Schmitt trigger adds about 0.25V hysteresis to the detection threshold. The Schmitt trigger output at the collector of Q4 switches between 3.3V and 0.9V, so D3 and R7 are required to ensure Q2 turns off.
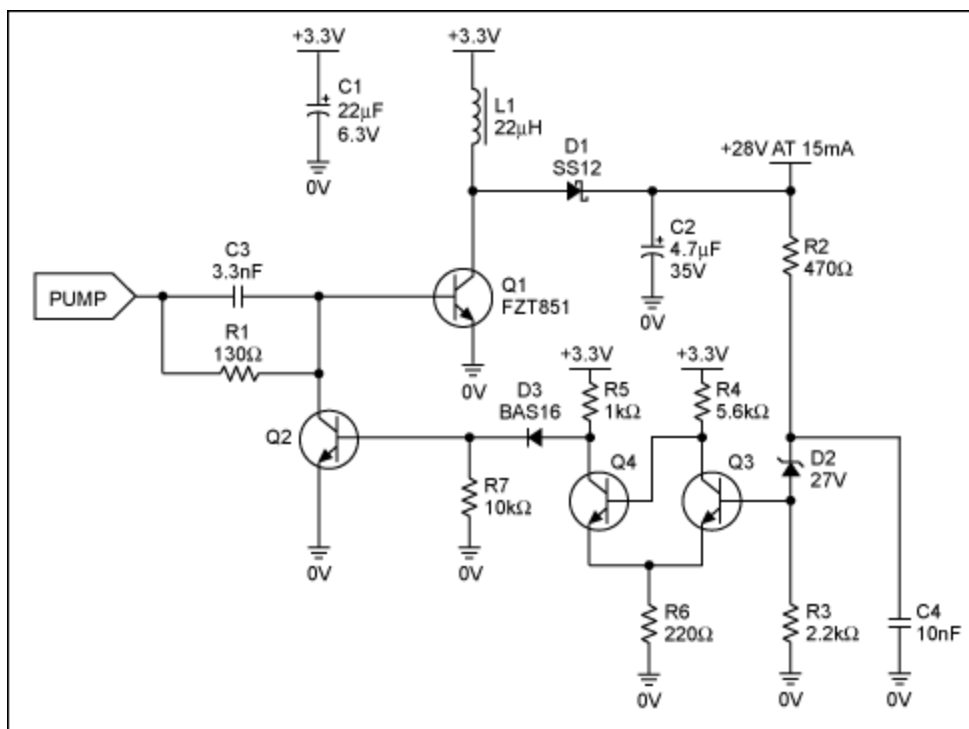

Figure 4. Schmitt tigger feedback control.

An easy way to select component values for the power path is to work with power. The converter must be capable of transferring enough power to maintain the output voltage at the output load current, from the minimum input supply voltage. Let's define some parameters:

$V_{IN}(min)$ = Minimum input supply voltage
V_{SW} = Voltage drop across Q1 switch transistor
$V_{IN}(max)$ = Maximum input supply voltage
P_{IN} = Input supply power at rated output load
$I_{IN}(avg)$ = Input average current
V_{OUT} = Output supply voltage
I_{OUT} = Output maximum load current
P_{OUT} = Output maximum load power
V_{RIPPLE} = Output supply voltage ripple due to inductor dumping its power into the output capacitor
V_{DROOP} = Output supply voltage droop due load drawing current from the output capacitor
Eff = Expected power conversion efficiency (power path only—Q1 base current not included)
L = Inductance of L1
I_{pk} = Peak inductor current
f_{PUMP} = PUMP frequency
t_{ON} = Converter power switch on time

Now we derive some equations for this architecture (final equations are in bold):

$$P_{OUT} = V_{OUT} \times I_{OUT} \hspace{3cm} \text{Eq. 01}$$

Since the PUMP duty cycle is 50:50

$$t_{ON} = 1/(2 \times f_{PUMP}) \hspace{3cm} \text{Eq. 02}$$

Output power comes from the energy stored in the inductor

$$P_{OUT} = 0.5 \times L \times (I_{pk})^2 \times f_{PUMP} \hspace{2cm} \text{Eq. 03}$$

Since inductor current ramps from 0 to I_{pk} during half the f_{PUMP} period

$$I_{IN}(avg) = I_{pk}/4 \hspace{3cm} \text{Eq. 04}$$

Equations for input and output powers:

$$P_{OUT} = Eff \times P_{IN} \hspace{3cm} \text{Eq. 05}$$

$$P_{OUT} = V_{OUT} \times I_{OUT} \hspace{3cm} \text{Eq. 06}$$

$$P_{IN} = V_{IN} \times I_{IN}(avg) \hspace{3cm} \text{Eq. 07}$$

Which gives us the equation for I_{pk}:

$$\mathbf{I_{pk} = (V_{OUT} \times I_{OUT} \times 4)/(Eff \times V_{IN}(min))} \hspace{1cm} \textbf{Eq. 08}$$

From I_{pk} we can calculate that maximum value of L:

$$L(max) = (V_{IN}(min) - V_{SW}) \times t_{ON}/I_{pk} \qquad \text{Eq. 09}$$

Including Eq. 04 gives us

$$L(max) = (V_{IN}(min) - V_{SW})/(2 \times f_{PUMP} \times I_{pk}) \qquad \textbf{Eq. 10}$$

The chosen value for L gives us a maximum value for I_{pk} at maximum input supply voltage. The L1, Q1, and D1 must be rated for this peak current:

$$I_{pk}(max) = (V_{IN}(max) - V_{SW})/(2 \times f_{PUMP} \times L) \qquad \textbf{Eq. 11}$$

We also need to consider output ripple voltage across capacitor C2. An estimate for ripple voltage is obtained by presuming all the inductor energy gets dumped into C2.

$$1/2 \times C2 \times (V_{OUT} + V_{RIPPLE})^2 = (1/2 \times C2 \times V_{OUT}^2) + 1/2 \times L1 \times I_{pk}^2 \qquad \text{Eq. 12}$$

This reduces to:

$$V_{RIPPLE} = (V_{OUT}^2 + (I_{pk}^2 \times L1/C2))^{1/2} - V_{OUT} \qquad \textbf{Eq. 13}$$

The voltage across capacitor C2 also droops due to the load. A estimate for droop voltage is obtained by presuming that the output voltage decays from V_{OUT} for a whole cycle of f_{PUMP} before being restored to V_{OUT} again. From $Q = C \times V = I \times t$, we get:

$$V_{DROOP} = I_{OUT}/C2/f_{PUMP} \qquad \textbf{Eq. 14}$$

For a worked example, consider a requirement for 28V at 15mA generated from a 3.3V ±0.3V input supply. From Eq. 08:

$$I_{pk} = (28 \times 0.015 \times 4)/(0.8 \times 3) \text{ using an estimated 80\% power conversion efficiency}$$

So:

$$I_{pk} = 0.7A$$

From Eq. 10:

$$L(max) = (3 - 0.3)/(2 \times 80000 \times 0.7) \text{ using an estimated 300mV Q1 transistor saturation voltage}$$

So:

$$L(max) = 24.1\mu H$$

We choose **L = 22µH**

From Eq. 11:

$$I_{pk}(max) = (3.6 - 0.3)/(2 \times 80000 \times 22 \times 10^{-6})$$

So:

$I_{pk} = 0.94A$

L1, Q1, and D1 must be rated at 0.94A peak.

We choose Zetex FZT851 NPN transistor for Q1. This transistor has a maximum over temperature $V_{CE(sat)}$ figure of 300mV at $I_C = 1A$, confirming our estimate for V_{SW}. h_{FE} at 1A collector current is 100 minimum. Presuming the MAX6850–MAX6853 VFD controller is operating from 3.3V ±10%, we want a base current of 0.94/70 = 13.4mA, where 70 is our design value for h_{FE} to ensure saturation. The PUMP output rises to 200mV under this 13.4mA load (from the V_{OL} vs I_{SINK} typical operating characteristic in MAX6850–MAX6853 data sheets). We can now calculate a value for R1 = (3.0 - 0.9 - 0.2)/0.0134 = 130Ω where 0.9 is the $V_{BE(sat)}$ for the FZT851 under these operating conditions.

A logic level NMOS FET could be used instead of the NPN transistor. However, it is difficult to source 3V logic level power FETs with VDS ratings of 30V or more.

Now we consider the output capacitor C2:

From Eq. 13:

$V_{RIPPLE} = (28^2 + (0.94^2 \times 22/4.7))^{1/2}$ - 28 using a trial value of 4.7µF for C2.
$V_{RIPPLE} = 36mV$

From Eq. 14:

$V_{DROOP} = 0.015/(4.7 \times 10^{-6})/80000$ again using the trial value of 4.7µF for C2.
$V_{DROOP} = 40mV$

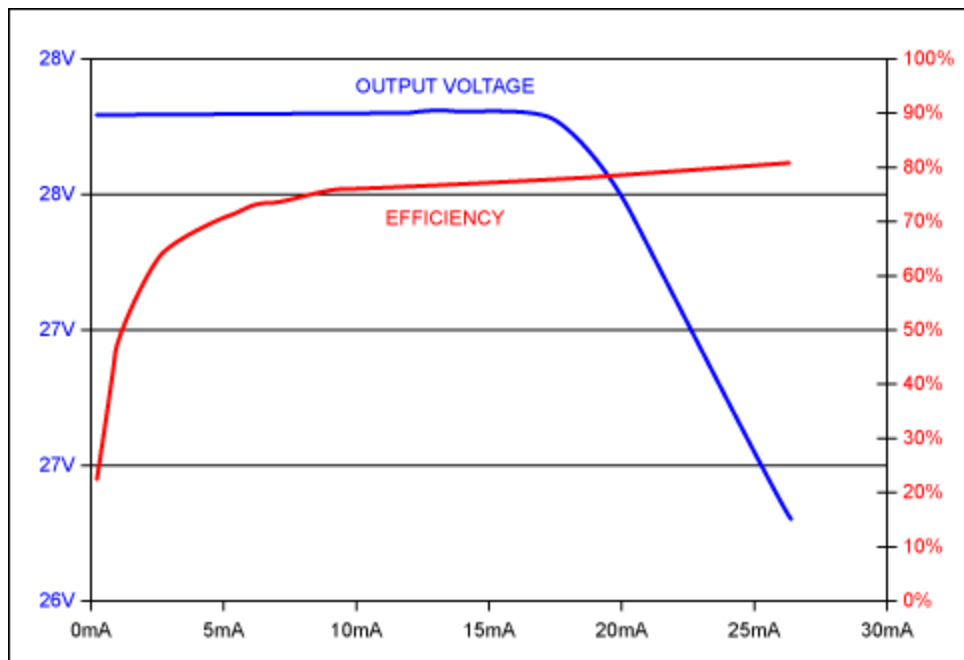The combined ripple and noise is less than 100mV. This is less than the 250mV Schmitt hysteresis, so it is acceptable.

Figure 5. Regulation and efficiency curves for the circuit of Figure 4.

Related Parts

MAX6850	4-Wire Interfaced, 7-, 14-, and 16-Segment Alphanumeric Vacuum-Fluorescent Display Controller
MAX6851	2-Wire Interfaced, 7-, 14-, and 16-Segment Alphanumeric Vacuum-Fluorescent Display Controller
MAX6852	4-Wire Interfaced, 5 x 7 Matrix Vacuum-Fluorescent Display Controller
MAX6853	2-Wire Interfaced, 5 x 7 Matrix Vacuum-Fluorescent Display Controller

More Information

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