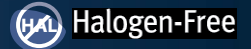
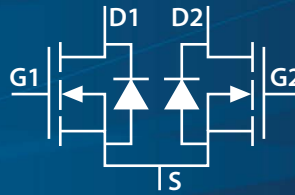


EPC2221 – Automotive 100 V (D-S) Enhancement Mode Power Transistor

$R_{DS(on)}$, 58 mΩ max

I_D , 5 A

AEC-Q101



The EPC2221 is a common source dual eGaN FET suitable for multi-channel lidar applications up to 20 Apk per channel. The low inductance and capacitance allow fast switching (100 MHz) and narrow pulse widths (2 ns) for high resolution and high efficiency. Additionally, the ultra-small size reduces PCB cost and total solution size. Gallium nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

APPLICATION NOTES:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)

- Top of FET is electrically connected to source

- Questions: [Ask a GaN Expert](#)



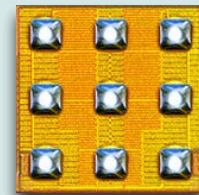
| Maximum Ratings | | | |
|-----------------|---|------------|------|
| PARAMETER | | VALUE | UNIT |
| V_{DS} | Drain-to-Source Voltage (Continuous) | 100 | V |
| | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C) | 120 | |
| I_D | Continuous ($T_A = 25^\circ\text{C}$) | 5 | A |
| | Pulsed (25°C, $T_{PULSE} = 300 \mu\text{s}$) | 20 | |
| V_{GS} | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| T_J | Operating Temperature | -40 to 150 | °C |
| T_{STG} | Storage Temperature | -40 to 150 | |

| Thermal Characteristics* | | | |
|--------------------------|--|-----|------|
| PARAMETER | | TYP | UNIT |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Case TOP) | 2.2 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board (Case BOTTOM) | 8.7 | |
| $R_{\theta JA_JEDEC}$ | Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB) | 99 | |
| $R_{\theta JA_EVB}$ | Thermal Resistance, Junction-to-Ambient (using EPC99012 EVB) | 55 | |

* Thermal resistances are calculated based on the total power dissipated by the two FETs. For example, if power P is simultaneously dissipated in each FET, then the total power dissipated is 2P and the maximum junction temperature is $T_A + R_{TH} \cdot 2P$.

| Static Characteristics# ($T_J = 25^\circ\text{C}$ unless otherwise stated) | | | | | | |
|---|---------------------------------|---|-----|-------|-----|---------------|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| BV_{DSS} | Drain-to-Source Voltage | $V_{GS} = 0 \text{ V}, I_D = 70 \mu\text{A}$ | 100 | | | V |
| I_{DSS} | Drain-Source Leakage | $V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$ | | 3 | 70 | μA |
| I_{GSS} | Gate-to-Source Forward Leakage | $V_{GS} = 6 \text{ V}$ | | 0.003 | 1 | mA |
| | Gate-to-Source Forward Leakage# | $V_{GS} = 6 \text{ V}, T_J = 125^\circ\text{C}$ | | 0.1 | 2 | mA |
| | Gate-to-Source Reverse Leakage | $V_{GS} = -4 \text{ V}$ | | 3 | 70 | μA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 0.7 \text{ mA}$ | 0.7 | 1.2 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS} = 5 \text{ V}, I_D = 4 \text{ A}$ | | 40 | 58 | mΩ |
| V_{SD} | Source-Drain Forward Voltage# | $I_S = 0.5 \text{ A}, V_{GS} = 0 \text{ V}$ | | 1.5 | | V |

Defined by design. Not subject to production test.



EPC2221 eGaN® FETs are supplied only in passivated die form with solder bumps

Die Size: 1.35 x 1.35 mm

Features

- Dual eGaN FET, Common Source
- Low Capacitance, Low Inductance
- Ultra-Fast Switching
- Narrow Pulse-Width Capability

Applications

- Automotive Lidar/ToF
- High-frequency DC-DC
- Wireless Power

Benefits

- High Resolution and Efficiency in Lidar Applications
- Ultra-Small footprint
- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G



Dynamic Characteristics* ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|---|---|-----|------|-----|----------|
| C_{ISS} | Input Capacitance | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$ | | 94 | 150 | pF |
| C_{RSS} | Reverse Transfer Capacitance | | | 0.9 | | |
| C_{OSS} | Output Capacitance | | | 63 | 72 | |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 1) | $V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$ | | 74 | | pF |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 2) | | | 93 | | |
| R_G | Gate Resistance | | | 1.0 | | Ω |
| Q_G | Total Gate Charge | $V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 4\text{ A}$ | | 0.85 | 1.2 | nC |
| Q_{GS} | Gate to Source Charge | $V_{DS} = 50\text{ V}, I_D = 4\text{ A}$ | | 0.27 | | |
| Q_{GD} | Gate to Drain Charge | | | 0.19 | | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | | 0.19 | | |
| Q_{OSS} | Output Charge | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$ | | 4.7 | 5.6 | |
| Q_{RR} | Source-Drain Recovery Charge | | | 0 | | |

Defined by design. Not subject to production test.

Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Figure 1: Typical Output Characteristics at 25°C

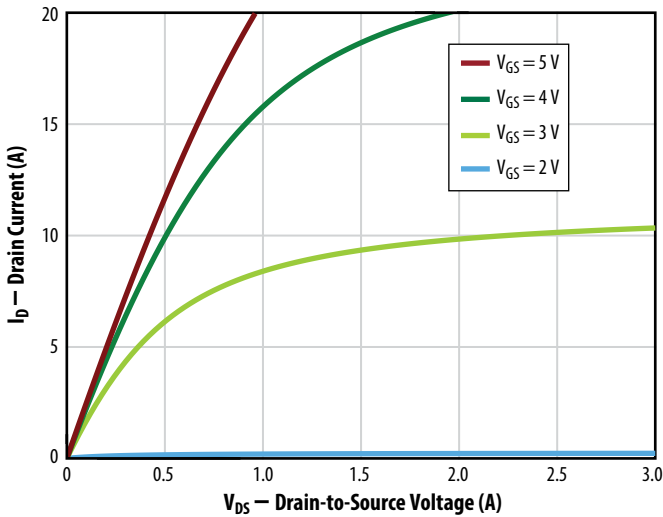


Figure 2: Transfer Characteristics

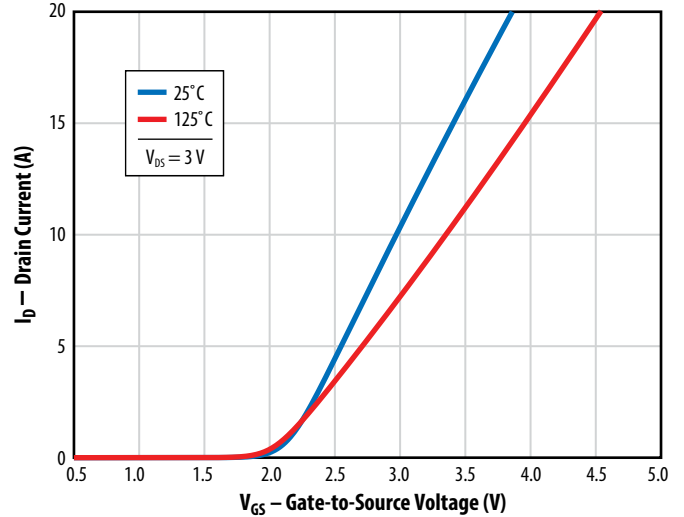


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

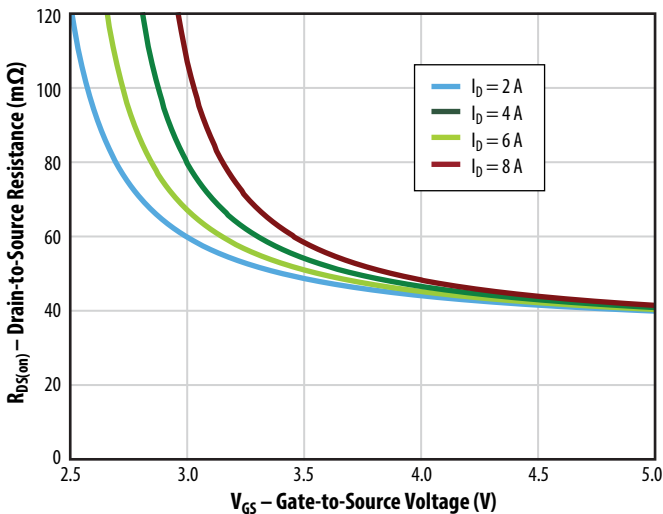


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

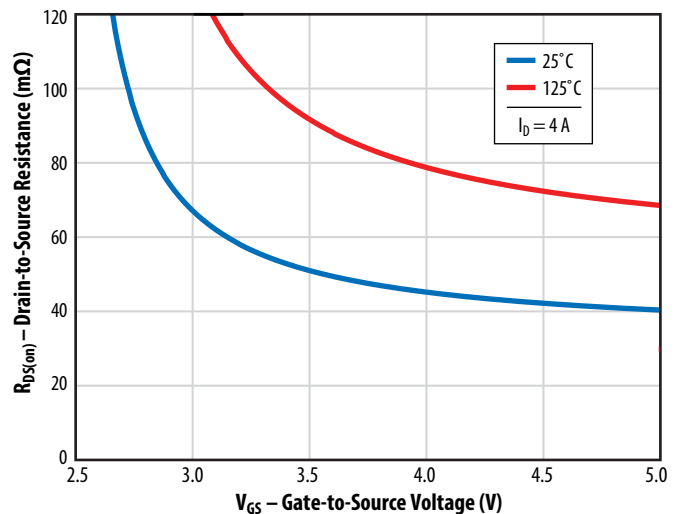


Figure 5a: Capacitance (Linear Scale)

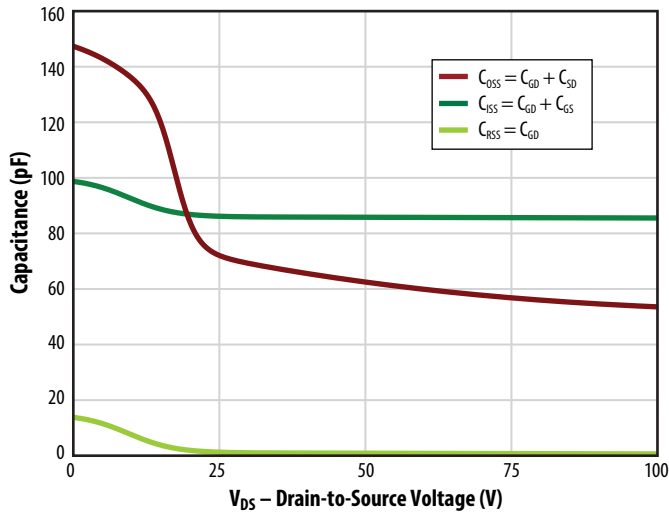


Figure 5b: Capacitance (Log Scale)

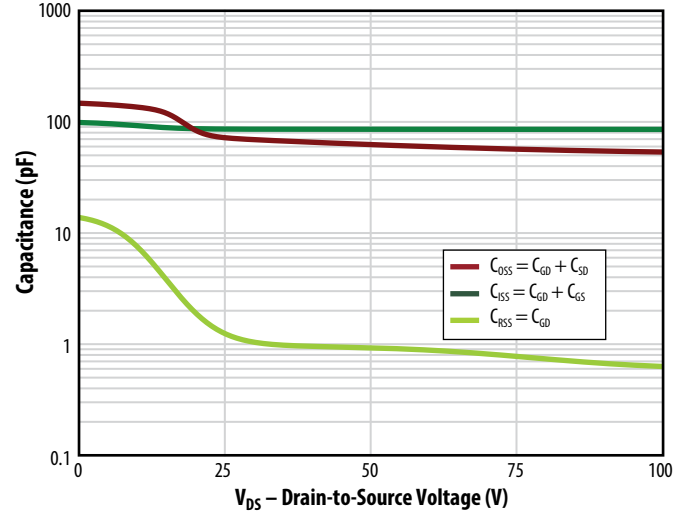


Figure 6: Output Charge and C_{OSS} Stored Energy

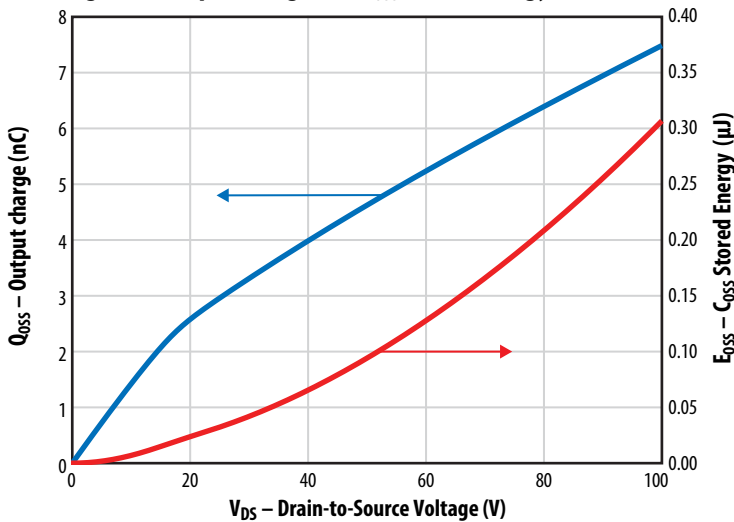


Figure 7: Typical Gate Charge

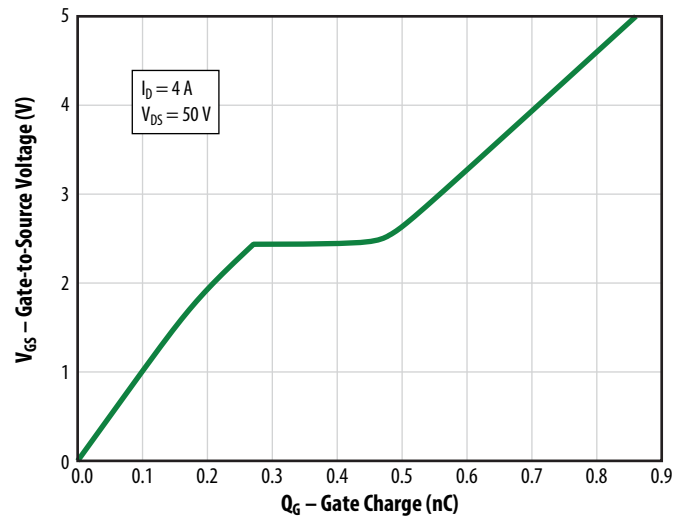


Figure 8: Reverse Drain-Source Characteristics

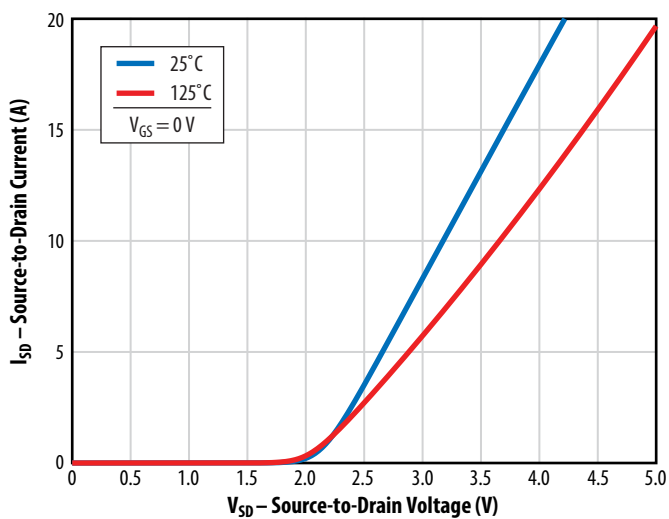
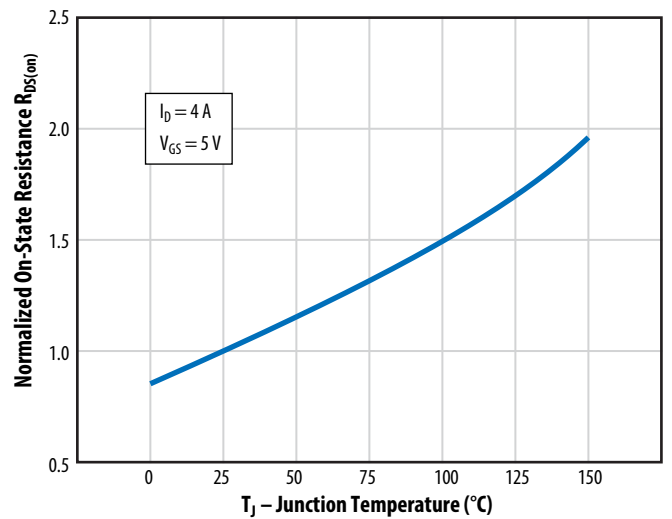


Figure 9: Normalized On-State Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0V for OFF.

All measurements were done with substrate shorted to source.

Figure 10: Normalized Threshold Voltage vs. Temperature

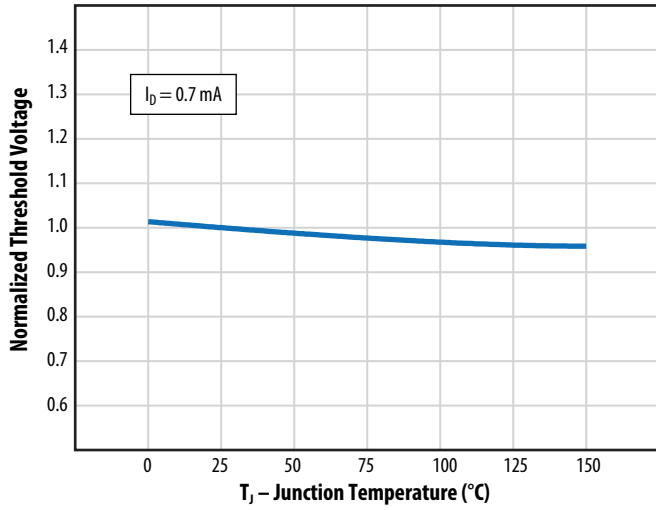


Figure 11: Safe Operating Area

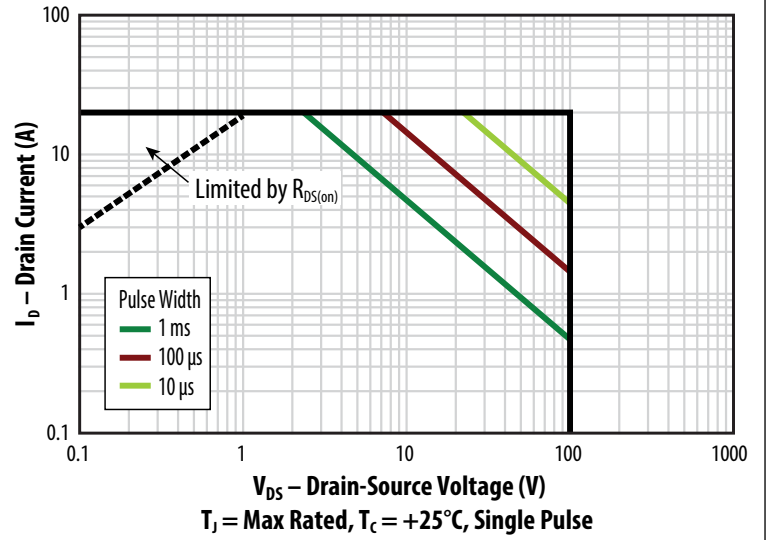
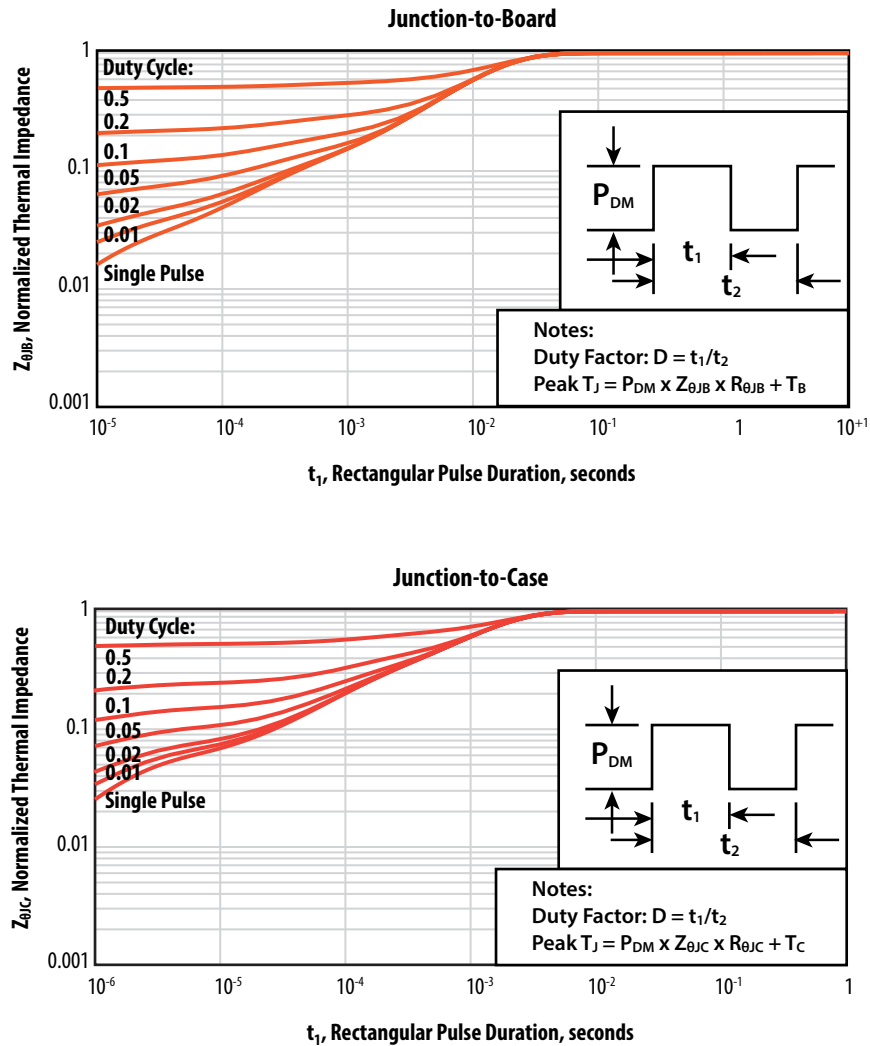
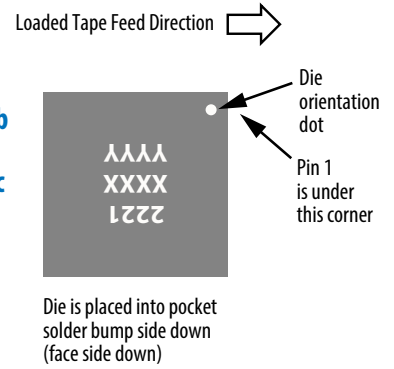
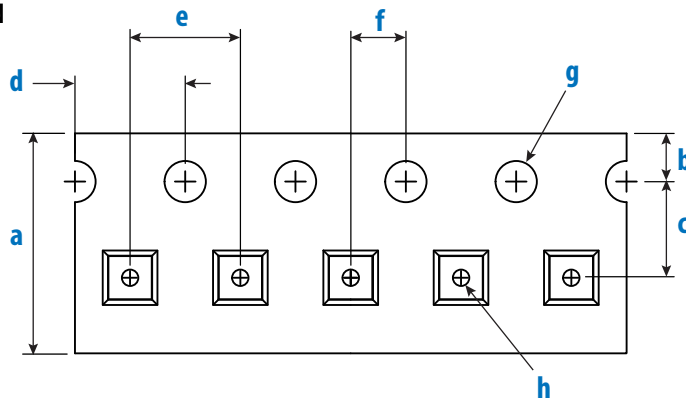
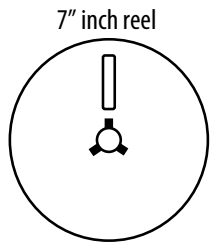


Figure 12: Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

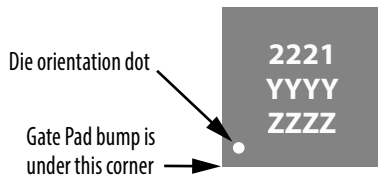


| EPC2221 (Note 1) | Dimension (mm) | | |
|------------------|----------------|------|------|
| | Target | MIN | MAX |
| a | 8.00 | 7.90 | 8.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (Note 2) | 3.50 | 3.45 | 3.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (Note 2) | 2.00 | 1.95 | 2.05 |
| g | 1.50 | 1.40 | 1.60 |
| h | 0.60 | 0.65 | 0.50 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

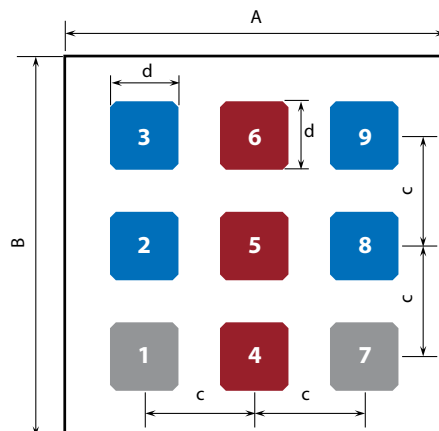
DIE MARKINGS



| Part Number | Laser Markings | | |
|-------------|-----------------------|------------------------------|------------------------------|
| | Part # Marking Line 1 | Lot Date Code Marking Line 2 | Lot Date Code Marking Line 3 |
| EPC2221 | 2221 | YYYY | ZZZZ |

DIE OUTLINE

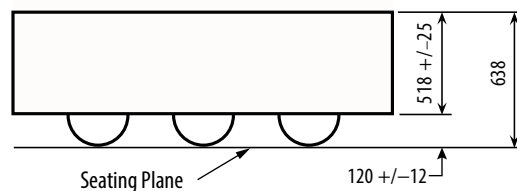
Solder Bump View

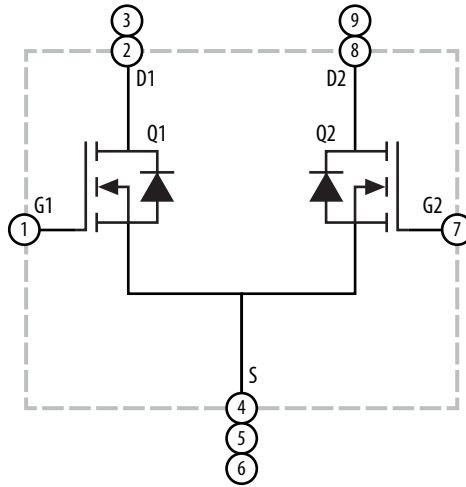


Pad 1 is Gate 1;
Pad 7 is Gate 2;
Pads 2, 3 are Drain 1;
Pads 8, 9 are Drain 2;
Pads 4, 5, 6 are Source

| DIM | Micrometers | | |
|-----|-------------|---------|------|
| | MIN | Nominal | MAX |
| A | 1320 | 1350 | 1380 |
| B | 1320 | 1350 | 1380 |
| c | | 450 | |
| d | | 225 | |

Side View

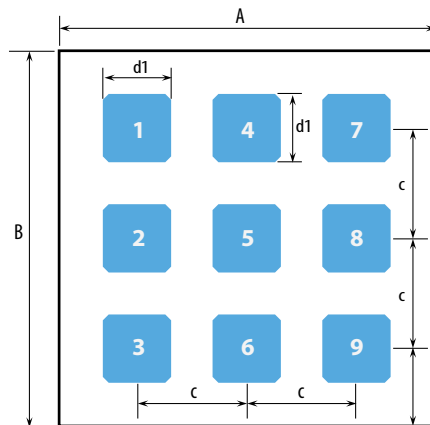




EPC2221 – Detailed Schematic

Note: The EPC2221 can be connected in parallel or used as independent FETs with common source.

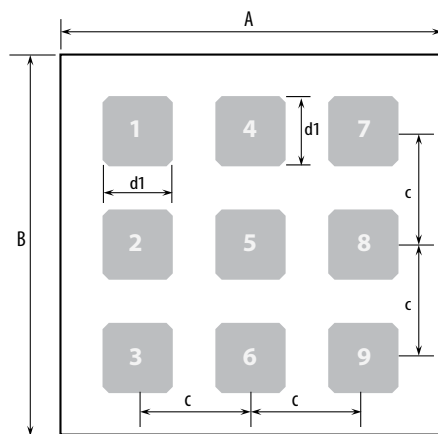
RECOMMENDED LAND PATTERN
(measurements in μm)



| DIM | Micrometers |
|-----------|-------------|
| A | 1350 |
| B | 1350 |
| c | 450 |
| d1 | 205 |

The land pattern is solder mask defined
Solder mask is 10 μm smaller per side than bump

RECOMMENDED STENCIL DRAWING
(measurements in μm)



| DIM | Micrometers |
|-----------|-------------|
| A | 1350 |
| B | 1350 |
| c | 450 |
| d1 | 225 |

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional Resources Available

- Assembly resources available at:
<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>
- Library of Altium footprints for production FETs and ICs:
<https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>
(for preliminary device Altium footprints, contact EPC)

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