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## NTE4511B & NTE4511BT Integrated Circuit CMOS, BCD-to-Seven Segment Latch/Decoder/Driver

### **Description:**

The NTE4511B (16-Lead DIP) and NTE4511BT (SOIC-16) BCD-to-seven segment latch/decoder/drivers are constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ( $\overline{LT}$ ), blanking ( $\overline{BI}$ ), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.), display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

### **Features:**

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25mA)
- Latching Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on All Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3Vcd to 10Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

### **Absolute Maximum Ratings:** (Voltages Referenced to $V_{SS}$ , Note 1)

DC Supply Voltage, $V_{DD}$ .....	-0.5 to +18.0V
Input Voltage (All Inputs), $V_{in}$ .....	-0.5 to $V_{DD} + 0.5V$
DC Current Drain (Per Pin), $I$ .....	10mA
Maximum Output Drive Current (Source) Per Output, $I_{OHmax}$ .....	25mA
Maximum Continuous Output Power (Source) Per Output (Note 2), $P_{OHmax}$ .....	50mW
Operating Temperature Range, $T_A$ .....	-55 to +125°C
Storage Temperature Range, $T_{stg}$ .....	-65 to +150°C

Note 1. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if  $V_{in}$  and  $V_{out}$  is not constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Due to the sourcing capability of these circuits, damage can occur to the device if  $V_{DD}$  is applied, and the outputs are shorted to  $V_{SS}$  and are at a logical 1 (See Absolute Maximum Ratings)

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ).

Note 2.  $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$



**Electrical Characteristics (Cont'd):** (Voltages referenced to V<sub>SS</sub>, Note 3)

Parameter	Symbol	V <sub>DD</sub> Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Drive Current Sink (V <sub>OL</sub> = 0.4Vdc) (V <sub>OL</sub> = 0.5Vdc) (V <sub>OL</sub> = 1.5Vdc)	I <sub>OL</sub>	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I <sub>in</sub>	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μAdc
Input Capacitance (V <sub>IN</sub> = 0)	C <sub>in</sub>	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	μAdc
		15	–	15	–	0.015	15	–	600	μAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C <sub>L</sub> = 50pF on All Outputs, All Buffers Switching Note 4, Note 6)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.9μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (3.8μA/kHz) f + I <sub>DD</sub>							μAdc
		15	I <sub>T</sub> = (6.7μA/kHz) f + I <sub>DD</sub>							μAdc

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C.

Note 5. Noise immunity specified for worst–case input combination.

Noise margin for both “1” and “0” = 1.0Vdc min @ V<sub>DD</sub> = 5Vdc  
 2.0Vdc min @ V<sub>DD</sub> = 10Vdc  
 2.5Vdc min @ V<sub>DD</sub> = 15Vdc

Note 6. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 3.5 \times 10^{-3}(C_L - 50) V_{DD}f$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V<sub>DD</sub> in volts and f in kHz is input frequency.

**Switching Characteristics:** (C<sub>L</sub> = 50pF, T<sub>A</sub> = +25°C, Note 3)

Parameter	Symbol	V <sub>DD</sub> Vdc	Min	Typ	Max	Unit
Output Rise Time t <sub>TLH</sub> = (1.5ns/pf) C <sub>L</sub> + 50ns t <sub>TLH</sub> = (0.75ns/pf) C <sub>L</sub> + 37.5ns t <sub>TLH</sub> = (0.55ns/pf) C <sub>L</sub> + 37.5ns	t <sub>TLH</sub>	5.0	–	40	80	ns
		10	–	30	60	ns
		15	–	25	60	ns
Output Fall Time t <sub>THL</sub> = (1.5ns/pf) C <sub>L</sub> + 50ns t <sub>THL</sub> = (0.75ns/pf) C <sub>L</sub> + 37.5ns t <sub>THL</sub> = (0.55ns/pf) C <sub>L</sub> + 37.5ns	t <sub>THL</sub>	5.0	–	125	250	ns
		10	–	75	150	ns
		15	–	65	130	ns
Data Propagation Delay Time t <sub>PLH</sub> = (0.40ns/pf) C <sub>L</sub> + 620ns t <sub>PLH</sub> = (0.25ns/pf) C <sub>L</sub> + 237.5ns t <sub>PLH</sub> = (0.20ns/pf) C <sub>L</sub> + 165ns t <sub>PHL</sub> = (1.3ns/pf) C <sub>L</sub> + 655ns t <sub>PHL</sub> = (0.60ns/pf) C <sub>L</sub> + 260ns t <sub>PHL</sub> = (0.35ns/pf) C <sub>L</sub> + 182.5ns	t <sub>PLH</sub>	5.0	–	640	1280	ns
		10	–	250	500	ns
		15	–	175	350	ns
	t <sub>PHL</sub>	5.0	–	720	1440	ns
		10	–	290	580	ns
		15	–	200	400	ns

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C.

**Switching Characteristics (Cont'd):** ( $C_L = 50\text{pF}$ ,  $T_A = +25^\circ\text{C}$ , Note 3)

Parameter	Symbol	V <sub>DD</sub> Vdc	Min	Typ	Max	Unit
Blank Propagation Delay Time $t_{PLH} = (0.30\text{ns/pf}) C_L + 305\text{ns}$ $t_{PLH} = (0.25\text{ns/pf}) C_L + 117.5\text{ns}$ $t_{PLH} = (0.15\text{ns/pf}) C_L + 92.5\text{ns}$ $t_{PHL} = (0.85\text{ns/pf}) C_L + 442.5\text{ns}$ $t_{PHL} = (0.45\text{ns/pf}) C_L + 177.5\text{ns}$ $t_{PHL} = (0.35\text{ns/pf}) C_L + 142.5\text{ns}$	t <sub>PLH</sub>	5.0	–	600	750	ns
		10	–	200	300	ns
		15	–	150	220	ns
	t <sub>PHL</sub>	5.0	–	485	970	ns
		10	–	200	400	ns
		15	–	160	320	ns
Lamp Test Propagation Delay Time $t_{PLH} = (0.45\text{ns/pf}) C_L + 290.5\text{ns}$ $t_{PLH} = (0.25\text{ns/pf}) C_L + 112.5\text{ns}$ $t_{PLH} = (0.20\text{ns/pf}) C_L + 80\text{ns}$ $t_{PHL} = (1.3\text{ns/pf}) C_L + 248\text{ns}$ $t_{PHL} = (0.45\text{ns/pf}) C_L + 102.5\text{ns}$ $t_{PHL} = (0.35\text{ns/pf}) C_L + 72.5\text{ns}$	t <sub>PLH</sub>	5.0	–	313	625	ns
		10	–	125	250	ns
		15	–	90	180	ns
	t <sub>PHL</sub>	5.0	–	313	625	ns
		10	–	125	250	ns
		15	–	90	180	ns
Setup Time	tsu	5.0	180	90	–	ns
		10	76	38	–	ns
		15	40	20	–	ns
Hold Time	th	5.0	0	–90	–	ns
		10	0	–38	–	ns
		15	0	–20	–	ns
Latch Enable Pulse Width	t <sub>WL</sub>	5.0	520	260	–	ns
		10	220	110	–	ns
		15	130	65	–	ns

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

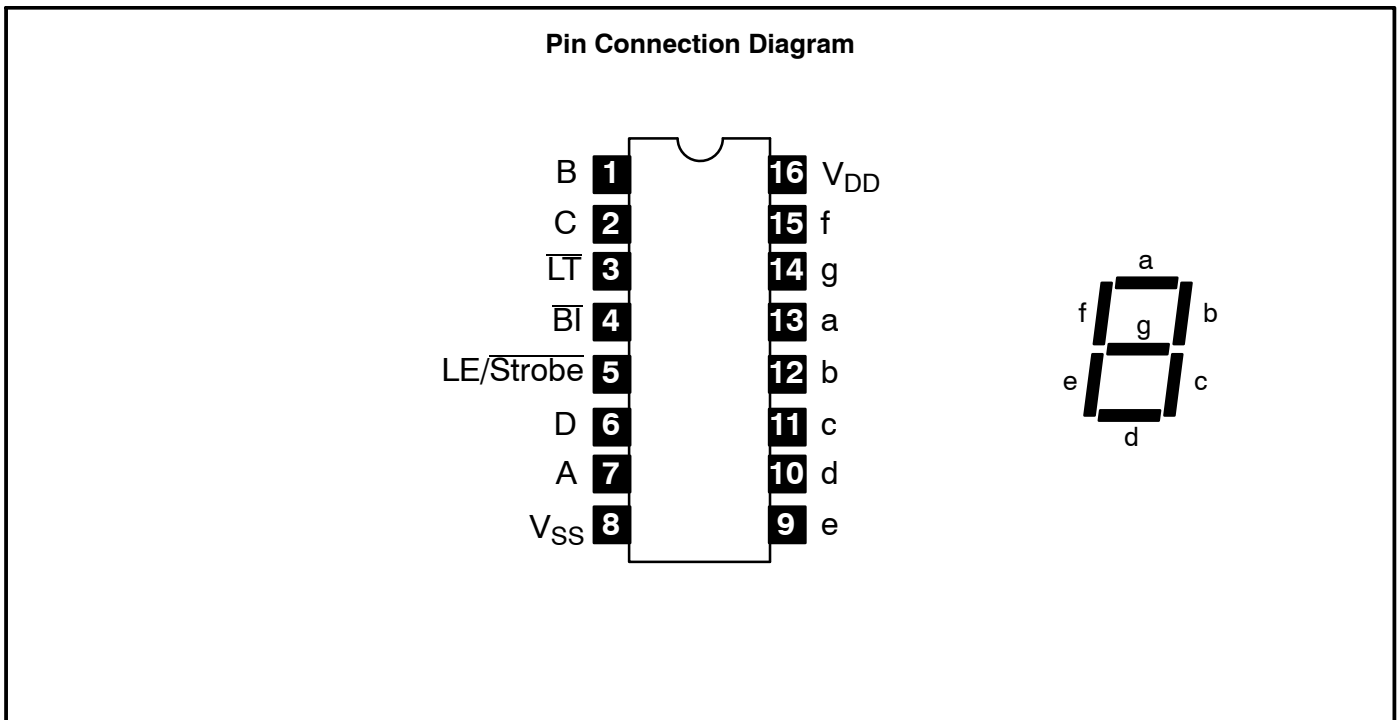
Note 4. The formulas given are for the typical characteristics only at +25°C.

### Truth Table:

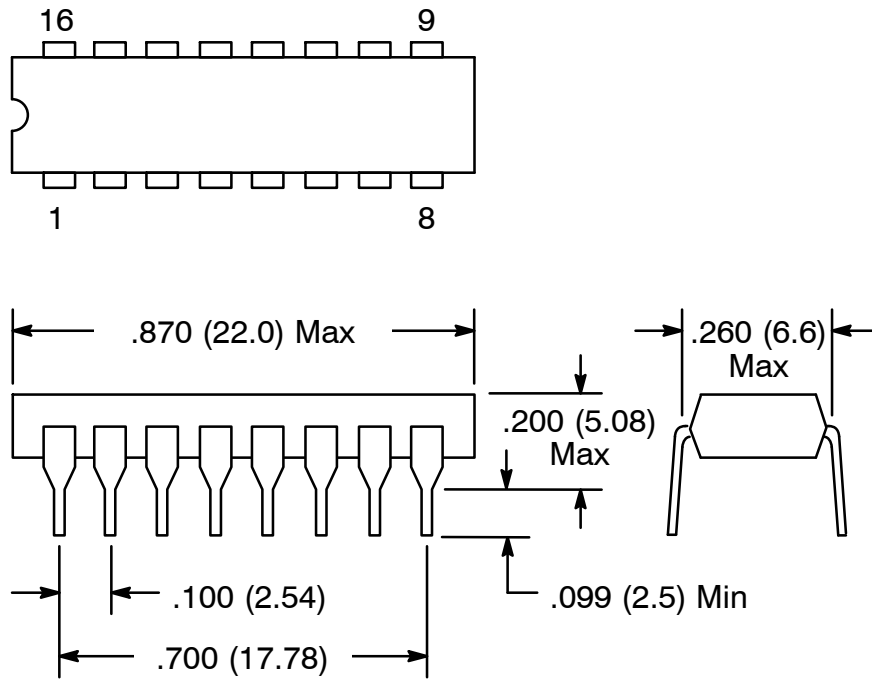
Inputs							Outputs							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X = Don't Care

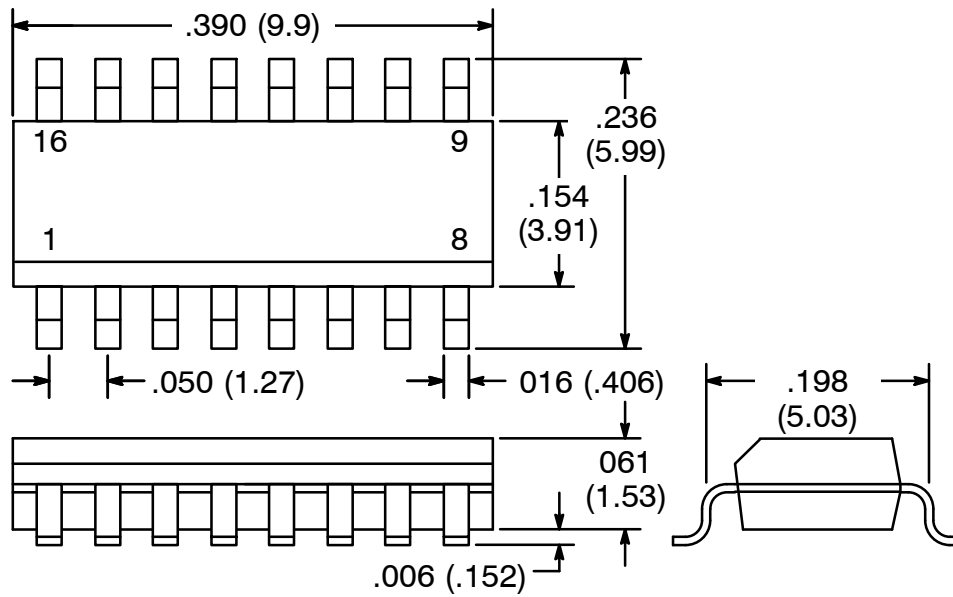
\* Depends upon the BCD code previously applied when LE = 0



### NTE4511B



### NTE4511BT



NOTE: Pin1 on Beveled Edge