COMPARE PRO, STANDARD, AND LITE EDITIONS

Intel® Quartus® Prime Design Software

The Intel® Quartus® Prime software is revolutionary in performance and productivity for FPGA, CPLD, and SoC designs, providing a fast path to convert your concept into reality. The Intel Quartus Prime software also supports many third-party tools for synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

INTEL QUARTUS PRIME DESIGN SOFTWARE V19.1			AVAILABILITY		
			PRO EDITION ($)	STANDARD EDITION ($)	LITE EDITION (FREE)
Device Support	Stratix® series	IV, V		✓	
		10	✓		
	Arria® series	II			✓[1]
		II, V		✓	
		10	✓	✓	
	Cyclone® series	IV, V		✓	✓
		10 LP		✓	✓
		10 GX	✓[2]		
	MAX® series			✓	✓
Design Flow	Partial reconfiguration		✓	✓[3]	
	Rapid recompile		✓	✓[4]	
	Block-based design		✓		
	Incremental optimization		✓		
Design Entry/Planning	IP Base Suite		✓	✓	Available for purchase
	Intel HLS Compiler		✓	✓	✓
	Platform Designer (Standard)			✓	✓
	Platform Designer (Pro)		✓		
	Design Partition Planner		✓	✓	
	Chip Planner		✓	✓	✓
	Interface Planner		✓		
	Logic Lock regions		✓	✓	
	VHDL		✓	✓	✓
	Verilog		✓	✓	✓
	SystemVerilog		✓	✓[5]	✓[5]
	VHDL-2008		✓	✓[5]	
Functional Simulation	ModelSim*-Intel FPGA Starter Edition software		✓	✓	✓
	ModelSim-Intel FPGA Edition software		✓[6]	✓[6]	✓[6]
Compilation (Synthesis & Place and Route)	Fitter (Place and Route)		✓	✓	✓
	Early placement		✓		
	Register retiming		✓	✓	
	Fractal synthesis		✓		
	Multiprocessor support		✓	✓	
Timing and Power Verification	Timing Analyzer		✓	✓	✓
	Design Space Explorer II		✓	✓	✓
	Power Analyzer		✓	✓	✓
In-System Debug	Signal Tap Logic Analyzer		✓	✓	✓
	Transceiver toolkit		✓	✓	
	Intel Advanced Link Analyzer		✓	✓	
Operating System (OS) Support	Windows*/Linux* 64 bit support		✓	✓	✓
Price			Buy Fixed - $3,995 Float - $4,995	Buy Fixed - $2,995 Float - $3,995	Free
Download			Download Now	Download Now	Download Now

Notes:
1. The only Arria II FPGA supported is the EP2AGX45 device.
2. The Intel Cyclone 10 GX device support is available for free in the Pro Edition software.
3. Available for Cyclone V and Stratix V devices only and requires a partial reconfiguration license.
4. Available for Stratix V, Arria V, and Cyclone V devices.
5. Limited language support.
6. Requires an additional license.

ADDITIONAL DEVELOPMENT TOOLS

TOOLS	DESCRIPTION
Intel FPGA SDK for OpenCL™	• No additional licenses are required. • Supported with the Intel Quartus Prime Pro/Standard Edition software. • The software installation file includes the Intel Quartus Prime Pro/Standard Edition software and the OpenCL software.
Intel HLS Compiler	• No additional license required. • Now available as a separate download. • Supported with all editions of the Intel Quartus Prime software.
DSP Builder for Intel FPGAs	• Additional licenses are required. • DSP Builder for Intel FPGAs (Advanced Blockset only) is supported with the Intel Quartus Prime Pro Edition software for Intel Stratix 10 and Intel Arria 10 devices. • DSP Builder for Intel FPGAs (Standard Blockset and Advanced Blockset) is supported with the Intel Quartus Prime Standard Edition software for Intel Arria 10, Stratix V, Arria V, and Cyclone V devices.
Nios® II Embedded Design Suite	• No additional licenses are required. • Supported with all editions of the Intel Quartus Prime software. • Includes Nios II software development tools and libraries.
Intel SoC FPGA Embedded Development Suite (SoC EDS)	• Requires additional licenses for Arm* Development Studio 5* (DS-5*) Intel SoC FPGA Edition. • The SoC EDS Standard Edition is supported with the Intel Quartus Prime Lite/Standard Edition software and the SoC EDS Pro Edition is supported with the Intel Quartus Prime Pro Edition software.

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INTEL QUARTUS PRIME DESIGN SOFTWARE FEATURES SUMMARY

Interface Planner	Enables you to quickly create your I/O design using real time legality checks.
Pin planner	Eases the process of assigning and managing pin assignments for high-density and high-pin-count designs.
Platform Designer	Automates system development by integrating IP functions and subsystems (collection of IP functions) using a hierarchical approach and a high-performance interconnect based on a network-on-a-chip architecture.
Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Intel and from Intel's third-party IP partners.
Synthesis	Provides expanded language support for System Verilog and VHDL 2008.
Scripting support	Supports command-line operation and Tcl scripting, as well as graphical user interface (GUI) design.
Rapid recompile	Maximizes your productivity by reducing your compilation time (for a small design change after a full compile). Improves design timing preservation.
Incremental optimization	Offers a faster methodology to converge to design sign-off. The traditional fitter stage is divided into finer stages for more control over the design flow.
Partial reconfiguration	Creates a physical region on the FPGA that can be reconfigured to execute different functions. Synthesize, place, route, close timing, and generate configuration bitstreams for the functions implemented in the region.
Block-based design flows	Provides flexibility of reusing timing-closed modules or design blocks across projects and teams.
Intel Hyperflex™ FPGA Architecture	Provides increased core performance and power efficiency for Intel Stratix 10 devices.
Physical synthesis	Uses post placement and routing delay knowledge of a design to improve performance.
Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Intel Quartus Prime software settings to find optimal results.
Extensive cross-probing	Provides support for cross-probing between verification tools and design source files.
Optimization advisors	Provides design-specific advice to improve performance, resource usage, and power consumption.
Chip planner	Reduces verification time while maintaining timing closure by enabling small, post-placement and routing design changes to be implemented in minutes.
Timing Analyzer	Provides native Synopsys* Design Constraint (SDC) support and allowing you to create, manage, and analyze complex timing constraints and quickly perform advanced timing verification.
Signal Tap logic analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
System Console	Enables you to easily debug your FPGA in real time using read and write transactions. It also enables you to quickly create a GUI to help monitor and send data into your FPGA.
Power Analyzer	Enables you to analyze and optimize both dynamic and static power consumption accurately.
Design Assistant	A design rules checking tool that allows you to get to design closure faster by reducing the number of iterations needed and by enabling faster iterations with targeted guidance provided by the tool at various stages of compilation.
Fractal synthesis	Enables the Intel Quartus Prime software to efficiently pack arithmetic operations in FPGA's logic resources resulting in significantly improved performance.
EDA partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification. To see a complete list of partners, visit www.intel.com/fpgaedapartners.

Getting Started Steps

Step 1: Download the free Intel Quartus Prime Lite Edition software
www.intel.com/quartus

Step 2: Get oriented with the Intel Quartus Prime software interactive tutorial
After installation, open the interactive tutorial on the welcome screen.

Step 3: Sign up for training
www.intel.com/fpgatraining

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