High Accuracy GMR Wheel Speed Sensor IC

FEATURES AND BENEFITS

- **GMR technology** integrates high sensitivity MR (magnetoresistive) sensor elements and high precision BiCMOS circuits on a single silicon integrated circuit, offering high accuracy, low magnetic field operation
- **Integrated capacitor** in a single overmolded miniature package provides greater EMC robustness
- **SolidSpeed Digital Architecture** supports advanced digital processing providing highly accurate edge performance in the presence of extreme system-level disturbances
- **Compatible orientation** for Hall replacement
- **ASIL B(D) rating** based on integrated diagnostics and certified safety design process
- **Two-wire current source output** supporting speed and ASIL
- **EEPROM** offers device traceability throughout the production process

PACKAGE:

2-Pin SIP
(suffix UB)

Not to scale

DESCRIPTION

The A19250 is a giant magnetoresistance (GMR) integrated circuit (IC) that provides a user-friendly two-wire solution for applications where speed information is required. The small integrated package includes an integrated capacitor and GMR IC in a single overmold design with an additional molded lead-stabilizing bar for robust shipping and ease of assembly.

The GMR-based IC is designed for use in conjunction with front-biased ring magnet encoders. State-of-the-art GMR technology with industry-leading signal processing algorithms accurately switch in response to low-level differential magnetic signals. The high sensitivity of GMR combined with differential sensing offers inherent rejection of interfering common-mode magnetic fields, low jitter, and high pitch accuracy, commonly required in wheel speed sensing applications.

Patented GMR technology allows the same orientation as Hall-effect for a drop-in solution in the application.

Integrated diagnostics are used to detect an IC failure which impacts the output protocol's accuracy, providing coverage compatible with ASIL B(D) compliance. Built-in EEPROM scratch memory offers traceability of the device throughout the IC's production process.

The IC is offered in the UB package, which integrates the IC and a high-temperature ceramic capacitor in a single overmold SIP package for enhanced EMC performance. The 2-pin SIP package is lead (Pb) free, with tin leadframe plating.

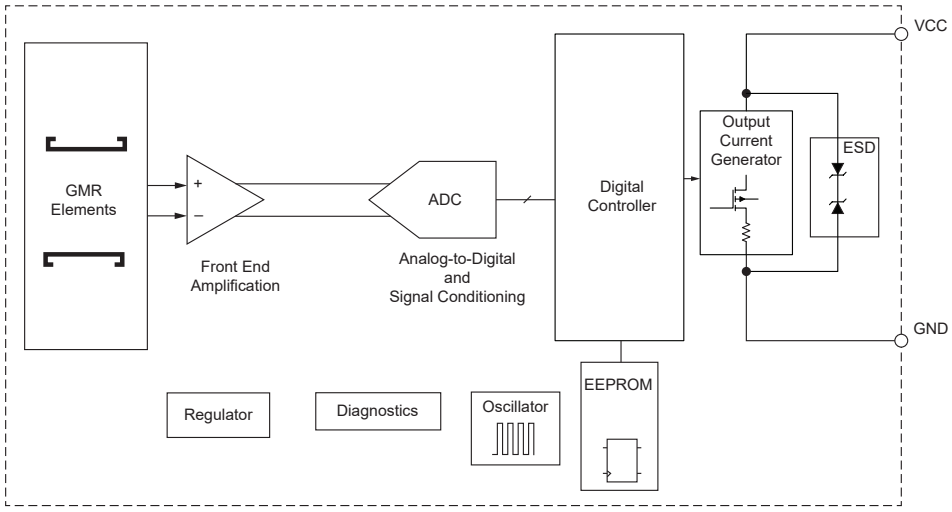


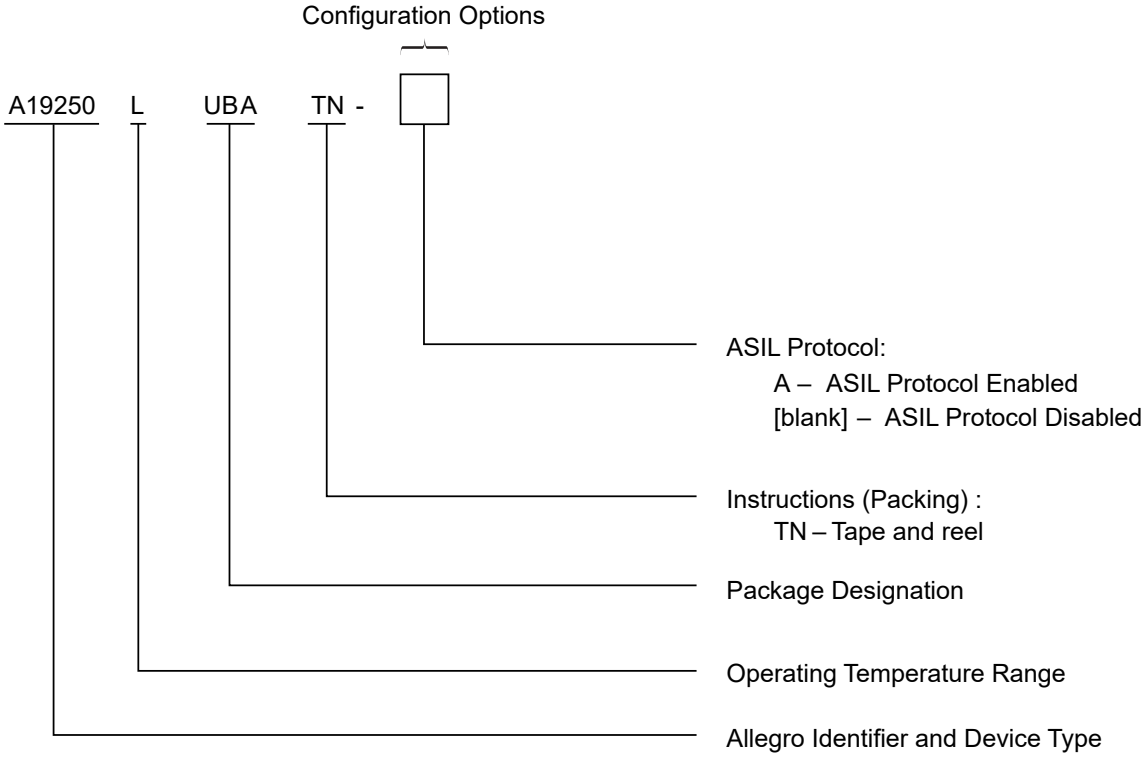
Figure 1: Functional Block Diagram

SELECTION GUIDE*

Part Number	Packing
A19250LUBATN	Tape and Reel, 4000 pieces per reel
A19250LUBATN-A	

* Not all combinations are available. Contact Allegro sales for availability and pricing of custom programming options.

Complete Part Number Format



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SPECIFICATIONS

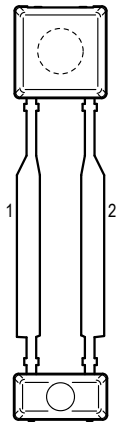
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to Power Derating section; potential between pin 1 and pin 2	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A		–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C
Applied Magnetic Flux Density	B	In any direction; no permanent damage; functionality not guaranteed	630	G

INTERNAL DISCRETE CAPACITOR RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Nominal Capacitance	C_{SUPPLY}	Connected between pin 1 and pin 2 (see Figure 2)	2.2	nF

PINOUT DIAGRAM AND LIST



Package UB, 2-Pin SIP Pinout Diagram

Pinout List

Pin Name	Pin Number	Function
VCC	1	Supply Voltage
GND	2	Ground

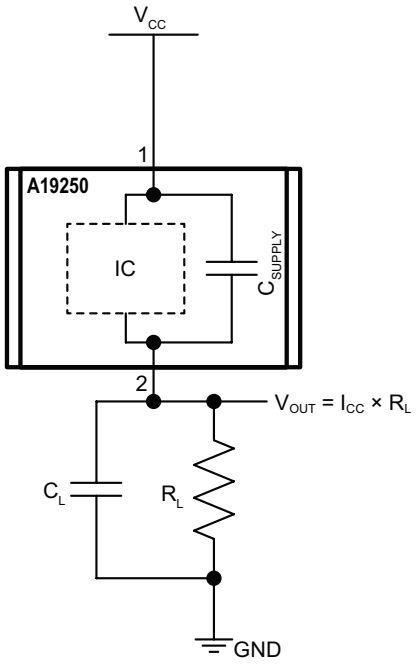


Figure 2: Application Circuit

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OPERATING CHARACTERISTICS: Valid throughout full operating voltage and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Potential between pin 1 and pin 2	4.25	–	24	V
Reverse Supply Current [3]	I_{RCC}	V_{CC} = –18 V	–10	–	–	mA
Supply Zener Clamp Voltage	$V_{Zsupply}$	$I_{CC} = I_{CC(MAX)} + 3$ mA, T_A = 25°C	28	–	–	V
Undervoltage Lockout	$V_{CC(OFF)}$	Turn-off level	–	–	3.5	V
	$V_{CC(ON)}$	Turn-on level	3.75	–	4.25	V
Supply Current	$I_{CC(LOW)}$	Low-current state	5.9	7	8.4	mA
	$I_{CC(HIGH)}$	High-current state	12	14	16	mA
Supply Current Ratio [4]	$I_{CC(HIGH)}/I_{CC(LOW)}$	Measured as a ratio of high current to low current (isothermal)	1.9	–	–	–
ASIL Safety Current	I_{RESET}	$V_{CC} > V_{CC(OFF)}$	1.5	2.2	3.9	mA
		$V_{CC} < V_{CC(OFF)}$	0	–	3.9	mA
Output Rise/Fall Time	t_r, t_f	V_{CC} = 5 V	0	–	1.5	µs
POWER-ON CHARACTERISTICS						
Power-On State	POS	$V_{CC} > V_{CC(min)}$	$I_{CC(LOW)}$			mA
Power-On Time	t_{PO}	$V_{CC} > V_{CC(min)}$	–	–	1	ms
OUTPUT PROTOCOLS						
Output Protocol	–		Speed			–
ASIL Safety Current Time	$t_{RESET(EP1)}$	See Figure 9 (Error Protocol 1)	145	–	215	µs
	$t_{RESET(EP2)}$	See Figure 9 (Error Protocol 2)	4	–	7.5	ms

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative Power Derating section.
[3] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[4] Supply current ratio is taken as a mean value of $I_{CC(HIGH)} / I_{CC(LOW)}$.

Continued on the next page…

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OPERATING CHARACTERISTICS (continued): Valid throughout full operating voltage and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
INPUT CHARACTERISTICS AND PERFORMANCE						
Operating Frequency	f_{IN}	Corresponds to wheel speed multiplied by number of target pole-pairs	0	–	5000	Hz
Operating Differential Magnetic Input [5]	$B_{DIFF(pk-pk)}$	Peak-to-peak of differential magnetic input (see Figure 4)	2.5	–	–	G
Operating Differential Magnetic Range [5]	B_{DIFF}	See Figure 4	–900	–	900	G
Operating Differential Magnetic Offset	$B_{DIFFEXT}$	Differential magnetic offset; see Figure 4	–40	–	40	G
Allowable Differential Sequential Signal Variation	$B_{SEQ(n+1)}/B_{SEQ(n)}$	Signal period-to-period variation (see Figure 3)	60	–	200	%
Operate Point	B_{OP}	% of peak-to-peak IC-processed signal	–	60	–	%
Release Point	B_{RP}	% of peak-to-peak IC-processed signal	–	40	–	%
Repeatability [6]	$Err_{\theta E}$	Constant air gap (greater than 20 G(pk-pk)), temperature, and target speed. Sinusoidal input signal. Greater than 1000 output edges captured.	–	–	0.3	%
Calibration Period	N_{CAL}	Number of Cycles after rotation until to first accurate edge (See Figure 5 for T_{CYCLE} Definition)	0.75 × T_{CYCLE}	1.00 × T_{CYCLE}	1.25 × T_{CYCLE}	–
THERMAL CHARACTERISTICS						
Magnetic Temperature Coefficient [7]	TC	Valid for full temperature range based on ferrite	–	0.2	–	%/°C
Package Thermal Resistance	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	–	213	–	°C/W

[5] Differential magnetic field measured for Channel A (E1-E2) channel's differential magnetic field is measured between two GMR elements spaced by 1.75 mm. Magnetic field is measured in the By direction (Refer to Figure 7 and Figure 8). |Bx| field needs to be less than 80 G.
[6] Repeatability (i.e. jitter) is tested to 6 sigma and is guaranteed by design and characterization only.
[7] Ring magnet decreases in magnetic strength with rising temperature, and the device compensates. Note that $B_{DIFF(pk-pk)}$ requirement is not influenced by this.

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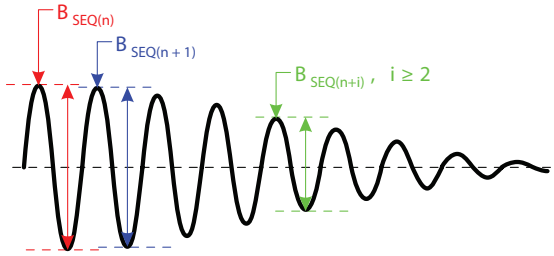


Figure 3: Differential Signal Variation

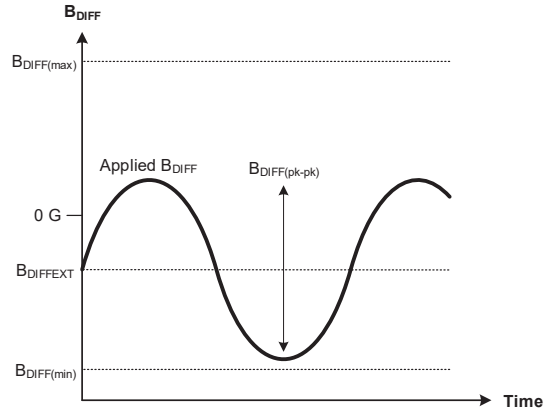
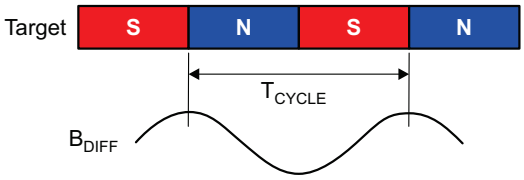


Figure 4: Input Signal Definition



B_{DIFF} = Differential Input Signal; the differential magnetic flux sensed by the sensor

T_{CYCLE} = Target Cycle; the amount of rotation that moves one north pole and one south pole across the sensor

Figure 5: Definition of T_{CYCLE}

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FUNCTIONAL DESCRIPTION

The A19250 sensor IC contains a single-chip GMR circuit that uses spaced elements. These elements are used in differential pairs to provide electrical signals containing information regarding edge position and direction of rotation. The A19250 is intended for use with ring magnet targets as shown in Figure 7. The IC detects the peaks of the magnetic signals and sets dynamic thresholds based on these detected signals.

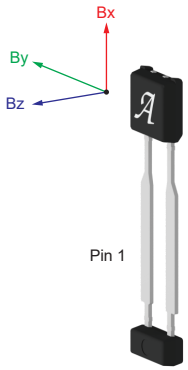

Figure 6: Package Orientation

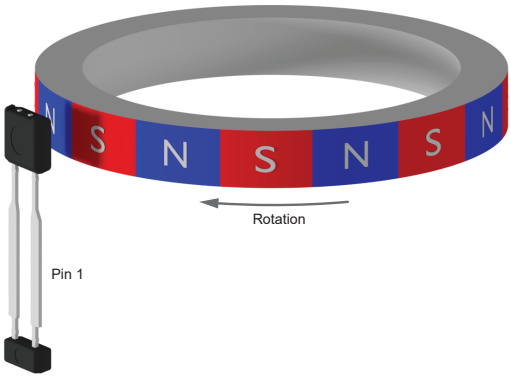

Figure 7: Parallel Orientation

Data Protocol Description

When a target passes in front of the device (opposite the branded face of the package case), the A19250 generates an output pulse for each magnetic pole-pair of the target. Speed information is provided by the output pulse rate. The sensor IC can sense target movement in both the forward and reverse directions.

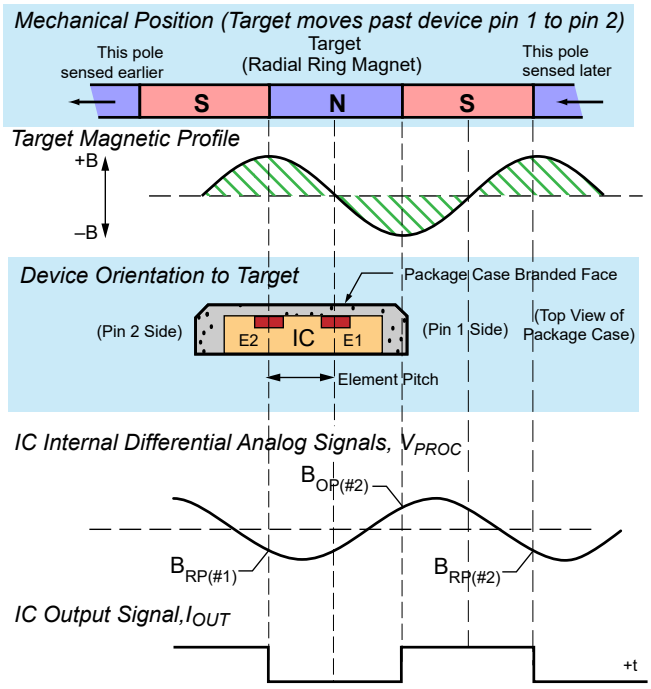

Figure 8: Basic Operation

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ASIL Safe State Output Protocol

The A19250 sensor IC contains diagnostic circuitry that will continuously monitor occurrences of failure defects within the IC. Refer to Figure 9 for the output protocol of the ASIL safe state after an internal defect has been detected. Error Protocol 1 will result from faults due to over frequency conditions from the input signal. Error Protocol 2 will result from hard failures detected within the A19250 such as a regulator and front-end fault.

Note: If a fault exists continuously, the device will stay in permanent safe state. Refer to the A19250 Safety Manual for additional details on the ASIL Safe State Output Protocol.

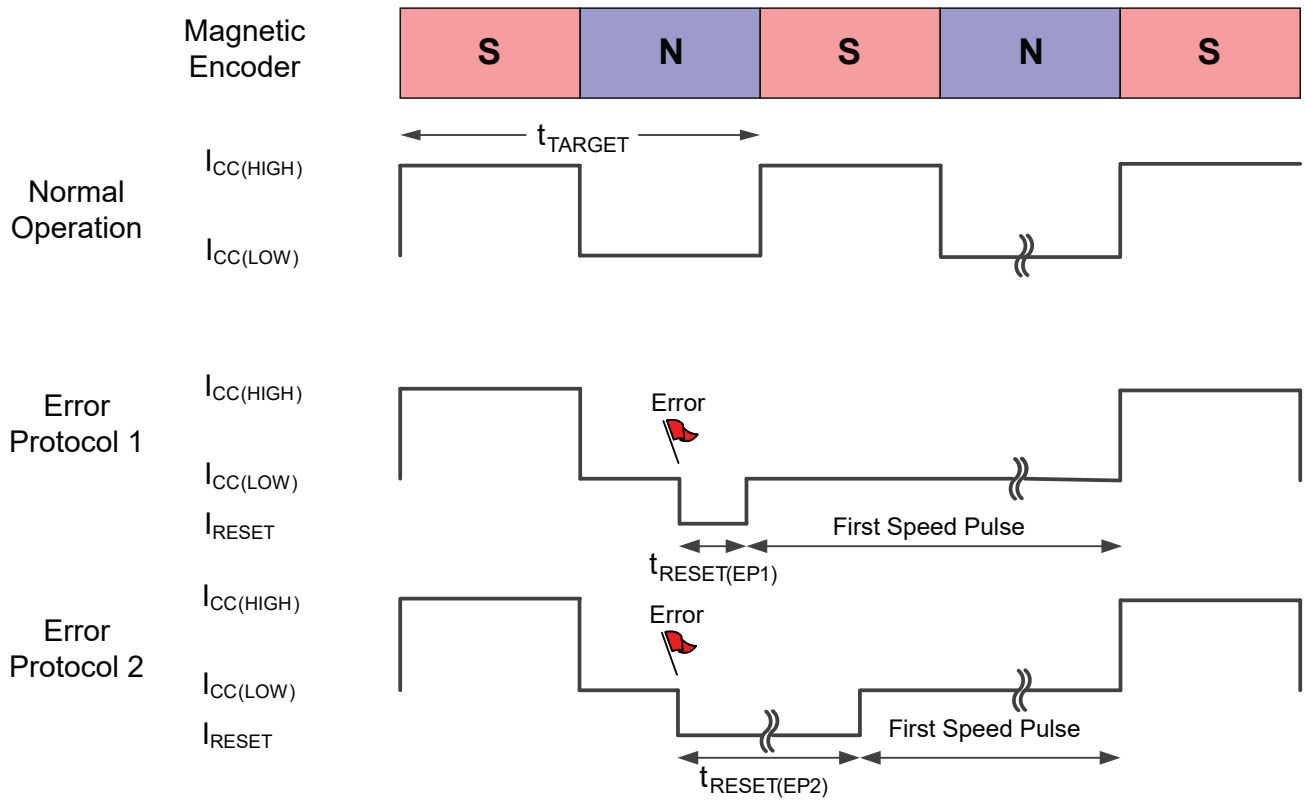

Figure 9: Output Protocol for –A Variant (ASIL Safe State)

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D) can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as:

T_A= 25°C, V_{CC} = 12 V, I_{CC} = 7.15 mA, and $R_{\theta JA}$ = 213°C/W,

then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 7.15\ mA = 85.8\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 85.8\ mW \times 213°C/W = 18.3°C$$

$$T_J = T_A + \Delta T = 25°C + 18.3°C = 43.3°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A = 150°C.

Observe the worst-case ratings for the device, specifically:

$R_{\theta JA}$ = 213°C/W (subject to change), $T_{J(max)}$ = 165°C, $V_{CC(max)}$ = 24 V, and $I_{CC(AVG)}$ = 14.8 mA. $I_{CC(AVG)}$ is computed using $I_{CC(HIGH)(max)}$ and $I_{CC(LOW)(max)}$, with a duty cycle of 84% computed from $t_{w(REV)(max)}$ on-time and $t_{w(PRE)(min)}$ off-time (pulse-width protocol).

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 213°C/W = 70.4\ mW$$

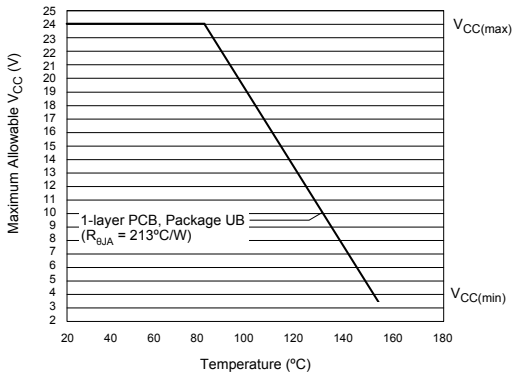
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 70.4\ mW \div 14.8\ mA = 4.8\ V$$

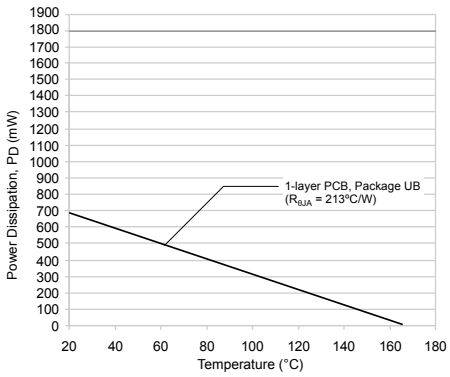
The result indicates that, at T_A , the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000408, Rev. 3)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

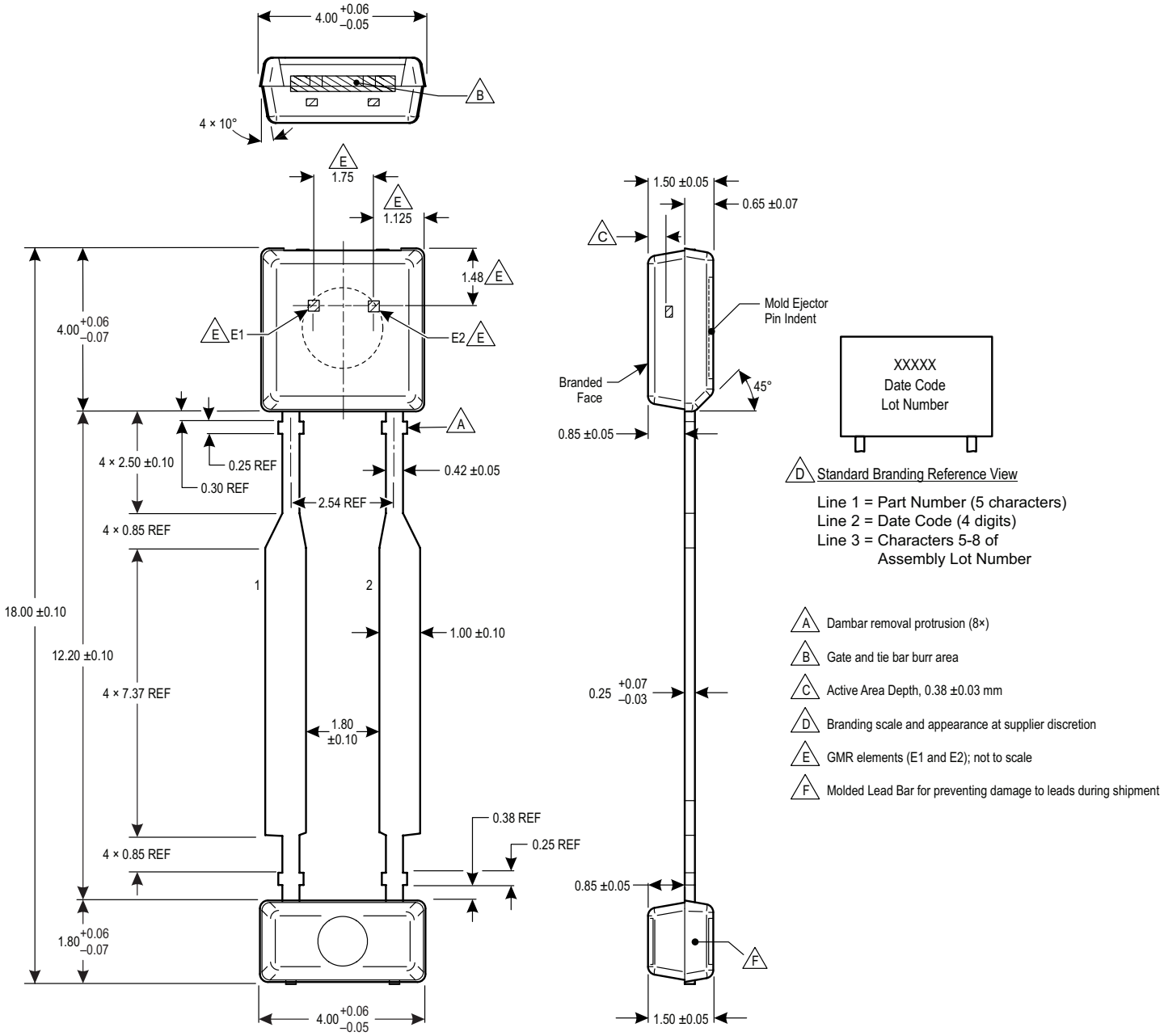

Figure 10: Package UB, 2-Pin SIP

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Revision History

Number	Date	Description
–	January 16, 2019	Initial release
1	February 12, 2020	Minor editorial updates
2	December 15, 2020	Updated “ASIL B” to “ASIL B(D)” (page 1), Operating Frequency min value, Operating Differential Magnetic Input min value, Operating Differential Magnetic Range values, and footnote 5 (page 5); removed Operating Differential Magnetic Input 2nd test conditions and values and Target Pitch characteristic (page 5); added Operating Differential Magnetic Offset (page 5); updated Figure 4 (page 6).

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