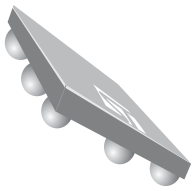
TS2007FC

3 W, filter-free, class-D audio power amplifier with 6 or 12 dB fixed gain select

Datasheet - production data

TS2007EIJT, 9-bump Flip-chip



Features

- Operates from V_{CC} = 2.4 V to 5.5 V
- Standby mode active low
- Output power: 1.4 W at 5 V or 0.5 W at 3.0 V into 8 Ω with 1% THD+N max.
- Output power: 2.3 W at 5 V or 0.75 W at 3.0 V into 4 Ω with 1% THD+N max.
- Two fixed gain selects: 6 dB or 12 dB
- Low current consumption
- Efficiency: 86% typ.
- Signal-to-noise ratio: 90 dB typ.
- PSRR: 68 dB typical at 217 Hz with 6 dB gain
- PWM base frequency: 280 kHz
- Low pop and click noise
- Thermal shutdown protection
- Output short-circuit protection
- Flip-chip lead-free 9-bump package with back coating in option

Applications

- Cellular phones
- PDAs
- Notebook PCs

Description

The TS2007FC is a class-D audio power amplifier. It is able to drive up to 1.4 W into an 8 Ω load at 5 V, it achieves better efficiency than typical class-AB audio power amplifiers.

This device can switch between two gain settings, 6 dB or 12 dB via a logic signal on the gain select pin. The pop and click reduction circuitry provides low on/off switching noise which allows the device to start within 1 ms typically.

A standby mode function (active low) keeps the current consumption down to 1 µA typically.

The TS2007FC is available in a 9-bump Flip-chip lead-free package.

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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	6	V
V_{in}	Input voltage(2)	GND to V_{CC}	
T_{oper}	Operating free-air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction to ambient(3)	200	°C/W
P_d	Power dissipation	Internally limited(4)	W
ESD	Human body model(5)	2	kV
	Machine model(6)	200	V
Latch-up	Latch-up immunity	Class A = 200	mA
	Lead temperature (soldering, 10 s)	260	°C
	Output short-circuit protection	Internally limited(7)	A
R_L	Minimum load resistor	3.2	Ω

1. All voltage values are measured with respect to the ground pin
2. The magnitude of the input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V
3. The device is protected from over heating by a thermal shutdown active @ 150° C
4. Exceeding the power derating curves during a long period provokes abnormal operating conditions
5. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
6. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
7. Implemented short-circuit protection protects the amplifier against damage by short-circuit between positive and negative outputs and between outputs and ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.4 to 5.5	V
V_{in}	Input voltage range	GND to V_{CC}	
V_{icm}	Input common mode voltage range(1)	GND + 0.15 V to V_{CC} - 0.7 V	
V_{STBY}	Standby voltage input(2): Device ON Device OFF	 $1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ (3)	
V_{GS}	Gain select input voltage(4): Gain = 6 dB Gain = 12 dB	 $1.4 \leq V_{GS} \leq V_{CC}$ $GND \leq V_{GS} \leq 0.4$	
R_L	Load resistor	≥ 4	Ω
R_{thja}	Thermal resistance junction to ambient(5)	90	°C/W

1. $|V_{oo}| \leq 35$ mV max with both differential gains
2. Without any signal on V_{STBY}, the device is in standby (internal 300 kΩ pull-down resistor)
3. Minimum current consumption is obtained when V_{STBY} = GND
4. Without any signal on GS pin, the device is in a 6 dB gain configuration (internal 300 kΩ pull up resistor)
5. When mounted on 4-layer PCB

2 Application information

Table 3. External component description

Components	Functional description
C_s	Supply capacitor that provides power supply filtering
C_{in}	Input coupling capacitors (optional) that block the DC voltage at the amplifier input terminal. These capacitors also form a high-pass filter with Z_{in} ($Fc = 1 / (2 \times \pi \times Z_{in} \times C_{in})$).

Figure 1. 9-bump Flip-chip pinout (top view)

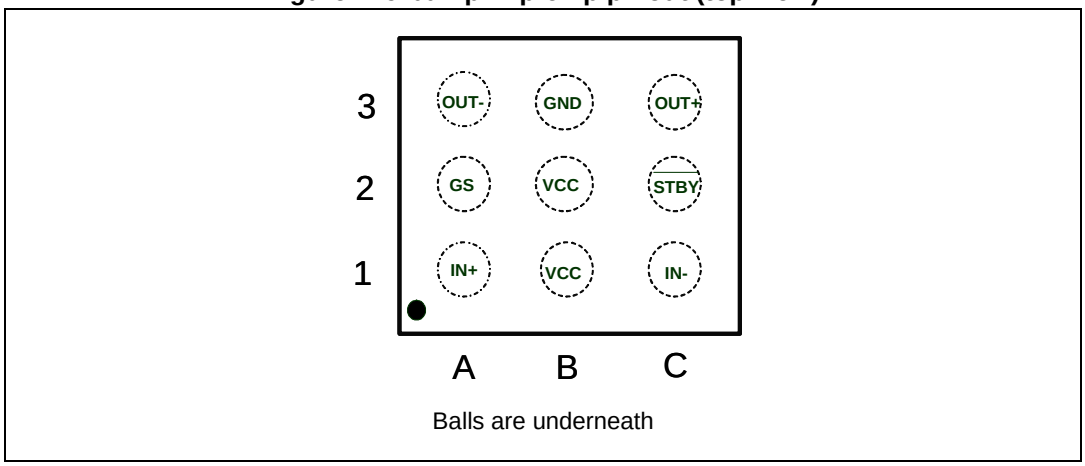
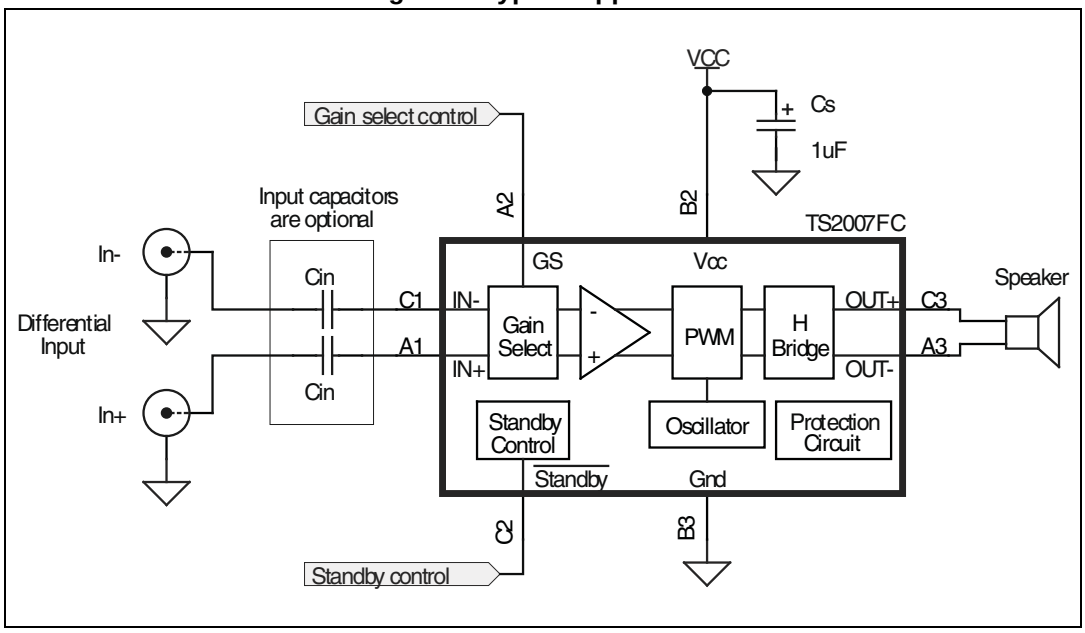


Table 4. Pin description

Pin name	Pin description
IN+	Positive differential input
VCC	Power supply
IN-	Negative differential input
GS	Gain select input
STDBY	Standby pin (active low)
GND	Ground
OUT+	Positive differential output
OUT-	Negative differential output

Figure 2. Typical application



Note: *See Section 4.10: Output filter considerations.*

3 Electrical characteristics

3.1 Electrical characteristics tables

Table 5. V_{CC} = +5 V, GND = 0 V, V_{ic} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current, no input signal, no load		2.5	4	mA
$I_{CC-STBY}$	Standby current(1), no input signal, V_{STBY} = GND		1	2	µA
V_{oo}	Output offset voltage, floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		 2.3 1.4 3 1.75		W
THD + N	Total harmonic distortion + noise P_o = 900 mW_{RMS}, G = 6 dB, F= 1 kHz, R_L = 8 Ω		0.12		%
Efficiency	Efficiency Po = 2.3 W_{rms}, R_L = 4 Ω (with LC output filter) Po = 1.4 W_{rms}, R_L = 8 Ω (with LC output filter)		 86 92		%
PSRR	Power supply rejection ratio with inputs grounded, C_{IN} = 1 µF (2) F= 217 Hz, R_L = 8 Ω, Gain = 6 dB, V_{ripple} = 200 mV_{pp} F= 217 Hz, R_L = 8 Ω, Gain = 12 dB, V_{ripple} = 200 mV_{pp}		 68 65		dB
CMRR	Common mode rejection ratio C_{in}=1 µF, R_L = 8 Ω 20 Hz < F< 20 kHz, Gain = 6 dB, ΔV_{ICM} = 200 mV_{pp}		60		dB
Gain	Gain value, Gs = 0 V Gain value, G_S = V_{CC}	11.5 5.5	12 6	12.5 6.5	dB
Z_{in}	Single ended input impedance (3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting), F = 1 kHz, Po = 1.9 W G = 6 dB, R_L = 4 Ω (with LC output filter)		93		dB
t_{WU}	Wake-up time		1	3	ms
t_{STBY}	Standby time		1		ms
V_N	Output voltage noise, F = 20 Hz to 20 kHz, R_L = 4 Ω Unweighted (filterless, G = 6 dB) A-weighted (filterless, G = 6 dB) Unweighted (with LC output filter, G = 6 dB) A-weighted (with LC output filter, G = 6 dB) Unweighted (filterless, G = 12 dB) A-weighted (filterless, G = 12 dB) Unweighted (with LC output filter, G = 12 dB) A-weighted (with LC output filter, G = 12 dB)		 87 60 83 58 106 77 101 75		$µV_{rms}$

1. Standby mode is active when V_{STBY} is tied to GND
2. Dynamic measurement - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ F =217 Hz.
3. Independent of gain configuration (6 or 12 dB) and between IN+ or IN- and GND

Table 6. V_{CC} = +4.2 V, GND = 0 V, V_{ic} = 2.1 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current, no input signal, no load		2	3.3	mA
$I_{CC-STBY}$	Standby current(1), no input signal, V_{STBY} = GND		0.85	2	µA
V_{oo}	Output offset voltage, floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		 1.6 0.95 2 1.2		W
THD + N	Total harmonic distortion + noise P_o = 600 mW_{rms}, G = 6 dB, F = 1 kHz, R_L = 8 Ω		0.09		%
Efficiency	Efficiency P_o = 1.6 W_{rms}, R_L = 4 Ω (with LC output filter) P_o = 0.95 W_{rms}, R_L = 8 Ω (with LC output filter)		 86 92		
PSRR	Power supply rejection ratio with inputs grounded, C_{in} = 1 µF(2) F = 217 Hz, R_L = 8 Ω, Gain = 6 dB, V_{ripple} = 200 mV_{pp} F = 217 Hz, R_L = 8 Ω, Gain = 12 dB, V_{ripple} = 200 mV_{pp}		 68 65		dB
CMRR	Common mode rejection ratio C_{in} = 1 µF, R_L = 8 Ω, 20 Hz < F< 20 kHz, Gain = 6 dB, ΔV_{ICM} = 200 mV_{pp}		60		
Gain	Gain value Gs = 0 V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	
Z_{IN}	Single ended input impedance(3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting), F = 1 kHz, Po = 1.3 W G = 6 dB, R_L = 4 Ω (with LC output filter)		92		dB
t_{WU}	Wake-up time		1	3	ms
t_{STBY}	Standby time		1		
V_N	Output voltage noise, F = 20 Hz to 20 kHz, R_L = 4 Ω Unweighted (filterless, G = 6 dB) A-weighted (filterless, G = 6 dB) Unweighted (with LC output filter, G = 6 dB) A-weighted (with LC output filter, G = 6 dB) Unweighted (filterless, G = 12 dB) A-weighted (filterless, G = 12 dB) Unweighted (with LC output filter, G = 12 dB) A-weighted (with LC output filter, G = 12 dB)		 86 59 82 57 105 74 100 74		$µV_{rms}$

1. Standby mode is active when V_{STBY} is tied to GND
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ F = 217 Hz
3. Independent of gain configuration (6 or 12 dB) and between IN+ or IN- and GND

Table 7. V_{CC} = +3.6 V, GND = 0 V, V_{ic} = 1.8 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current, no input signal, no load		1.7	3.1	mA
$I_{CC-STBY}$	Standby current(1), no input signal, V_{STBY} = GND		0.75	2	µA
V_{oo}	Output offset voltage, floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		 1.2 0.7 1.55 0.9		W
THD + N	Total harmonic distortion + noise P_o = 400 mW_{rms}, G = 6 dB, F = 1 kHz, R_L = 8 Ω		0.06		%
Efficiency	Efficiency P_o = 1.18 W_{rms}, R_L = 4 Ω (with LC output filter) P_o = 0.7 W_{rms}, R_L = 8 Ω (with LC output filter)		 86 92		
PSRR	Power supply rejection ratio with inputs grounded, C_{in} = 1 µF(2) F = 217 Hz, R_L = 8 Ω, Gain = 6 dB, V_{ripple} = 200 mV_{pp} F = 217 Hz, R_L = 8 Ω, Gain = 12 dB, V_{ripple} = 200 mV_{pp}		 68 65		dB
CMRR	Common mode rejection ratio C_{in} = 1 µF, R_L = 8 Ω, 20 Hz < F< 20 kHz, Gain = 6 dB, ΔV_{ICM} = 200 mV_{pp}		60		
Gain	Gain value Gs = 0 V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	
Z_{in}	Single ended input impedance(3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting), F=1 kHz, Po = 0.9 W G = 6 dB, R_L = 4 Ω (with LC output filter)		90		dB
t_{WU}	Wakeup time		1	3	ms
t_{STBY}	Standby time		1		
V_N	Output voltage noise, F = 20 Hz to 20 kHz, R_L = 4 Ω Unweighted (filterless, G = 6 dB) A-weighted (filterless, G = 6 dB) Unweighted (with LC output filter, G = 6 dB) A-weighted (with LC output filter, G = 6 dB) Unweighted (filterless, G = 12 dB) A-weighted (filterless, G = 12 dB) Unweighted (with LC output filter, G = 12 dB) A-weighted (with LC output filter, G = 12 dB)		 84 58 79 56 104 75 99 72		$µV_{RMS}$

1. Standby mode is active when V_{STBY} is tied to GND
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ F= 217 Hz
3. Independent of gain configuration (6 or 12 dB) and between IN+ or IN- and GND

Table 8. V_{CC} = +3.0 V, GND = 0 V, V_{ic} = 1.5 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current, no input signal, no load		1.5	2.9	mA
$I_{CC-STBY}$	Standby current(1), no input signal, V_{STBY} = GND		0.6	2	µA
V_{oo}	Output offset voltage, floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		 0.75 0.5 1 0.6		W
THD + N	Total harmonic distortion + noise P_o = 300 mW_{RMS}, G = 6 dB, F= 1 kHz, R_L = 8 Ω		0.04		%
Efficiency	Efficiency P_o = 0.8 W_{rms}, R_L = 4 Ω (with LC output filter) P_o = 0.5 W_{rms}, R_L = 8 Ω (with LC output filter)		 85 91		
PSRR	Power supply rejection ratio with inputs grounded, C_{in} = 1 µF (2) F = 217 Hz, R_L = 8 Ω, Gain = 6 dB, V_{ripple} = 200 mV_{pp} F = 217 Hz, R_L = 8 Ω, Gain = 12 dB, V_{ripple} = 200 mV_{pp}		 68 65		dB
CMRR	Common mode rejection ratio C_{in} = 1 µF, R_L = 8 Ω, 20 Hz < F< 20 kHz, Gain = 6 dB, ΔV_{ICM} = 200 mV_{pp}		60		
Gain	Gain value Gs = 0 V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	
Z_{in}	Single ended input impedance(3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting), F=1 kHz, Po = 0.6 W G = 6 dB, R_L = 4 Ω (with LC output filter)		89		dB
t_{WU}	Wakeup time		1	3	ms
t_{STBY}	Standby time		1		
V_N	Output voltage noise, F = 20 Hz to 20 kHz, R_L = 4 Ω Unweighted (filterless, G = 6 dB) A-weighted (filterless, G = 6 dB) Unweighted (with LC output filter, G = 6 dB) A-weighted (with LC output filter, G = 6 dB) Unweighted (filterless, G = 12 dB) A-weighted (filterless, G = 12 dB) Unweighted (with LC output filter, G = 12 dB) A-weighted (with LC output filter, G = 12 dB)		 82 57 78 55 103 74 99 71		$µV_{RMS}$

1. Standby mode is active when V_{STBY} is tied to GND
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ F = 217 Hz
3. Independent of gain configuration (6 or 12 dB) and between IN+ or IN- and GND

Table 9. V_{CC} = +2.7 V, GND = 0 V, V_{ic} = 1.35 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current, no input signal, no load		1.45	2.5	mA
$I_{CC-STBY}$	Standby current(1), no input signal, V_{STBY} = GND		0.5	2	µA
V_{oo}	Output offset voltage, floating inputs, R_L = 8 Ω			25	mV
P_o	Output power THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		 0.64 0.39 0.83 0.49		W
THD + N	Total harmonic distortion + noise P_o = 250 mW_{rms}, G = 6 dB, F = 1 kHz, R_L = 8 Ω		0.03		%
Efficiency	Efficiency P_o = 0.64 W_{rms}, R_L = 4 Ω (with LC output filter) P_o = 0.39 W_{rms}, R_L = 8 Ω (with LC output filter)		 84 91		
PSRR	Power supply rejection ratio with inputs grounded, C_{in} = 1 µF (2) F= 217 Hz, R_L = 8 Ω, Gain = 6 dB, V_{ripple} = 200 mV_{pp} F= 217 Hz, R_L = 8 Ω, Gain = 12 dB, V_{ripple} = 200 mV_{pp}		 68 65		dB
CMRR	Common mode rejection ratio C_{in} = 1 µF, R_L = 8 Ω, 20 Hz < F< 20 kHz, Gain = 6 dB, ΔV_{ICM} = 200 mV_{pp}		60		
Gain	Gain value Gs = 0 V G_S = V_{CC}	 11.5 5.5	 12 6	 12.5 6.5	
Z_{in}	Single ended input impedance(3)	68	75	82	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting), F=1 kHz, Po = 0.5 W G = 6 dB, R_L = 4 Ω (with LC output filter)		88		dB
t_{WU}	Wakeup time		1	3	ms
t_{STBY}	Standby time		1		
V_N	Output voltage noise, F = 20 Hz to 20 kHz, R_L = 4 Ω Unweighted (filterless, G = 6 dB) A-weighted (filterless, G = 6 dB) Unweighted (with LC output filter, G = 6 dB) A-weighted (with LC output filter, G = 6 dB) Unweighted (filterless, G = 12 dB) A-weighted (filterless, G = 12 dB) Unweighted (with LC output filter, G = 12 dB) A-weighted (with LC output filter, G = 12 dB)		 82 56 77 55 100 73 98 70		$µV_{RMS}$

1. Standby mode is active when V_{STBY} is tied to GND
2. Dynamic measurements - 20*log(rms(Vout)/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ F= 217 Hz
3. Independent of gain configuration (6 or 12 dB) and between IN+ or IN- and GND

3.2 Electrical characteristic curves

The graphs shown in this section use the following abbreviations:

- R_L+ 15 µH or 30 µH = pure resistor + very low series resistance inductor
- Filter = LC output filter (1 µF+ 30 µH for 4 Ω and 0.5 µF+15 µH for 8 Ω)

All measurements are made with C_{S1} = 1 µF and C_{S2} = 100 nF (*Figure 3*), except for the PSRR where C_{S1} is removed (*Figure 4*).

Figure 3. Test diagram for measurements

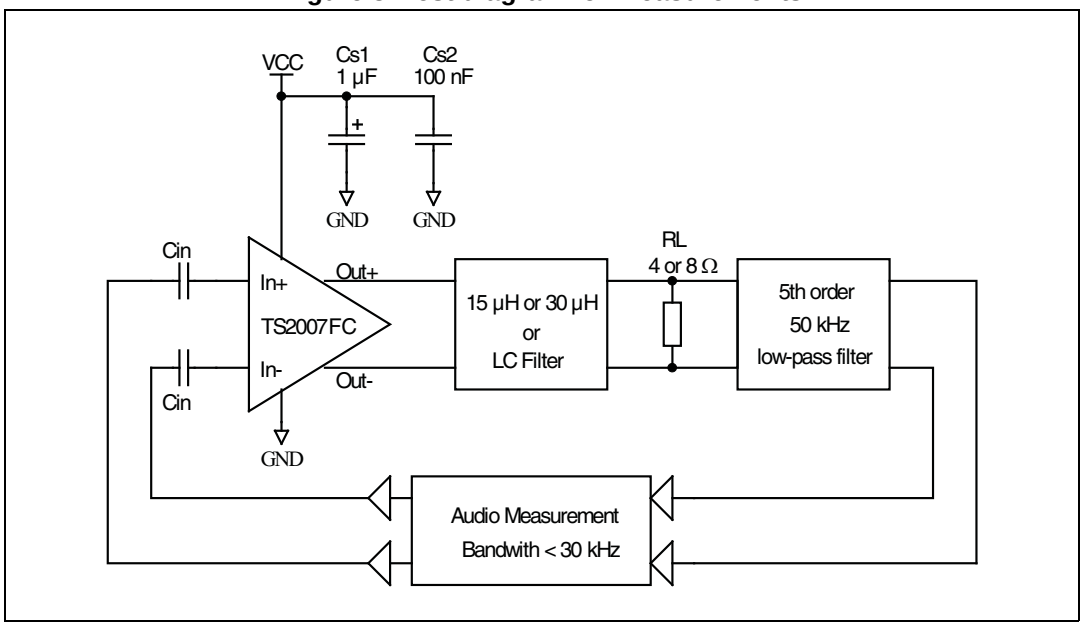
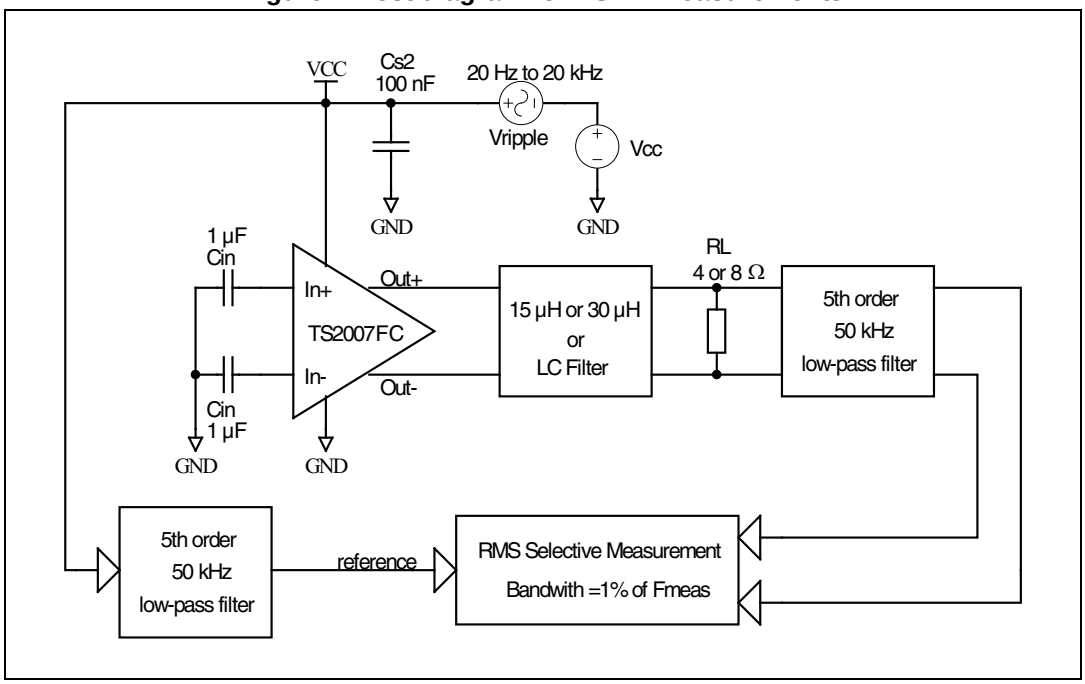


Figure 4. Test diagram for PSRR measurements



A list of the graphs shown in this section is provided in *Table 10*.

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Figure 5. Current consumption vs. power supply voltage

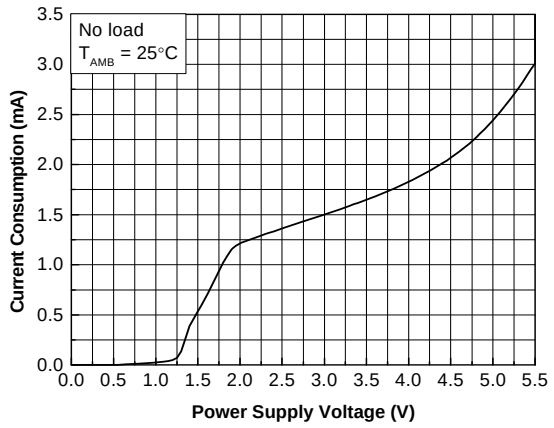


Figure 6. Standby current vs. power supply voltage

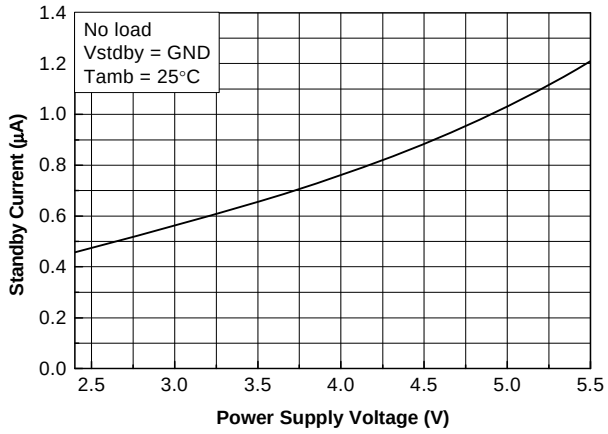


Figure 7. Current consumption vs. standby voltage

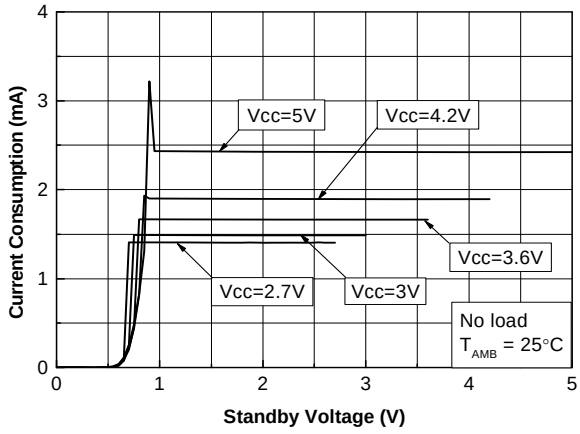


Figure 8. Efficiency vs. output power @ 5 V and 4 Ω

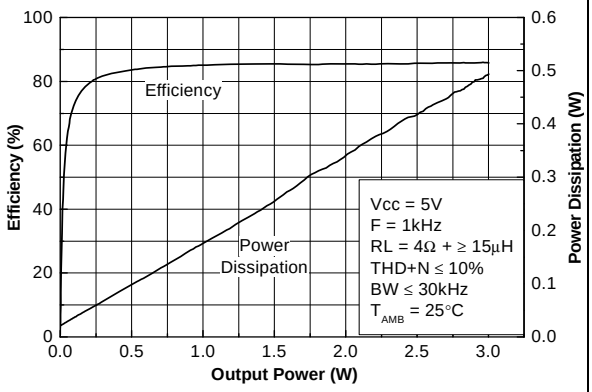


Figure 9. Efficiency vs. output power @ 5 V and 8 Ω

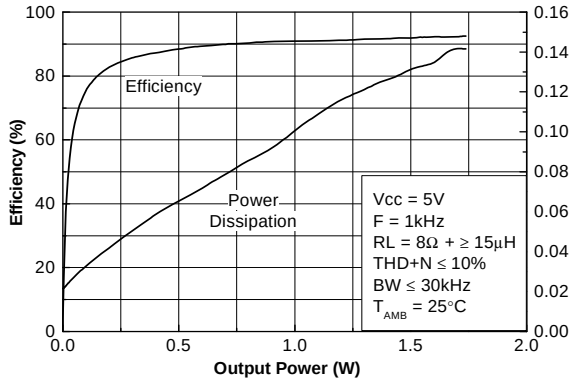


Figure 10. Efficiency vs. output power @ 3.6 V and 4 Ω

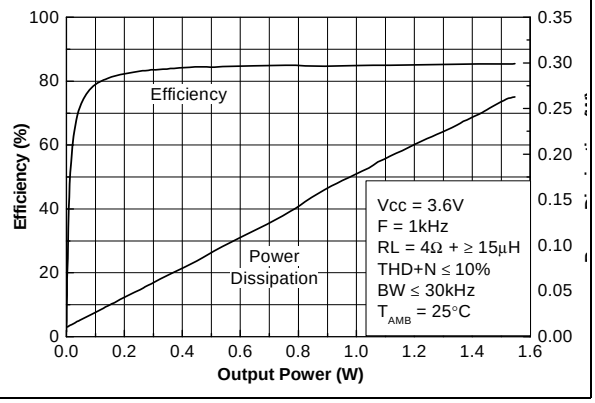


Figure 11. Efficiency vs. output power @ 3.6 V and 8 Ω

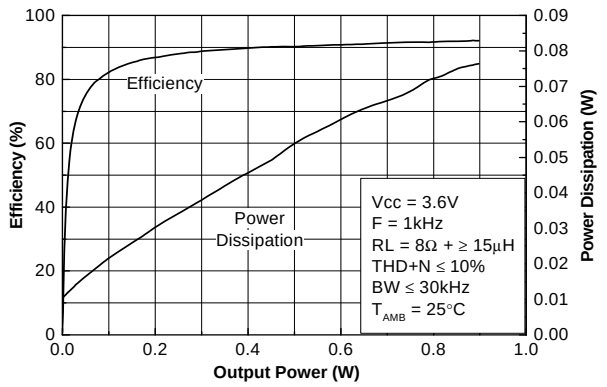


Figure 12. Efficiency vs. output power @ 2.7 V and 4 Ω

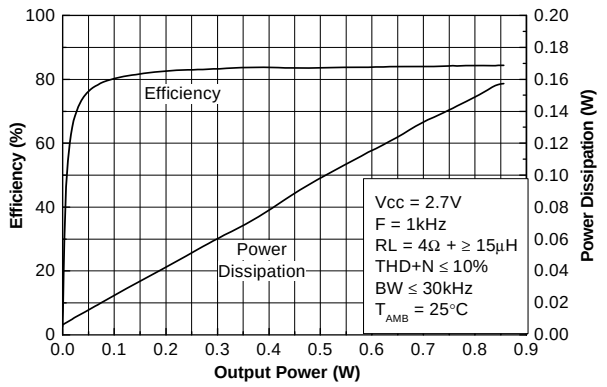


Figure 13. Efficiency vs. output power @ 2.7 V and 8 Ω

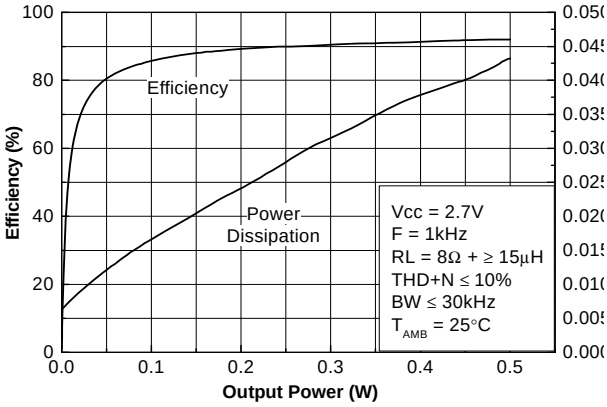


Figure 14. Output power vs. power supply voltage @ 1% THD+N

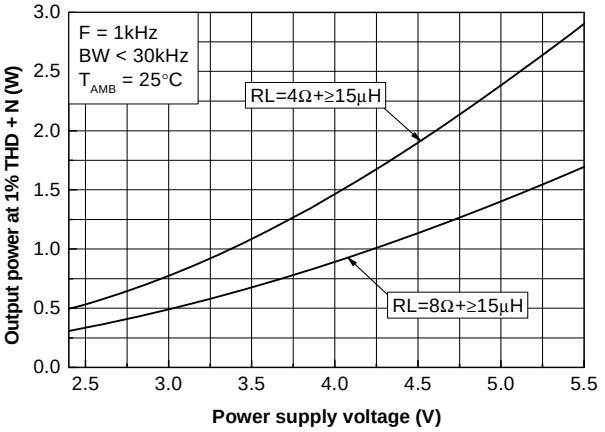


Figure 15. Output power vs. power supply voltage @ 10% THD+N

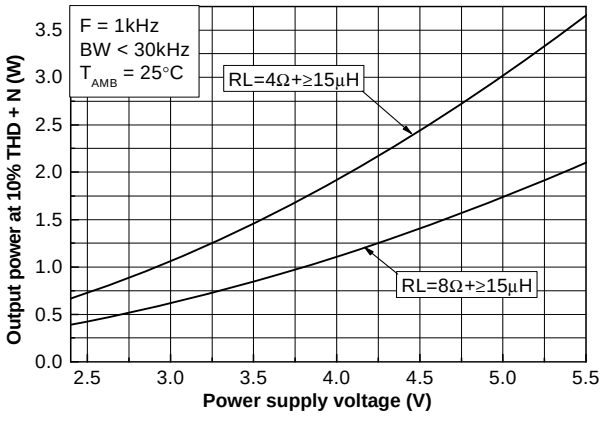


Figure 16. THD+N vs. output power @ 4 Ω and 100 Hz

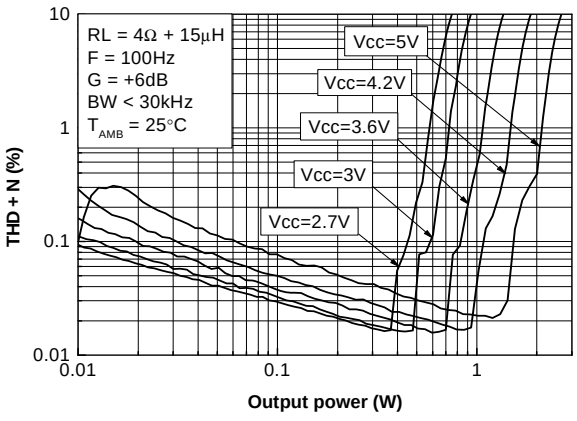


Figure 17. THD+N vs. output power @ 8 Ω and 100 kHz

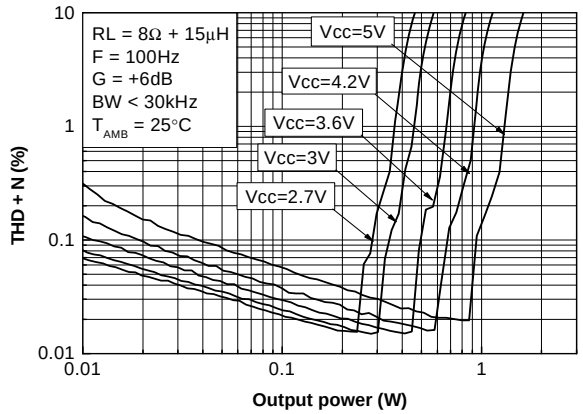


Figure 18. THD+N vs. frequency @ 4 Ω and 1 kHz

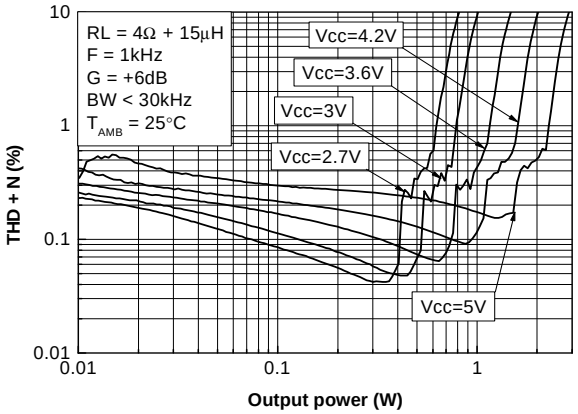


Figure 19. THD+N vs. output power @ 8 Ω and 1 kHz

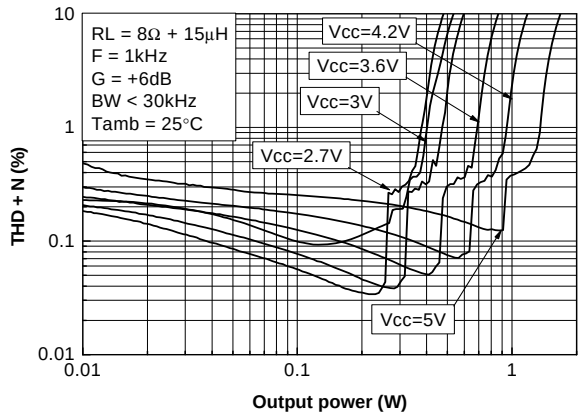


Figure 20. THD+N vs. frequency @ 5 V and 4 Ω

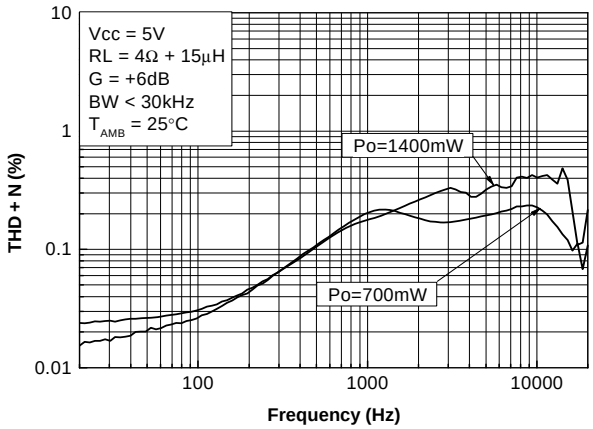


Figure 21. THD+N vs. frequency @ 5 V and 8 Ω

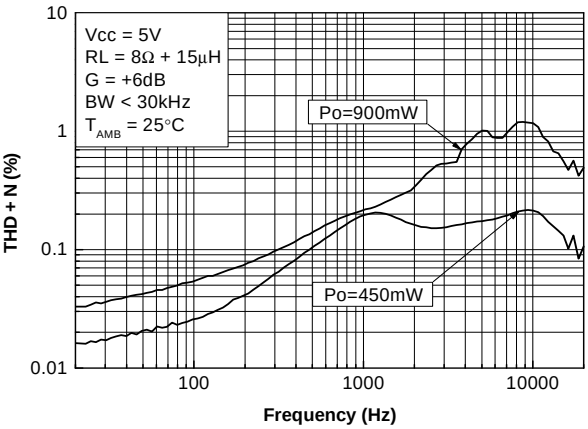


Figure 22. THD+N vs. frequency @ 4.2 V and 4 Ω

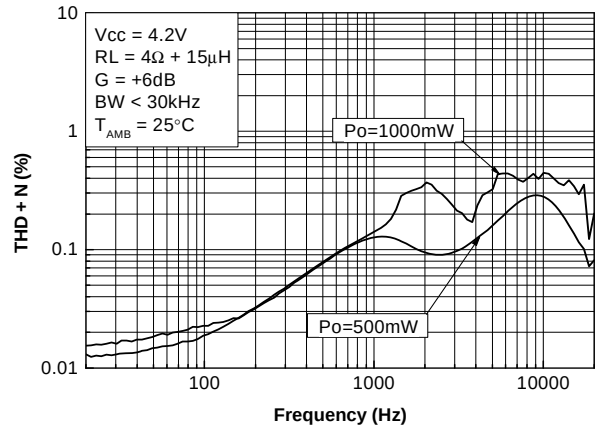


Figure 23. THD+N vs. frequency @ 4.2 V and 8 Ω

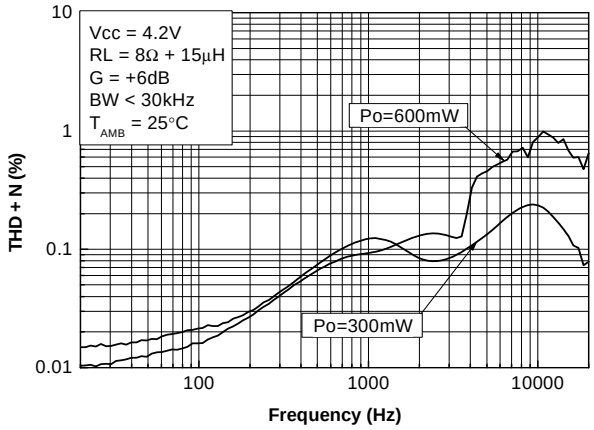


Figure 24. THD+N vs. frequency @ 3.6 V and 4 Ω

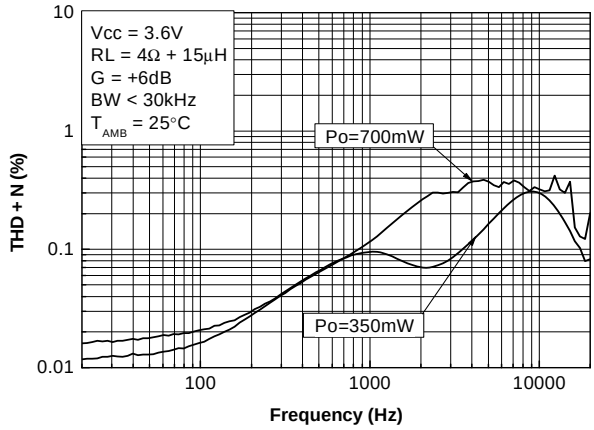


Figure 25. THD+N vs. frequency @ 3.6 V and 8 Ω

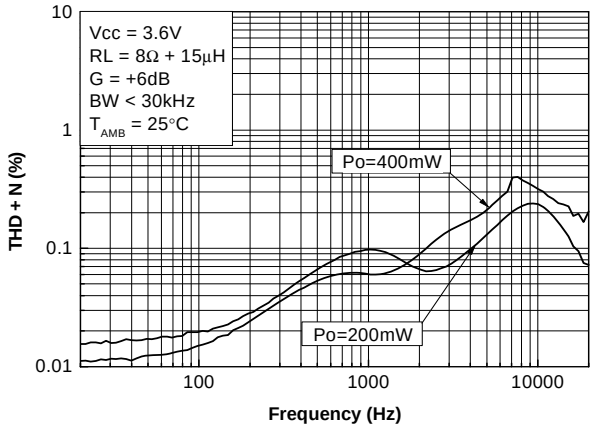


Figure 26. THD+N vs. frequency @ 3 V and 4 Ω

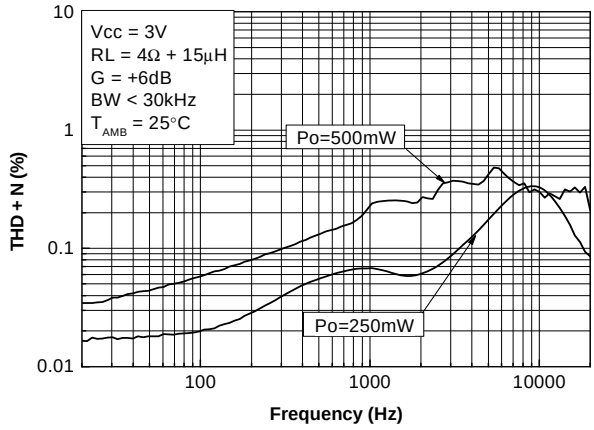


Figure 27. THD+N vs. frequency @ 3 V and 8 Ω

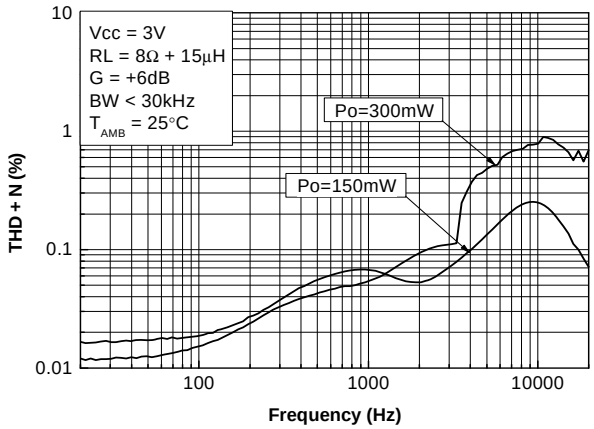


Figure 28. THD+N vs. frequency @ 2.7 V and 4 Ω

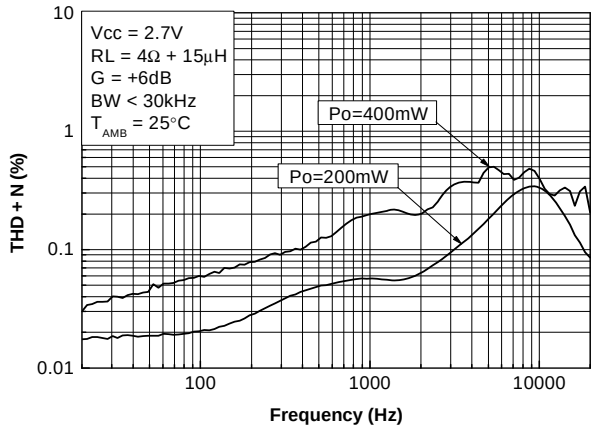


Figure 29. THD+N vs. frequency @ 2.7 V and 8 Ω

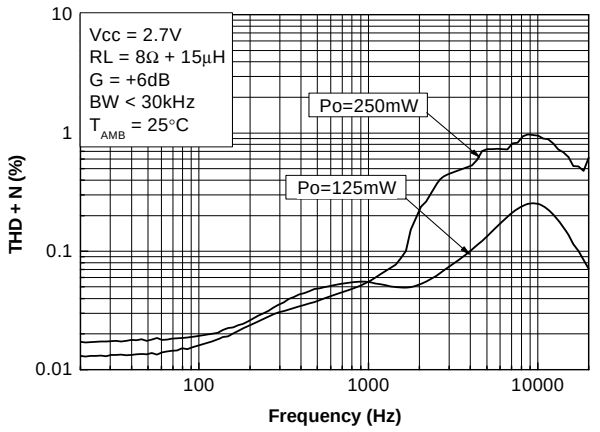


Figure 30. PSRR vs. frequency

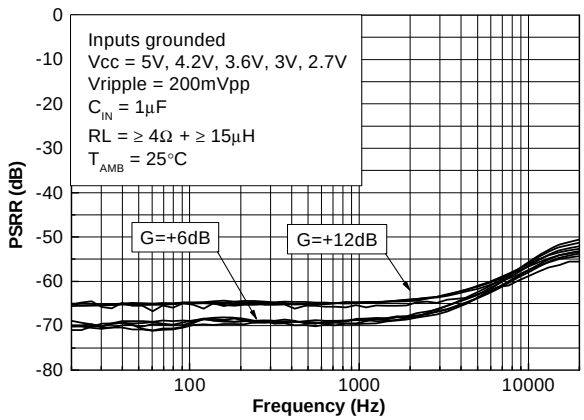


Figure 31. PSRR vs. common mode input voltage @ +6 dB gain

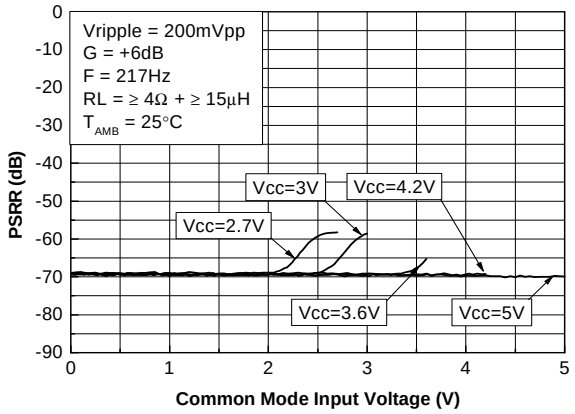


Figure 32. PSRR vs. common mode input voltage @ +12 dB gain

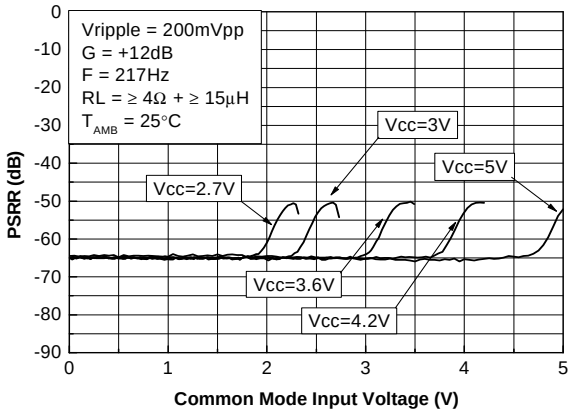


Figure 33. CMRR vs. frequency

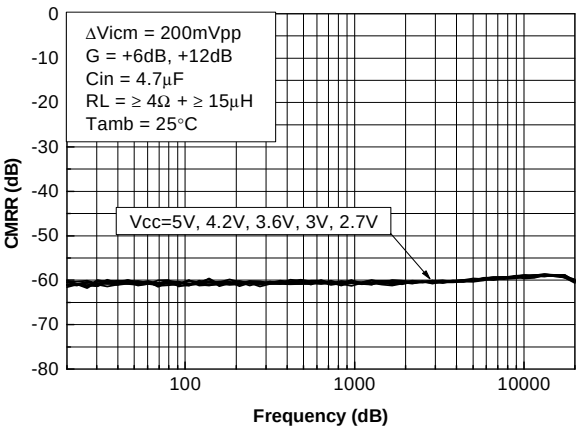


Figure 34. CMRR vs. common mode input voltage @ +6 dB gain

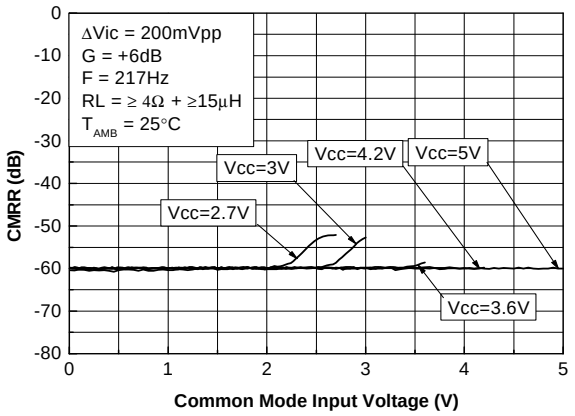


Figure 35. CMRR vs. common mode input voltage @ +12 dB gain

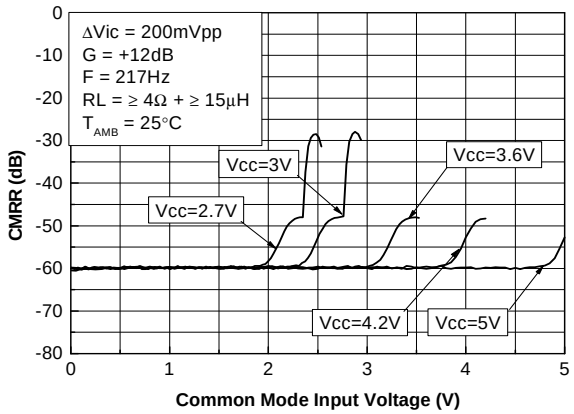


Figure 36. Gain vs. frequency @ +6 dB gain

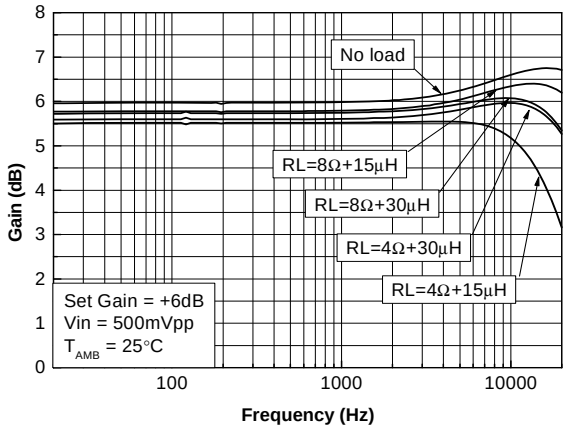


Figure 37. Gain vs. frequency @ +12 dB gain

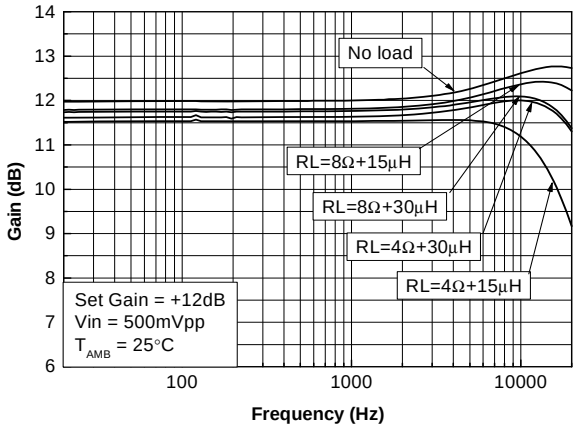


Figure 38. Output offset vs. common mode input voltage @ 5 V

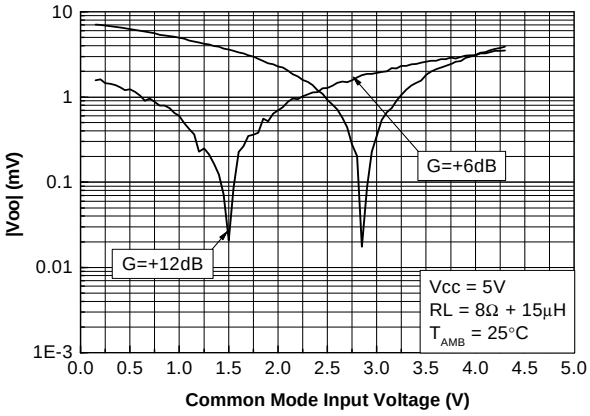


Figure 39. Output offset vs. common mode input voltage @ 3.6 V

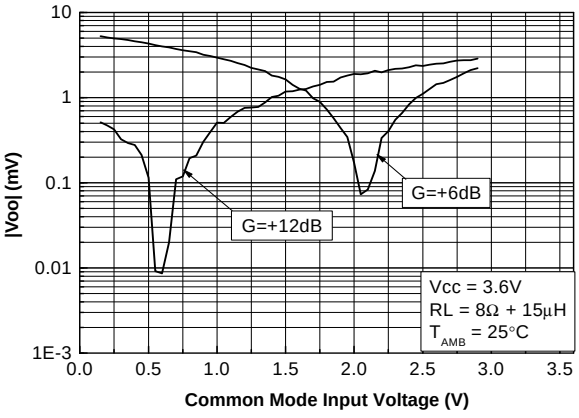


Figure 40. Output offset vs. common mode input voltage @ 2.7 V

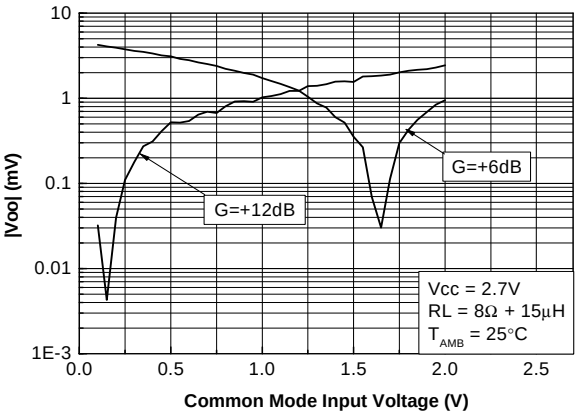


Figure 41. Power derating curves

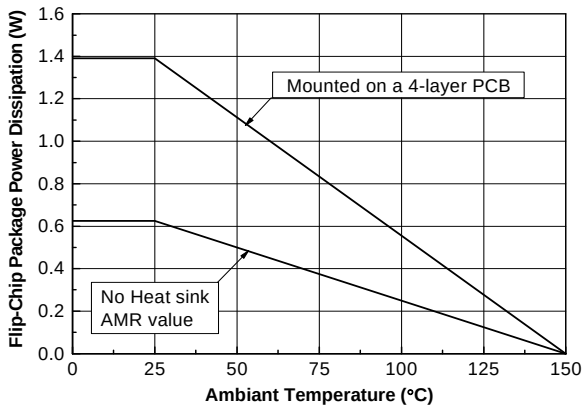


Figure 42. Startup and shutdown phase V_{CC} = 5 V, G = 6 dB, C_{in} = 1 µF, inputs grounded

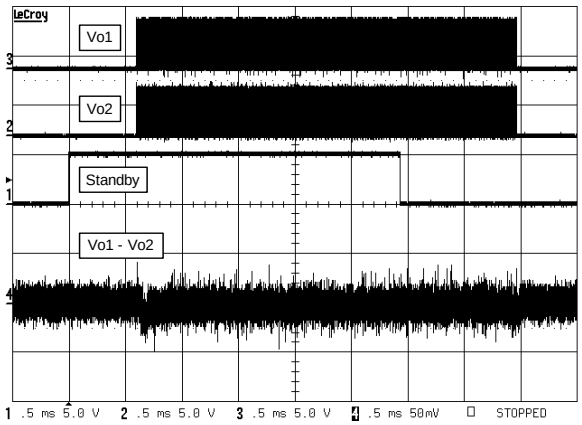


Figure 43. Startup and shutdown phase V_{CC} = 5 V, G = 6 dB, C_{in} = 1 µF, V_{in} = 1 V_{pp}, F = 10 kHz

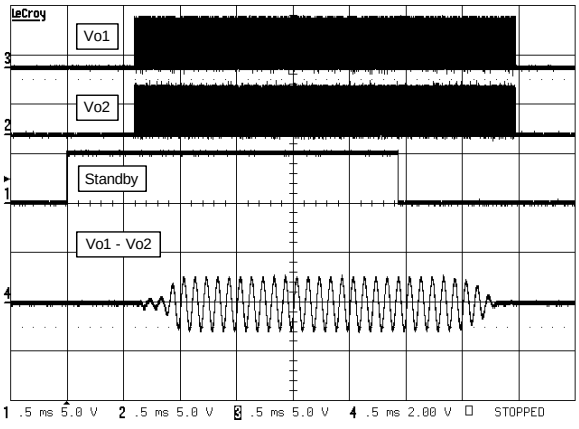
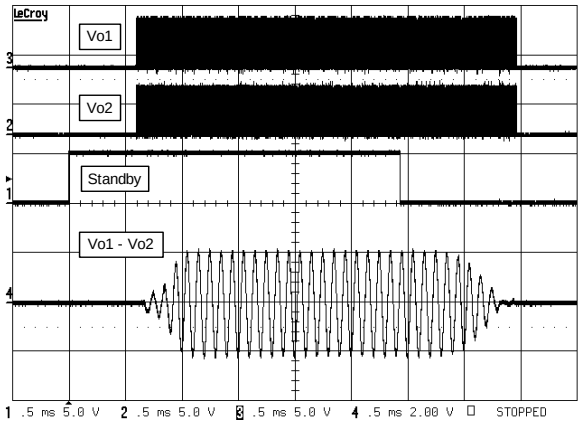


Figure 44. Startup and shutdown phase V_{CC} = 5 V, G = 12 dB, C_{in} = 1 µF, V_{in} = 1 V_{pp}, F = 10 kHz



4 Application information

4.1 Differential configuration principle

The TS2007FC is a monolithic, fully-differential input/output, class-D power amplifier. It includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ in the range of DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and consequently, maximizes the output power. In addition, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

A fully-differential amplifier has the following **advantages**:

- High PSRR (power supply rejection ratio)
- High CMRR (common mode noise rejection
- Virtually zero pop without additional circuitry, giving a faster startup time than conventional single-ended input amplifiers
- Easy interfacing with a differential output audio DAC
- No input coupling capacitors required since there is a common mode feedback loop

4.2 Gain settings

In the flat region of the frequency-response curve (no input coupling capacitor or internal feedback loop + load effect), the differential gain can be set to either 6 or 12 dB depending on the logic level of the GS pin.

Table 11. GS pin gains

GS pin	Gain (dB)	Gain (V/V)
1	6 dB	2
0	12 dB	4

Note: Between the GS pin and V_{CC} there is an internal 300 kΩ resistor. When the pin is floating the gain is 6 dB. In standby mode, this internal resistor is disconnected (HiZ input).

4.3 Common mode feedback loop limitations

The common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

Due to the V_{icm} limitation of the input stage (see *Table 2: Operating conditions*), the common mode feedback loop can fulfill its role only within the defined range.

4.4 Low frequency response

If a low frequency bandwidth limitation is required, it is possible to use input coupling capacitors. In the low frequency region, the input coupling capacitor C_{in} has a greater effect. C_{in} and the input impedance Z_{in} form a first-order high-pass filter with a -3 dB cutoff frequency (see *Table 5* to *Table 9*).

$$F_{CL} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot C_{in}}$$

where F_{CL} = cutoff frequency

So, for a desired cutoff frequency we can calculate C_{in} as follows:

$$C_{in} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot F_{CL}}$$

where F_{CL} is expressed in Hz, Z_{in} in Ω, and C_{in} in F.

The input impedance, Z_{in}, is for the whole power supply voltage range, typically 75 kΩ. There is also a tolerance around the typical value (see *Table 5* to *Table 9*). The tolerance of F_{CL} can also be calculated:

- $F_{CLmax} = 1.103 \cdot F_{CL}$
- $F_{CLmin} = 0.915 \cdot F_{CL}$

4.5 Circuit decoupling

A power supply capacitor, referred to as C_S, is needed to correctly bypass the TS2007FC.

The TS2007FC has a typical switching frequency of 280 kHz and an output fall and rise time of less than or equal to 5 ns. Due to these very fast transients, careful decoupling is mandatory.

A 1 µF ceramic capacitor is enough, but it must be located very close to the TS2007FC in order to avoid any extra parasitic inductance created by a long track wire. Parasitic loop inductance, in relation with di/dt, introduces overvoltage that decreases the global efficiency of the device and may cause, if this parasitic inductance is too high, a TS2007FC breakdown. For filtering low frequency noise signals on the power line, it is recommended to use a capacitor of at least 1 µF.

In addition, even if a ceramic capacitor has an adequate high frequency ESR (equivalent series resistance) value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4 Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1 µF/6.3 V capacitor used at 5 V, can loose about 50% of its value. With a power supply voltage of 5 V, the decoupling value, instead of 1 µF, can be reduced to 0.5 µF. As C_S has particular influence on the THD+N in the medium to high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots which can be problematic if they reach the power supply AMR value (6 V).

4.6 Wakeup time (t_{wu})

When the standby is released to set the device ON, there is a wait of 1 ms typically. The TS2007FC has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

Note: The gain increases smoothly (see Figure 43 and Figure 44) from the mute to the gain selected by the GS pin (Section 4.2).

4.7 Shutdown time

When the standby command is set to high, the time required to put the two output stages into high impedance and to put the internal circuitry in shutdown mode, is typically 1 ms. This time is used to decrease the gain and avoid any pop noise during shutdown.

Note: The gain decreases smoothly until the outputs are muted (see Figure 43 and Figure 44).

4.8 Consumption in shutdown mode

Between the shutdown pin and GND there is an internal 300 kΩ resistor. This resistor forces the TS2007FC to be in shutdown when the shutdown input is left floating.

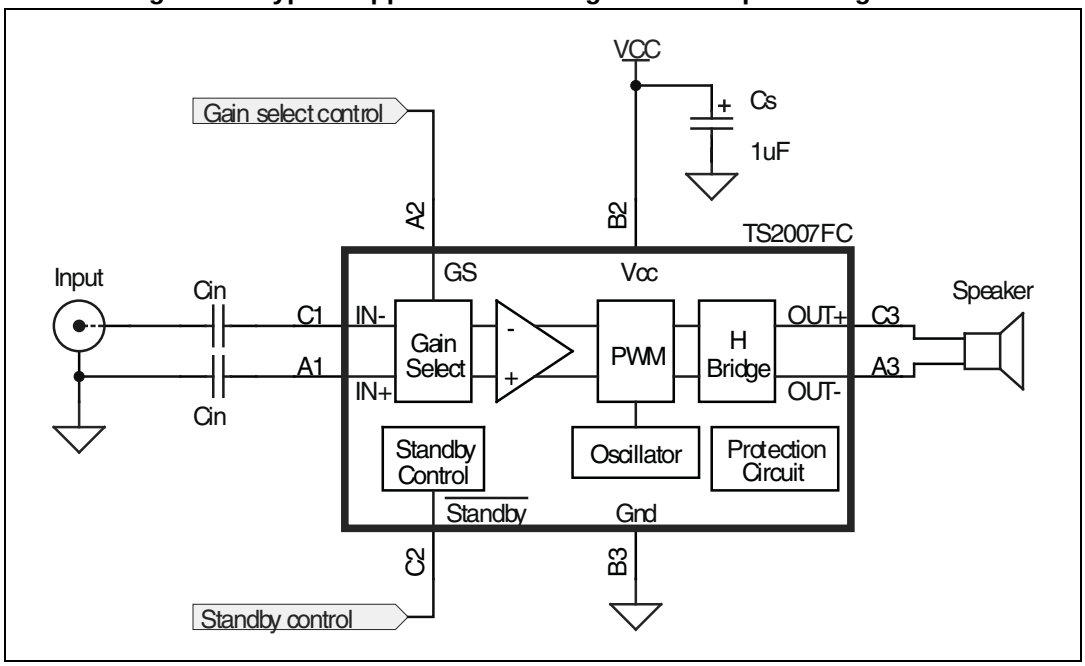
However, this resistor also introduces additional shutdown power consumption if the shutdown pin voltage does not equal 0 V. This extra current is provided by the device that drives the standby pin of the amplifier.

Referring to *Table 2: Operating conditions*, with a 0.4 V shutdown voltage pin for example, you must add 0.4 V/300 k = 1.3 µA in typical (0.4 V/273 k = 1.46 µA maximum) to the shutdown current specified in *Table 5* to *Table 9*.

4.9 Single-ended input configuration

It is possible to use the TS2007FC in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The following schematic diagram shows a typical single-ended input application.

Figure 45. Typical application for single-ended input configuration



4.10 Output filter considerations

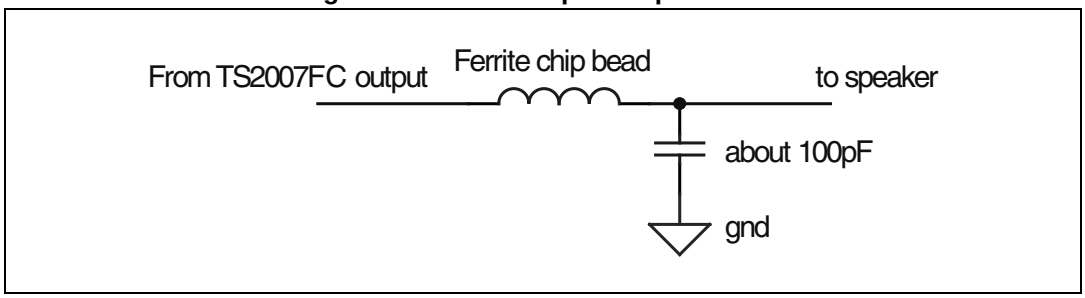
The TS2007FC is designed to operate without an output filter. However, due to very sharp transients on the TS2007FC output, EMI radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS2007FC outputs and loudspeaker terminal are long (typically more than 50 mm, or 100 mm in both directions). As the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow:

- Reduce, as much as possible, the distance between the TS2007FC output pins and the speaker terminals
- Use a ground plane for shielding sensitive wires
- Place, as close as possible to the TS2007FC and in series with each output, a ferrite bead with a rated current of minimum 2.5 A and impedance greater than 50 Ω at frequencies above 30 MHz
- Allow an extra footprint to place, if necessary, a capacitor to short perturbations to ground (*Figure 46*)

Figure 46. Ferrite chip bead placement



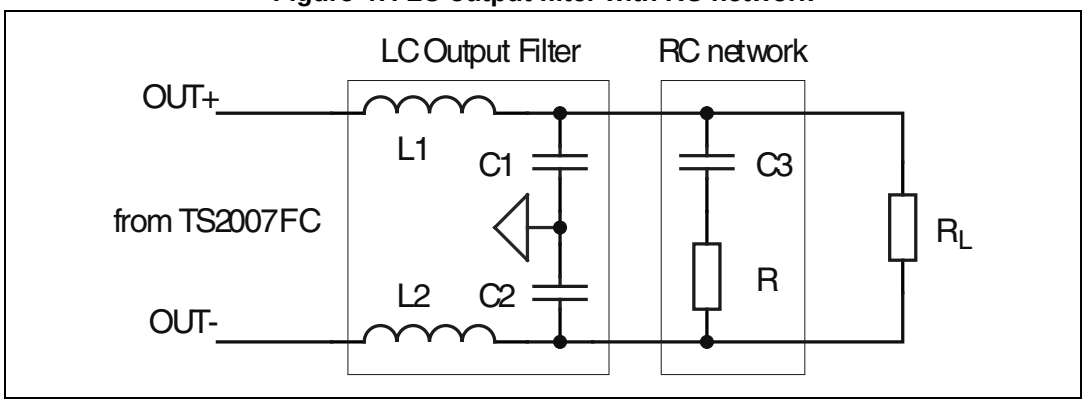
In the case where the distance between the TS2007FC output and the speaker terminals is too long, it is possible to have low frequency EMI issues due to the fact that the typical operating PWM frequency is 280 kHz and the fall and rise time of the output signal is less than or equal to 5 ns. In this configuration, it is necessary to use the output filter shown in *Figure 47*, that consists of L1, C1, L2, and C2 as close as possible to the TS2007FC outputs.

When an output filter is used and there exists a possibility to disconnect a load, it is recommended to use an RC network that consists of C3 and R as shown in *Figure 47*. In this case, when the output filter is connected without any load, the filter acts like a short-circuit for input frequencies above 10 kHz. The RC network corrects the frequency response of the output filter and compensates this limitation.

Table 12. Example of component choice

Component	R_L = 4 Ω	R_L = 8 Ω
L1	15 µH/1.4 A	30 µH/0.7 A
L2		
C1	2 µF/10 V	1 µF/10 V
C2		
C3	1 µF/10 V	
R	22 Ω/0.25 W	47 Ω/0.25 W

Figure 47. LC output filter with RC network



4.11 Short-circuit protection

The TS2007FC includes an output short-circuit protection. This protection prevents the device from being damaged if there are fault conditions on the amplifier outputs.

When a channel is in operating mode and a short-circuit occurs directly between two outputs (Out+ and Out-) or between an output and ground (Out+ and GND or Out- and GND), the short-circuit protection detects this situation and puts the amplifier into standby. To put the amplifier back into operating mode, put the standby pin to logical LO and then to logical HI.

4.12 Thermal shutdown

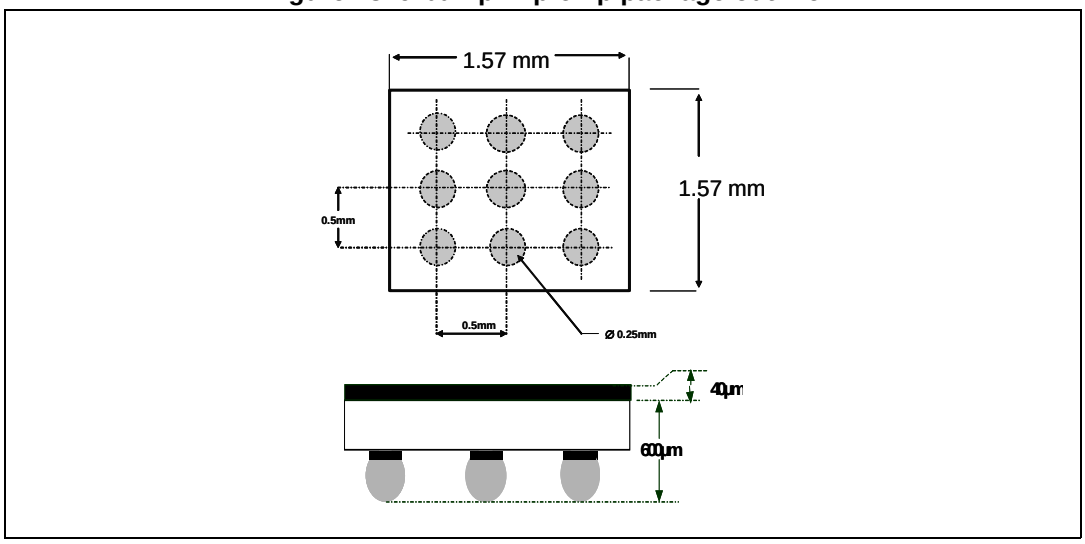
The TS2007FC device has an internal thermal shutdown protection in the event of extreme temperatures to protect the device from overheating. Thermal shutdown is active when the device reaches 150 °C. When the temperature decreases to a safe level, the circuit switches back to normal operation.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK is an ST trademark.

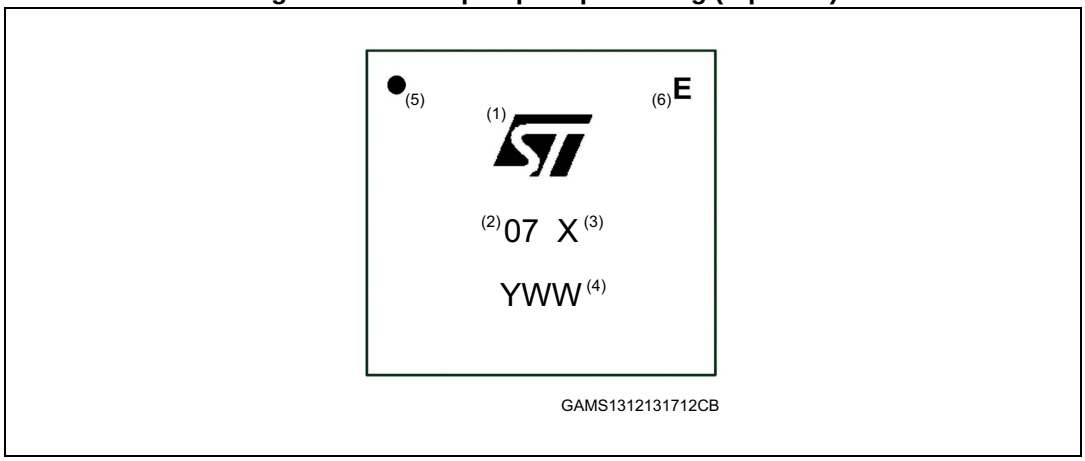
5.1 9-bump Flip-chip package information

Figure 48. 9-bump Flip-chip package outline



1. Die size: 1.57 mm x 1.57 mm ±30 µm
   Die height (including bumps): 600 µm
   Bump diameter: 315 µm ±50 µm
   Bump diameter before reflow: 300 µm ±10 µm
   Bump height: 250 µm ±40 µm
   Die height: 350 µm ±20 µm
   Pitch: 500 µm ±50 µm
   Back coating layer height (optional): 40 µm ±10 µm
   Coplanarity: 50 µm max.

Figure 49. 9-bump Flip-chip marking (top view)



1. Logo: ST
2. First two digits for part number: 07
3. Third digit for assembly plant: X
4. Three digit date code: YWW
5. Dot indicates pin A1
6. “E” symbol for lead free

6 Ordering information

Table 13. Order codes

Order code	Temperature range	Package	Marking
TS2007EIJT	-40° C to +85° C	Flip-chip	07

7 Revision history

Table 14. Document revision history

Date	Revision	Changes
19-Aug-2008	1	Initial release.
17-May-2011	2	Added minimum R_L to *Table 1: Absolute maximum ratings (AMR)* Updated ECOPACK® paragraph in *Section 5: Package information* Minor textual updates
28-Feb-2014	3	Removed pinout from cover page and added it to *Section 2: Application information*. *Table 1: Absolute maximum ratings (AMR)*: updated Updated following figure titles: *Figure 8* through to *Figure 29*; *Figure 31* and *Figure 32*; *Figure 34* through to *Figure 40*. *Section 5.1: 9-bump Flip-chip package information*: updated section layout. *Figure 49: 9-bump Flip-chip marking (top view)*: changed marking from “K7” to “07”. *Table 13: Order codes*: updated order code markings
15-Apr-2019	4	Removed the part number TS2007EKIJT.