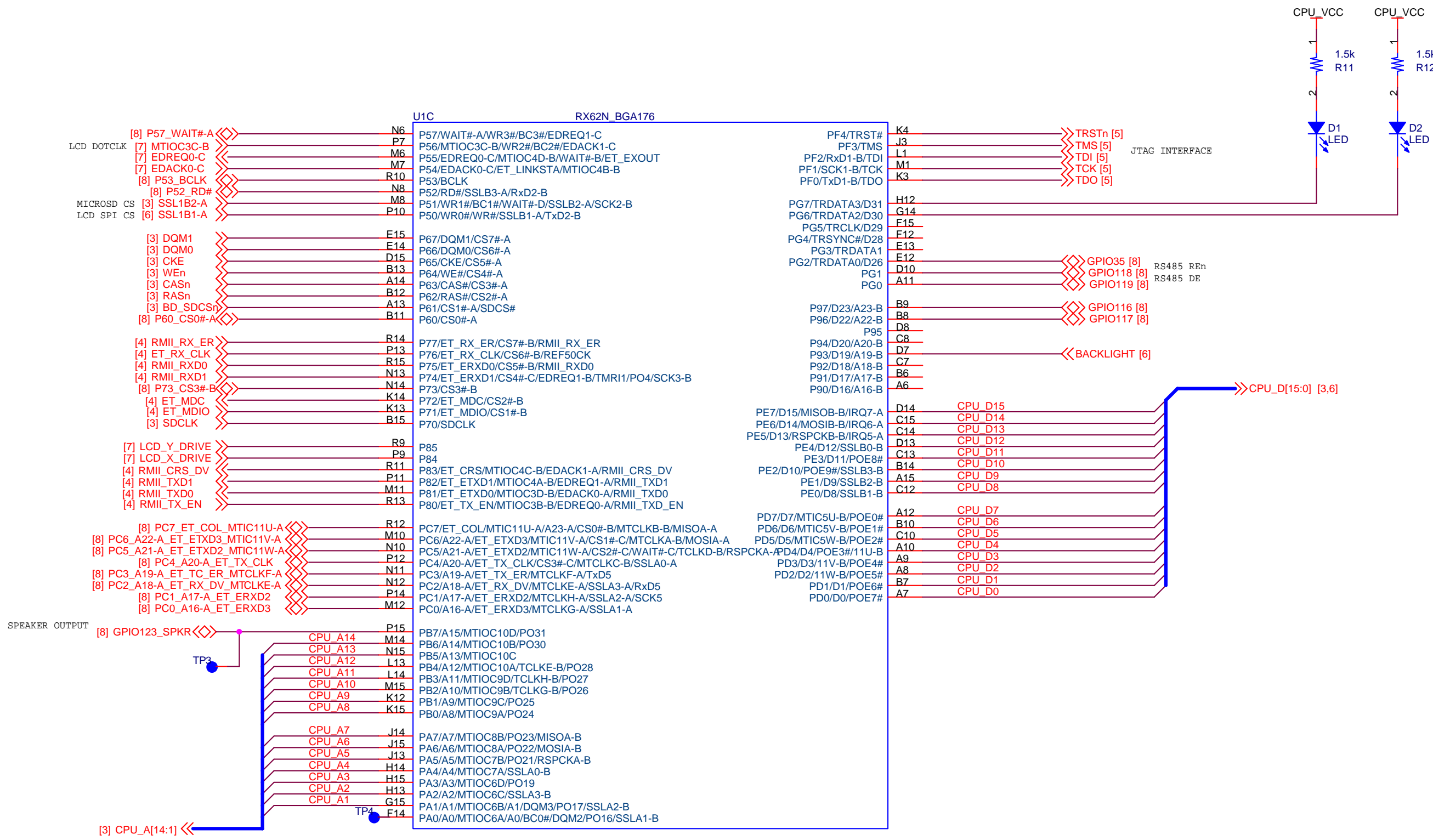
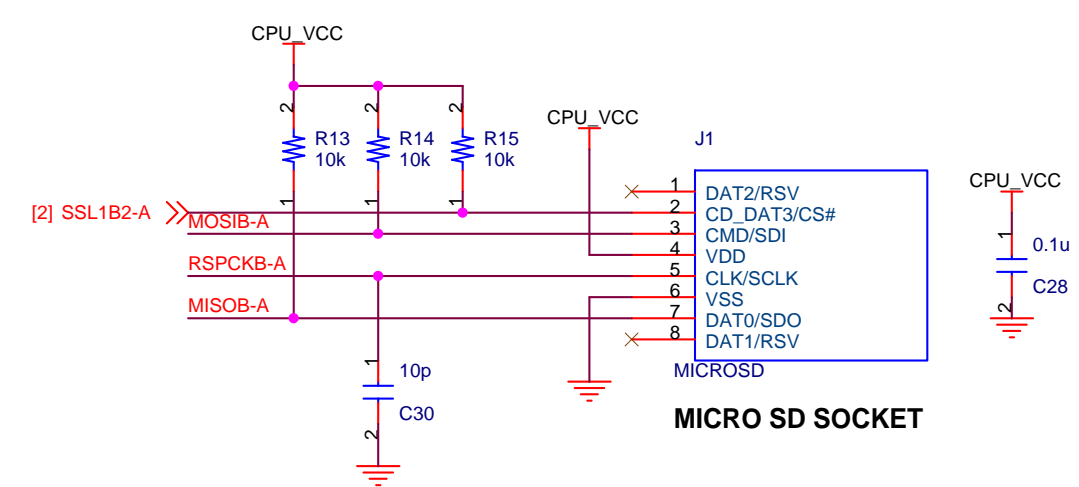
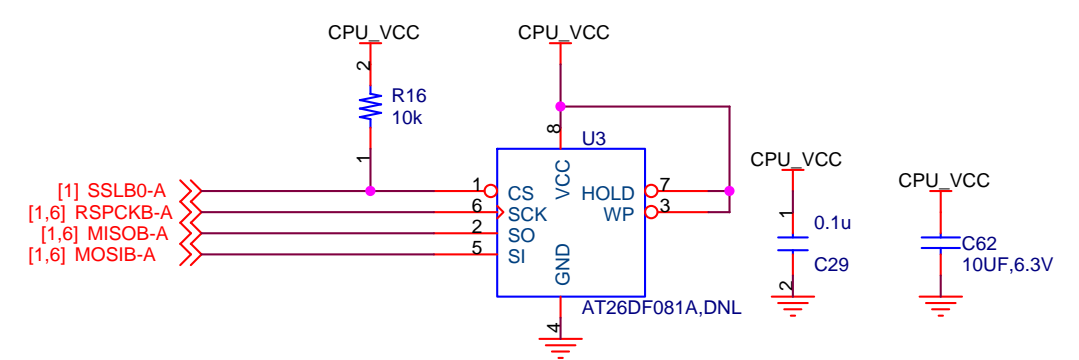
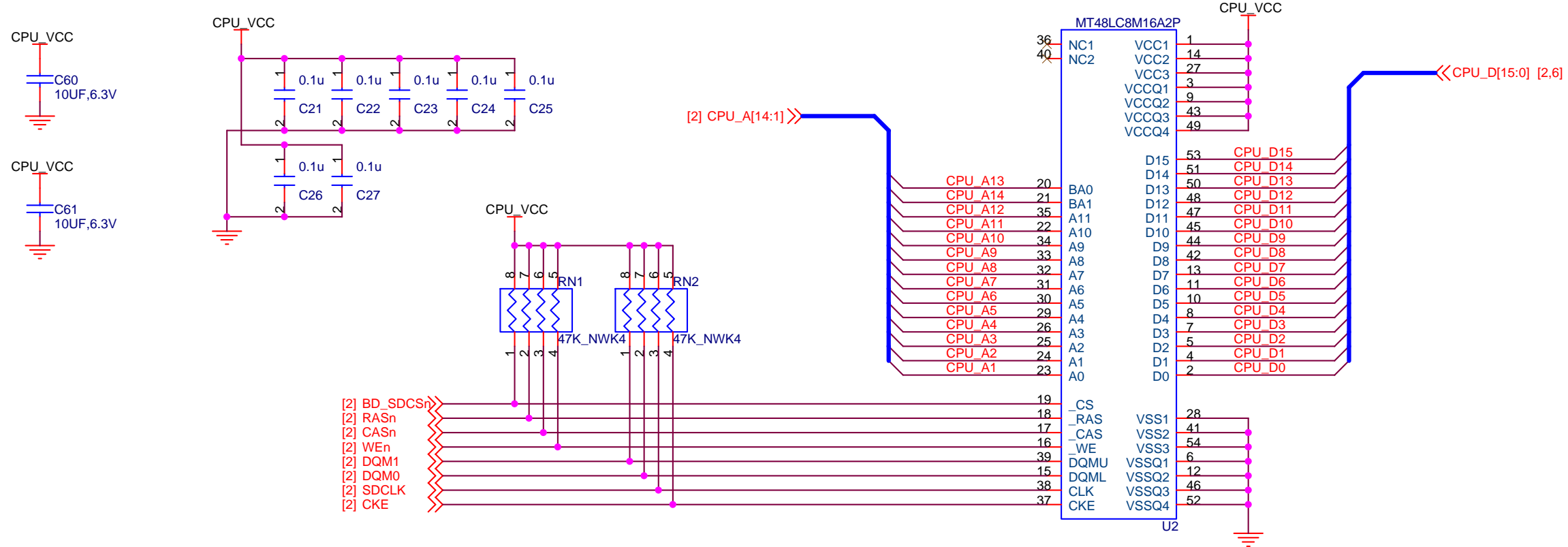


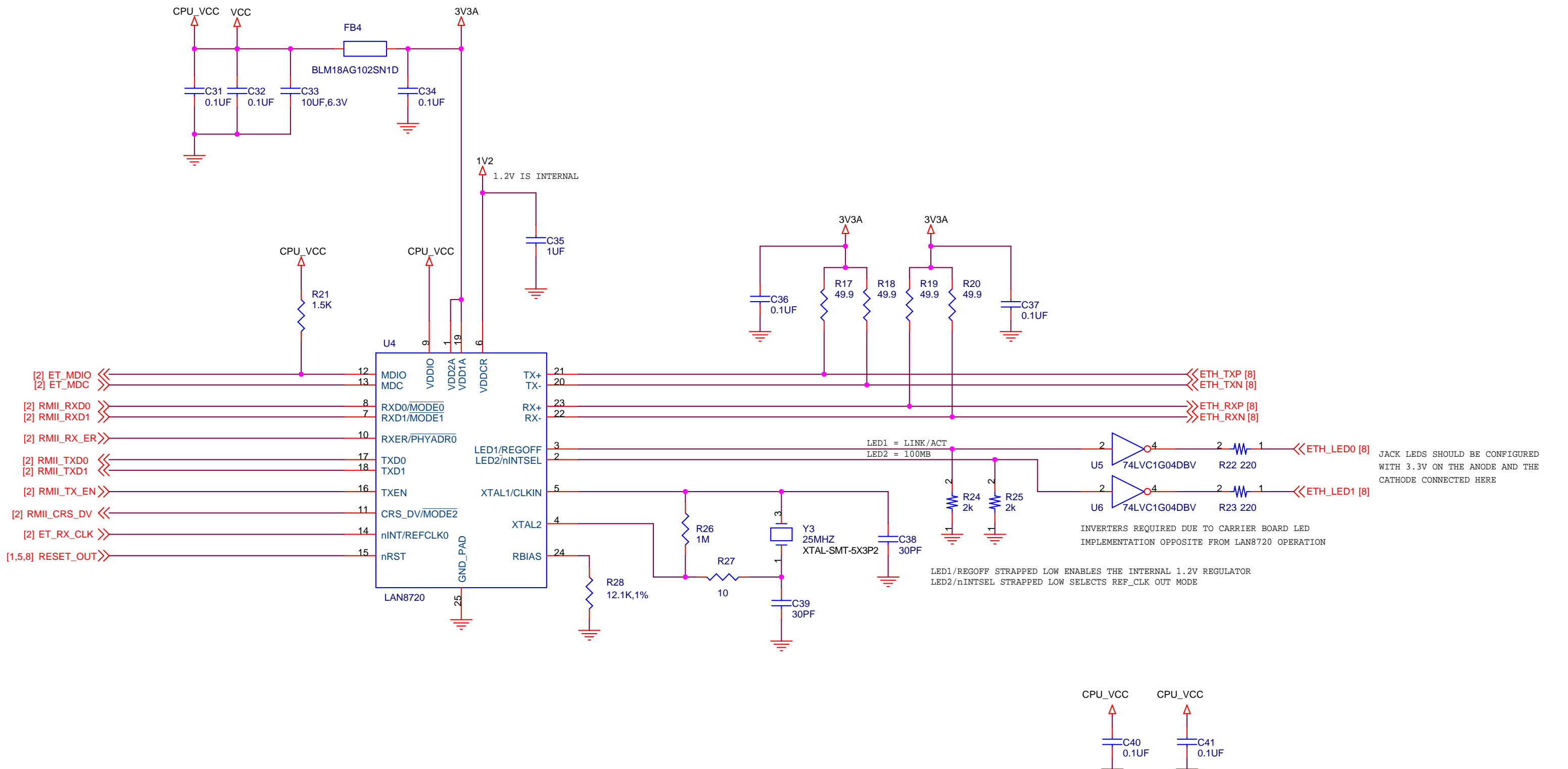
FUTURE DESIGNS, INC.		
Title: CPU IO AND POWER		
Size:	Document Number: SOMDIMM-RX62N	Rev: 1x
Date:	Monday, October 04, 2010	Sheet 1 of 8



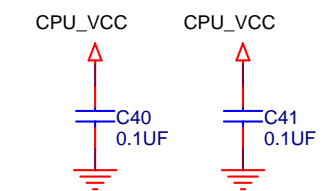
FUTURE DESIGNS, INC.		
Title: CPU MEMORY IO JTAG		
Size: B	Document Number: SOMDIMM-RX62N	Rev: 1x
Date: Monday, October 04, 2010	Sheet: 2	of 8



FUTURE DESIGNS, INC.		
Title SDRAM MEMORY EEPROM MICROSD		
Size B	Document Number SOMDIMM-RX62N	Rev 1x
Date: Monday, October 04, 2010	Sheet 3	of 8



ETHERNET



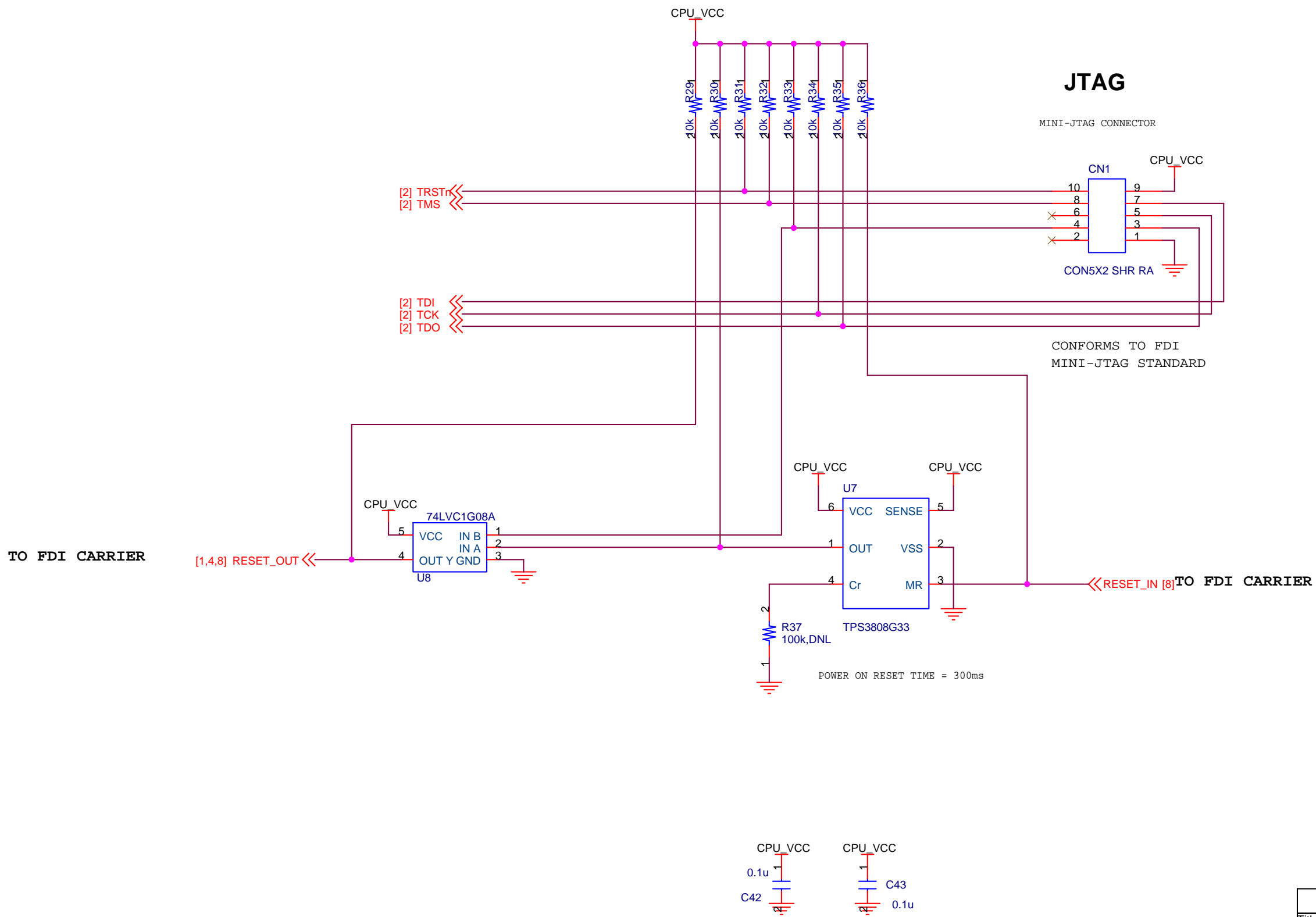
LED1 = LINK/ACT
LED2 = 100MB

JACK LEDS SHOULD BE CONFIGURED WITH 3.3V ON THE ANODE AND THE CATHODE CONNECTED HERE

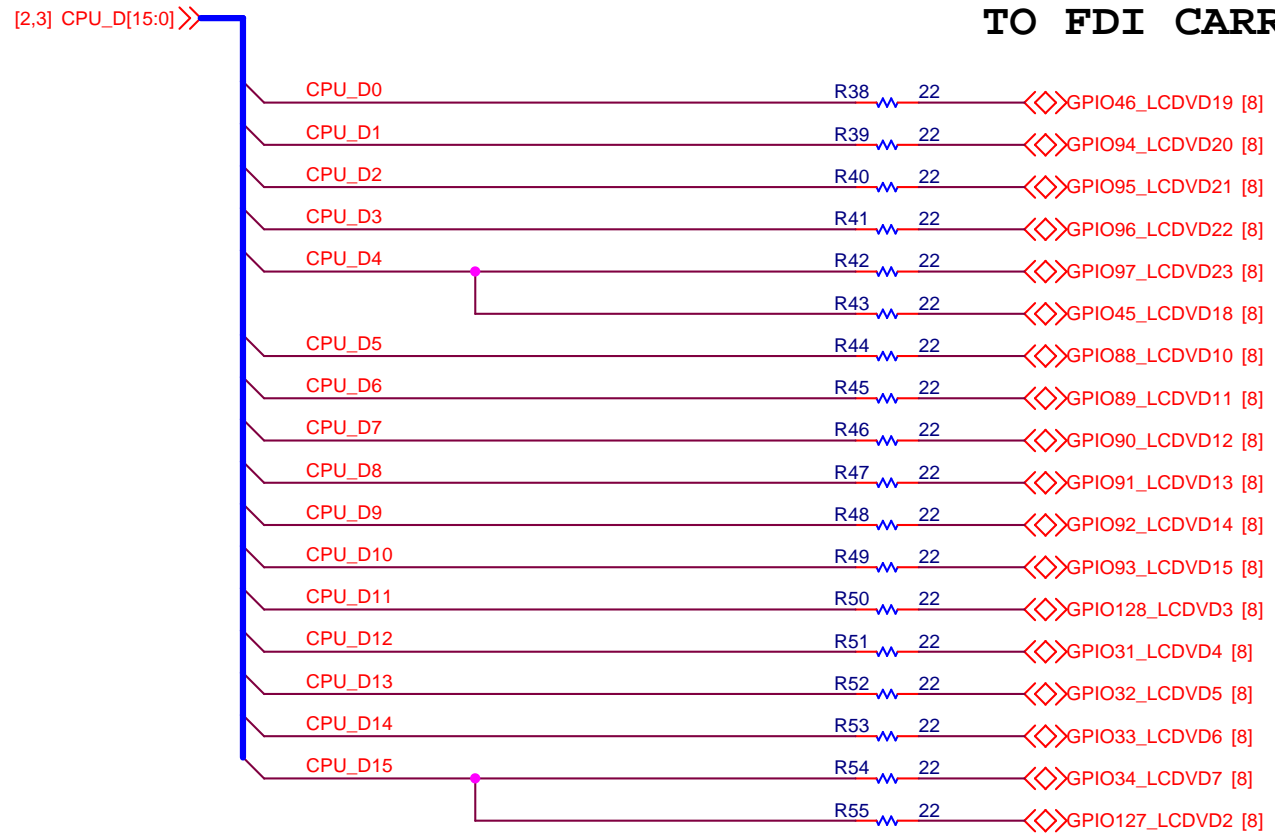
INVERTERS REQUIRED DUE TO CARRIER BOARD LED IMPLEMENTATION OPPOSITE FROM LAN8720 OPERATION

LED1/REGOFF STRAPPED LOW ENABLES THE INTERNAL 1.2V REGULATOR
LED2/nINTSEL STRAPPED LOW SELECTS REF_CLK OUT MODE

FUTURE DESIGNS, INC.		
Title ETHERNET		
Size B	Document Number SOMDIMM-RX62N	Rev 1x
Date: Monday, October 04, 2010	Sheet 4	of 8



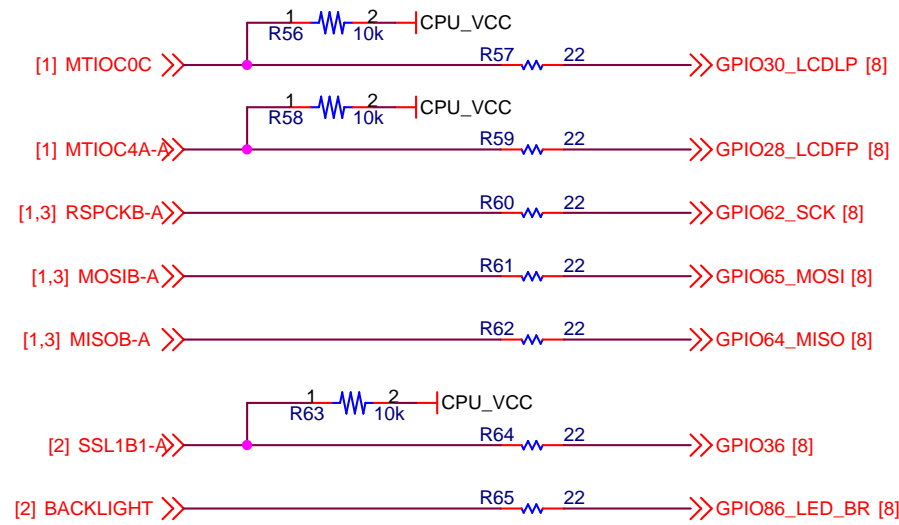
FUTURE DESIGNS, INC.		
Title SW, JTAG, Reset, SD		
Size B	Document Number SOMDIMM-RX62N	Rev 1x
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CPU_D0 = BLUE1 = LCDVD19
 |
 CPU_D4 = BLUE5 = LCDVD23
 LCDVD18 = LCDVD23

CPU_D5 = GREEN0 = LCDVD10
 |
 CPU_D10 = GREEN5 = LCDVD15

CPU_D11 = RED1 = LCDVD3
 |
 CPU_D15 = RED5 = LCDVD7
 LCDVD2 = LCDVD7



HORIZONTAL SYNC

VERTICAL SYNC

SPI CLOCK

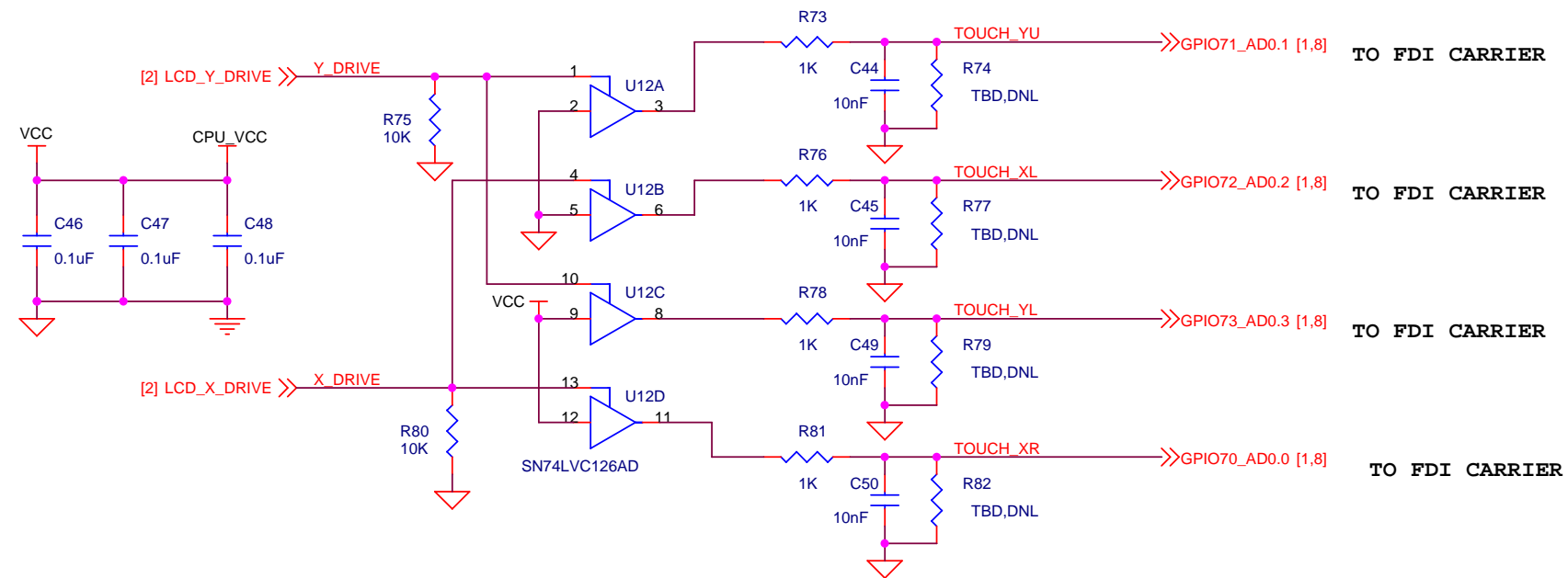
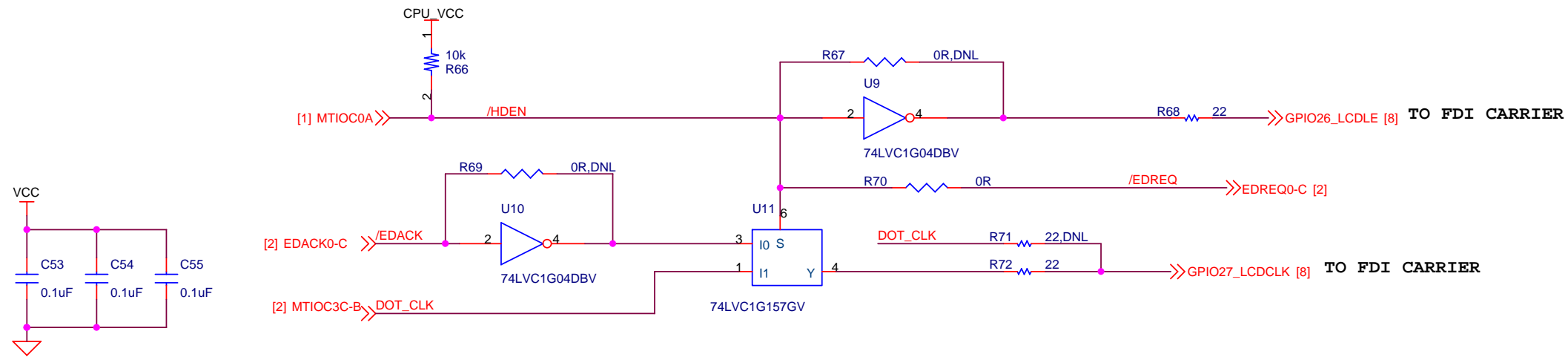
SPI MASTER DATA OUT

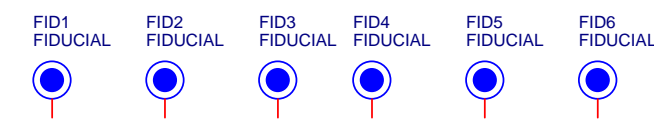
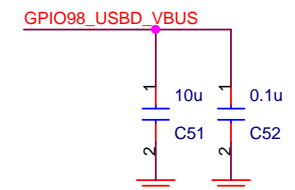
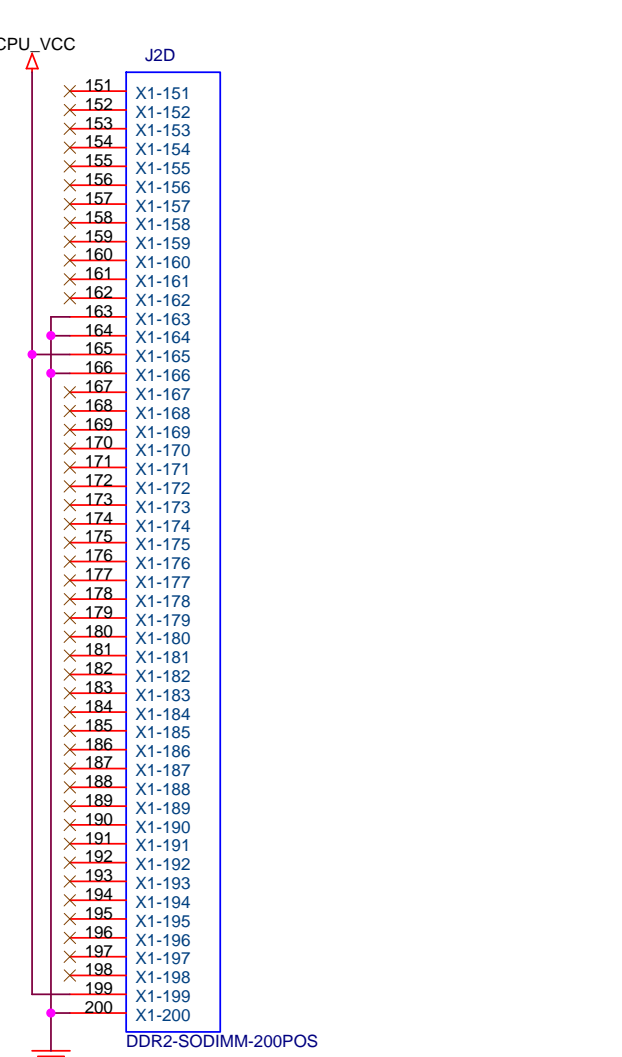
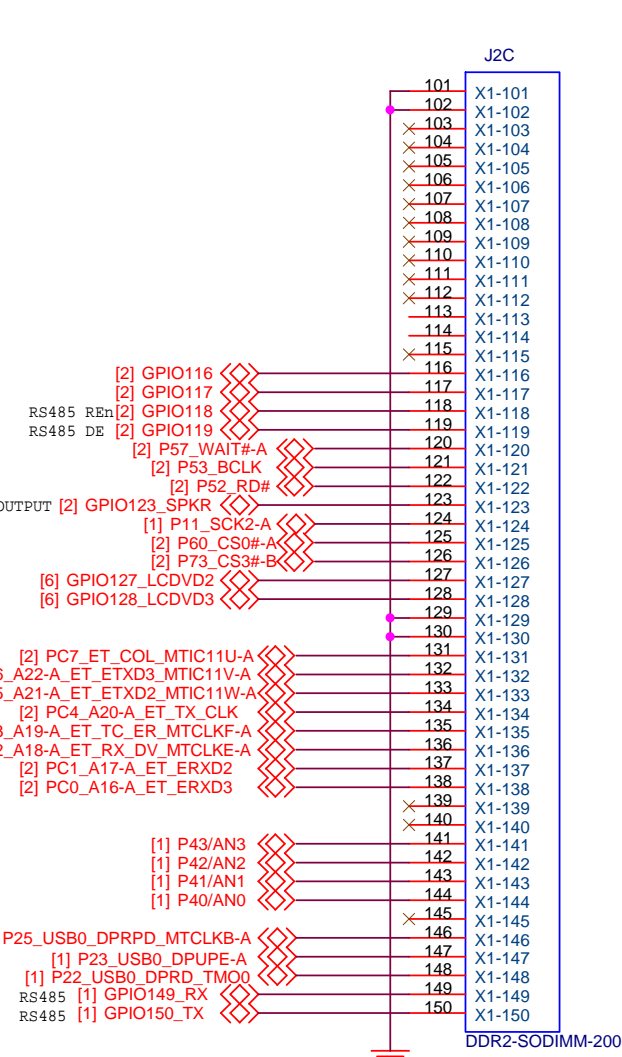
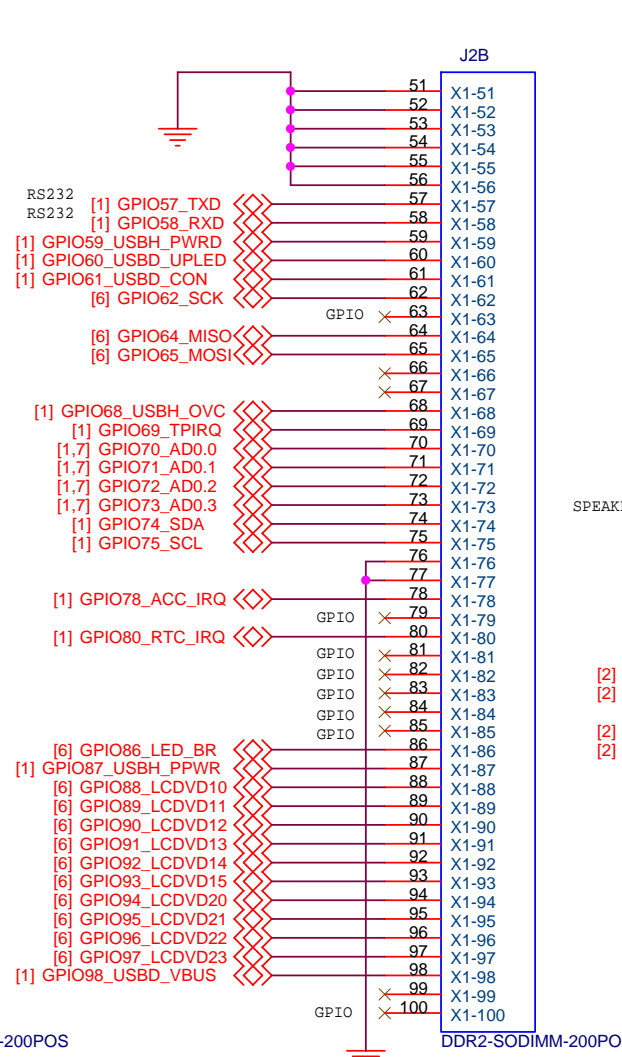
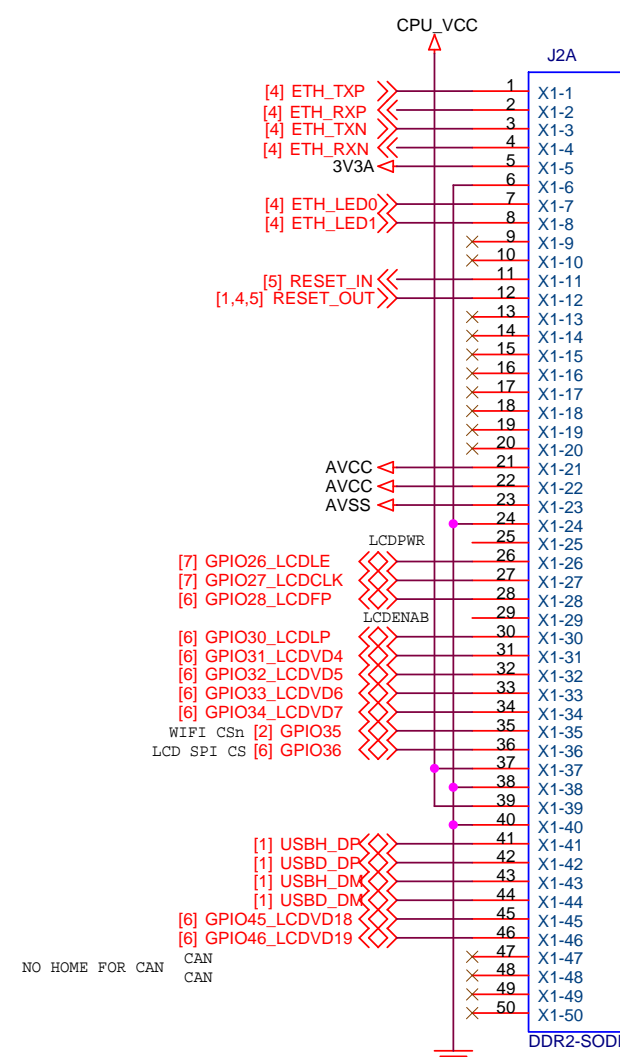
SPI MASTER DATA IN

SPI CHIP SELECT

BACKLIGHT PWM

FUTURE DESIGNS, INC.		
Title LCD INTERFACE		
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FUTURE DESIGNS, INC.		
Title SODIMM EDGE FINGERS		
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