LM2770,LM2852,LM3200,LM3671,LP3970

Power Management Design for Applications Processors

Literature Number: SNVA589

POWER | designer

Expert tips, tricks, and techniques for powerful designs

No. 105

Power Management Design for Applications Processors

— *By Jim Y. Wong, Principal Applications Engineer*

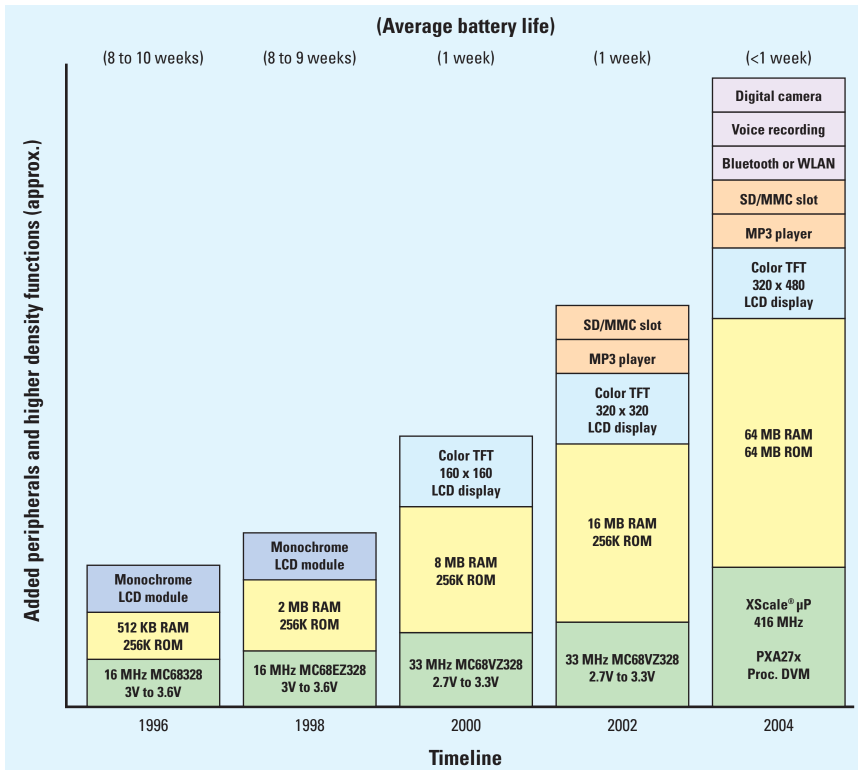


Figure 1. Evolution of PDAs and average battery life

Following Moore's Law, design innovations for portable electronics have seen exponential growth for the highly integrated applications processor cores in the latest PDAs, smartphones, and cellphones. From a system design point of view, the increasing number of added functions has almost doubled every couple of years, keeping pace with consumers' voracious appetites for innovative functions. Per Moore's original theory, the total cost of making a particular system functional must be minimized. To keep up with these design challenges while maintaining costs, the engineering design efforts are amortized by re-using the existing design and building upon new

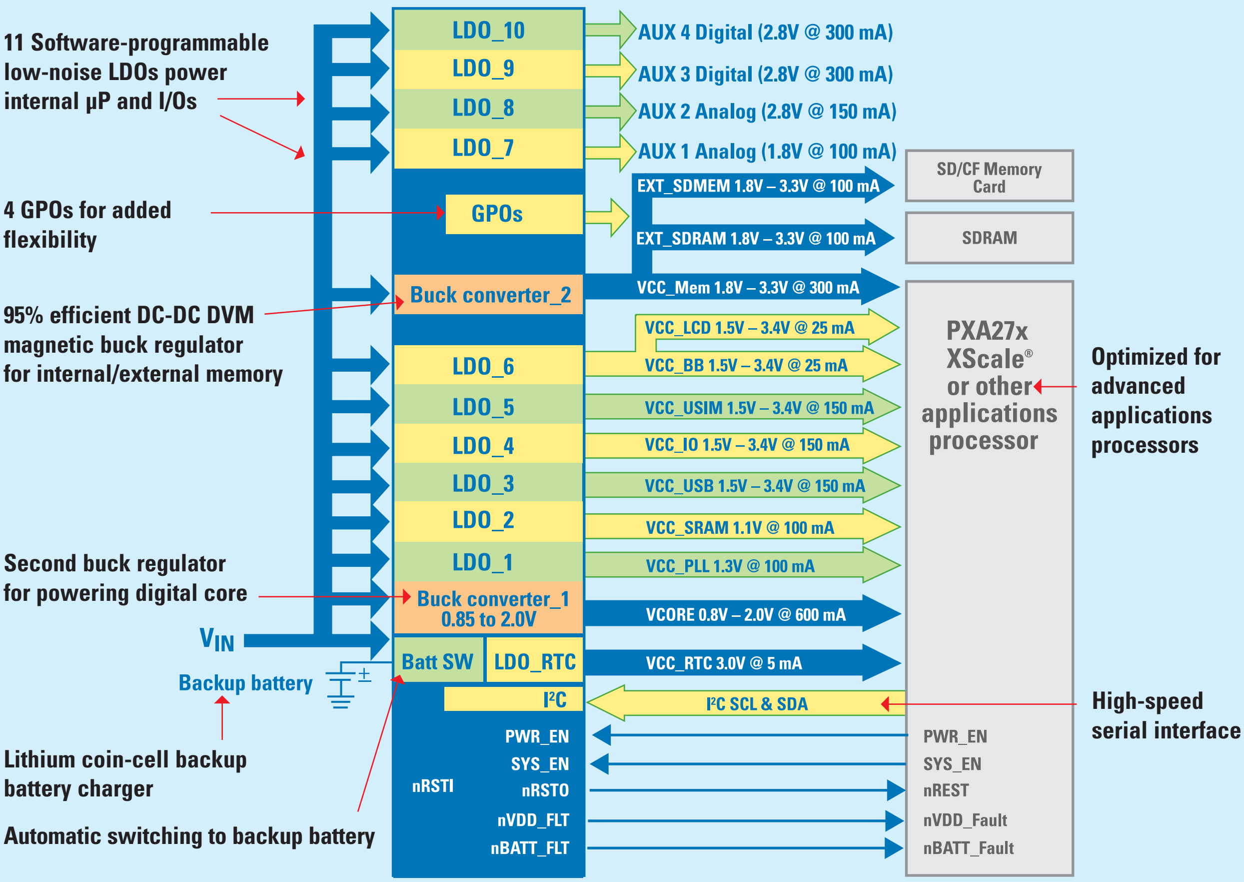
NEXT ISSUE:

Current-Mode Control Basics

National Semiconductor
The Sight & Sound of Information

Highly integrated PMIC for applications processors

LP3970 Flexible, multi-function programmable power management unit



- High-speed I²C programmability
- Standard interface to PXA27x processors
- Tiny, thermally enhanced LLP-48 package

Product Highlight:

Programmable low-power flexible PMU is optimized for advanced applications processors

Power Management Design for Applications Processors

or added features. Today's System-on-a-Chip (SoC) solutions weigh heavily in the process of meeting these challenges. Additional functions such as color LCD displays with backlighting, audio subsystems, camera functions, WLANs, Bluetooth® communications, and other integrated RF/analog functions have all stretched the battery power budget to its limits for high-end consumer applications. With the demand for converged voice, data, web-browsing and audio/video playback functions, the challenge in advanced power consumption management has become critical. ***Figure 1*** shows an evolutionary path of the increasing number of functions and the battery life expectancies.

Power-saving modes of previous-generation processors

Power-saving modes were usually pre-programmed within the processor and included doze mode, burst mode, and sleep mode. For a PDA profile, the system can process user-requested tasks (such as touch-screen input) and then implement a standby mode for the next touch-screen input. During the standby period, only the LCD screen remains active with the processor programmed for doze mode, which would then be disabled via an interrupt event. For burst-mode use in data polling applications, the highest operating frequency (worst case power consumption) on the processor can be similarly lowered by reducing the CPU duty cycle. Likewise, burst mode can be disabled during an interrupt event. When a battery reaches a critical low event or is turned off, the processor can be programmed into sleep mode, whereby all functions except the real-time clock (RTC) would be in an inactive state. For maintaining the correct date and time functions, the RTC typically consumes less than 1 µA. Thus the power savings are solely performed by the embedded processor's firmware code.

Design considerations for conserving power with applications processors

While applications processors have been the panacea for SoC solutions, the low-power design consideration rating is now measured in milliwatts per Megahertz (mW/MHz) performance. Some of these applications processors may have a minimum 0.08 mW/MHz ratio up to 0.42 mW/MHz. To support additional power-saving features, it may include integrated smart LCD displays which have internal memory for buffering the image and an independent controller that saves CPU cycles from refreshing the image on display. Other methods are made via a 0.13 micron fab process, thus reducing power to the internal I/O and core voltages as well as providing current leakage control. Other techniques include lowering the CPU duty cycle and frequency via power management software.

One example of using these techniques is Intel's ARM®-based, PXA27x XScale® processor architecture that directly scales back both voltage and operating frequency "on the fly" via intelligent switching to various low-power modes while still maintaining necessary application performance. With its six operating modes (normal, idle, deep idle, standby, sleep, and deep sleep), the PXA27x provides greater power savings. By implementing separate power domains which can be switched on and off independently, the PXA27x architecture requires up to 10 separate power domains. By scaling down the processor input core voltages and operating frequency, the processor could provide as much as a two-fold decrease in power drain. Usually a processor has a power dissipation that is proportional to the square of the core voltage input voltage as defined by the following equation:

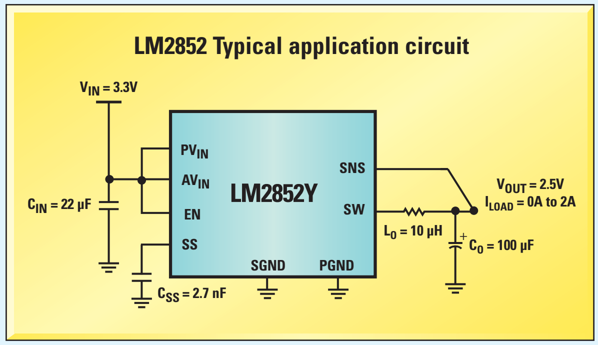
$$P = C * (V^2 f)$$

where C = chip capacitance, V = core voltage, and f = frequency.

High-performance synchronous buck regulators

LM2852 2A SIMPLE SYNCHRONOUS™ switching regulator

- Converts 2.7V to 5.5V input voltages to as low as 0.8V with extremely low external component count
- Factory-programmable EEPROM for any output voltage between 0.8V to 3.3V
- 500 kHz or 1500 kHz operation
- Superior performance at high frequencies
- Available in thermally enhanced, highly reliable ETSSOP-14 packaging

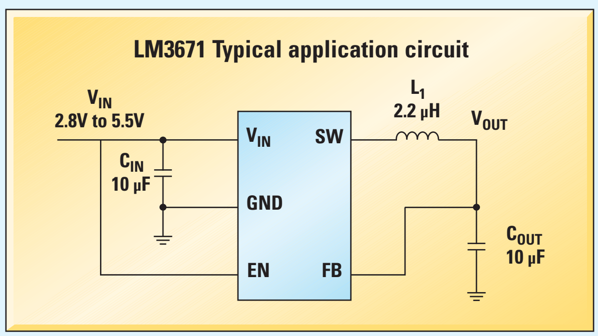


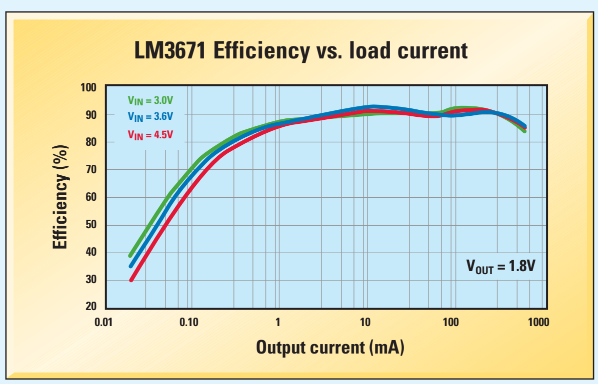
Product Highlight:

Highly integrated, high-efficiency switcher is very easy to use with few external components

LM3671 600 mA, 2 MHz synchronous buck regulator

- High switching frequency, ceramic capacitors, and SOT23-5 package enables an extremely small solution with standard components
- Automatic PFM-PWM mode switching enables longer battery life
- High output-voltage accuracy, low output-voltage ripple in PFM mode, and fast transient response allow the processor to obtain peak MIPs at the lowest possible power level
- 2 MHz, 600 mA output current provides design flexibility by supporting multiple applications





Product Highlight:

Achieves 95% efficiency with 2.2 µH inductor while enabling peak processors MIPS

Power Management Design for Applications Processors

While the PXA27x solution has power-saving merits, the power management IC (PMIC) solution will be encumbered by a long list of supply voltage requirements, including 1.1V, 1.3V, 1.8V, 2.5V and 3.3V. To support dynamic voltage scaling, the PMIC will need an additional programmable output power supply that ranges from 0.85V to 1.55V for powering the core voltage. The programmable range will have a resolution step-size value of 50 mV to 100 mV (see ***Figure 2***). With a common I^2C bus to the programmable registers, the PMIC simplifies the interface for most appplications processors.

Choosing the rechargeable backup battery

The popular single-cell Lithium-Ion (Li-Ion) battery carries a nominal 3.6V, with an actual range of 2.7V to a fully-charged 4.2V. Other battery types that are used for portable power design include Lithium Polymer (Li-Pol), Lithium-Manganese Dioxide ($Li\text{-}MnO_2$) coin-cell batteries, and Nickel-Metal Hydride (Ni-MH) batteries. Li-Ion batteries offer the highest density per unit weight, but usually need some form of protection circuit due to their volatility. Li-Pol batteries have a thin-profile geometry. Smartphones and cellphones have more mechanical design flexibility for using a higher density battery than the thin-profile dimensions of a PDA.

Choosing the power management devices

After evaluating the list of power requirements, we see two main types of power topologies:

- Programmable low-dropout (LDO) regulators for digital loads and RF loads, and a fixed LDO for the backup battery voltage
- Programmable DC-DC switching regulators for both light and heavy loads

For multiple sockets with both low input voltages and low output current, integrating several LDOs in a single chip using CMOS process technology is the best choice. The LDOs should typically support a 100 mV dropout voltage. For driving RF circuitry, an LDO should also be able to support low-output noise, such as 100 μV_{RMS} per a given bandwidth. There should also be an enable/disable function for each LDO. When the LDO is disabled, the quiescent current should be in the µA range for extending battery life.

Selecting a buck switching DC-DC regulator based upon high efficiency and high current drive provides a balanced approach to portable power. To minimize power drain and battery life, it is beneficial to select a PMIC device that supports about 90% efficiency or better. To accomplish this, the PMIC device needs to minimize switching losses via synchronous

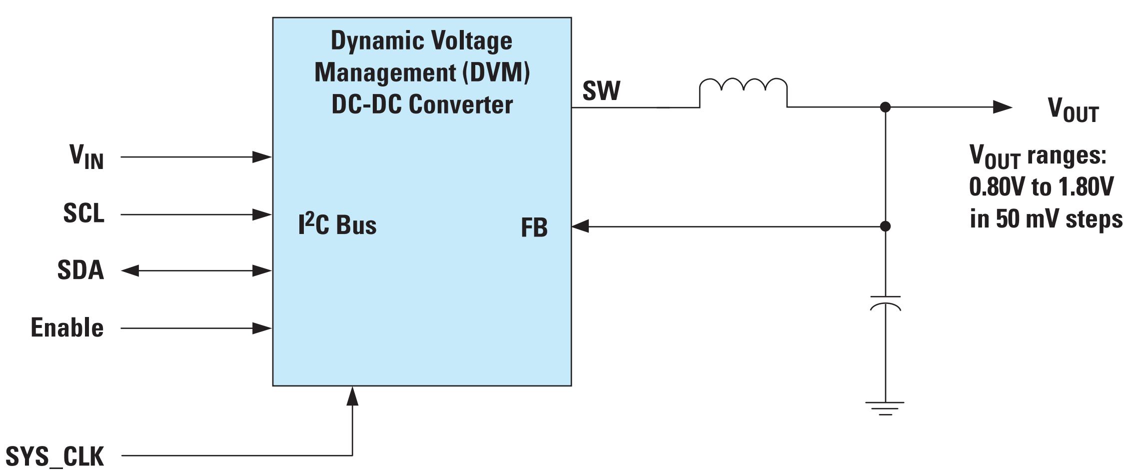
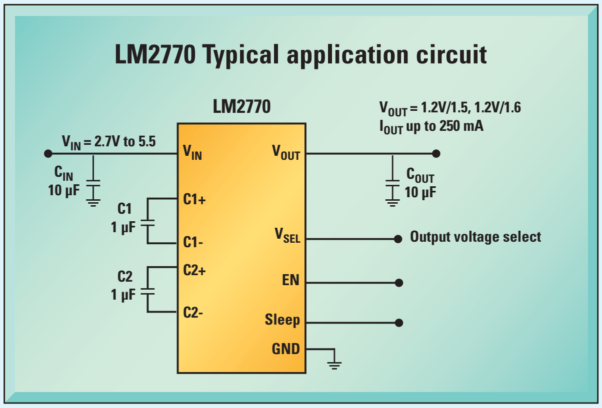


Figure 2. Smart power management for driving the core voltage in applications processors

High-efficiency DC-DC buck converters

LM2770 Switched capacitor buck regulator with sleep mode

- Multi-gain, gain-hopping architecture and low I_q sleep mode provide efficiency as high as 90%
- Input and output voltage monitoring helps prevent unexpected power loss and instability issues in the application
- No inductor, small capacitors, and miniature MSOP-8 and LLP-10 packaging provide a small solution size and reduced BOM for application
- Ideal for portable systems powered by Li-Ion or 3-cell NiMH/NiCd batteries as well as input voltage rails between 2.8V to 5.5V

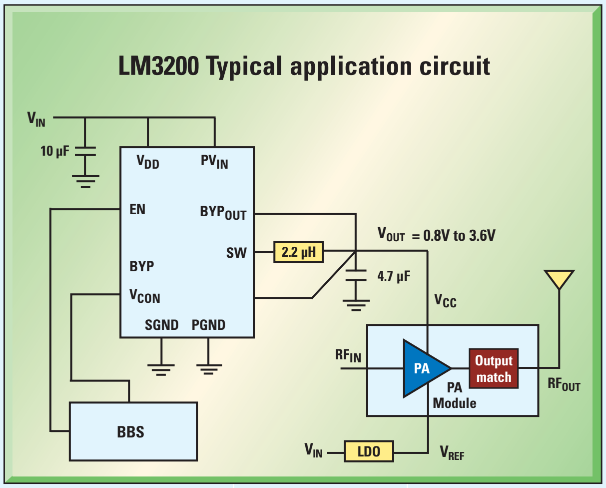


Product Highlight:

DC-DC converter provides optimal solution size and efficiency

LM3200 Miniature adjustable buck converter with bypass mode

- Dynamically adjustable output voltage maintains low RF PA power levels to optimize PA efficiency for increased battery life
- Bypass mode maintains maximum output power regardless of battery voltage
- Small micro-SMD package and 2 MHz switching frequency minimizes size impact to RF subsystem



Product Highlight:

Complete, easy-to-use switcher has smallest footprint and highest power density

Power Management Design for Applications Processors

rectification. This is done by using internal MOSFETs rather than the less-efficient conventional Schottky diodes. Ironically, the MOSFET device has its own high forward drop voltage due to its internal body diode, but using a Schottky diode in parallel helps prevent the forward drop losses. Of course, in portable power applications, it is standard to have the MOSFETs integrated into the PMIC. The switching buck regulator needs to conserve its current output drive by managing its duty cycle. When the switching regulator drives heavier loads, it can use PWM mode at a fixed frequency. During light loads, the switching regulator can switch to a lower frequency using PFM or pulse skipping mode. The buck regulator should be able to operate at a 100% duty cycle for supporting low dropout control of the output voltage even when the input voltage drops down to the lowest possible voltage. As in the LDO scenario, switching buck regulators need the enable/disable functions.

Another critical function is a backup battery charger with onboard battery monitoring and automated switching between the backup battery and the LDO powering the $V_{CC\text{-}BATT}$. Fortunately, there are integrated power management solutions that meet the majority of the above functions. Newly released solutions are offering powered SoC solutions (see LP3970 example on page 2) compared to previous solutions that required multiple PMICs and did not support dynamic voltage management.

Additional system design power requirements

Applications processors usually support other external peripherals, including external SRAM, Bluetooth, WLAN/802.11x, camera interfaces, MMC/SD cards, memory sticks, USB interfaces, external graphics processors, LCD displays, and backlighting displays (as shown in ***Figure 3***). By organizing the additional power supply requirements for these peripherals, the design engineer can then make an intelligent choice about whether or not the switching DC-DC buck regulators and/or LDOs can supply power to the additional supply rails. ■

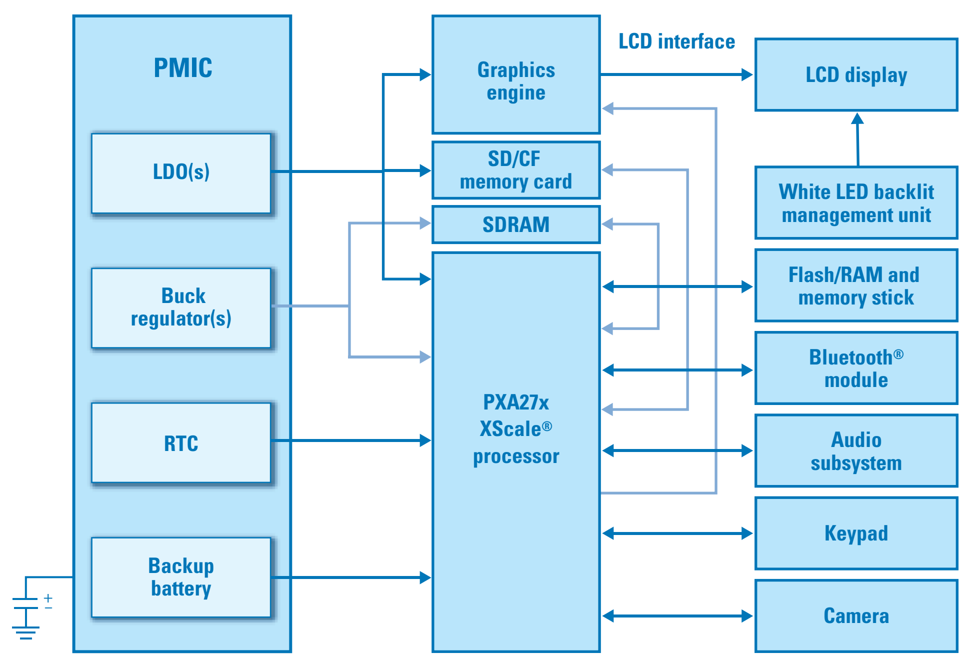
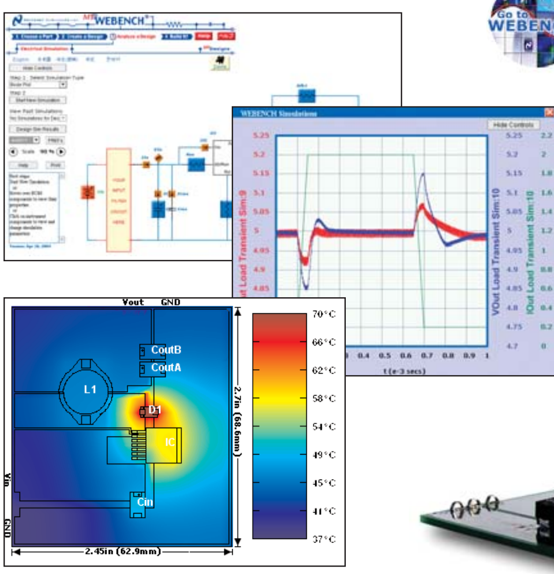


Figure 3. Power design considerations for an applications processor and system peripherals

Power design tools

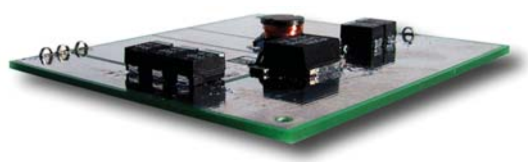


WEBENCH® online design environment

Our design and prototyping environment simplifies and expedites the entire design process.

1. Choose a part
2. Create a design
3. Analyze a power supply design
   – Perform electrical simulation
   – Simulate thermal behavior
4. Build it
   – Receive your custom prototype kit 24 hours later

webench.national.com



On-demand online seminars

Visit our library of online seminars for pertinent design topics including:

"Lighting Solutions for Portable Devices"

"Charge Techniques for Portable Applications"

"Magnetic Buck Converters for Portable Applications"

"The Evolution of Voltage Regulators with Focus on LDOs"

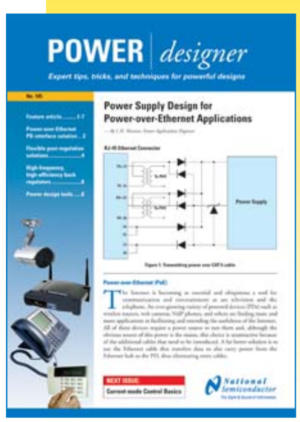
www.national.com/onlineseminar

National Semiconductor
2900 Semiconductor Drive
PO Box 58090
Santa Clara, CA 95052
1 800 272 9959

Visit our website at:
power.national.com

For more information, send email to:
new.feedback@nsc.com

Don't miss a single issue!



Subscribe now to receive email alerts when new issues are available:

power.national.com/designer

National Semiconductor
The Sight & Sound of Information

550263-005

IMPORTANT NOTICE