

***RoHS Compliant***

4GB DDR3 SDRAM SO-DIMM **Industrial**

***Product Specifications***

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*Version 1.3*



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## General Description

Apacer **75.B83CG.G040B** is a 512M x 64 DDR3 SDRAM (Synchronous DRAM) SO-DIMM. This high-density memory module consists of 16 pieces 256M x 8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM. The module is a 204-pins small-outlined, dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM. The following provides general specifications of this module.

## Ordering Information

| Part Number    | Bandwidth   | Speed Grade | Max Frequency | CAS Latency |
|----------------|-------------|-------------|---------------|-------------|
| 75.B83CG.G040B | 10.6 GB/sec | 1333 Mbps   | 666 MHz       | CL9         |

| Density | Organization | Component  | Rank |
|---------|--------------|------------|------|
| 4GB     | 512M x 64    | 256M x8*16 | 2    |

## Key Parameters

| MT/s        | DDR3-1066 | DDR3-1333 | DDR3-1600 | Unit |
|-------------|-----------|-----------|-----------|------|
| Grade       | -CL7      | -CL9      | -CL11     |      |
| tCK (min)   | 1.875     | 1.5       | 1.25      | ns   |
| CAS latency | 7         | 9         | 11        | tCK  |
| tRCD (min)  | 13.125    | 13.5      | 13.75     | ns   |
| tRP (min)   | 13.125    | 13.5      | 13.75     | ns   |
| tRAS (min)  | 37.5      | 36        | 35        | ns   |
| tRC (min)   | 50.625    | 49.5      | 48.75     | ns   |
| CL-tRCD-tRP | 7-7-7     | 9-9-9     | 11-11-11  | tCK  |

## Specifications:

- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 512 words x 64 bits, 2 ranks
- ◆ Integrating 16 pieces of 2G bits DDR3 SDRAM sealed in FBGA
- ◆ Package: 204-pin socket type small outline dual in-line memory module (SO-DIMM)
- ◆ PCB: height 30.0mm, lead pitch 0.6 mm (pin), lead-free (RoHS compliant)
- ◆ Power supply VDD: 1.5V ± 0.075V
- ◆ Serial Presence Detect (SPD)
- ◆ Eight Internal banks for concurrent operation (components)
- ◆ Interface: SSTL\_15
- ◆ Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- ◆ CAS Latency (CL): 6, 7, 8, 9
- ◆ CAS Write Latency (CWL): 5, 6, 7
- ◆ Supports auto pre-charge option for each burst access
- ◆ Supports auto-refresh/self-refresh
- ◆ Refresh cycles: 7.8  $\mu$ s at 0°C ≤ TC ≤ +85°C
- ◆ Operating case temperature range: Industrial (-40 °C ≤ TC ≤ +95°C)
- ◆ PCB: 30 $\mu$  inch gold finger

## Features:

- ◆ Double-data-rate architecture: 2 data transfers per clock cycle
- ◆ The high-speed data transfer is realized by the 8-bits prefetch pipelined architecture.
- ◆ Bi-directional differential data strobe (DQS and /DQS) is transmitted / received with data for capturing data at the receiver
- ◆ DQS: edge-aligned with data for read; center-aligned with data for write
- ◆ Differential clock inputs (CK and /CK)
- ◆ DLL aligns DQ and DQS transitions with CK transitions
- ◆ Data mask (DM) for writing data
- ◆ Posted CAS by programmable additive latency for enhanced command and data bus efficiency
- ◆ On-Die-Termination (ODT) for improved signal quality: Synchronous ODT/Dynamic ODT/Asynchronous ODT
- ◆ Multi-Purpose Register (MPR) for temperature read out
- ◆ ZQ calibration for DQ drive and ODT
- ◆ Programmable Partial Array Self-Refresh (PASR)
- ◆ /Reset pin for power-up sequence and reset function
- ◆ SRT range: normal/extended, auto/manual self-refresh
- ◆ Programmable output driver impedance control

## Pin Assignments

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1       | VREFDQ   | 53      | DQ19     | 105     | VDD      | 157     | DQ42     |
| 3       | VSS      | 55      | VSS      | 107     | A10(AP)  | 159     | DQ43     |
| 5       | DQ0      | 57      | DQ24     | 109     | BA0      | 161     | VSS      |
| 7       | DQ1      | 59      | DQ25     | 111     | VDD      | 163     | DQ48     |
| 9       | VSS      | 61      | VSS      | 113     | /WE      | 165     | DQ49     |
| 11      | DM0      | 63      | DM3      | 115     | /CAS     | 167     | VSS      |
| 13      | VSS      | 65      | VSS      | 117     | VDD      | 169     | /DQS6    |
| 15      | DQ2      | 67      | DQ26     | 119     | A13      | 171     | DQS6     |
| 17      | DQ3      | 69      | DQ27     | 121     | /CS1     | 173     | VSS      |
| 19      | VSS      | 71      | VSS      | 123     | VDD      | 175     | DQ50     |
| 21      | DQ8      | 73      | CKE0     | 125     | NC       | 177     | DQ51     |
| 23      | DQ9      | 75      | VDD      | 127     | VSS      | 179     | VSS      |
| 25      | VSS      | 77      | NC       | 129     | DQ32     | 181     | DQ56     |
| 27      | /DQS1    | 79      | BA2      | 131     | DQ33     | 183     | DQ57     |
| 29      | DQS1     | 81      | VDD      | 133     | VSS      | 185     | VSS      |
| 31      | VSS      | 83      | A12(BC)  | 135     | /DQS4    | 187     | DM7      |
| 33      | DQ10     | 85      | A9       | 137     | DQS4     | 189     | VSS      |
| 35      | DQ11     | 87      | VDD      | 139     | VSS      | 191     | DQ58     |
| 37      | VSS      | 89      | A8       | 141     | DQ34     | 193     | DQ59     |
| 39      | DQ16     | 91      | A5       | 143     | DQ35     | 195     | VSS      |
| 41      | DQ17     | 93      | VDD      | 145     | VSS      | 197     | SA0      |
| 43      | VSS      | 95      | A3       | 147     | DQ40     | 199     | VDDSPD   |
| 45      | /DQS2    | 97      | A1       | 149     | DQ41     | 201     | SA1      |
| 47      | DQS2     | 99      | VDD      | 151     | VSS      | 203     | VTT      |
| 49      | VSS      | 101     | CK0      | 153     | DM5      |         |          |
| 51      | DQ18     | 103     | /CK0     | 155     | VSS      |         |          |

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 2       | VSS      | 54      | VSS      | 106     | VDD      | 158     | DQ46     |
| 4       | DQ4      | 56      | DQ28     | 108     | BA1      | 160     | DQ47     |
| 6       | DQ5      | 58      | DQ29     | 110     | /RAS     | 162     | VSS      |
| 8       | VSS      | 60      | VSS      | 112     | VDD      | 164     | DQ52     |
| 10      | /DQS0    | 62      | /DQS3    | 114     | /CS0     | 166     | DQ53     |
| 12      | DQS0     | 64      | DQS3     | 116     | ODT0     | 168     | VSS      |
| 14      | VSS      | 66      | VSS      | 118     | VDD      | 170     | DM6      |
| 16      | DQ6      | 68      | DQ30     | 120     | ODT1     | 172     | VSS      |
| 18      | DQ7      | 70      | DQ31     | 122     | NC       | 174     | DQ54     |
| 20      | VSS      | 72      | VSS      | 124     | VDD      | 176     | DQ55     |
| 22      | DQ12     | 74      | CKE1     | 126     | VREFCA   | 178     | VSS      |
| 24      | DQ13     | 76      | VDD      | 128     | VSS      | 180     | DQ60     |
| 26      | VSS      | 78      | A15(NC)  | 130     | DQ36     | 182     | DQ61     |
| 28      | DM1      | 80      | A14(NC)  | 132     | DQ37     | 184     | VSS      |
| 30      | /RESET   | 82      | VDD      | 134     | VSS      | 186     | /DQS7    |
| 32      | VSS      | 84      | A11      | 136     | DM4      | 188     | DQS7     |
| 34      | DQ14     | 86      | A7       | 138     | VSS      | 190     | VSS      |
| 36      | DQ15     | 88      | VDD      | 140     | DQ38     | 192     | DQ62     |
| 38      | VSS      | 90      | A6       | 142     | DQ39     | 194     | DQ63     |
| 40      | DQ20     | 92      | A4       | 144     | VSS      | 196     | VSS      |
| 42      | DQ21     | 94      | VDD      | 146     | DQ44     | 198     | /EVENT   |
| 44      | VSS      | 96      | A2       | 148     | DQ45     | 200     | SDA      |
| 46      | DM2      | 98      | A0       | 150     | VSS      | 202     | SCL      |
| 48      | VSS      | 100     | VDD      | 152     | /DQS5    | 204     | VTT      |
| 50      | DQ22     | 102     | CK1      | 154     | DQS5     |         |          |
| 52      | DQ23     | 104     | /CK1     | 156     | VSS      |         |          |

## Pin Descriptions

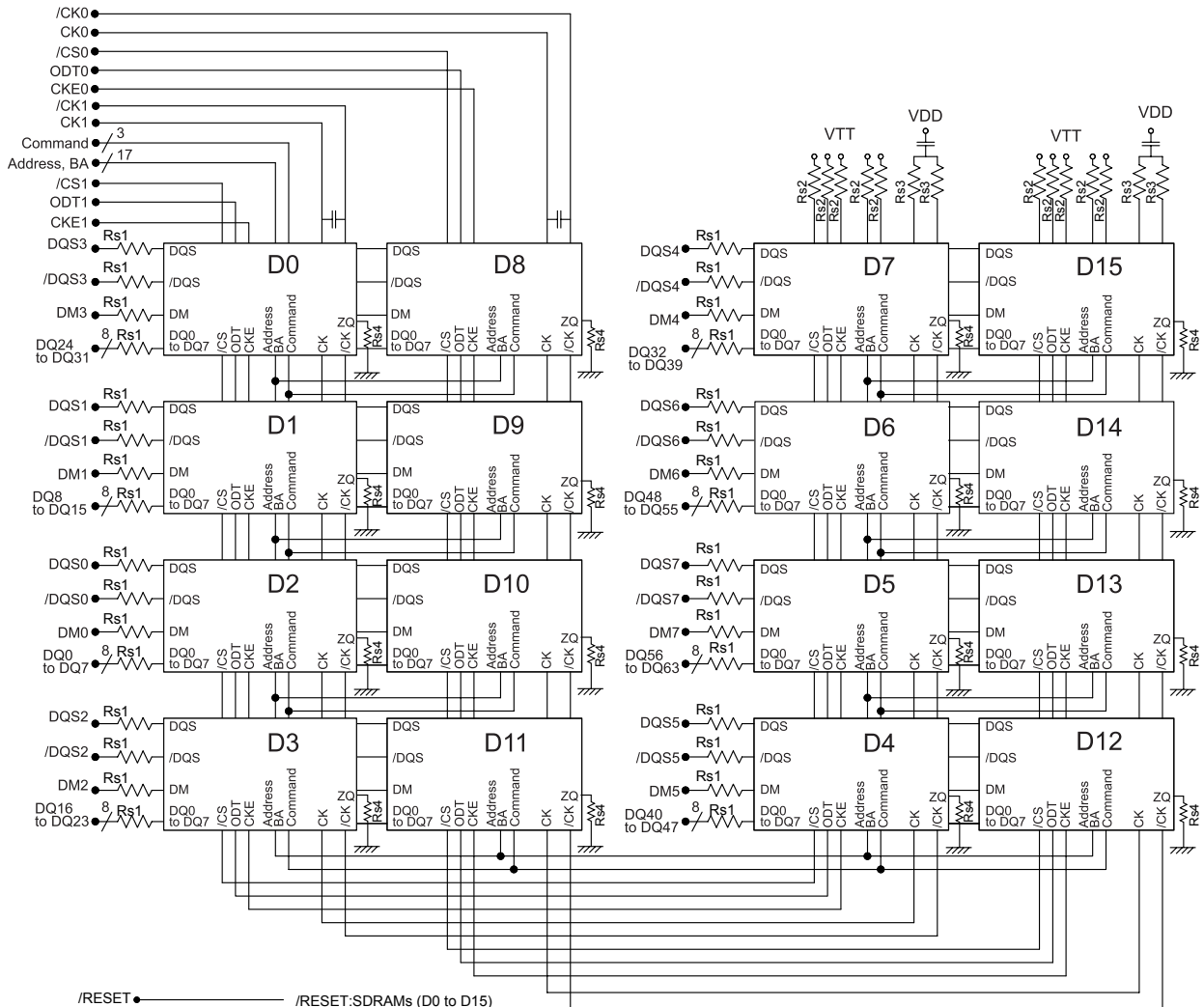
| Pin Name | Description   |
|----------|---|
| Ax*      | SDRAM address bus   |
| BAx      | SDRAM bank select   |
| DQx      | DIMM memory data bus  |
| /RAS     | SDRAM row address strobe  |
| /CAS     | SDRAM column address strobe   |
| /WE      | SDRAM write enable  |
| /CSx     | SDRAM Chip select lines   |
| CKEx     | SDRAM clock enable lines  |
| CKx      | SDRAM clock input   |
| /CKx     | SDRAM Differential clock input  |
| DQSx     | SDRAM data strobes(positive line of differential pair)                  |
| /DQSx    | SDRAM data strobes(negative line of differential pair)                  |
| DMx      | SDRAM input mask  |
| SCL      | Clock input for serial PD   |
| SDA      | Data input/output for serial PD   |
| SAX      | Serial address input  |
| VDD      | Power for internal circuit  |
| VDDSPD   | Serial EEPROM positive power supply                                     |
| VREFDQ   | SDRAM I/O reference supply  |
| VREFCA   | SDRAM command/address reference supply                                  |
| VSS      | Power supply return(ground)   |
| VTT      | SDRAM I/O termination supply  |
| /RESET   | Set DRAM to known state   |
| ODTx     | On-die termination control lines  |
| NC       | Spare pins(no connect)  |
| /EVENT   | An output of the thermal sensor to indicate critical module temperature |

\*IC Component Composition:

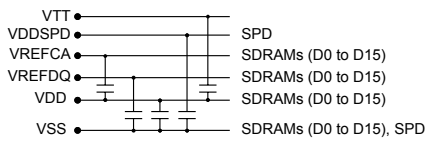
|         |        |
|---------|--------|
| 128Mx8  | A0~A13 |
| 256Mx8  | A0~A14 |
| 512Mx8  | A0~A15 |
| 1024Mx8 | A0~A15 |



# Functional Block Diagram



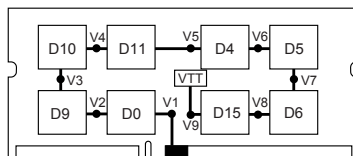
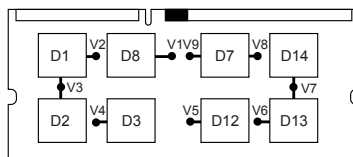
/RESET ● /RESET:SDRAMs (D0 to D15)



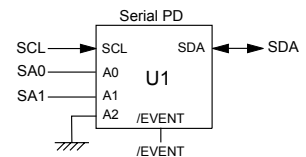
Notes :

1. DQ wiring may be changed within a byte.
2. DQ, DQS, /DQS, ODT, DM, CKE, /CS relationships must be maintained as shown.

\* D0 to D15: 4G bits DDR3 SDRAM  
 Address, BA: A0 to A15, BA0 to BA2  
 Command: /RAS, /CAS, /WE  
 U1: 256 bytes EEPROM  
 Rs1: 15Ω  
 Rs2: 36Ω  
 Rs3: 30Ω  
 Rs4: 240Ω



— Address and Control lines



## Absolute Maximum Ratings

| Parameter                           | Symbol            | Description       | Units |
|-------------------------------------|-------------------|-------------------|-------|
| Voltage on VDD pin relative to Vss  | $V_{DD}$          | - 0.4 V ~ 1.975 V | V     |
| Voltage on VDDQ pin relative to Vss | $V_{DDQ}$         | - 0.4 V ~ 1.975 V | V     |
| Voltage on any pin relative to Vss  | $V_{IN}, V_{OUT}$ | - 0.4 V ~ 1.975 V | V     |

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

# DRAM Component Operating Temperature Range

| Symbol | Parameter                   | Rating    | Units | Notes |
|--------|-----------------------------|-----------|-------|-------|
| TOPER  | Operating Temperature Range | -40 to 95 | °C    | 1,2   |

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40°C~95°C under all operating conditions.

**Industrial Temperature:**

The industrial temperature device requires that the case temperature not exceed -40°C or +95°C. JEDEC specifications require the refresh rate to double when TC exceeds +85°C; this also requires use of the high-temperature self refresh option.

- ◆ MAX operating case temperature. TC is measured in the center of the package.
- ◆ A thermal solution must be designed to ensure the DRAM device does not exceed the maximum TC during operation.
- ◆ Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.
- ◆ If TC exceeds +85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.

# Operating Conditions

## Recommended DC Operating Conditions - DDR3 (1.5V) operation

| Symbol | Parameter                 | Rating |      |       | Units |
|--------|---------------------------|--------|------|-------|-------|
|        |                           | Min.   | Typ. | Max.  |       |
| VDD    | Supply Voltage            | 1.425  | 1.5  | 1.575 | V     |
| VDDQ   | Supply Voltage for Output | 1.425  | 1.5  | 1.575 | V     |

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

## IDD Specifications

| Conditions  | Symbol  | Samsung-F | Unit |
|---|---------|-----------|------|
| <b>Operating one bank active-precharge current:</b><br>tCK = tCK (IDD); tRC = tRC (IDD); tRAS = tRAS MIN (IDD);<br>CKE is HIGH, CS# is HIGH between valid commands;<br>Address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | IDD0    | 400       | mA   |
| <b>Operating one bank active-read-precharge current:</b><br>IOOUT = 0 mA; BL = 8; CL = CL (IDD); AL = 0; tCK = tCK (IDD); tRC = tRC (IDD); tRAS = tRAS MIN (IDD); tRCD = tRCD (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | IDD1    | 512       | mA   |
| <b>Precharge power-down current:</b><br>All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING   | IDD2P-0 | 192       | mA   |
|   | IDD2P-1 | 192       | mA   |
| <b>Precharge standby current; All device banks idle:</b><br>tCK = tCK (IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | IDD2N   | 272       | mA   |
| <b>Precharge quiet standby current:</b><br>All device banks idle; tCK = tCK (IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING  | IDD2Q   | 240       | mA   |
| <b>Active power-down current:</b><br>All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING  | IDD3P   | 240       | mA   |
| <b>Active standby current:</b><br>All device banks open; tCK = tCK (IDD); tRP = tRP (IDD); tRAS = tRAS MAX (IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING  | IDD3N   | 320       | mA   |

|  |       |      |    |
|--|-------|------|----|
| <p><b>Operating burst read current:</b></p> <p>All device banks open; Continuous burst reads; IOU<sub>T</sub> = 0 mA; BL = 8; CL = CL (IDD); AL = 0; t<sub>CK</sub> = t<sub>CK</sub> (IDD); t<sub>RAS</sub> = t<sub>RAS</sub> MAX (IDD); t<sub>RP</sub> = t<sub>RP</sub> (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data patten is same as IDD4W</p>  | IDD4R | 752  | mA |
| <p><b>Operating burst write current:</b></p> <p>All device banks open; Continuous burst writes; BL = 8; CL = CL(IDD);AL = 0; t<sub>CK</sub>= t<sub>CK</sub>(IDD); t<sub>RAS</sub>= t<sub>RAS</sub> MAX(IDD); t<sub>RP</sub>= t<sub>RP</sub>(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.</p>  | IDD4W | 792  | mA |
| <p><b>Burst refresh current:</b></p> <p>t<sub>CK</sub>=t<sub>CK</sub>(IDD); Refresh command at every t<sub>RFC</sub>(IDD) interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.</p>  | IDD5B | 1496 | mA |
| <p><b>Self refresh current:</b></p> <p>CK and CK# at 0V; CKE &lt; 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.</p>   | IDD6  | 192  | mA |
| <p><b>Operating bank interleave read current</b></p> <p>All bank interleaving reads; IOU<sub>T</sub> = 0mA; BL = 8; CL = CL(IDD); AL = t<sub>RCD</sub>(IDD) - 1*t<sub>CK</sub>(IDD); t<sub>CK</sub>= t<sub>CK</sub>(IDD); t<sub>RC</sub>= t<sub>RC</sub>(IDD); t<sub>RRD</sub> = t<sub>RRD</sub>(IDD); t<sub>RCD</sub> = 1*t<sub>CK</sub>(IDD) ; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.</p> | IDD7  | 1256 | mA |
| <p><b>Reset current</b></p>  | IDD8  | 192  | mA |

Notes:

\*Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

\*\*Value calculated reflects all module ranks in this operating condition.

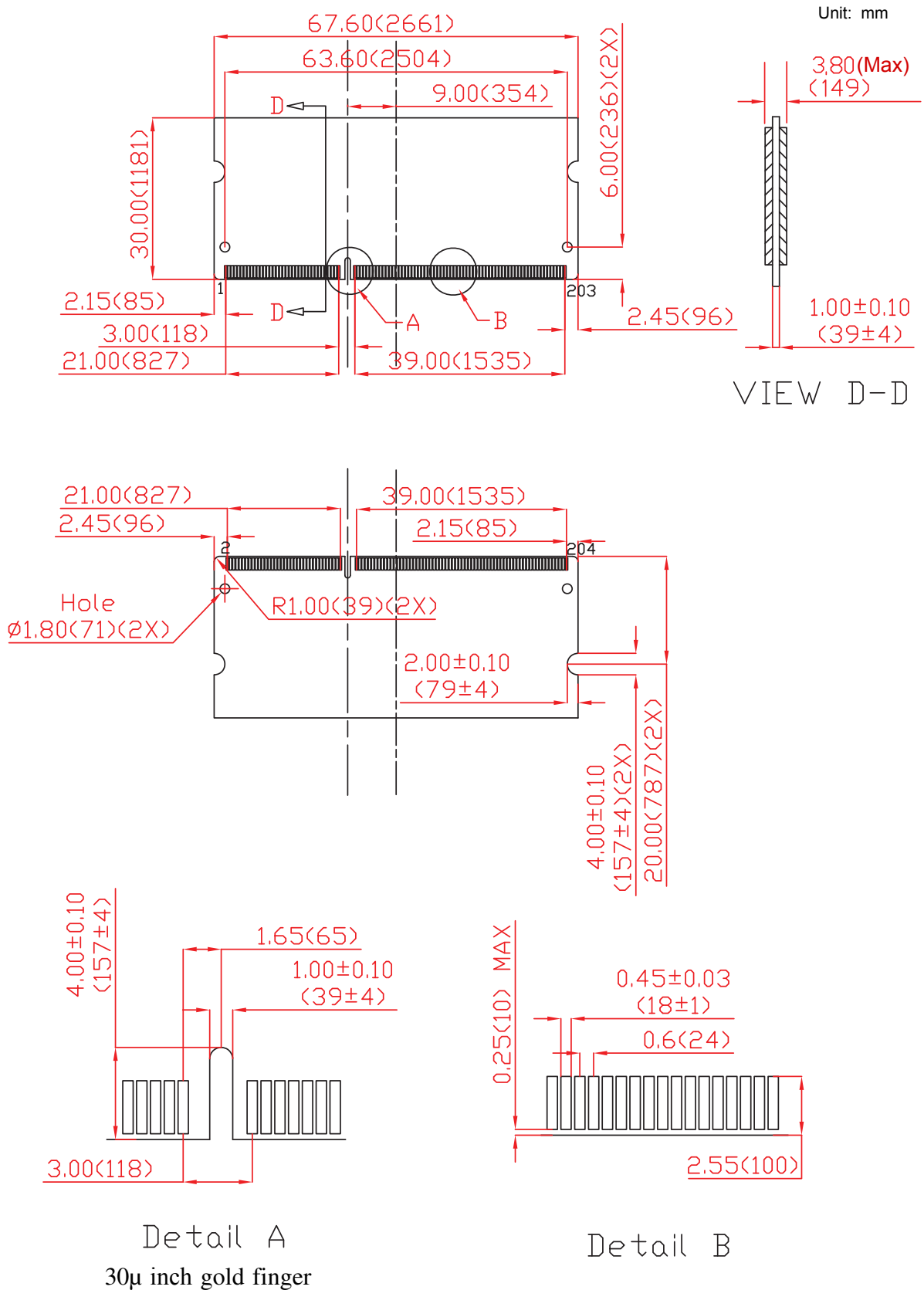
## Environmental Requirements

| Symbol | Parameter                                 | Rating      | Units | Notes |
|--------|---|-------------|-------|-------|
| TOPR   | Operating Temperature (ambient)           | 0 to +55    | °C    | 3     |
| HOPR   | Operating Humidity (relative)             | 10 to 90    | %     |       |
| TSTG   | Storage Temperature                       | -50 to +100 | °C    | 1     |
| HSTG   | Storage Humidity (without condensation)   | 5 to 95     | %     | 1     |
| PBAR   | Barometric Pressure (operating & storage) | 105 to 69   | kPa   | 1,2   |

Notes:

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (TCASE) shall not exceed the value specified in the DDR4 SDRAM component specification, JESD79-4.

# Mechanical Drawing





## Revision History

| <b>Revision</b> | <b>Date</b> | <b>Description</b>             | <b>Remark</b> |
|-----------------|-------------|--------------------------------|---------------|
| 0.9             | 08/28/2012  | Official release               |               |
| 1.0             | 08/29/2012  | release                        |               |
| 1.1             | 07/23/2013  | Changed headquarters address   |               |
| 1.2             | 05/08/2015  | Updated Mechanical Drawing     |               |
| 1.3             | 03/15/2017  | Add Environmental Requirements |               |

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