ARM® Cortex®-M0

32-bit Microcontroller

NuMicro® Family
M051 DN/DE Series
Product Brief

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1   GENERAL DESCRIPTION

The NuMicro® M051 DN/DE series 32-bit microcontroller is embedded with ARM® Cortex®-M0 core for industrial control and applications which need rich communication interfaces. The NuMicro® M051 DN/DE series includes the following part numbers: M052xDN/xDE, M054xDN/xDE, M058xDN/xDE and M0516xDN/xDE.

The NuMicro® M051 DN/DE series can run up to 50 MHz and operate at 2.5V ~ 5.5V, -40℃ ~ 85℃, while M05xxDE operates at -40℃ ~ 105℃, and thus can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro® M051 DN/DE series offers 8/16/32/64 KB flash, 4 KB Data Flash, 4 KB flash for the ISP, and 4 KB SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I²C, PWM, ADC, Watchdog Timer, Window Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into The NuMicro® M051 DN/DE series in order to reduce component count, board space and system cost. These useful functions make The NuMicro® M051 DN/DE series powerful for a wide range of applications.

Additionally, the NuMicro® M051 DN/DE series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, and IAP (In-Application Programming), which allow the user to update the program memory without removing the chip from the actual end product.

Item	M05xxBN	M05xxDN	M05xxDE
Operating Temperature	-40℃ ~ 85℃	-40℃ ~ 85℃	-40℃ ~ 105℃
Hardware Divider	-	●	●
IAP Mode	-	●	●
Window WDT	-	●	●
Analog Comparators	2	4	4
Configurable I/O mode after POR	-	●	●
I²C	1	2 (Supports Wake-up)	2 (Supports Wake-up)
SPI	- Only Supports HCLK as SPI clock source - No FIFO	- Supports HCLK and PLL as SPI clock source - 4-level FIFO	- Supports HCLK and PLL as SPI clock source - 4-level FIFO
PWM and ADC	PWM cannot trigger ADC	- PWM can trigger ADC conversion	- PWM can trigger ADC conversion

Table 1-1 M05xxBN, M05xxDN and M05xxDE Difference List

2 FEATURES

- Core

    - ARM® Cortex®-M0 core running up to 50 MHz
    - One 24-bit system timer
    - Supports Low Power Sleep mode
    - A single-cycle 32-bit hardware multiplier
    - NVIC for the 32 interrupt inputs, each with 4-levels of priority
    - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
    - Provides hardware divider and supports signed 32-bit dividend, 16-bit divisor operation

- Wide Operating Voltage Range: 2.5V to 5.5V

- Memory

    - 8KB/16KB/32KB/64KB Flash for program memory (APROM)
    - 4KB Flash for data memory (Data Flash)
    - 4KB Flash for loader (LDROM)
    - 4KB SRAM for internal scratch-pad RAM (SRAM)

- Clock Control

    - Programmable system clock source
    - 22.1184 MHz internal oscillator
    - 4~24 MHz external crystal input
    - 10 kHz low-power oscillator for Watchdog Timer and wake-up in Sleep mode
    - PLL allows CPU operation up to the maximum 50 MHz

- I/O Port

    - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
    - Four I/O modes:
        - Quasi-bidirectional
        - Push-Pull output
        - Open-Drain output
        - Input only with high impendence
    - TTL/Schmitt trigger input selectable
    - I/O pin can be configured as interrupt source with edge/level setting
    - Supports high driver and high sink I/O mode
    - Configurable I/O mode after POR

- Timer

    - Provides four channel 32-bit timers; one 8-bit pre-scale counter with 24-bit up-timer for each timer
    - Independent clock source for each timer
    - 24-bit timer value is readable through TDR (Timer Data Register)
    - Provides One-shot, Periodic and Toggle operation modes
    - Provides event counter function
    - Provides external capture/reset counter function
    - Two more timer clock sources from external trigger and internal 10 kHz
    - TIMER wake-up function
    - External capture input source selected from ACMP or TxEX
    - Toggle mode output pins selected from TxEX or TMx
    - Inter-Timer trigger mode

- WDT (Watchdog Timer)

- Multiple clock sources
- Supports wake-up from Power-down or Sleep mode
- Interrupt or reset selectable on watchdog time-out
- Time-out reset delay period time can be selected

● WWDT (Window Watchdog Timer)

- 6-bit down counter with 11-bit pre-scale for wide range window selected

● PWM

- Up to four built-in 16-bit PWM generators, providing eight PWM outputs or four complementary paired PWM outputs
- Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
- PWM interrupt synchronized to PWM period
- 16-bit digital Capture timers with rising/falling capture inputs
- Supports capture interrupt
- Internal 10 kHz to PWM clock source
- Polar inverse function
- Center-aligned type function
- Timer duty interrupt enable function
- Two kinds of PWM interrupt period/duty type selection
- Period/duty trigger ADC function
- PWM Timer synchronous start function

● UART

- Up to two sets of UART devices
- Programmable baud-rate generator
- Buffered receiver and transmitter, each with 15 bytes FIFO
- Optional flow control function (CTS and RTS)
- Supports IrDA(SIR) function
- Supports RS485 function
- Supports LIN function

● SPI

- Up to two sets of SPI devices
- Supports Master/Slave mode
- Full-duplex synchronous serial data transfer
- Provides 3 wire function
- Variable length of transfer data from 1 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- PLL clock source
- 4-level depth FIFO buffer for better performance and flexibility in SPI Burst Transfer mode

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- I^{2}C

  - Up to two sets of I^{2}C modules
  - Supports Master/Slave mode
  - Bidirectional data transfer between master and slave
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition (four slave addresses with mask option)

- ADC

  - 12-bit SAR ADC
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports Single mode/Burst mode/Single-cycle Scan mode/Continuous Scan mode
  - Supports 2' complement/un-signed format in differential mode conversion results
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion started either by software trigger or external pin trigger
  - A/D conversion started by PWM center-aligned trigger or edge-aligned trigger
  - PWM trigger delay function
  - Supports conversion result with signed format in Differential input and Burst mode

- Analog Comparator

  - Up to four sets of Comparator analog modules
  - External input or internal band-gap voltage selectable at negative node
  - Interrupt when compared results change
  - Power-down wake-up

- EBI (External Bus Interface) for external memory-mapped device access

  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8-bit or 16-bit data width
  - Supports byte-write in 16-bit data width

- ISP (In-System Programming) and ICP (In-Circuit Programming)

- IAP (In-Application Programming)

- One built-in temperature sensor with 1℃ resolution

- BOD (Brown-out Detector)

  - With 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Supports Brown-out interrupt and reset option

- 96-bit unique ID

- LVR (Low Voltage Reset)

  - Threshold voltage level: 2.0V

- Operating Temperature:

- ■ M05xxDN: -40℃~85℃
- ■ M05xxDE: -40℃~105℃
- ● Packages:

  - ■ Green package (RoHS)
  - ■ 48-pin LQFP, 33-pin QFN

3   PARTS INFORMATION AND PIN CONFIGURATION

3.1   NuMicro® M051 Series M05xxDN Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			COMP	PWM (16-Bit)	ADC (12-Bit)	WDT	WWDT	EBI	ISP/ICP/IAP	Package	Operating Temperature Range(℃)
							UART	SPI	I²C									
M052LDN	8	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M052ZDN	8	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M054LDN	16	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M054ZDN	16	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M058LDN	32	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M058ZDN	32	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M0516LDN	64	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M0516ZDN	64	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85

Table 5-2 NuMicro® M051 Series M05xxDN Product Selection Guide

3.2   NuMicro® M051 Series M05xxDE Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			COMP	PWM (16-Bit)	ADC (12-Bit)	WDT	WWDT	EBI	ISP/ICP/IAP	Package	Operating Temperature Range(℃)
							UART	SPI	I²C									
M052LDE	8	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M052ZDE	8	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M054LDE	16	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M054ZDE	16	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M058LDE	32	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M058ZDE	32	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M0516LDE	64	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M0516ZDE	64	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105

Table 5-2 NuMicro® M051 Series M05xxDE Product Selection Guide

M0 5X - X X X

**CPU core
ARM Cortex M0**

Part Number
52:    8 KB Flash ROM
54:   16 KB Flash ROM
58:   32 KB Flash ROM
516: 64 KB Flash ROM

Package
L : LQFP48
Z : QFN33

Temperature
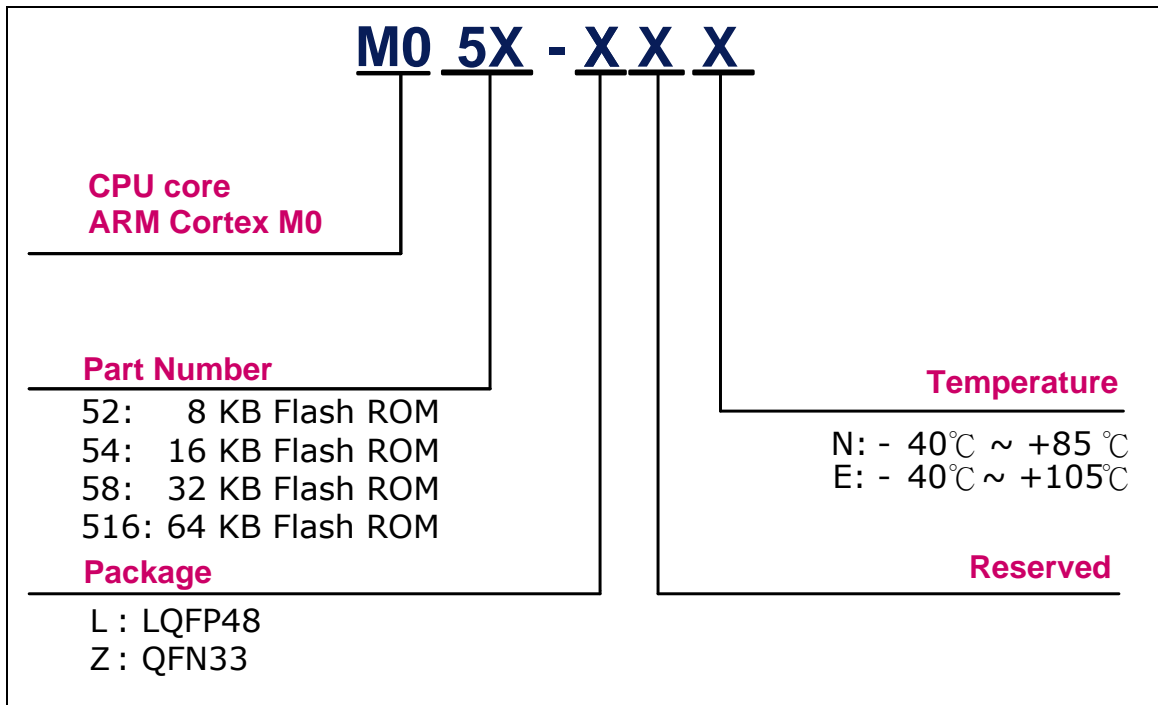N: - 40℃ ~ +85 ℃
E: - 40℃ ~ +105℃

Reserved

Figure 3-1 NuMicro® M051 DN/DE Series Naming Rule

3.3 Pin Diagrams
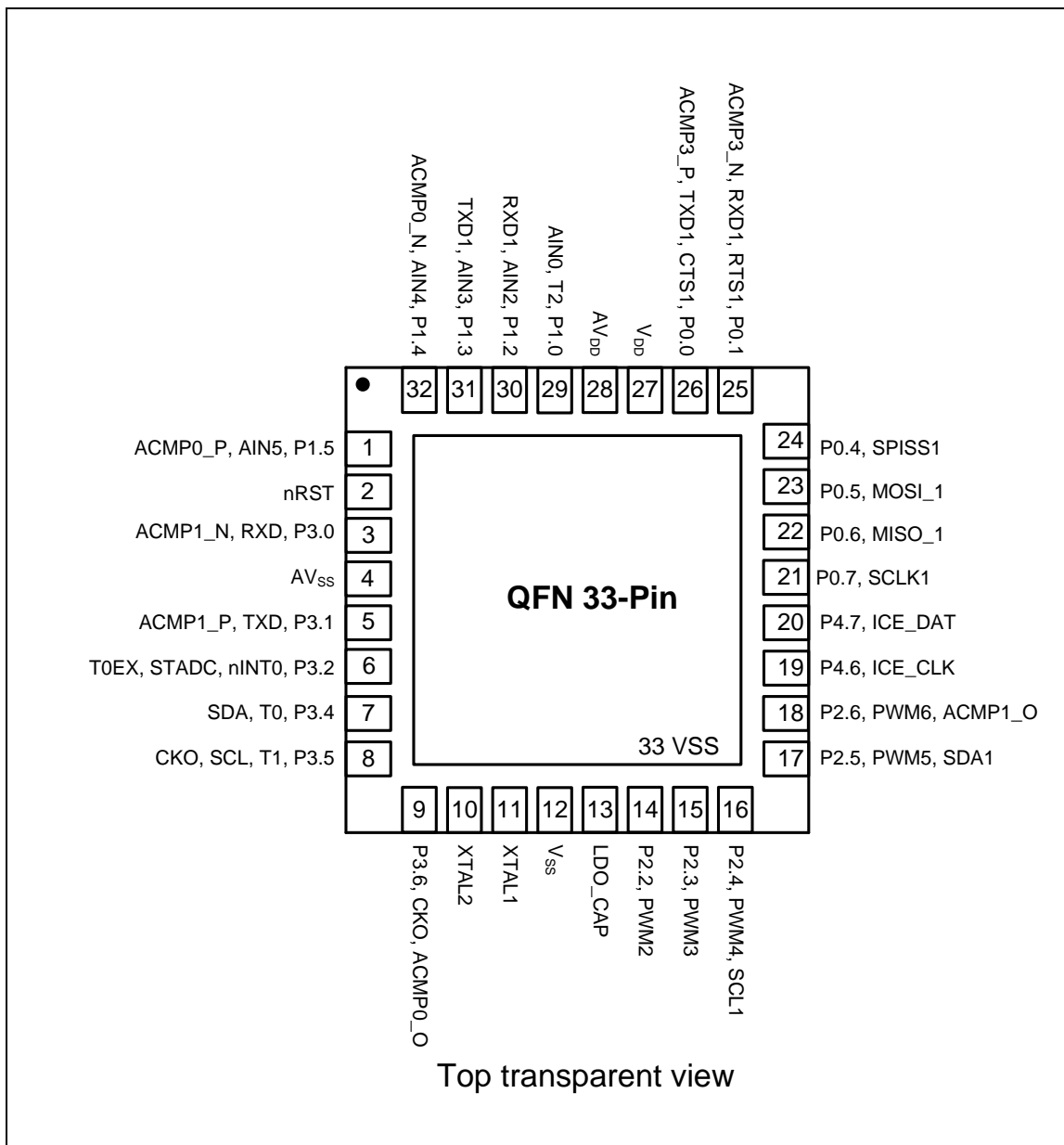
3.3.1 QFN 33-pin

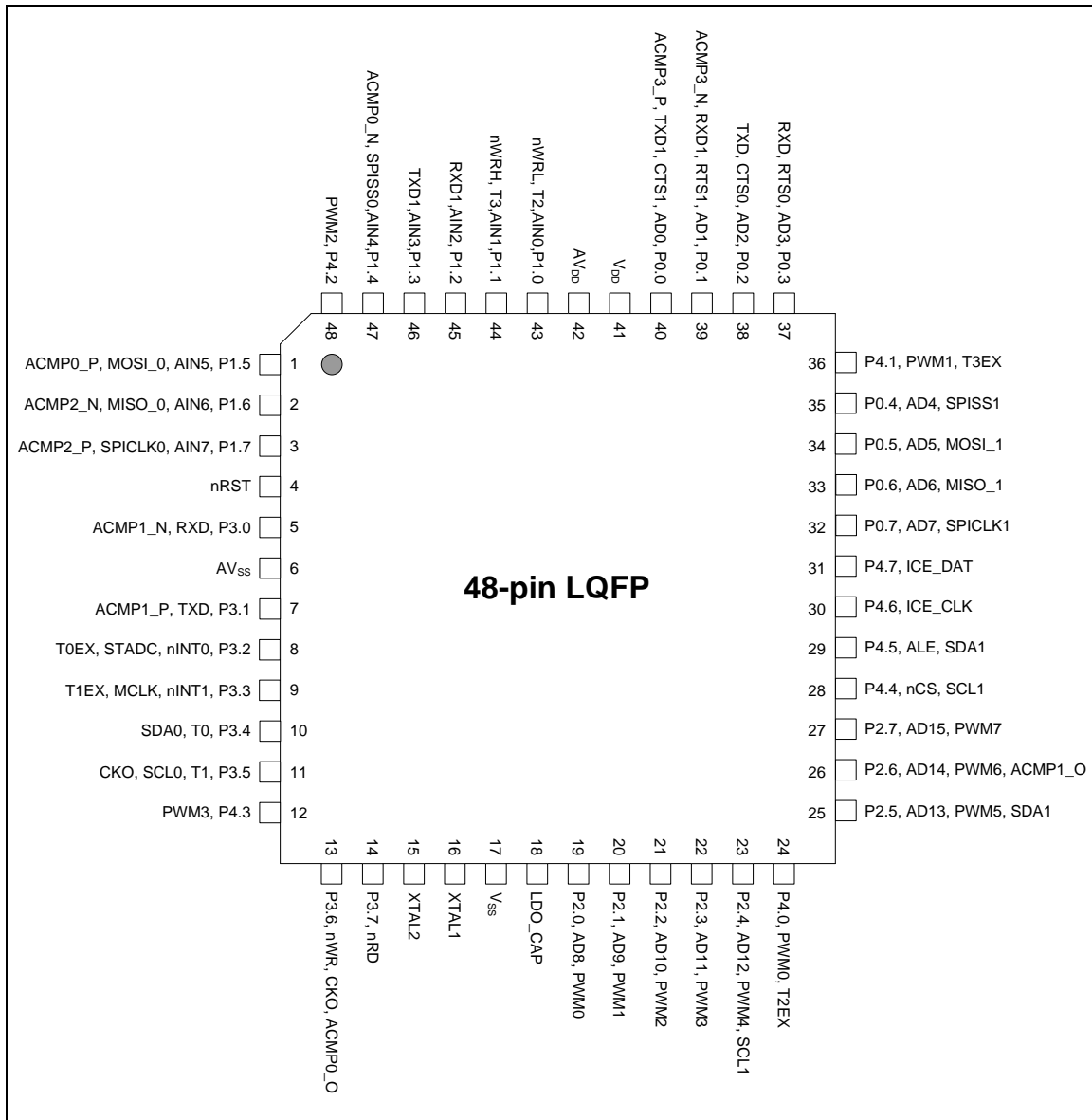Figure 3-2 NuMicro® M051 DN/DE Series QFN-33 Pin Diagram

3.3.2 LQFP 48-pin

Figure 3-3 NuMicro® M051 DN/DE Series LQFP-48 Pin Diagram
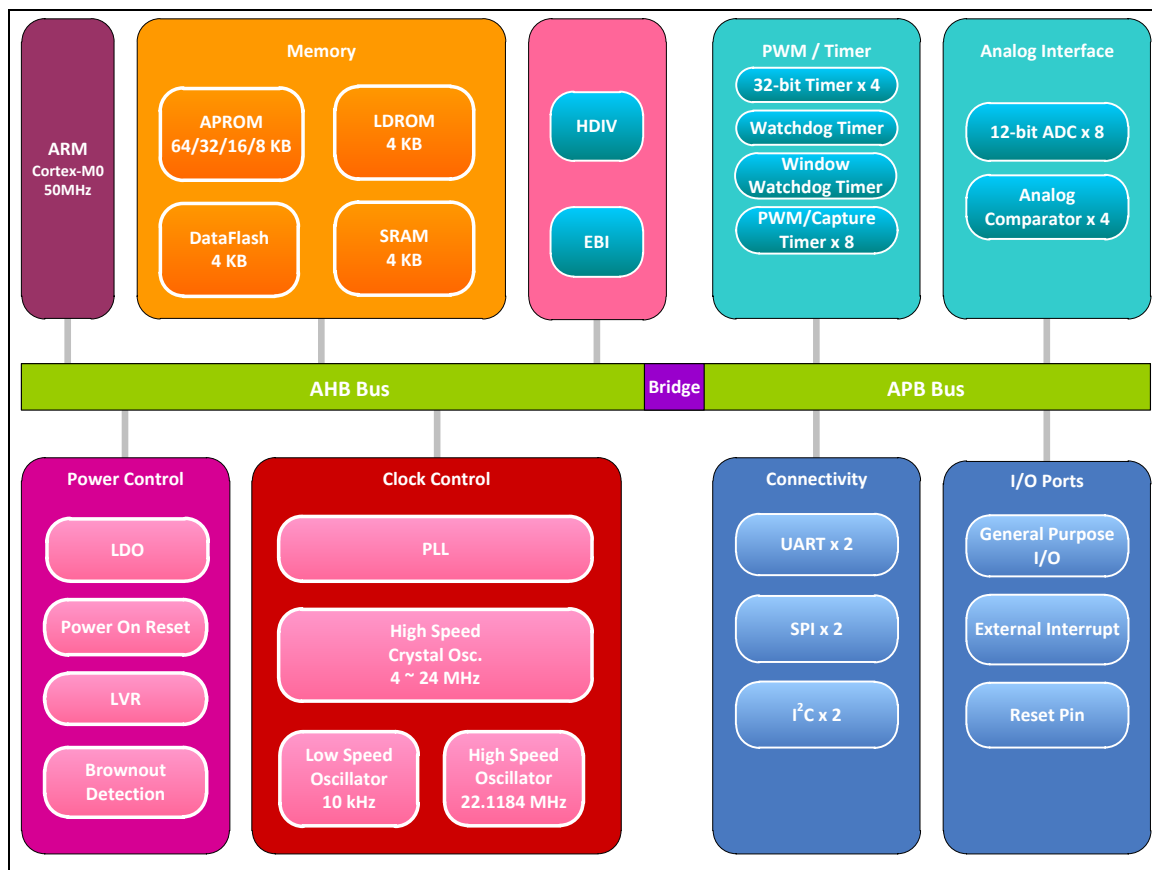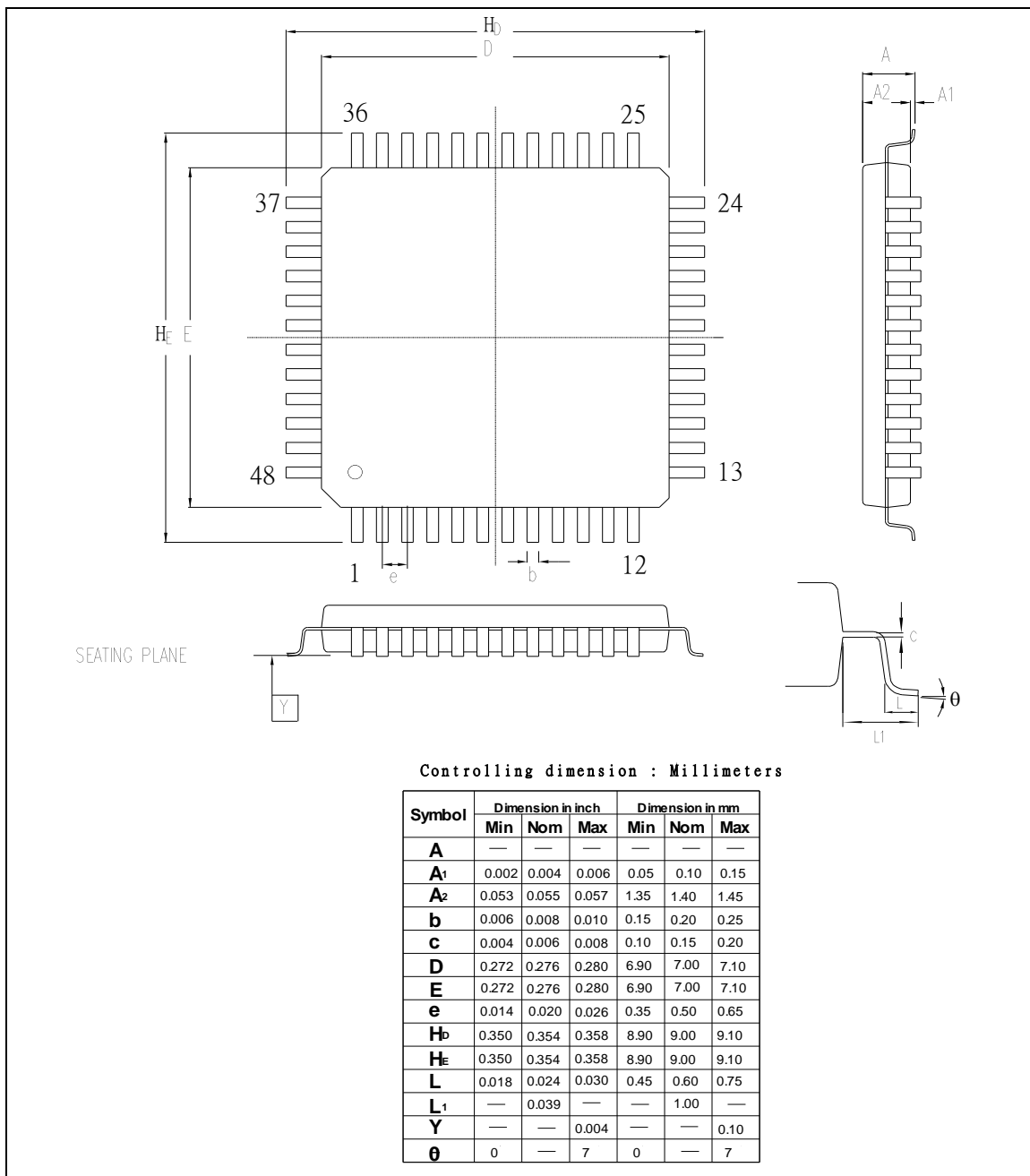
4 BLOCK DIAGRAM

Figure 4-1 NuMicro® M051 DN/DE Series Block Diagram

5   PACKAGE DIMENSIONS

5.1   LQFP-48 (7x7x1.4mm^2 Footprint 2.0mm)

Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A$_1$	0.002	0.004	0.006	0.05	0.10	0.15
A$_2$	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H$_D$	0.350	0.354	0.358	8.90	9.00	9.10
H$_E$	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L$_1$	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

5.2   QFN-33 (5X5 mm^2, Thickness 0.8mm, Pitch 0.5 mm)

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	
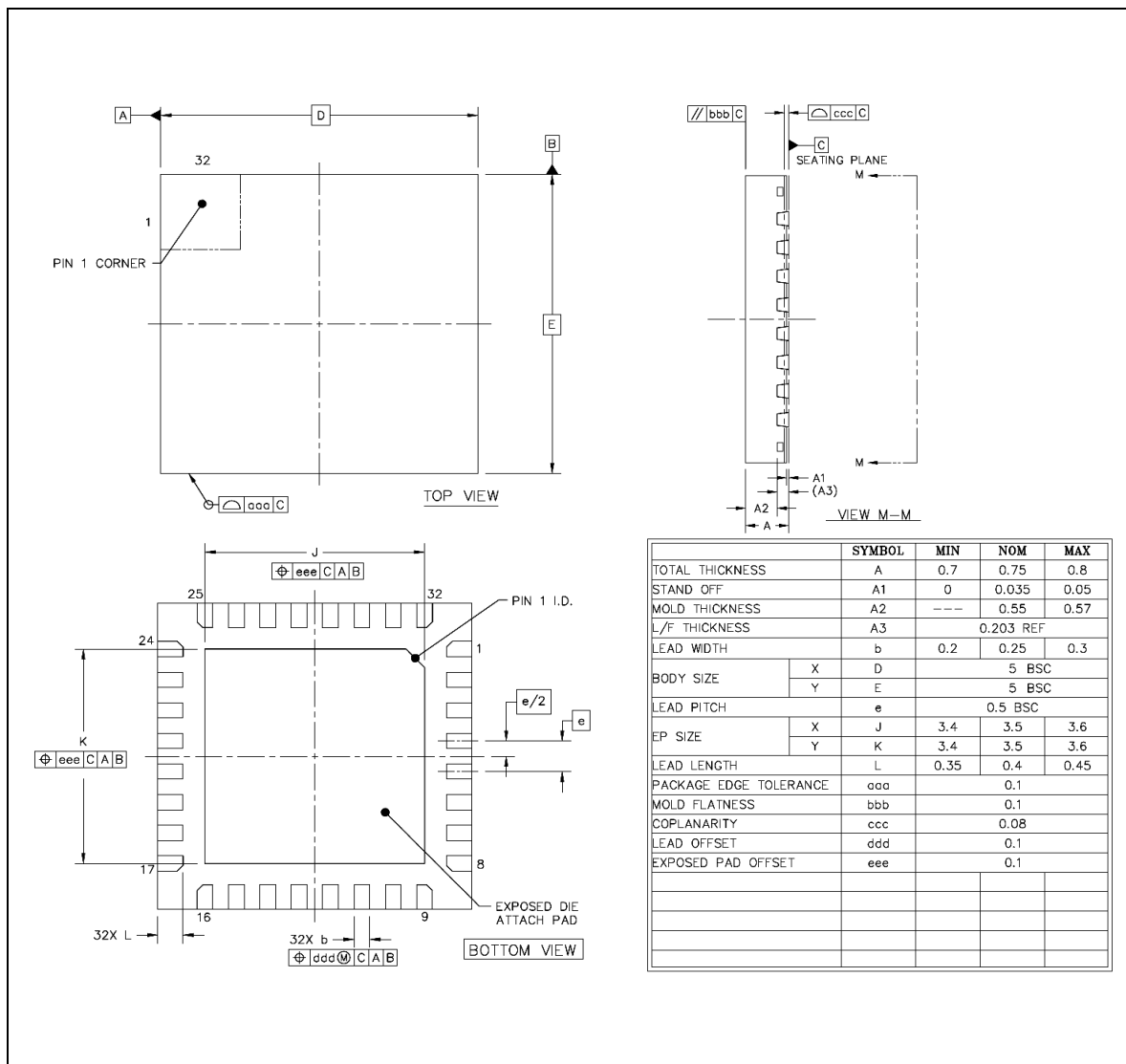
6 REVISION HISTORY

Date	Revision	Description
2013.09.15	1.00	1. Initially issued.
2015.05.12	1.01	1. Changed the order of Chapter 4 BLOCK DIAGRAM 2. Fixed typos and obscure description. 3. Fixed the number of COMP. sets in 3.1 NuMicro® M051 Series M05xxDN Selection Guide and 3.2 NuMicro® M051 Series M05xxDE Selection Guide 4. Removed description about ACMP output inverse function available on M05xxDN.
2015.10.05	1.02	1. Changed NuMicro™ to NuMicro®. 2. Updated Figure 4-1 NuMicro® M051 DN/DE Series Block Diagram.

M051 DN/DE SERIES PRODUCT BRIEF

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