AFE58JD16 16-Channel Ultrasound AFE with 90-mW/Channel Power, 1-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC and Passive CW Mixer

1 Features

- 16-Channel, AFE for Ultrasound Applications:
  - Input Attenuator, LNA, LPF, ADC, and CW Mixer
  - Digital Time Gain Compensation (DTGC)
  - Total Gain Range: 6 dB to 45 dB
  - Linear Input Range: 1 V_{PP}
- Input Attenuator with DTGC:
  - 8-dB to 0-dB Attenuation with 0.125-dB Step
  - Supports Matched Impedance for:
    - 50-Ω to 800-Ω Source Impedance
- Low-Noise Amplifier (LNA) with DTGC:
  - 14-dB to 45-dB Gain with 0.125-dB Step
  - Low Input Current Noise: 1.2 pA/√Hz
- 3rd-Order, Linear-Phase, Low-Pass Filter (LPF):
  - 10 MHz, 15 MHz, 20 MHz, and 25 MHz
- Analog-to-Digital Converter (ADC):
  - 14-Bit ADC: 75-dBFS SNR at 65 MSPS
  - 12-Bit ADC: 72-dBFS SNR at 80 MSPS
- LVDS Interface with a Maximum Speed Up to 1 GBPS
- Optimized for Noise and Power:
  - 90 mW/Ch at 1 nV/√Hz, 65 MSPS
  - 55 mW/Ch at 1.45 nV/√Hz, 40 MSPS
  - 59 mW/Ch in CW Mode
- Excellent Device-to-Device Gain Matching:
  - ±0.5 dB (Typical)
- Low Harmonic Distortion: –60-dBc Level
- Fast and Consistent Overload Recovery
- Continuous Wave (CW) Path with:
  - Low Close-In Phase Noise of –148 dBc/Hz at 1-kHz frequency
  - Phase Resolution: λ / 16
  - Supports 16X, 8X, 4X, and 1X CW Clocks
- Digital Features:
  - Digital I/Q Demodulator after ADC:
    - Fractional Decimation Filter M = 1 to 63 with 0.25X Increment Step
    - Data Throughput Reduction After Decimation
    - On-Chip RAM with 32 Preset Profiles
- 5-Gbps JESD Interface:
  - JESD204B Subclass 0, 1, and 2
  - 2, 4, or 8 Channels per JESD Lane
- Small Package: 15-mm × 15-mm NFBGA-289

2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipment
- Sonar Imaging Equipment
- Multichannel, High-Speed Data Acquisition

3 Description

The AFE58JD16 is a highly-integrated, analog front-end (AFE) solution specifically designed for ultrasound systems where high performance, low power, and small size are required.

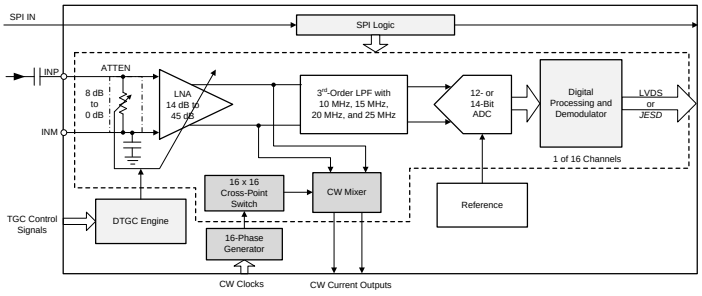
To request a full datasheet or other design resources: request AFE58JD16

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE58JD16	nFBGA (289)	15.00 mm × 15.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2015) to Revision A	Page
• Added link to request full data sheet	1

5 Description (continued)

The AFE58JD16 is an integrated analog front-end (AFE) optimized for medical ultrasound application. The AFE58JD16 is a multichip module (MCM) device with two dies: VCA and ADC_CONV. Each die has total of 16 channels.

Each channel in the VCA die can be configured in two modes: time gain compensation (TGC) mode and continuous wave (CW) mode. In TGC mode, each channel includes an input attenuator (ATTEN), a low-noise amplifier (LNA) with variable-gain, and a third-order, low-pass filter (LPF). The attenuator supports an attenuation range of 8 dB to 0 dB, and the LNA supports gain ranges from 14 dB to 45 dB. The LPF cutoff frequency can be configured at 10 MHz, 15 MHz, 20 MHz, or 25 MHz to support ultrasound applications with different frequencies. In CW mode, each channel includes an LNA with a fixed gain of 18 dB, and a low-power passive mixer with 16 selectable phase delays. Different phase delays can be applied to each analog input signal to perform an on-chip beamforming operation. A harmonic filter in the CW mixer suppresses the third and fifth harmonic to enhance the sensitivity of the CW Doppler measurement. CW mode supports three clock modes: 16X, 8X, and 4X.

Each channel of the ADC_CONV die has a high-performance analog-to-digital converter (ADC) with a programmable resolution of 14 bits or 12 bits. The ADC achieves 75-dBFS signal-to-noise ratio (SNR) in 14-bit mode, and 72-dBFS SNR in 12-bit mode. This ADC provides excellent SNR at low-channel gain. The devices operate at maximum speeds of 65 MSPS and 80 MSPS, providing 14-bit and 12-bit output, respectively. The ADC is designed to scale power with sampling rate. The output interface of the ADC is a low-voltage differential signaling (LVDS) or JESD interface that can easily interface with low-cost field-programmable gate arrays (FPGAs).

The AFE58JD16 includes an optional digital demodulator and JESD204B data packing blocks after the 12- or 14-bit ADC. The digital in-phase and quadrature (I/Q) demodulator with programmable fractional decimation filters accelerates computationally-intensive algorithms at low power. The device also supports an optional JESD204B interface that runs up to 5 Gbps and further reduces the circuit-board routing challenges in high-channel count systems.

The AFE58JD16 also allows various power and noise combinations to be selected for optimizing system performance. Therefore, these devices are suitable ultrasound AFE solutions for systems with strict battery-life requirements. The AFE58JD16 is available in a 15-mm × 15-mm NFBGA-289 package (ZAV package, S-PBGA-N289) and is specified for operation from –40°C to +85°C. The device pinout is also similar to the AFE5818 family.

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

AFE5818 Data Sheet, SBAS687

ADS8413 Data Sheet, SLAS490

ADS8472 Data Sheet, SLAS514

CDCE72010 Data Sheet, SCAS858

CDCM7005 Data Sheet, SCAS793

ISO7240 Data Sheet, SLLS868

LMK04803 Data Sheet, SNAS489

OPA1632 Data Sheet, SBOS286

OPA2211 Data Sheet, SBOS377

SN74AUP1T04 Data Sheet, SCES800

THS4130 Data Sheet, SLOS318

MicroStar BGA Packaging Reference Guide, SSYZ015

WEBENCH® Filter Designer

6.2 Trademarks

All trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE58JD16ZAV	ACTIVE	NFBGA	ZAV	289	126	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE58JD16	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

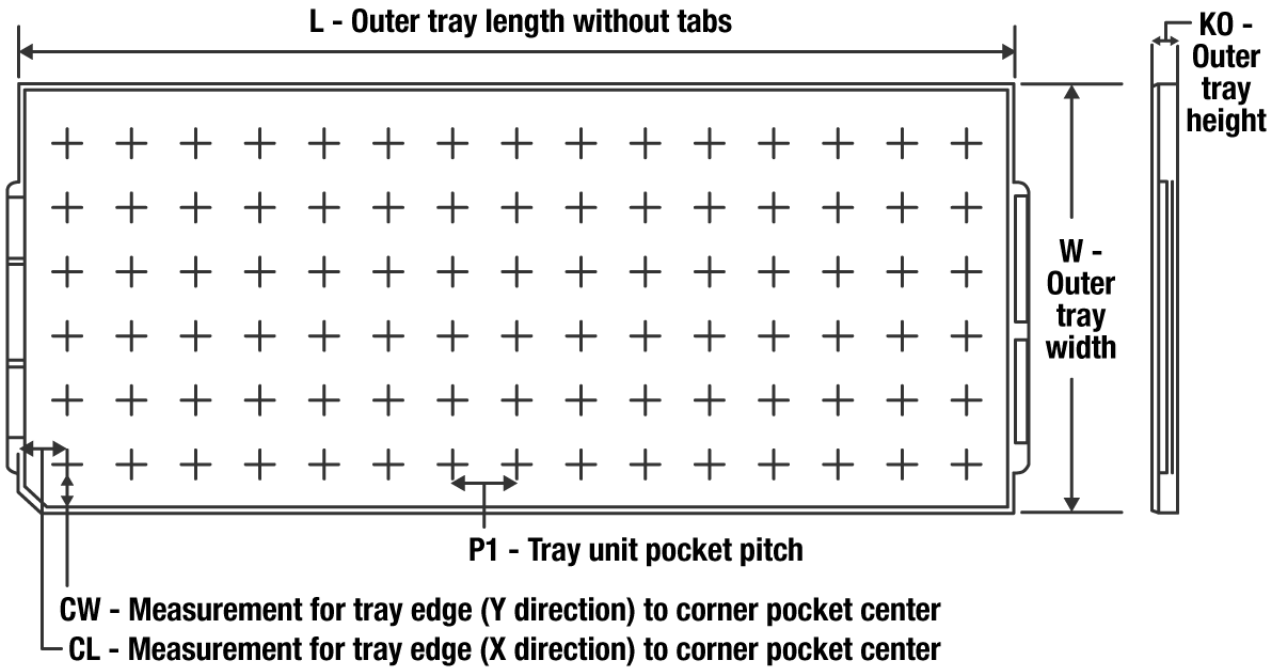
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

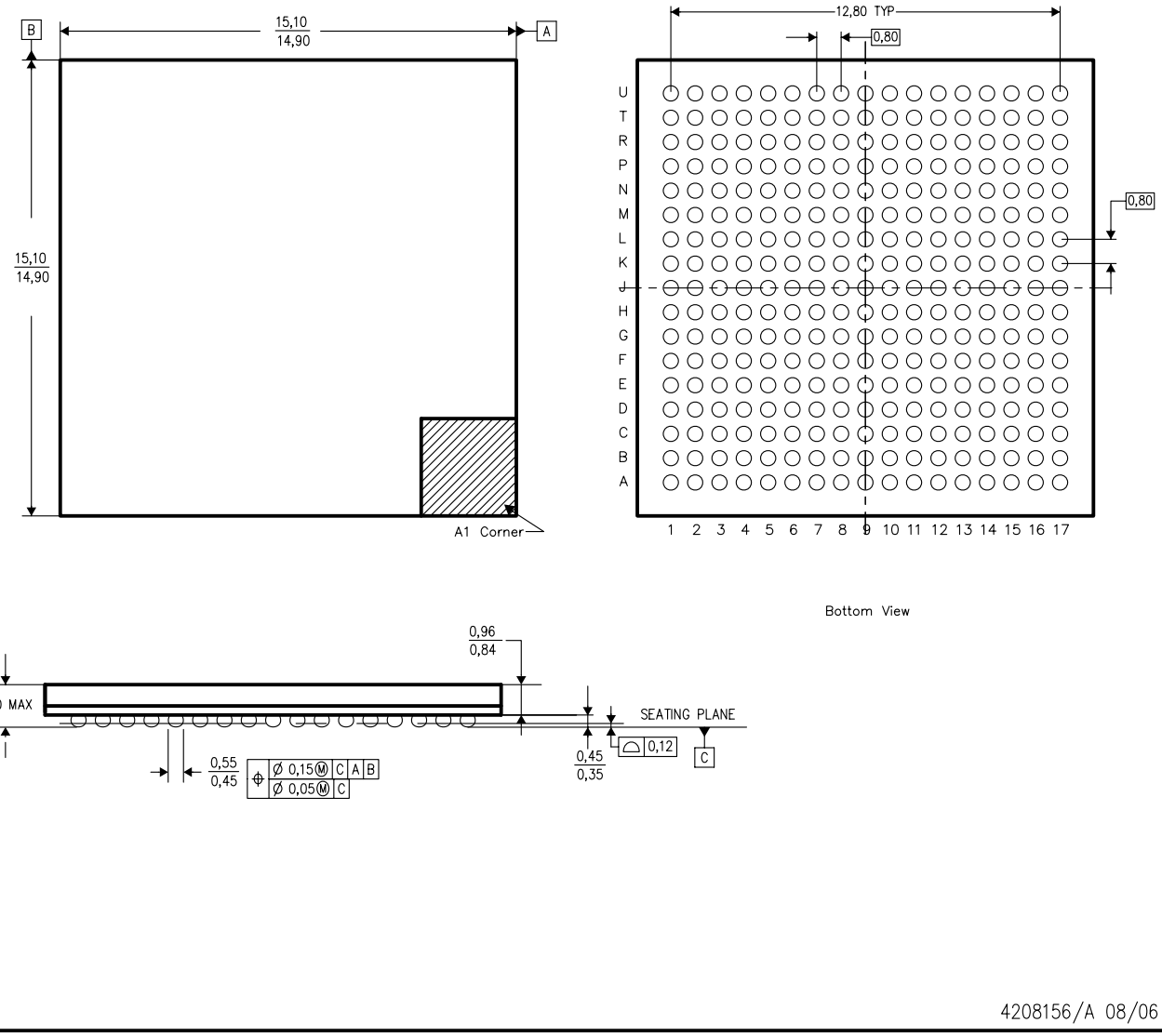


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE58JD16ZAV	ZAV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35

ZAV (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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