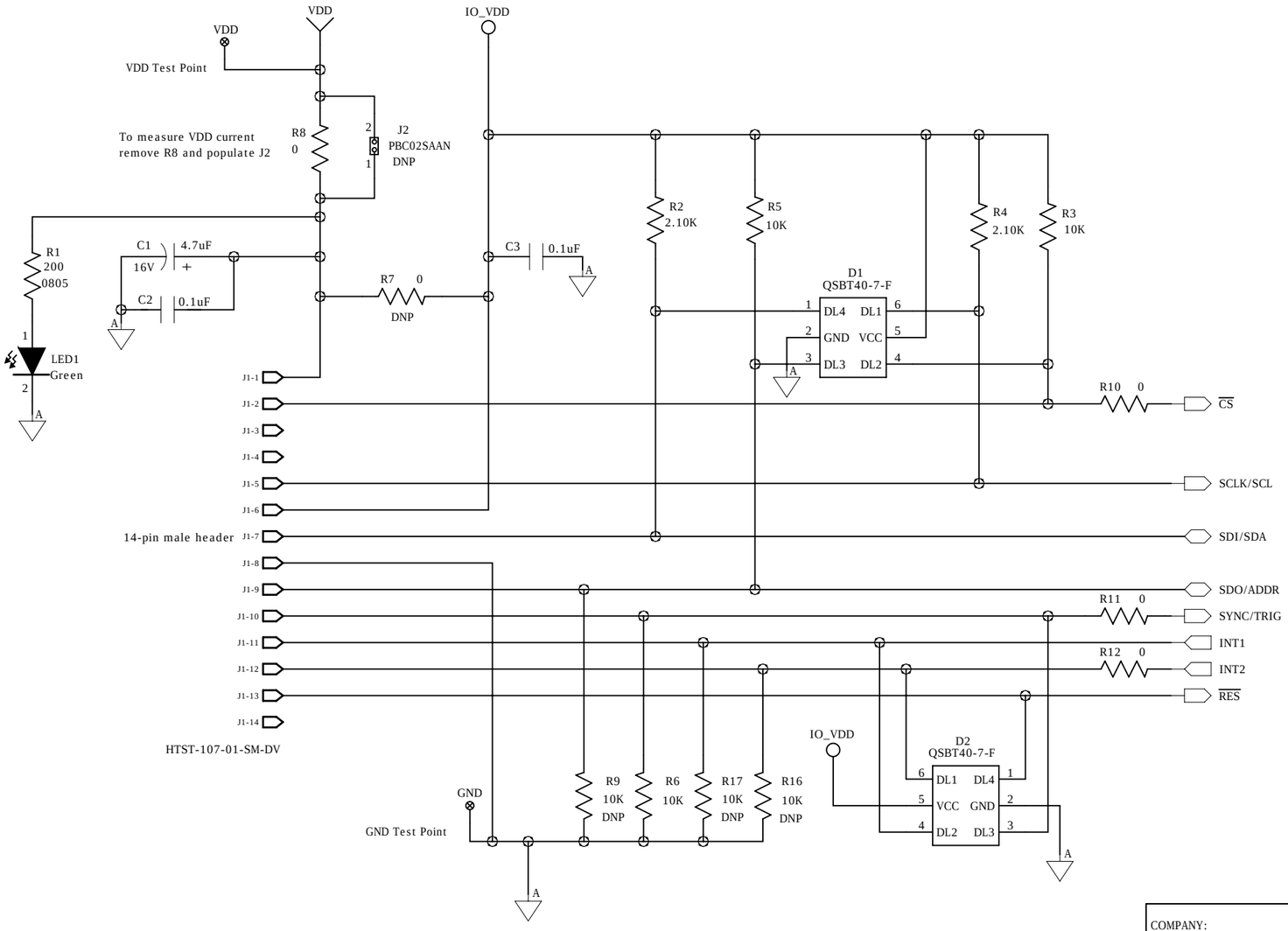


NOTES:

1) All resistors are 1%, 1/10W, 0603 unless otherwise specified.
2) All ceramic capacitors are 0.1uF, 10%, 50V, X7R, 0603 unless otherwise specified.
3) Index:
   - Sheet 1: Interface Connector J1; this sheet.
   - Sheet 2: U1 - 2x2 LGA 12-Pin.
   - Sheet 3: U2 - 2x2 LGA 12-pin (2) (*Alternative Pinout)
   - Sheet 4: U3 - 3x3 LGA 10-Pin.
   - Sheet 5: U4 - 3x3 LGA 16-Pin.
   - Sheet 6: U5 - 5x5 DFN 14-Pin.
   - Sheet 7: U6 - 3x2.5 LGA 14-Pin.
   - Sheet 8: Revision History.

DRAWN: J Zappala	DATED: 05/02/2019
CHECKED: A Chernyakov	DATED: 02/08/2019
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

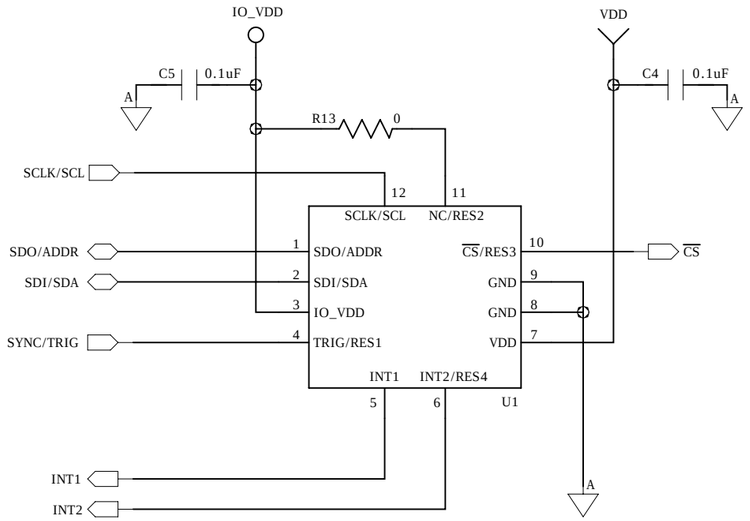
COMPANY: Kionix Inc.

TITLE: RoKiX Digital Evaluation Board
Interface Connector

CODE:	SIZE:	DRAWING NO:	REV:
DWG1029	B	KMAEDA006R00	D

SCALE: NONE

SHEET: 1 of 8



2x2 LGA 12-Pin

PIN	Pinout Type-1	Pinout Type-2	Pinout Type-3
1	SDO/ADDR	ADDR	ADDR
2	SDI/SDA	SDA	SDA
3	IO_VDD	IO_VDD	IO_VDD
4	TRIG	RES****	RES****
5	INT1	INT1	INT1
6	INT2	GND*	GND*
7	VDD	VDD	VDD
8	GND	GND	GND
9	GND	GND	GND
10	nCS	VDD**	VDD**
11	NC	IO_VDD	IO_VDD***
12	SCLK/SCL	SCL	SCL

* GND pins 6, 8, and 9 are internally tied together. Thus, pin 6 may be left floating.
** VDD pins 7, and 10 are internally tied together. Thus, pin 10 may be left floating.
*** IO_VDD pins 3, and 11 are internally tied together. Thus, pin 11 may be left floating. (Does not apply to KXTJ2)
**** RES pin 4 connect to GND. Do not leave floating.

1) Population-
a) Pinout Type 1: KX021, KX022, KX112, KX122, KX116, KX126, KX222, KX132
X i. Populate: R10, R12, R13 (optional)
X ii. Remove:
b) Pinout Type 2: KXTJ2:
X i. Populate: R6, R11, R13
X ii. Remove: R10, R12
c) Pinout Type 3: KXTJ3:
X i. Populate: R6, R11, R13 (optional)
X ii. Remove: R10, R12

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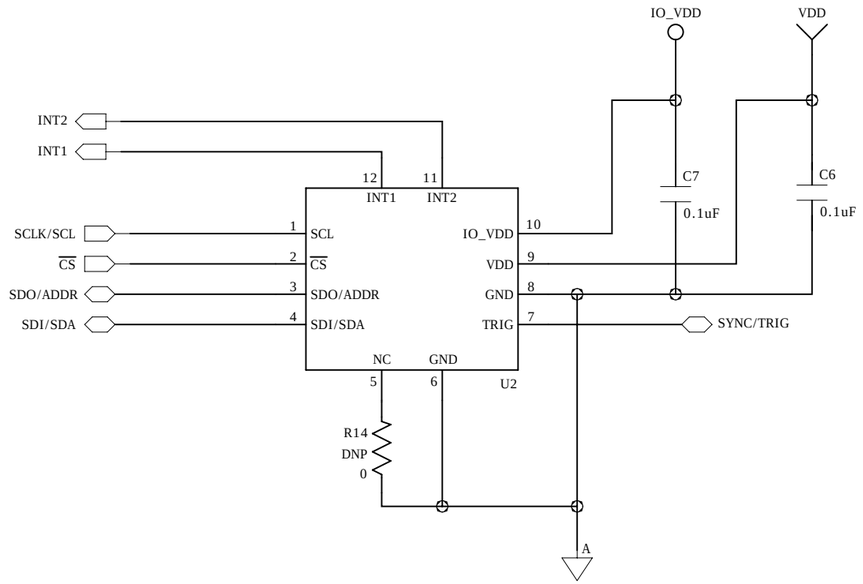
COMPANY: Kionix Inc.

TITLE: RoKiX Digital Evaluation Board
2x2 LGA12-Pin

CODE:	SIZE:	DRAWING NO:	REV:
DWG1029	B	KMAEDA006R00	D

SCALE: NONE SHEET: 2 of 8



2x2 LGA 12-Pin (2)

*Alternative Pinout

PIN	Pinout Type-1	Pinout Type-2
1	SCLK/SCL	SCL
2	nCS	NC
3	SDO/ADDR	ADDR
4	SDI/SDA	SDA
5	NC	NC
6	GND	GND*
7	TRIG	RES**
8	GND	GND*
9	VDD	VDD
10	IO_VDD	IO_VDD
11	INT2	NC
12	INT1	INT

* GND pins 6, 8 are internally tied together
** Reserved. Connect to GND. Do not leave floating.

1) Population-
a) Pinout Type 1: KX127
X i. Populate:
X ii. Remove:
b) Pinout Type 2: KX003
X i. Populate:
X ii. Remove:

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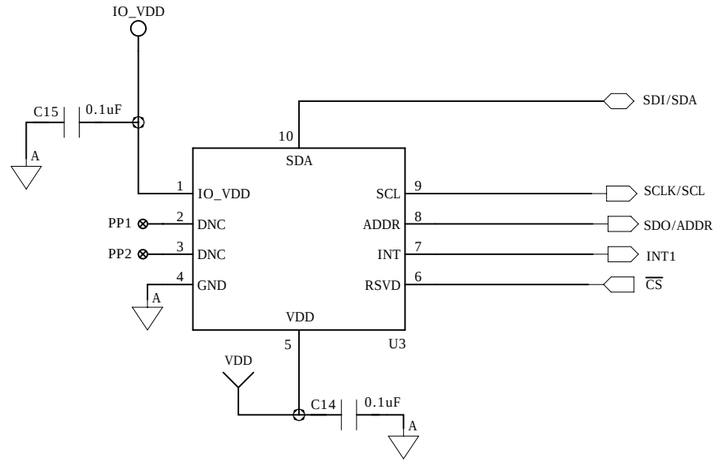
CHECKED: A Chernyakov	DATED: 02/08/2019	TITLE: RoKiX Digital Evaluation Board 2x2 LGA 12-Pin (2)	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: DWG1029	SIZE: B
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: KMAEDA006R00	REV: D
		SCALE: NONE	SHEET: 3 of 8



3x3 LGA 10-Pin

PIN	Pinout Type-1
1	IO_VDD
2	Reserved*
3	Reserved*
4	GND
5	VDD
6	Reserved**
7	INT1
8	ADDR
9	SCL
10	SDA

* Reserved pins 2 and 3 should be left floating

* Reserved pint 6 should be connected to GND, VDD, or IO_VDD

1) Population-
   a) Pinout Type 1: KXCJB, KXCJC
   X i. Populate:
   X ii. Remove:

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RELEASED: <Released By>	DATED: <Release Date>

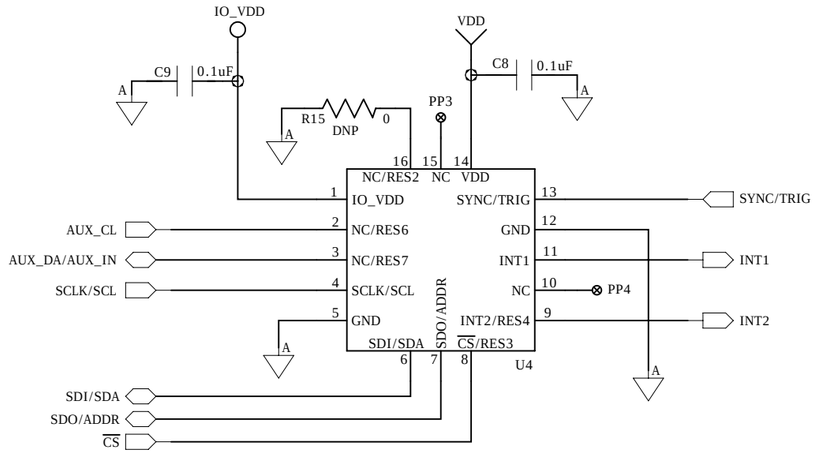
COMPANY: Kionix Inc.

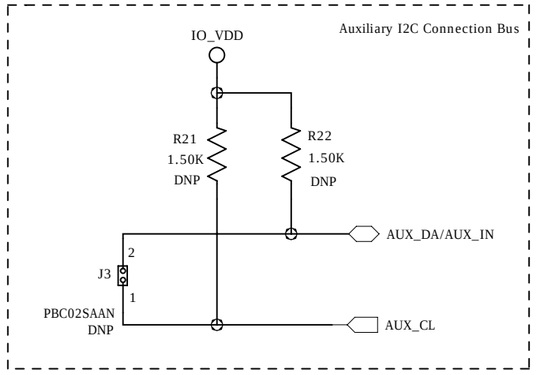
TITLE: RoKiX Digital Evaluation Board
3x3 LGA 10-Pin

CODE:	SIZE:	DRAWING NO:	REV:
DWG1029	B	KMAEDA006R00	D

SCALE: NONE

SHEET: 4 of 8





1) Population (pinout type specific):
   a) Pinout Type 1: KX023, KX123, KX124, KX224, KX134
   X i. Populate:
   X ii. Remove:
   b) Pinout Type 2: KMX62, KMX63
   X i. Populate:
   X ii. Remove:
   c) Pinout Type 3: KMX64, KMX65
   X i. Populate:
   X ii. Remove:
   c) Pinout Type 3: KX007
   X i. Populate:
   X ii. Remove:

3x3 LGA 16-Pin

PIN	Pinout Type-1	Pinout Type-2	Pinout Type-3	Pinout Type-4	
1	IO_VDD	IO_VDD	IO_VDD	IO_VDD	
2	NC	CAP	NC	AUX_CL	
3	NC	GND**	NC	AUX_DA	
4	SCLK/SCL	SCL	SCLK/SCL	SCLK/SCL	
5	GND	GND**	GND^	NC	
6	SDI/SDA	SDA	SDI/SDA	MOSI/SDA	
7	SDO/ADDR	ADDR	SDO/ADDR	MISO/ADDR	
8	nCS	NC	nCS	nCS	
9	INT2	GPIO2*	GPIO2*	INT2	
10	NC	NC	NC	NC	
11	INT1	GPIO1*	GPIO1*	INT1	
12	GND	GND**	GND^	GND	
13	TRIG	NC	NC	SYNC_TRIG	
14	VDD	VDD	VDD	VDD	
15	NC	NC	NC	NC	
16	NC	NC	NC	NC	

NC: Not Connected internally. Can be connected to IO_VDD, GND, or left floating.
*GPIO1, GPIO2 (pins 11, 9) cannot float when configured as an input
**GND pins 3, 5, 12 are internally tied together to GND
^GND pins 5 and 12 are internally tied together to GND

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QUALITY CONTROL: <QC By>	DATED: <QC Date>	
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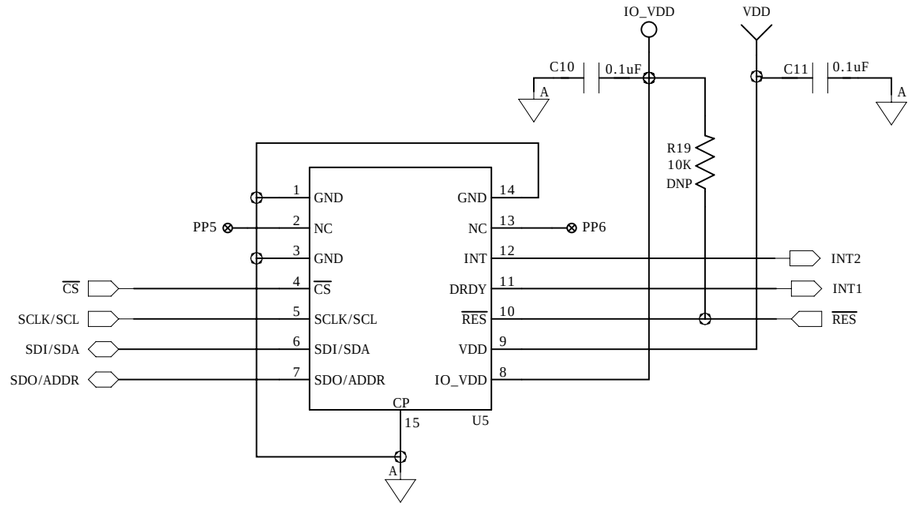
COMPANY: Kionix Inc.

TITLE: RoKiX Digital Evaluation Board
3x3 LGA 16-Pin

CODE:	SIZE:	DRAWING NO:	REV:
DWG1029	B	KMAEDA006R00	D

SCALE: NONE SHEET: 5 of 8



5x5 DFN 14-Pin

PIN	Pinout Type-1
1	GND
2	NC
3	GND
4	$\overline{CS}$
5	SCLK/SCL
6	SDI/SDA
7	SDO/ADDR
8	IO_VDD
9	VDD
10	$\overline{RES}$
11	DRDY
12	INT
13	NC
14	GND

1) Population-
   a) Pinout Type 1: KX03A, KX03B, KX03C, KX03D
   X i. Populate: R19
   X ii. Remove:

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RELEASED: <Released By>	DATED: <Release Date>		

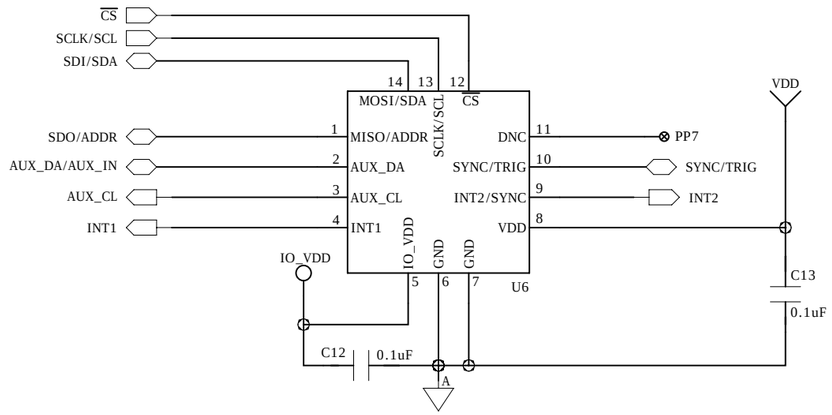
COMPANY: Kionix Inc.

TITLE: RoKiX Digital Evaluation Board
5x5 DFN 14-Pin

CODE:	SIZE:	DRAWING NO:	REV:
DWG1029	B	KMAEDA006R00	D

SCALE: NONE

SHEET: 6 of 8



3x2.5 LGA 14-Pin

PIN	Pinout Type-1
1	MISO/ADDR
2	AUX_DA
3	AUX_CLK
4	INT1
5	IO_VDD
6	GND
7	GND
8	VDD
9	INT2/SYNC
10	SYNC/TRIG
11	DNC*
12	$\overline{CS}$
13	SCLK/SCL
14	MOSI/SDA

*DNC Pin 11: Connect to GND or leave floating.

1) Population-
a) Pinout Type 1: KXG08
X i. Populate:
X ii. Remove:

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QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		

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TITLE: RoKiX Digital Evaluation Board
3x2.5 LGA 14-Pin

CODE:	SIZE:	DRAWING NO:	REV:
DWG1029	B	KMAEDA006R00	D

SCALE: NONE SHEET: 7 of 8

REVISION RECORD				
DATE:	DRAWN BY:	DESCRIPTION:	CHECKED BY:	DATE:
01/24/2019	J Zappala	1) Initial release.		
01/31/2019	J Zappala	1) Rearrange devices on sheets to match layout and update sheet names.		
		2) Rename: TPX to PPX; net TRIG to SYNC/TRIG; net SYNC to RES; $\overline{\text{U4}}$-10 from NC/RES5; U4-13 from TRIG/RES1; PPS sequentially.		
		3) Replace capacitor connected to U6-11 with a PP.		
		4) Add: Note 3, Sheet 1; PPX to U4-10; RES $\overline{\text{net}}$.		
		5) Delete: connection to U4-10; 10K pull-dowm on J1-13.		
02/08/2019	A Chernyakov	1) Updated Notes.		
05/02/2019	A Chernyakov	1) Add DNP to R19.		

MTHOLE1 MTHOLE150
MTHOLE2 MTHOLE150
MTHOLE3 MTHOLE150
MTHOLE4 MTHOLE150
FD1 FIDUCIAL_40MIL
FD2 FIDUCIAL_40MIL
FD3 FIDUCIAL_40MIL

DRAWN: J Zappala	DATED: 05/02/2019		
CHECKED: A Chernyakov	DATED: 02/08/2019		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		

COMPANY: Kionix Inc.

TITLE: RoKiX Digital Evaluation Board
Revision History

CODE:	SIZE:	DRAWING NO:	REV:
DWG1029	B	KMAEDA006R00	D

SCALE: NONE SHEET: 8 of 8