TPS659037 Register Map

Technical Reference Manual

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Introduction

This document presents a summary of the hardware interface for the TPS659037 device. Each module instance within the design is shown as well as the module register map and bit definitions for each bit field.

1.1 Register Address Mapping

This document describes the register mapping of the TPS659037 device. The operation of the IC is described in the device data sheet, *TPS659037 Power Management Unit (PMU) for Processor*.

The 3 hex digits of the physical address of the register indicated in this document are mapped as 0xPAA, while P stands for the page number of the register, and AA stands for the register address within the memory page. The page numbers are mapped to the slave device address as following:

Page = 0x0 — Slave device address 0x12 for DVS registers

Page = 0x1 — Slave device address 0x48 or 0x58 for power registers

Page = 0x2 — Slave device address 0x49 or 0x59 for interface and auxiliary registers

Page = 0x3 — Slave device address 0x4A or 0x5A for trimming and test registers

Page = 0x4 — Slave device address 0x4B or 0x5B for OTP programming registers

For the reset of the registers, the registers are defined by the following three categories:

- POR: Power-on-reset registers
- HWRST: Hardware reset registers
- SWORST: Switch-off reset registers

Table 1-1 lists these categories of registers.

Table 1-1. Reset Levels

LEVEL	RESET TAG	REGISTERS AFFECTED	COMMENT
0	POR	POR, HW, SWO	This reset level is the lowest level, for which all registers are reset.
1	HWRST	HW, SWO	During hardware reset (HWRST), all registers are reset except the POR registers.
2	SWORST	SWO	Only the SWO registers are reset.

A bit reset value of 0bX indicates that the bit value is coming from the OTP memory.

NOTE: All reserved bits are read only (R). A read to an unmapped register returns the previous read value.

Register Physical Address

2.1 Register Module Base Address

Table 2-1 lists the base address and address space for the module instances.

Table 2-1. Functional Registers Module Instance Summary

Address	Register	Section
0x020	FUNC_SMPS_DVS	Section 3.1
0x100	FUNC_RTC	Section 3.2
0x118	FUNC_BACKUP	Section 3.3
0x120	FUNC_SMPS	Section 3.4
0x150	FUNC_LDO	Section 3.5
0x17F	FUNC_SPI	Section 3.6
0x1A0	FUNC_PMU_CONTROL	Section 3.7
0x1D4	FUNC_RESOURCE	Section 3.8
0x1F4	FUNC_PAD_CONTROL	Section 3.9
0x210	FUNC_INTERRUPT	Section 3.10
0x24F	FUNC_ID	Section 3.11
0x280	FUNC_GPIO	Section 3.12
0x2C0	FUNC_GPADC	Section 3.13
0x357	FUNC_DESIGNREV	Section 3.14
0x3C1	FUNC_OSCILLATOR	Section 3.15
0x3CD	FUNC_TRIM_GPADC	Section 3.16

Complex bit access types are encoded to fit into small table cells. Table 2-2 shows the codes that are used for access types in this document.

Table 2-2. FUNC_PAD_CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
C	C	Clear by performing either a read or a write
Write Type		
W	W	Write
C	C	Clear by performing either a read or a write

Register Descriptions

3.1 FUNC_SMPS_DVS Registers

Table 3-1 lists the memory-mapped registers for the FUNC_SMPS_DVS. All register offset addresses not listed in Table 3-1 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. FUNC_SMPS_DVS Registers

Address	Acronym	Register Name	Section
22h	SMPS12_FORCE	SMPS12 DVS Register	Section 3.1.1
23h	SMPS12_VOLTAGE	SMPS12 DVS Register	Section 3.1.2
2Ah	SMPS45_FORCE	SMPS45 DVS Register	Section 3.1.3
2Bh	SMPS45_VOLTAGE	SMPS45 DVS Register	Section 3.1.4
2Eh	SMPS6_FORCE	SMPS6 DVS Register	Section 3.1.5
2Fh	SMPS6_VOLTAGE	SMPS6 DVS Register	Section 3.1.6
36h	SMPS8_FORCE	SMPS8 DVS Register	Section 3.1.7
37h	SMPS8_VOLTAGE	SMPS8 DVS Register	Section 3.1.8

3.1.1 SMPS12_FORCE Register (Address = 22h) [reset = X]

SMPS12_FORCE is shown in Figure 3-1 and described in Table 3-2.

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SMPS12 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-1. SMPS12_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-2. SMPS12_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS12_FORCE.VSEL voltage is applied When 1: SMPS12_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS12_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).

3.1.2 SMPS12_VOLTAGE Register (Address = 23h) [reset = X]

SMPS12_VOLTAGE is shown in Figure 3-2 and described in Table 3-3.

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SMPS12 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-2. SMPS12_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-3. SMPS12_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS12_VOLTAGE.VSEL and SPMS12_FORCE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).

3.1.3 SMPS45_FORCE Register (Address = 2Ah) [reset = X]

SMPS45_FORCE is shown in Figure 3-3 and described in Table 3-4.

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SMPS45 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-3. SMPS45_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-4. SMPS45_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS45_FORCE.VSEL voltage is applied When 1: SMPS45_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS45_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).

3.1.4 SMPS45_VOLTAGE Register (Address = 2Bh) [reset = X]

SMPS45_VOLTAGE is shown in Figure 3-4 and described in Table 3-5.

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SMPS45 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-4. SMPS45_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-5. SMPS45_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS45_VOLTAGE.VSEL and SPMS45_FORCE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).

3.1.5 SMPS6_FORCE Register (Address = 2Eh) [reset = X]

SMPS6_FORCE is shown in Figure 3-5 and described in Table 3-6.

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SMPS6 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-5. SMPS6_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-6. SMPS6_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS6_FORCE.VSEL voltage is applied When 1: SMPS6_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS6_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).

3.1.6 SMPS6_VOLTAGE Register (Address = 2Fh) [reset = X]

SMPS6_VOLTAGE is shown in Figure 3-6 and described in Table 3-7.

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SMPS6 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-6. SMPS6_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-7. SMPS6_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS6_VOLTAGE.VSEL and SPMS6_FORCE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).

3.1.7 SMPS8_FORCE Register (Address = 36h) [reset = X]

SMPS8_FORCE is shown in Figure 3-7 and described in Table 3-8.

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SMPS8 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-7. SMPS8_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-8. SMPS8_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS8_FORCE.VSEL voltage is applied When 1: SMPS8_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS8_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).

3.1.8 SMPS8_VOLTAGE Register (Address = 37h) [reset = X]

SMPS8_VOLTAGE is shown in Figure 3-8 and described in Table 3-9.

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SMPS8 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-8. SMPS8_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-9. SMPS8_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS8_VOLTAGE.VSEL and SPMS8_FORCE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register (page1).

3.2 FUNC_RTC Registers

Table 3-10 lists the memory-mapped registers for the FUNC_RTC. All register offset addresses not listed in Table 3-10 should be considered as reserved locations and the register contents should not be modified.

Table 3-10. FUNC_RTC Registers

Address	Acronym	Register Name	Section
100h	SECONDS_REG	RTC Register for Seconds	Section 3.2.1
101h	MINUTES_REG	RTC Register for Minutes	Section 3.2.2
102h	HOURS_REG	RTC Register for Hours	Section 3.2.3
103h	DAYS_REG	RTC Register for Days	Section 3.2.4
104h	MONTHS_REG	RTC Register for Months	Section 3.2.5
105h	YEARS_REG	RTC Register for Years	Section 3.2.6
106h	WEEKS_REG	RTC Register for Day of the Week	Section 3.2.7
108h	ALARM_SECONDS_REG	RTC Register for Alarm Programmation for Seconds	Section 3.2.8
109h	ALARM_MINUTES_REG	RTC Register for Alarm Programmation for Minutes	Section 3.2.9
10Ah	ALARM_HOURS_REG	RTC Register for Alarm Programmation for Hours	Section 3.2.10
10Bh	ALARM_DAYS_REG	RTC Register for Alarm Programmation for Days	Section 3.2.11
10Ch	ALARM_MONTHS_REG	RTC Register for Alarm Programmation for Months	Section 3.2.12
10Dh	ALARM_YEARS_REG	RTC Register for Alarm Programmation for Years	Section 3.2.13
110h	RTC_CTRL_REG	RTC Control Register	Section 3.2.14
111h	RTC_STATUS_REG	RTC Status Register	Section 3.2.15
112h	RTC_INTERRUPTS_REG	RTC Interrupt Control Register	Section 3.2.16
113h	RTC_COMP_LSB_REG	RTC Compensation Register (LSB)	Section 3.2.17
114h	RTC_COMP_MSB_REG	RTC Compensation Register (MSB)	Section 3.2.18
115h	RTC_RES_PROG_REG	RTC Register Containing Oscillator Resistance Value	Section 3.2.19
116h	RTC_RESET_STATUS_REG	RTC Register for Reset Status	Section 3.2.20

3.2.1 SECONDS_REG Register (Address = 100h) [reset = 0h]

SECONDS_REG is shown in Figure 3-9 and described in Table 3-11.

Return to Summary Table.

RTC register for seconds
RESET register domain: POR
MSECURE register protected : Yes

Figure 3-9. SECONDS_REG Register

7	6	5	4	3	2	1	0
RESERVED	SEC1			SEC0			
R-0h	R/W-0h			R/W-0h			

Table 3-11. SECONDS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved bit
6-4	SEC1	R/W	0h	Second digit of seconds (range is 0 up to 5)
3-0	SEC0	R/W	0h	First digit of seconds (range is 0 up to 9)

3.2.2 MINUTES_REG Register (Address = 101h) [reset = 0h]

MINUTES_REG is shown in Figure 3-10 and described in Table 3-12.

Return to Summary Table.

RTC register for minutes
RESET register domain: POR
MSECURE register protected : Yes

Figure 3-10. MINUTES_REG Register

7	6	5	4	3	2	1	0
RESERVED	MIN1			MIN0			
R-0h	R/W-0h			R/W-0h			

Table 3-12. MINUTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved bit
6-4	MIN1	R/W	0h	Second digit of minutes (range is 0 up to 5)
3-0	MIN0	R/W	0h	First digit of minutes (range is 0 up to 9)

3.2.3 HOURS_REG Register (Address = 102h) [reset = 0h]

HOURS_REG is shown in Figure 3-11 and described in Table 3-13.

Return to Summary Table.

RTC register for hours
RESET register domain: POR
MSECURE register protected : Yes

Figure 3-11. HOURS_REG Register

7	6	5	4	3	2	1	0
PM_nAM	RESERVED	HOUR1		HOUR0			
R/W-0h	R-0h	R/W-0h		R/W-0h			

Table 3-13. HOURS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PM_nAM	R/W	0h	Only used in PM_AM mode (otherwise it is set to 0) 0 is AM 1 is PM
6	RESERVED	R	0h	Reserved bit
5-4	HOUR1	R/W	0h	Second digit of hours(range is 0 up to 2)
3-0	HOUR0	R/W	0h	First digit of hours (range is 0 up to 9)

3.2.4 DAYS_REG Register (Address = 103h) [reset = 1h]

DAYS_REG is shown in Figure 3-12 and described in Table 3-14.

Return to Summary Table.

RTC register for days
RESET register domain: POR
MSECURE register protected : Yes

Figure 3-12. DAYS_REG Register

7	6	5	4	3	2	1	0
RESERVED		DAY1		DAY0			
R-0h		R/W-0h		R/W-1h			

Table 3-14. DAYS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved bit
5-4	DAY1	R/W	0h	Second digit of days (range is 0 up to 3)
3-0	DAY0	R/W	1h	First digit of days (range is 0 up to 9)

3.2.5 MONTHS_REG Register (Address = 104h) [reset = 1h]

MONTHS_REG is shown in Figure 3-13 and described in Table 3-15.

Return to Summary Table.

RTC register for months
RESET register domain: POR
MSECURE register protected : Yes

Figure 3-13. MONTHS_REG Register

7	6	5	4	3	2	1	0
RESERVED			MONTH1	MONTH0			
R-0h			R/W-0h	R/W-1h			

Table 3-15. MONTHS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved bit
4	MONTH1	R/W	0h	Second digit of months (range is 0 up to 1)
3-0	MONTH0	R/W	1h	First digit of months (range is 0 up to 9)

3.2.6 YEARS_REG Register (Address = 105h) [reset = 0h]

YEARS_REG is shown in Figure 3-14 and described in Table 3-16.

Return to Summary Table.

RTC register for years
RESET register domain: POR
MSECURE register protected : Yes

Figure 3-14. YEARS_REG Register

7	6	5	4	3	2	1	0
YEAR1				YEAR0			
R/W-0h				R/W-0h			

Table 3-16. YEARS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	YEAR1	R/W	0h	Second digit of years (range is 0 up to 9)
3-0	YEAR0	R/W	0h	First digit of years (range is 0 up to 9)

3.2.7 WEEKS_REG Register (Address = 106h) [reset = 0h]

WEEKS_REG is shown in Figure 3-15 and described in Table 3-17.

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RTC register for day of the week
RESET register domain: POR
MSECURE register protected : Yes

Figure 3-15. WEEKS_REG Register

7	6	5	4	3	2	1	0
RESERVED					WEEK		
R-0h					R/W-0h		

Table 3-17. WEEKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved bit
2-0	WEEK	R/W	0h	First digit of day of the week (range is 0 up to 6)

3.2.8 ALARM_SECONDS_REG Register (Address = 108h) [reset = 0h]

ALARM_SECONDS_REG is shown in Figure 3-16 and described in Table 3-18.

Return to Summary Table.

RTC register for alarm programmation for seconds
RESET register domain: POR
MSECURE register protected : No

Figure 3-16. ALARM_SECONDS_REG Register

7	6	5	4	3	2	1	0
RESERVED	ALARM_SEC1			ALARM_SEC0			
R-0h	R/W-0h			R/W-0h			

Table 3-18. ALARM_SECONDS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved bit
6-4	ALARM_SEC1	R/W	0h	Second digit of alarm programmation for seconds (range is 0 up to 5)
3-0	ALARM_SEC0	R/W	0h	First digit of alarm programmation for seconds (range is 0 up to 9)

3.2.9 ALARM_MINUTES_REG Register (Address = 109h) [reset = 0h]

ALARM_MINUTES_REG is shown in Figure 3-17 and described in Table 3-19.

Return to Summary Table.

RTC register for alarm programmation for minutes
RESET register domain: POR
MSECURE register protected : No

Figure 3-17. ALARM_MINUTES_REG Register

7	6	5	4	3	2	1	0
RESERVED	ALARM_MIN1			ALARM_MIN0			
R-0h	R/W-0h			R/W-0h			

Table 3-19. ALARM_MINUTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved bit
6-4	ALARM_MIN1	R/W	0h	Second digit of alarm programmation for minutes (range is 0 up to 5)
3-0	ALARM_MIN0	R/W	0h	First digit of alarm programmation for minutes (range is 0 up to 9)

3.2.10 ALARM_HOURS_REG Register (Address = 10Ah) [reset = 0h]

ALARM_HOURS_REG is shown in Figure 3-18 and described in Table 3-20.

Return to Summary Table.

RTC register for alarm programmation for hours
RESET register domain: POR
MSECURE register protected : No

Figure 3-18. ALARM_HOURS_REG Register

7	6	5	4	3	2	1	0
ALARM_PM_nAM	RESERVED	ALARM_HOUR1		ALARM_HOUR0			
R/W-0h	R-0h	R/W-0h		R/W-0h			

Table 3-20. ALARM_HOURS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALARM_PM_nAM	R/W	0h	Only used in PM_AM mode for alarm programmation (otherwise it is set to 0) 0 is AM 1 is PM
6	RESERVED	R	0h	Reserved bit
5-4	ALARM_HOUR1	R/W	0h	Second digit of alarm programmation for hours(range is 0 up to 2)
3-0	ALARM_HOUR0	R/W	0h	First digit of alarm programmation for hours (range is 0 up to 9)

3.2.11 ALARM_DAYS_REG Register (Address = 10Bh) [reset = 1h]

ALARM_DAYS_REG is shown in Figure 3-19 and described in Table 3-21.

Return to Summary Table.

RTC register for alarm programmation for days
RESET register domain: POR
MSECURE register protected : No

Figure 3-19. ALARM_DAYS_REG Register

7	6	5	4	3	2	1	0
RESERVED		ALARM_DAY1		ALARM_DAY0			
RRSpecial-0h		R/W-0h		R/W-1h			

Table 3-21. ALARM_DAYS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	RRSpecial	0h	Reserved bit
5-4	ALARM_DAY1	R/W	0h	Second digit of alarm programmation for days (range is 0 up to 3)
3-0	ALARM_DAY0	R/W	1h	First digit of alarm programmation for days (range is 0 up to 9)

3.2.12 ALARM_MONTHS_REG Register (Address = 10Ch) [reset = 1h]

ALARM_MONTHS_REG is shown in Figure 3-20 and described in Table 3-22.

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RTC register for alarm programmation for months
RESET register domain: POR
MSECURE register protected : No

Figure 3-20. ALARM_MONTHS_REG Register

7	6	5	4	3	2	1	0
RESERVED			ALARM_MONTH1	ALARM_MONTH0			
R-0h			R/W-0h	R/W-1h			

Table 3-22. ALARM_MONTHS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved bit
4	ALARM_MONTH1	R/W	0h	Second digit of alarm programmation for months (range is 0 up to 1)
3-0	ALARM_MONTH0	R/W	1h	First digit of alarm programmation for months (range is 0 up to 9)

3.2.13 ALARM_YEARS_REG Register (Address = 10Dh) [reset = 0h]

ALARM_YEARS_REG is shown in Figure 3-21 and described in Table 3-23.

Return to Summary Table.

RTC register for alarm programmation for years
RESET register domain: POR
MSECURE register protected : No

Figure 3-21. ALARM_YEARS_REG Register

7	6	5	4	3	2	1	0
ALARM_YEAR1				ALARM_YEAR0			
R/W-0h				R/W-0h			

Table 3-23. ALARM_YEARS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ALARM_YEAR1	R/W	0h	Second digit of alarm programmation for years (range is 0 up to 9)
3-0	ALARM_YEAR0	R/W	0h	First digit of alarm programmation for years (range is 0 up to 9)

3.2.14 RTC_CTRL_REG Register (Address = 110h) [reset = 0h]

RTC_CTRL_REG is shown in Figure 3-22 and described in Table 3-24.

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RTC control register:
NOTES: A dummy read of this register is necessary before each I2C read in order to update the ROUND_30S bit value.
RESET register domain: POR
MSECURE register protected : Yes (excepted GET_TIME bit)

Figure 3-22. RTC_CTRL_REG Register

7	6	5	4	3	2	1	0
RTC_V_OPT	GET_TIME	SET_32_COUNTER	TEST_MODE	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-24. RTC_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RTC_V_OPT	R/W	0h	RTC date / time register selection: 0: Read access directly to dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG, WEEKS_REG) 1: Read access to static shadowed registers: (see GET_TIME bit).
6	GET_TIME	R/W	0h	When writing a 1 into this register, the content of the dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG and WEEKS_REG) is transferred into static shadowed registers. Each update of the shadowed registers needs to be done by re-asserting GET_TIME bit to 1 (i.e.: reset it to 0 and then re-write it to 1) Note: Shadowed registers, linked to the GET_TIME feature, are a parallel set of calendar static registers, at the same I2C addresses as the dynamic registers. Note: The GET_TIME feature loads the RTC counter in the shadow registers and make the content of the shadow registers available and stable for reading. Note: The GET_TIME bit has to be set to 0 and again to 1 to get a new timing value. Note: If the time reading is done without GET_TIME, the read value comes directly from the RTC counter and software has to manage the counter change during the reading. Time reading remains always at the same address, with or without using the GET_TIME feature. Note: This bit is not protected by MSECURE.
5	SET_32_COUNTER	R/W	0h	0: No action 1: set the 32kHz counter with RTC_COMP_MSB_REG/RTC_COMP_LSB_REG value Note: This bit must only be used when the RTC is frozen.
4	TEST_MODE	R/W	0h	0: functional mode 1: test mode (Auto compensation is enable when the 32kHz counter reaches at its end)
3	MODE_12_24	R/W	0h	0: 24 hours mode 1: 12 hours mode (PM-AM mode) Note: It is possible to switch between the two modes at any time without disturbed the RTC, read or write are always performed with the current mode.
2	AUTO_COMP	R/W	0h	0: No auto compensation 1: Auto compensation enabled

Table 3-24. RTC_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ROUND_30S	R/W	0h	0: No update 1: When a one is written, the time is rounded to the closest minute Note: This bit is a toggle bit, the micro-controller can only write one and RTC clears it. If the micro-controller sets the ROUND_30S bit and then read it, the micro-controller will read one until the rounded to the closet minute is perform at the next second.
0	STOP_RTC	R/W	0h	0: RTC is frozen 1: RTC is running

3.2.15 RTC_STATUS_REG Register (Address = 111h) [reset = 80h]

RTC_STATUS_REG is shown in Figure 3-23 and described in Table 3-25.

Return to Summary Table.

RTC status register:
NOTES: A dummy read of this register is necessary before each I2C read in order to update the status register value.
RESET register domain: POR
MSECURE register protected : No

Figure 3-23. RTC_STATUS_REG Register

7	6	5	4	3	2	1	0
POWER_UP	ALARM	EVENT_1D	EVENT_1H	EVENT_1M	EVENT_1S	RUN	RESERVED
R/W-1h	R/W-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-25. RTC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	POWER_UP	R/W	1h	Indicates that a reset occurred (bit cleared to 0 by writing 1) and that RTC data are not valid anymore. Note: POWER_UP is set by a reset, is cleared by writing one in this bit. Note: The POWER_UP (RTC_STATUS_REG) and RESET_STATUS (RTC_RESET_STATUS_REG) register bits indicate the same information.
6	ALARM	R/W	0h	Indicates that an alarm interrupt has been generated (bit clear by writing 1). Note: The alarm interrupt keeps its low level, until the micro-controller write 1 in the ALARM bit of the RTC_STATUS_REG register. Note: The timer interrupt is a low-level pulse (15us duration).
5	EVENT_1D	R	0h	One day has occurred
4	EVENT_1H	R	0h	One hour has occurred
3	EVENT_1M	R	0h	One minute has occurred
2	EVENT_1S	R	0h	One second has occurred
1	RUN	R	0h	0: RTC is frozen 1: RTC is running Note: This bit shows the real state of the RTC, indeed because of STOP_RTC (RTC_CTRL_REG) signal was resynchronized on 32kHz clock, the action of this bit is delayed.
0	RESERVED	R	0h	

3.2.16 RTC_INTERRUPTS_REG Register (Address = 112h) [reset = 0h]

RTC_INTERRUPTS_REG is shown in Figure 3-24 and described in Table 3-26.

Return to Summary Table.

RTC interrupt control register
RESET register domain: POR
MSECURE register protected : No

Figure 3-24. RTC_INTERRUPTS_REG Register

7	6	5	4	3	2	1	0
RESERVED			IT_SLEEP_MASK_EN	IT_ALARM	IT_TIMER	EVERY	
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 3-26. RTC_INTERRUPTS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved bit
4	IT_SLEEP_MASK_EN	R/W	0h	1: Mask periodic interrupt while the device is in SLEEP mode. Interrupt event is back up in a register and occurred as soon as the device is no more in SLEEP mode. 0: Normal mode, no interrupt masked
3	IT_ALARM	R/W	0h	Enable one interrupt when the alarm value is reached (TC ALARM registers: ALARM_SECONDS_REG, ALARM_MINUTES_REG, ALARM_HOURS_REG, ALARM_DAYS_REG, ALARM_MONTHS_REG, ALARM_YEARS_REG)) by the TC registers
2	IT_TIMER	R/W	0h	Enable periodic interrupt 0: interrupt disabled 1: interrupt enabled
1-0	EVERY	R/W	0h	Interrupt period 00: every second 01: every minute 10: every hour 11: every day

3.2.17 RTC_COMP_LSB_REG Register (Address = 113h) [reset = 0h]

RTC_COMP_LSB_REG is shown in Figure 3-25 and described in Table 3-27.

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RTC compensation register (LSB)
NOTES: This register must be written in 2-complement. This means that to add one 32kHz period every hour, micro-controller needs to write FFFF into RTC_COMP_MSB_REG and RTC_COMP_LSB_REG. To remove one 32kHz period every hour, micro-controller needs to write 0001 into RTC_COMP_MSB_REG and RTC_COMP_LSB_REG.
The 7FFF value is forbidden.
RESET register domain: POR
MSECURE register protected : No

Figure 3-25. RTC_COMP_LSB_REG Register

7	6	5	4	3	2	1	0
RTC_COMP_LSB							
R/W-0h							

Table 3-27. RTC_COMP_LSB_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RTC_COMP_LSB	R/W	0h	This register contains the number of 32kHz periods to be added into the 32kHz counter every hour [LSB]

3.2.18 RTC_COMP_MSB_REG Register (Address = 114h) [reset = 0h]

RTC_COMP_MSB_REG is shown in Figure 3-26 and described in Table 3-28.

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RTC compensation register (MSB)
NOTES: See RTC_COMP_LSB_REG Notes.
RESET register domain: POR
MSECURE register protected : No

Figure 3-26. RTC_COMP_MSB_REG Register

7	6	5	4	3	2	1	0
RTC_COMP_MSB							
R/W-0h							

Table 3-28. RTC_COMP_MSB_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RTC_COMP_MSB	R/W	0h	This register contains the number of 32kHz periods to be added into the 32kHz counter every hour [MSB]

3.2.19 RTC_RES_PROG_REG Register (Address = 115h) [reset = 27h]

RTC_RES_PROG_REG is shown in Figure 3-27 and described in Table 3-29.

Return to Summary Table.

RTC register containing oscillator resistance value
RESET register domain: POR
MSECURE register protected : No

Figure 3-27. RTC_RES_PROG_REG Register

7	6	5	4	3	2	1	0
RESERVED		SW_RES_PROG					
R-0h		R/W-27h					

Table 3-29. RTC_RES_PROG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved bit
5-0	SW_RES_PROG	R/W	27h	Value of the oscillator resistance

3.2.20 RTC_RESET_STATUS_REG Register (Address = 116h) [reset = 0h]

RTC_RESET_STATUS_REG is shown in Figure 3-28 and described in Table 3-30.

Return to Summary Table.

RTC register for reset status
RESET register domain: POR
MSECURE register protected : No

Figure 3-28. RTC_RESET_STATUS_REG Register

7	6	5	4	3	2	1	0
RESERVED							RESET_STATUS
R-0h							R/W-0h

Table 3-30. RTC_RESET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved bit
0	RESET_STATUS	R/W	0h	This bit can only be set to one and is cleared when a manual reset or a POR (case of VBAT below the VBAT min) occur. If this bit is reset it means that the RTC has lost its configuration. Note: The RESET_STATUS (RTC_RESET_STATUS_REG) and POWER_UP (RTC_STATUS_REG) register bits indicate the same information.

3.3 FUNC_BACKUP Registers

Table 3-31 lists the memory-mapped registers for the FUNC_BACKUP. All register offset addresses not listed in Table 3-31 should be considered as reserved locations and the register contents should not be modified.

Table 3-31. FUNC_BACKUP Registers

Address	Acronym	Register Name	Section
118h	BACKUP0	Backup Register 0	Section 3.3.1
119h	BACKUP1	Backup Register 1	Section 3.3.2
11Ah	BACKUP2	Backup Register 2	Section 3.3.3
11Bh	BACKUP3	Backup Register 3	Section 3.3.4
11Ch	BACKUP4	Backup Register 4	Section 3.3.5
11Dh	BACKUP5	Backup Register 5	Section 3.3.6
11Eh	BACKUP6	Backup Register 6	Section 3.3.7
11Fh	BACKUP7	Backup Register 7	Section 3.3.8

3.3.1 BACKUP0 Register (Address = 118h) [reset = 0h]

BACKUP0 is shown in Figure 3-29 and described in Table 3-32.

Return to Summary Table.

Backup register #0 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-29. BACKUP0 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-32. BACKUP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.3.2 BACKUP1 Register (Address = 119h) [reset = 0h]

BACKUP1 is shown in Figure 3-30 and described in Table 3-33.

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Backup register #1 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-30. BACKUP1 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-33. BACKUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.3.3 BACKUP2 Register (Address = 11Ah) [reset = 0h]

BACKUP2 is shown in Figure 3-31 and described in Table 3-34.

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Backup register #2 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-31. BACKUP2 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-34. BACKUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.3.4 BACKUP3 Register (Address = 11Bh) [reset = 0h]

BACKUP3 is shown in Figure 3-32 and described in Table 3-35.

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Backup register #3 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-32. BACKUP3 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-35. BACKUP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.3.5 BACKUP4 Register (Address = 11Ch) [reset = 0h]

BACKUP4 is shown in Figure 3-33 and described in Table 3-36.

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Backup register #4 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-33. BACKUP4 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-36. BACKUP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.3.6 BACKUP5 Register (Address = 11Dh) [reset = 0h]

BACKUP5 is shown in Figure 3-34 and described in Table 3-37.

Return to Summary Table.

Backup register #5 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-34. BACKUP5 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-37. BACKUP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.3.7 BACKUP6 Register (Address = 11Eh) [reset = 0h]

BACKUP6 is shown in Figure 3-35 and described in Table 3-38.

Return to Summary Table.

Backup register #6 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-35. BACKUP6 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-38. BACKUP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.3.8 BACKUP7 Register (Address = 11Fh) [reset = 0h]

BACKUP7 is shown in Figure 3-36 and described in Table 3-39.

Return to Summary Table.

Backup register #7 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-36. BACKUP7 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-39. BACKUP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.4 FUNC_SMPS Registers

Table 3-40 lists the memory-mapped registers for the FUNC_SMPS. All register offset addresses not listed in Table 3-40 should be considered as reserved locations and the register contents should not be modified.

Table 3-40. FUNC_SMPS Registers

Address	Acronym	Register Name	Section
120h	SMPS12_CTRL	SMPS12 Control Register	Section 3.4.1
122h	SMPS12_FORCE	SMPS12 DVS Register	Section 3.4.2
123h	SMPS12_VOLTAGE	SMPS12 DVS Register	Section 3.4.3
124h	SMPS3_CTRL	SMPS3 Control Register	Section 3.4.4
127h	SMPS3_VOLTAGE	SMPS3 Register	Section 3.4.5
128h	SMPS45_CTRL	SMPS45 Control Register	Section 3.4.6
12Ah	SMPS45_FORCE	SMPS45 DVS Register	Section 3.4.7
12Bh	SMPS45_VOLTAGE	SMPS45 DVS Register	Section 3.4.8
12Ch	SMPS6_CTRL	SMPS6 Control Register	Section 3.4.9
12Eh	SMPS6_FORCE	SMPS6 DVS Register	Section 3.4.10
12Fh	SMPS6_VOLTAGE	SMPS6 DVS Register	Section 3.4.11
130h	SMPS7_CTRL	SMPS7 Control Register	Section 3.4.12
133h	SMPS7_VOLTAGE	SMPS7 Register	Section 3.4.13
134h	SMPS8_CTRL	SMPS8 Control Register	Section 3.4.14
136h	SMPS8_FORCE	SMPS8 DVS Register	Section 3.4.15
137h	SMPS8_VOLTAGE	SMPS8 DVS Register	Section 3.4.16
138h	SMPS9_CTRL	SMPS9 Control Register	Section 3.4.17
13Bh	SMPS9_VOLTAGE	SMPS9 Register	Section 3.4.18
144h	SMPS_CTRL	SMPS Control Register	Section 3.4.19
145h	SMPS_PD_CTRL	SMPS Pull-Down Enable Register	Section 3.4.20
147h	SMPS_THERMAL_EN	SMPS Thermal Feature Enable Register	Section 3.4.21
148h	SMPS_THERMAL_STATUS	SMPS Thermal Status Register	Section 3.4.22
149h	SMPS_SHORT_STATUS	SMPS Short Circuit Status	Section 3.4.23
14Ah	SMPS_NEGATIVE_CURRENT_LIMIT_EN	Iload Negative Current Comparator Enable Register (Negative Current Measurement)	Section 3.4.24
14Bh	SMPS_POWERGOOD_MASK1	SMPS Power Good (POWERGOOD) Mask Register 1	Section 3.4.25
14Ch	SMPS_POWERGOOD_MASK2	SMPS Power Good (POWERGOOD) Mask Register 2	Section 3.4.26

3.4.1 SMPS12_CTRL Register (Address = 120h) [reset = 0h]

SMPS12_CTRL is shown in Figure 3-37 and described in Table 3-41.

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SMPS12 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-37. SMPS12_CTRL Register

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R/W-0h	R-0h		R/W-0h		R/W-0h	

Table 3-41. SMPS12_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS12_VOLTAGE.VSEL and SMPS12_FORCE.VSEL register and re-load the default value (reset value) in SMPS12_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	ROOF_FLOOR_EN	R/W	0h	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS12_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1).
5-4	STATUS	R	0h	SMPS12 status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS12 SLEEP Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS12 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.4.2 SMPS12_FORCE Register (Address = 122h) [reset = X]

SMPS12_FORCE is shown in Figure 3-38 and described in Table 3-42.

Return to Summary Table.

SMPS12 DVS register. Voltage to apply to the resourcewhen it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-38. SMPS12_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-42. SMPS12_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS12_FORCE.VSEL voltage is applied When 1: SMPS12_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS12_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register

3.4.3 SMPS12_VOLTAGE Register (Address = 123h) [reset = X]

SMPS12_VOLTAGE is shown in Figure 3-39 and described in Table 3-43.

Return to Summary Table.

SMPS12 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-39. SMPS12_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-43. SMPS12_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS12_VOLTAGE.VSEL and SMPS12_FORCE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.

Table 3-43. SMPS12_VOLTAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	VSEL	R/W	X	VSEL[6:0] cross table voltage (OFF,0.7V to 3.3V) RANGE[0]=0 (x1 multiplier)/ 1(x2 multiplier) 0000000 = SMPS ON/OFF 1000000 = 1.08V/2.16V 0000001 = 0.70V/1.4V 1000001 = 1.09V/2.18V 0000010 = 0.70V/1.4V 1000010 = 1.1V/2.2V 0000011 = 0.70V/1.4V 1000011 = 1.11V/2.22V 0000100 = 0.70V/1.4V 1000100 = 1.12V/2.24V 0000101 = 0.70V/1.4V 1000101 = 1.13V/2.26V 0000110 = 0.70V/1.4V 1000110 = 1.14V/2.28V 0000111 = 0.70V/1.4V 1000111 = 1.15V/2.3V 0001000 = 0.70V/1.4V 1001000 = 1.16V/2.32V 0001001 = 0.70V/1.4V 1001001 = 1.17V/2.34V 0001010 = 0.70V/1.4V 1001010 = 1.18V/2.36V 0001011 = 0.70V/1.4V 1001011 = 1.19V/2.38V 0001100 = 0.70V/1.4V 1001100 = 1.2V/2.4V 0001101 = 0.70V/1.4V 1001101 = 1.21V/2.42V 0001110 = 0.70V/1.4V 1001110 = 1.22V/2.44V 0001111 = 0.70V/1.4V 1001111 = 1.23V/2.46V 0010000 = 0.70V/1.4V 1010000 = 1.24V/2.48V 0010001 = 0.70V/1.4V 1010001 = 1.25V/2.5V 0010010 = 0.70V/1.4V 1010010 = 1.26V/2.52V 0010011 = 0.70V/1.4V 1010011 = 1.27V/2.54V 0010100 = 0.70V/1.4V 1010100 = 1.28V/2.56V 0010101 = 0.70V/1.4V 1010101 = 1.29V/2.58V 0010110 = 0.70V/1.4V 1010110 = 1.3V/2.6V 0010111 = 0.70V/1.4V 1010111 = 1.31V/2.62V 0011000 = 0.70V/1.4V 1011000 = 1.32V/2.64V 0011001 = 0.70V/1.4V 1011001 = 1.33V/2.66V 0011010 = 0.70V/1.4V 1011010 = 1.34V/2.68V 0011011 = 0.71V/1.42V 1011011 = 1.35V/2.7V 0011100 = 0.72V/1.44V 1011100 = 1.36V/2.72V 0011101 = 0.73V/1.46V 1011101 = 1.37V/2.74V 0011110 = 0.74V/1.48V 1011110 = 1.38V/2.76V 0011111 = 0.75V/1.50V 1011111 = 1.39V/2.78V 0100000 = 0.76V/1.52V 1100000 = 1.4V/2.8V 0100001 = 0.77V/1.54V 1100001 = 1.41V/2.82V 0100010 = 0.78V/1.56V 1100010 = 1.42V/2.84V 0100011 = 0.79V/1.58V 1100011 = 1.43V/2.86V 0100100 = 0.8V/1.6V 1100100 = 1.44V/2.88V 0100101 = 0.81V/1.62V 1100101 = 1.45V/2.9V 0100110 = 0.82V/1.64V 1100110 = 1.46V/2.92V 0100111 = 0.83V/1.66V 1100111 = 1.47V/2.94V 0101000 = 0.84V/1.68V 1101000 = 1.48V/2.96V 0101001 = 0.85V/1.7V 1101001 = 1.49V/2.98V 0101010 = 0.86V/1.72V 1101010 = 1.5V/3V 0101011 = 0.87V/1.74V 1101011 = 1.51V/3.02V 0101100 = 0.88V/1.76V 1101100 = 1.52V/3.04V 0101101 = 0.89V/1.78V 1101101 = 1.53V/3.06V 0101110 = 0.9V/1.8V 1101110 = 1.54V/3.08V

Table 3-43. SMPS12_VOLTAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101111 = 0.91V/1.82V 1101111 = 1.55V/3.1V
				0110000 = 0.92V/1.84V 1110000 = 1.56V/3.12V
				0110001 = 0.93V/1.86V 1110001 = 1.57V/3.14V
				0110010 = 0.94V/1.88V 1110010 = 1.58V/3.16V
				0110011 = 0.95V/1.90V 1110011 = 1.59V/3.18V
				0110100 = 0.96V/1.92V 1110100 = 1.6V/3.2V
				0110101 = 0.97V/1.94V 1110101 = 1.61V/3.22V
				0110110 = 0.98V/1.96V 1110110 = 1.62V/3.24V
				0110111 = 0.99V/1.98V 1110111 = 1.63V/3.26V
				0111000 = 1.00V/2V 1111000 = 1.64V/3.28V
				0111001 = 1.01V/2.02V 1111001 = 1.65V/3.3V
				0111010 = 1.02V/2.04V 1111010 = 1.65V/3.3V
				0111011 = 1.03V/2.06V 1111011 = 1.65V/3.3V
				0111100 = 1.04V/2.08V 1111100 = 1.65V/3.3V
				0111101 = 1.05V/2.1V 1111101 = 1.65V/3.3V
				0111110 = 1.06V/2.12V 1111110 = 1.65V/3.3V
				0111111 = 1.07V/2.14V 1111111 = 1.65V/3.3V

3.4.4 SMPS3_CTRL Register (Address = 124h) [reset = 0h]

SMPS3_CTRL is shown in Figure 3-40 and described in Table 3-44.

Return to Summary Table.

SMPS3 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-40. SMPS3_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R-0h	R-0h		R/W-0h		R/W-0h	

Table 3-44. SMPS3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP in SMPS3_VOLTAGE.VSEL register during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	RESERVED	R	0h	
5-4	STATUS	R	0h	SMPS3 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS3 SLEEP mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS3 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.4.5 SMPS3_VOLTAGE Register (Address = 127h) [reset = X]

SMPS3_VOLTAGE is shown in Figure 3-41 and described in Table 3-45.

Return to Summary Table.

SMPS3 register. Voltage to apply to the resource.
RESET register domain: SWORST

Figure 3-41. SMPS3_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-45. SMPS3_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS3_VOLTAGE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.6 SMPS45_CTRL Register (Address = 128h) [reset = 0h]

SMPS45_CTRL is shown in Figure 3-42 and described in Table 3-46.

Return to Summary Table.

SMPS45 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-42. SMPS45_CTRL Register

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R/W-0h	R-0h		R/W-0h		R/W-0h	

Table 3-46. SMPS45_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS45_VOLTAGE.VSEL and SMPS45_FORCE.VSEL register and re-load the default value (reset value) in SMPS45_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	ROOF_FLOOR_EN	R/W	0h	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS45_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1).
5-4	STATUS	R	0h	SMPS45 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS45 SLEEP mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS45 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.4.7 SMPS45_FORCE Register (Address = 12Ah) [reset = X]

SMPS45_FORCE is shown in Figure 3-43 and described in Table 3-47.

Return to Summary Table.

SMPS45 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-43. SMPS45_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-47. SMPS45_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS45_FORCE.VSEL voltage is applied When 1: SMPS45_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS45_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.8 SMPS45_VOLTAGE Register (Address = 12Bh) [reset = X]

SMPS45_VOLTAGE is shown in Figure 3-44 and described in Table 3-48.

Return to Summary Table.

SMPS45 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-44. SMPS45_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-48. SMPS45_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS45_VOLTAGE.VSEL and SMPS45_FORCE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.9 SMPS6_CTRL Register (Address = 12Ch) [reset = 0h]

SMPS6_CTRL is shown in Figure 3-45 and described in Table 3-49.

Return to Summary Table.

SMPS6 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-45. SMPS6_CTRL Register

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R/W-0h	R-0h		R/W-0h		R/W-0h	

Table 3-49. SMPS6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS6_VOLTAGE.VSEL and SMPS6_FORCE.VSEL register and re-load the default value (reset value) in SMPS6_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	ROOF_FLOOR_EN	R/W	0h	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS6_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1).
5-4	STATUS	R	0h	SMPS6 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS6 SLEEP mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS6 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.4.10 SMPS6_FORCE Register (Address = 12Eh) [reset = X]

SMPS6_FORCE is shown in Figure 3-46 and described in Table 3-50.

Return to Summary Table.

SMPS6 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-46. SMPS6_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-50. SMPS6_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS6_FORCE.VSEL voltage is applied When 1: SMPS6_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS6_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.11 SMPS6_VOLTAGE Register (Address = 12Fh) [reset = X]

SMPS6_VOLTAGE is shown in Figure 3-47 and described in Table 3-51.

Return to Summary Table.

SMPS6 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-47. SMPS6_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-51. SMPS6_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS6_VOLTAGE.VSEL and SMPS6_FORCE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.12 SMPS7_CTRL Register (Address = 130h) [reset = 0h]

SMPS7_CTRL is shown in Figure 3-48 and described in Table 3-52.

Return to Summary Table.

SMPS7 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-48. SMPS7_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R-0h	R-0h		R/W-0h		R/W-0h	

Table 3-52. SMPS7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS7_VOLTAGE.VSEL register during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	RESERVED	R	0h	
5-4	STATUS	R	0h	SMPS7 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS7 SLEEP mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS7 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.4.13 SMPS7_VOLTAGE Register (Address = 133h) [reset = X]

SMPS7_VOLTAGE is shown in Figure 3-49 and described in Table 3-53.

Return to Summary Table.

SMPS7 register. Voltage to apply to the resource.
RESET register domain: SWORST

Figure 3-49. SMPS7_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-53. SMPS7_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS7_VOLTAGE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled. Note: For Dual-phase and triple-phase modes, RANGE=1 (1V to 3.3V) is not supported.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.14 SMPS8_CTRL Register (Address = 134h) [reset = 0h]

SMPS8_CTRL is shown in Figure 3-50 and described in Table 3-54.

Return to Summary Table.

SMPS8 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-50. SMPS8_CTRL Register

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R/W-0h	R-0h		R/W-0h		R/W-0h	

Table 3-54. SMPS8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS8_VOLTAGE.VSEL and SMPS8_FORCE.VSEL register and re-load the default value (reset value) in SMPS8_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	ROOF_FLOOR_EN	R/W	0h	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS8_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1).
5-4	STATUS	R	0h	SMPS8 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS8 SLEEP mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS8 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.4.15 SMPS8_FORCE Register (Address = 136h) [reset = X]

SMPS8_FORCE is shown in Figure 3-51 and described in Table 3-55.

Return to Summary Table.

SMPS8 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-51. SMPS8_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-55. SMPS8_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS8_FORCE.VSEL voltage is applied When 1: SMPS8_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS8_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.16 SMPS8_VOLTAGE Register (Address = 137h) [reset = X]

SMPS8_VOLTAGE is shown in Figure 3-52 and described in Table 3-56.

Return to Summary Table.

SMPS8 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-52. SMPS8_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-56. SMPS8_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS8_VOLTAGE.VSEL and SMPS8_FORCE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.17 SMPS9_CTRL Register (Address = 138h) [reset = 0h]

SMPS9_CTRL is shown in Figure 3-53 and described in Table 3-57.

Return to Summary Table.

SMPS9 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-53. SMPS9_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R-0h	R-0h		R/W-0h		R/W-0h	

Table 3-57. SMPS9_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS9_VOLTAGE.VSEL register during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	RESERVED	R	0h	
5-4	STATUS	R	0h	SMPS9 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS9 SLEEP Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS9 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.4.18 SMPS9_VOLTAGE Register (Address = 13Bh) [reset = X]

SMPS9_VOLTAGE is shown in Figure 3-54 and described in Table 3-58.

Return to Summary Table.

SMPS9 register. Voltage to apply to the resource.
RESET register domain: SWORST

Figure 3-54. SMPS9_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-58. SMPS9_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS9_VOLTAGE.VSEL 0: 0.7V to 1.65V 1: 1.0 to 3.3V Note: RANGE must not be changed on the fly when the SMPS is Active. To change the operation voltage range, SMPS has to be disabled.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register.

3.4.19 SMPS_CTRL Register (Address = 144h) [reset = X]

SMPS_CTRL is shown in Figure 3-55 and described in Table 3-59.

Return to Summary Table.

SMPS control register.
RESET register domain: HWRST

Figure 3-55. SMPS_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		SMPS45_SMPS457_EN	SMPS12_SMPS123_EN	SMPS45_PHASE_CTRL		SMPS123_PHASE_CTRL	
R-0h		R-X	R-X	R/W-0h		R/W-0h	

Table 3-59. SMPS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	SMPS45_SMPS457_EN	R	X	Selection of the type of configuration of the SMPS457 0: SMPS45 dual phase, SMPS7 single phase 1: SMPS457 triple phase (Reserved)
4	SMPS12_SMPS123_EN	R	X	Selection of the type of configuration of the SMPS123 0: SMPS12 dual phase, SMPS3 single phase 1: SMPS123 triple phase
3-2	SMPS45_PHASE_CTRL	R/W	0h	Selection of the phase mode of the SMPS45 00: Automatic Phase Selection - Multi Phase or Single Phase (default) 11: Automatic Phase Selection - Multi Phase or Single Phase 01: Force Single Phase mode 10: Force Multi Phase phase mode - Prohibited under no-load condition
1-0	SMPS123_PHASE_CTRL	R/W	0h	Selection of the phase mode of the SMPS123 (SMPS12 Dual Phase + SMPS3 Single Phase configuration or SMPS123 Triple Phase configuration) 00: Automatic Phase Selection per SMPS - Multi Phase or Single Phase (default) 11: Automatic Phase Selection per SMPS - Multi Phase or Single Phase 01: Force Single Phase mode (for SMPS12 and SMPS3) 10: Force Multi Phase mode (for SMPS12 and SMPS3) - Prohibited under no-load condition

3.4.20 SMPS_PD_CTRL Register (Address = 145h) [reset = 7Fh]

SMPS_PD_CTRL is shown in Figure 3-56 and described in Table 3-60.

Return to Summary Table.

SMPS Pull-Down enable register.
RESET register domain: HWRST
Notes:
SMPS pull-down register bits validate the control of the active discharge of each power resource to full-fill the turn-off timing requirements.
When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restart correctly at the next power-up sequence.

Figure 3-56. SMPS_PD_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 3-60. SMPS_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SMPS9	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS9 is in OFF state (default)
5	SMPS8	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS8 is in OFF state (default)
4	SMPS7	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS7 is in OFF state (default)
3	SMPS6	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS6 is in OFF state (default)
2	SMPS45	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS45 is in OFF state (default)
1	SMPS3	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS3 is in OFF state (default)
0	SMPS12	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS12 is in OFF state (default)

3.4.21 SMPS_THERMAL_EN Register (Address = 147h) [reset = FFh]

SMPS_THERMAL_EN is shown in Figure 3-57 and described in Table 3-61.

Return to Summary Table.

SMPS Thermal feature enable register.
RESET register domain: HWRST

Figure 3-57. SMPS_THERMAL_EN Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	SMPS6	SMPS457	RESERVED	SMPS123
R-1h	R-1h	R-1h	R-1h	R/W-1h	R/W-1h	R-1h	R/W-1h

Table 3-61. SMPS_THERMAL_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	1h	
6	RESERVED	R	1h	
5	RESERVED	R	1h	
4	RESERVED	R	1h	
3	SMPS6	R/W	1h	0: SMPS6 Thermal feature is not enabled 1: SMPS6 Thermal feature is enabled (default)
2	SMPS457	R/W	1h	0: SMPS457 Thermal feature is not enabled 1: SMPS457 Thermal feature is enabled (default)
1	RESERVED	R	1h	
0	SMPS123	R/W	1h	0: SMPS123 Thermal feature is not enabled 1: SMPS123 Thermal feature is enabled (default) Note: A unique Thermal Sensor is protecting SMPS12 and SMPS3

3.4.22 SMPS_THERMAL_STATUS Register (Address = 148h) [reset = 0h]

SMPS_THERMAL_STATUS is shown in Figure 3-58 and described in Table 3-62.

Return to Summary Table.

SMPS Thermal status register.
RESET register domain: POR

Figure 3-58. SMPS_THERMAL_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	SMPS6	SMPS457	RESERVED	SMPS123
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-62. SMPS_THERMAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	SMPS6	R	0h	0: SMPS6 Thermal measurement is below the limit (SMPS is functional) 1: SMPS6 Thermal measurement is over the limit (see specification)
2	SMPS457	R	0h	0: SMPS457 Thermal measurement is below the limit (SMPS is functional) 1: SMPS457 Thermal measurement is over the limit (see specification)
1	RESERVED	R	0h	
0	SMPS123	R	0h	0: SMPS123 Thermal measurement is below the limit (SMPS is functional) 1: SMPS123 Thermal measurement is over the limit (see specification)

3.4.23 SMPS_SHORT_STATUS Register (Address = 149h) [reset = 0h]

SMPS_SHORT_STATUS is shown in Figure 3-59 and described in Table 3-63.

Return to Summary Table.

SMPS Short circuit status.
RESET register domain: POR

Figure 3-59. SMPS_SHORT_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-63. SMPS_SHORT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SMPS9	R	0h	0: SMPS9 is functional . No short detected (default) 1: SMPS9 output is shorted
5	SMPS8	R	0h	0: SMPS8 is functional . No short detected (default) 1: SMPS8 output is shorted
4	SMPS7	R	0h	0: SMPS7 is functional . No short detected (default) 1: SMPS7 output is shorted Note: This bit is un-relevant when SMPS123 is in Triple phase mode
3	SMPS6	R	0h	0: SMPS6 is functional . No short detected (default) 1: SMPS6 output is shorted
2	SMPS45	R	0h	0: SMPS45 (or SMPS457 in Triple phase mode) is functional . No short detected (default) 1: SMPS45 (or SMPS457 in Triple phase mode) output is shorted
1	SMPS3	R	0h	0: SMPS3 is functional . No short detected (default) 1: SMPS3 output is shorted Note: This bit is un-relevant when SMPS123 is in Triple phase mode
0	SMPS12	R	0h	0: SMPS12 (or SMPS123 in Triple phase mode) is functional . No short detected (default) 1: SMPS12 (or SMPS123 in Triple phase mode) output is shorted

3.4.24 SMPS_NEGATIVE_CURRENT_LIMIT_EN Register (Address = 14Ah) [reset = FFh]

SMPS_NEGATIVE_CURRENT_LIMIT_EN is shown in Figure 3-60 and described in Table 3-64.

Return to Summary Table.

Iload Negative Current Comparator enable register (Negative Current measurement).
RESET register domain: HWRST

Figure 3-60. SMPS_NEGATIVE_CURRENT_LIMIT_EN Register

7	6	5	4	3	2	1	0
RESERVED	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12
R-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 3-64. SMPS_NEGATIVE_CURRENT_LIMIT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	1h	
6	SMPS9	R/W	1h	0: SMPS9 Negative Current comparator for measurement is not enabled 1: SMPS9 Negative Current comparator for measurement is enabled (default)
5	SMPS8	R/W	1h	0: SMPS8 Negative Current comparator for measurement is not enabled 1: SMPS8 Negative Current comparator for measurement is enabled (default)
4	SMPS7	R/W	1h	0: SMPS7 Negative Current comparator for measurement is not enabled 1: SMPS7 Negative Current comparator for measurement is enabled (default)
3	SMPS6	R/W	1h	0: SMPS6 Negative Current comparator for measurement is not enabled 1: SMPS6 Negative Current comparator for measurement is enabled (default)
2	SMPS45	R/W	1h	0: SMPS45 Negative Current comparator for measurement is not enabled 1: SMPS45 Negative Current comparator for measurement is enabled (default)
1	SMPS3	R/W	1h	0: SMPS3 Negative Current comparator for measurement is not enabled 1: SMPS3 Negative Current comparator for measurement is enabled (default)
0	SMPS12	R/W	1h	0: SMPS12 Negative Current comparator for measurement is not enabled 1: SMPS12 Negative Current comparator for measurement is enabled (default)

3.4.25 SMPS_POWERGOOD_MASK1 Register (Address = 14Bh) [reset = FEh]

SMPS_POWERGOOD_MASK1 is shown in Figure 3-61 and described in Table 3-65.

Return to Summary Table.

SMPS Power Good (POWERGOOD) mask #1
RESET register domain: POR

Figure 3-61. SMPS_POWERGOOD_MASK1 Register

7	6	5	4	3	2	1	0
RESERVED	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12
R-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h

Table 3-65. SMPS_POWERGOOD_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	1h	
6	SMPS9	R/W	1h	SMPS9 POWERGOOD Mask bit register 0: SMPS9 line is enabled. The SMPS9 state is generated on POWERGOOD line 1: SMPS9 line is masked. No SMPS9 state is generated on POWERGOOD line (default)
5	SMPS8	R/W	1h	SMPS8 POWERGOOD Mask bit register 0: SMPS8 line is enabled. The SMPS8 state is generated on POWERGOOD line 1: SMPS8 line is masked. No SMPS8 state is generated on POWERGOOD line (default)
4	SMPS7	R/W	1h	SMPS7 POWERGOOD Mask bit register 0: SMPS7 line is enabled. The SMPS7 state is generated on POWERGOOD line 1: SMPS7 line is masked. No SMPS7 state is generated on POWERGOOD line (default)
3	SMPS6	R/W	1h	SMPS6 POWERGOOD Mask bit register 0: SMPS6 line is enabled. The SMPS6 state is generated on POWERGOOD line 1: SMPS6 line is masked. No SMPS6 state is generated on POWERGOOD line (default)
2	SMPS45	R/W	1h	SMPS45 POWERGOOD Mask bit register 0: SMPS45 line is enabled. The SMPS45 state is generated on POWERGOOD line 1: SMPS45 line is masked. No SMPS45 state is generated on POWERGOOD line (default)
1	SMPS3	R/W	1h	SMPS3 POWERGOOD Mask bit register 0: SMPS3 line is enabled. The SMPS3 state is generated on POWERGOOD line 1: SMPS3 line is masked. No SMPS3 state is generated on POWERGOOD line (default)
0	SMPS12	R/W	0h	SMPS12 POWERGOOD Mask bit register 0: SMPS12 line is enabled. The SMPS12 state is generated on POWERGOOD line (default) 1: SMPS12 line is masked. No SMPS12 state is generated on POWERGOOD line

3.4.26 SMPS_POWERGOOD_MASK2 Register (Address = 14Ch) [reset = 7h]

SMPS_POWERGOOD_MASK2 is shown in Figure 3-62 and described in Table 3-66.

Return to Summary Table.

SMPS Power Good (POWERGOOD) mask #2
RESET register domain: POR (excepted POWERGOOD_TYPE_SELECT which is under HWRST)

Figure 3-62. SMPS_POWERGOOD_MASK2 Register

7	6	5	4	3	2	1	0
POWERGOOD_TYPE_SELECT	RESERVED				GPIO_7	RESERVED	RESERVED
R/W-0h	R-0h				R/W-1h	R/W-1h	R/W-1h

Table 3-66. SMPS_POWERGOOD_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	POWERGOOD_TYPE_SELECT	R/W	0h	Selection of the POWERGOOD type of monitoring 0: Voltage monitoring (above threshold)) AND Current monitoring (over current) (default) 1: Current monitoring only (over current)
6-3	RESERVED	R	0h	
2	GPIO_7	R/W	1h	GPIO_7 POWERGOOD Mask bit register 0: GPIO_7 line is enabled. The GPIO_7 state is generated on POWERGOOD line 1: GPIO_7 line is masked. No GPIO_7 state is generated on POWERGOOD line (default)
1	RESERVED	R/W	1h	
0	RESERVED	R/W	1h	

3.5 FUNC_LDO Registers

Table 3-67 lists the memory-mapped registers for the FUNC_LDO. All register offset addresses not listed in Table 3-67 should be considered as reserved locations and the register contents should not be modified.

Table 3-67. FUNC_LDO Registers

Address	Acronym	Register Name	Section
150h	LDO1_CTRL	LDO1 Control Register	Section 3.5.1
151h	LDO1_VOLTAGE	LDO1 Voltage Selection Register (OTP_Config)	Section 3.5.2
152h	LDO2_CTRL	LDO2 Control Register	Section 3.5.3
153h	LDO2_VOLTAGE	LDO2 Voltage Selection Register (OTP_Config)	Section 3.5.4
154h	LDO3_CTRL	LDO3 Control Register	Section 3.5.5
155h	LDO3_VOLTAGE	LDO3 Voltage Selection Register (OTP_Config)	Section 3.5.6
156h	LDO4_CTRL	LDO4 Control Register	Section 3.5.7
157h	LDO4_VOLTAGE	LDO4 Voltage Selection (OTP_Config)	Section 3.5.8
160h	LDO9_CTRL	LDO9 Control Register	Section 3.5.9
161h	LDO9_VOLTAGE	LDO9 Voltage Selection Register (OTP_Config)	Section 3.5.10
162h	LDOLN_CTRL	LDOLN Control Register	Section 3.5.11
163h	LDOLN_VOLTAGE	LDOLN Voltage Selection Register (OTP_Config)	Section 3.5.12
164h	LDOUSB_CTRL	LDOUSB Control Register	Section 3.5.13
165h	LDOUSB_VOLTAGE	LDOUSB Voltage Selection Register (OTP_Config)	Section 3.5.14
16Ah	LDO_CTRL	LDO Control Register	Section 3.5.15
16Bh	LDO_PD_CTRL1	LDO Pull-Down Enable Register 1	Section 3.5.16
16Ch	LDO_PD_CTRL2	LDO Pull-Down Enable Register 2	Section 3.5.17
16Dh	LDO_SHORT_STATUS1	LDO Short Circuit Status Register 1	Section 3.5.18
16Eh	LDO_SHORT_STATUS2	LDO Short Circuit Status Register 2	Section 3.5.19

3.5.1 LDO1_CTRL Register (Address = 150h) [reset = 0h]

LDO1_CTRL is shown in Figure 3-63 and described in Table 3-68.

Return to Summary Table.

LDO1 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-63. LDO1_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED		STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R-0h		R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-68. LDO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO1_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6-5	RESERVED	R	0h	
4	STATUS	R	0h	LDO1 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO1 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO1 ACTIVE Mode 0: OFF 1: ON This bit can be updated by power-up sequencer

3.5.2 LDO1_VOLTAGE Register (Address = 151h) [reset = X]

LDO1_VOLTAGE is shown in Figure 3-64 and described in Table 3-69.

Return to Summary Table.

LDO1 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-64. LDO1_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-69. LDO1_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	VSEL[5:0] cross table voltage (OFF,0.9V to 3.3V) 000000 0V 100000 2,45V 000001 0,9V 100001 2,5V 000010 0,95V 100010 2,55V 000011 1V 100011 2,6V 000100 1,05V 100100 2,65V 000101 1,1V 100101 2,7V 000110 1,15V 100110 2,75V 000111 1,2V 100111 2,8V 001000 1,25V 101000 2,85V 001001 1,3V 101001 2,9V 001010 1,35V 101010 2,95V 001011 1,4V 101011 3V 001100 1,45V 101100 3,05V 001101 1,5V 101101 3,1V 001110 1,55V 101110 3,15V 001111 1,6V 101111 3,2V 010000 1,65V 110000 3,25V 010001 1,7V 110001 3,3V 010010 1,75V 110010 3,3V 010011 1,8V 110011 3,3V 010100 1,85V 110100 3,3V 010101 1,9V 110101 3,3V 010110 1,95V 110110 3,3V 010111 2V 110111 3,3V 011000 2,05V 111000 3,3V 011001 2,1V 111001 3,3V 011010 2,15V 111010 3,3V 011011 2,2V 111011 3,3V 011100 2,25V 111100 3,3V 011101 2,3V 111101 3,3V 011110 2,35V 111110 3,3V 011111 2,4V 111111 3,3V

3.5.3 LDO2_CTRL Register (Address = 152h) [reset = 0h]

LDO2_CTRL is shown in Figure 3-65 and described in Table 3-70.

Return to Summary Table.

LDO2 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1, signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-65. LDO2_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED		STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R-0h		R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-70. LDO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO2_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6-5	RESERVED	R	0h	
4	STATUS	R	0h	LDO2 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO2 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO2 ACTIVE Mode 0: OFF 1: ON

3.5.4 LDO2_VOLTAGE Register (Address = 153h) [reset = X]

LDO2_VOLTAGE is shown in Figure 3-66 and described in Table 3-71.

Return to Summary Table.

LDO2 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-66. LDO2_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-71. LDO2_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.5.5 LDO3_CTRL Register (Address = 154h) [reset = 0h]

LDO3_CTRL is shown in Figure 3-67 and described in Table 3-72.

Return to Summary Table.

LDO3 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
MODE_SLEEP is used when NSLEEP/ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP/ENABLE1 signals select the resource.

Figure 3-67. LDO3_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED		STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R-0h		R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-72. LDO3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO3_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6-5	RESERVED	R	0h	
4	STATUS	R	0h	LDO3 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO3 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO3 ACTIVE Mode 0: OFF 1: ON

3.5.6 LDO3_VOLTAGE Register (Address = 155h) [reset = X]

LDO3_VOLTAGE is shown in Figure 3-68 and described in Table 3-73.

Return to Summary Table.

LDO3 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-68. LDO3_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-73. LDO3_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.5.7 LDO4_CTRL Register (Address = 156h) [reset = 0h]

LDO4_CTRL is shown in Figure 3-69 and described in Table 3-74.

Return to Summary Table.

LDO4 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
MODE_SLEEP is used when NSLEEP/ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP/ENABLE1 signals select the resource.

Figure 3-69. LDO4_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED		STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R-0h		R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-74. LDO4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO4_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6-5	RESERVED	R	0h	
4	STATUS	R	0h	LDO4 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO4 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO4 ACTIVE Mode 0: OFF 1: ON

3.5.8 LDO4_VOLTAGE Register (Address = 157h) [reset = X]

LDO4_VOLTAGE is shown in Figure 3-70 and described in Table 3-75.

Return to Summary Table.

LDO4 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-70. LDO4_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-75. LDO4_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.5.9 LDO9_CTRL Register (Address = 160h) [reset = 0h]

LDO9_CTRL is shown in Figure 3-71 and described in Table 3-76.

Return to Summary Table.

LDO9 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-71. LDO9_CTRL Register

7	6	5	4	3	2	1	0
WR_S	LDO_BYPASS_EN	RESERVED	STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-76. LDO9_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO9_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6	LDO_BYPASS_EN	R/W	0h	LDO bypass enable 0: no bypass enabled (default) 1: bypass enabled
5	RESERVED	R	0h	
4	STATUS	R	0h	LDO9 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO9 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO9 ACTIVE Mode 0: OFF 1: ON

3.5.10 LDO9_VOLTAGE Register (Address = 161h) [reset = X]

LDO9_VOLTAGE is shown in Figure 3-72 and described in Table 3-77.

Return to Summary Table.

LDO9 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-72. LDO9_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-77. LDO9_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.5.11 LDOLN_CTRL Register (Address = 162h) [reset = 0h]

LDOLN_CTRL is shown in Figure 3-73 and described in Table 3-78.

Return to Summary Table.

LDOLN control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-73. LDOLN_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED		STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R-0h		R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-78. LDOLN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDOLN_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6-5	RESERVED	R	0h	
4	STATUS	R	0h	LDOLN Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDOLN SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDOLN ACTIVE Mode 0: OFF 1: ON

3.5.12 LDOLN_VOLTAGE Register (Address = 163h) [reset = X]

LDOLN_VOLTAGE is shown in Figure 3-74 and described in Table 3-79.

Return to Summary Table.

LDOLN Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-74. LDOLN_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-79. LDOLN_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.5.13 LDOUSB_CTRL Register (Address = 164h) [reset = 0h]

LDOUSB_CTRL is shown in Figure 3-75 and described in Table 3-80.

Return to Summary Table.

LDOUSB control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP or ENABLE1 signals select the resource. MODE_ACTIVE is used when none of NSLEEP or ENABLE1 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-75. LDOUSB_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED		STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R-0h		R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-80. LDOUSB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDOUSB_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6-5	RESERVED	R	0h	
4	STATUS	R	0h	LDOUSB Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDOUSB SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDOUSB ACTIVE Mode 0: OFF 1: ON

3.5.14 LDOUSB_VOLTAGE Register (Address = 165h) [reset = X]

LDOUSB_VOLTAGE is shown in Figure 3-76 and described in Table 3-81.

Return to Summary Table.

LDOUSB Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-76. LDOUSB_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-81. LDOUSB_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.5.15 LDO_CTRL Register (Address = 16Ah) [reset = X]

LDO_CTRL is shown in Figure 3-77 and described in Table 3-82.

Return to Summary Table.

LDO Control register
RESET register domain: SWORST

Figure 3-77. LDO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							LDOUSB_ON_VBUS_VSYS
R-0h							R/W-X

Table 3-82. LDO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	LDOUSB_ON_VBUS_VSYS	R/W	X	LDOUSB inputs controls. Controlled by internal switch. 0: LDOUSB_IN2 connected is connected to the LDO - Case VBUS 1: LDOUSB_IN1 connected is connected to the LDO - Case VSYS

3.5.16 LDO_PD_CTRL1 Register (Address = 16Bh) [reset = FFh]

LDO_PD_CTRL1 is shown in Figure 3-78 and described in Table 3-83.

Return to Summary Table.

LDO Pull-Down enable register #1
RESET register domain: HWRST
NOTES:
LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements.
When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.

Figure 3-78. LDO_PD_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	LDO4	LDO3	LDO2	LDO1
				R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 3-83. LDO_PD_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1h	Reserved
6	RESERVED	R/W	1h	Reserved
5	RESERVED	R/W	1h	Reserved
4	RESERVED	R/W	1h	Reserved
3	LDO4	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDO4 is in OFF state
2	LDO3	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDO3 is in OFF state
1	LDO2	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDO2 is in OFF state
0	LDO1	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDO1 is in OFF state

3.5.17 LDO_PD_CTRL2 Register (Address = 16Ch) [reset = Fh]

LDO_PD_CTRL2 is shown in Figure 3-79 and described in Table 3-84.

Return to Summary Table.

LDO Pull-Down enable register #2
RESET register domain: HWRST
NOTES:
LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements.
When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.

Figure 3-79. LDO_PD_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED				LDOVANA	LDOUSB	LDOLN	LDO9
R-0h				R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 3-84. LDO_PD_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	LDOVANA	R/W	1h	LDOVANA (internal LDO - reserved) 0: Pull-Down is disable 1: Pull-Down is enabled when LDOVANA is in OFF state
2	LDOUSB	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDOUSB is in OFF state
1	LDOLN	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDOLN is in OFF state
0	LDO9	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDO9 is in OFF state

3.5.18 LDO_SHORT_STATUS1 Register (Address = 16Dh) [reset = 0h]

LDO_SHORT_STATUS1 is shown in Figure 3-80 and described in Table 3-85.

Return to Summary Table.

LDO Short circuit status register #1
At Power-On, LDO short input informations are masked during 1 ms. This 1 ms masking is activated and re-started each time one LDO is enabled.
RESET register domain: POR

Figure 3-80. LDO_SHORT_STATUS1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	LDO4	LDO3	LDO2	LDO1
				R-0h	R-0h	R-0h	R-0h

Table 3-85. LDO_SHORT_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	LDO4	R	0h	0: LDO4 is functional. No short detected (default) 1: LDO4 output is short detected
2	LDO3	R	0h	0: LDO3 is functional. No short detected (default) 1: LDO3 output is short detected
1	LDO2	R	0h	0: LDO2 is functional. No short detected (default) 1: LDO2 output is short detected
0	LDO1	R	0h	0: LDO1 is functional. No short detected (default) 1: LDO1 output is short detected

3.5.19 LDO_SHORT_STATUS2 Register (Address = 16Eh) [reset = 0h]

LDO_SHORT_STATUS2 is shown in Figure 3-81 and described in Table 3-86.

Return to Summary Table.

LDO short circuit status register #2
RESET register domain: POR

Figure 3-81. LDO_SHORT_STATUS2 Register

7	6	5	4	3	2	1	0
RESERVED				LDOVANA	LDOUSB	LDOLN	LDO9
R-0h				R-0h	R-0h	R-0h	R-0h

Table 3-86. LDO_SHORT_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	LDOVANA	R	0h	LDOVANA (internal LDO - reserved) 0: LDOVANA is functional. No short detected (default) 1: LDOVANA output is short detected
2	LDOUSB	R	0h	0: LDOUSB is functional. No short detected (default) 1: LDOUSB output is short detected
1	LDOLN	R	0h	0: LDOLN is functional. No short detected (default) 1: LDOLN output is short detected
0	LDO9	R	0h	0: LDO9 is functional. No short detected (default) 1: LDO9 output is short detected

3.6 FUNC_SPI Registers

Table 3-87 lists the memory-mapped registers for the FUNC_SPI. All register offset addresses not listed in Table 3-87 should be considered as reserved locations and the register contents should not be modified.

Table 3-87. FUNC_SPI Registers

Address	Acronym	Register Name	Section
17Fh	SPI_PAGE_CTRL	SPI Page Control Register	Section 3.6.1

3.6.1 SPI_PAGE_CTRL Register (Address = 17Fh) [reset = 0h]

SPI_PAGE_CTRL is shown in Figure 3-82 and described in Table 3-88.

Return to Summary Table.

SPI Page Control register (used only when SPI interface is used).
RESET register domain: SWORST
MSECURE register protected : Yes

Figure 3-82. SPI_PAGE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							SPI_PAGE_ACCESS
R-0h							R/W-0h

Table 3-88. SPI_PAGE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	SPI_PAGE_ACCESS	R/W	0h	Page selection for SPI interface only 0: page1 (ID1=48) and page2 (ID2=49) 1: page1 (ID1=48) and page3 (ID2=4A)

3.7 FUNC_PMU_CONTROL Registers

Table 3-89 lists the memory-mapped registers for the FUNC_PMU_CONTROL. All register offset addresses not listed in Table 3-89 should be considered as reserved locations and the register contents should not be modified.

Table 3-89. FUNC_PMU_CONTROL Registers

Address	Acronym	Register Name	Section
1A0h	DEV_CTRL	Device Control Register	Section 3.7.1
1A1h	POWER_CTRL	Power Control Register	Section 3.7.2
1A2h	VSYS_LO	VSYS Low Threshold Register	Section 3.7.3
1A3h	VSYS_MON	VSYS Monitoring Register	Section 3.7.4
1A5h	WATCHDOG	Watch Dog Timer Register	Section 3.7.5
1A6h	BOOT_STATUS	BOOT Status Register	Section 3.7.6
1A8h	VRTC_CTRL	VRTC Control Register	Section 3.7.7
1A9h	LONG_PRESS_KEY	Long Press Key (LPK) Configuration Register	Section 3.7.8
1AAh	OSC_THERM_CTRL	Oscillator and Thermal Control Register	Section 3.7.9
1AFh	SWOFF_HWRST	Switch Off Events for HW RESET Qualify Register (Configuration Of Behavior Of The Device)	Section 3.7.10
1B0h	SWOFF_COLDRST	Switch Off Events for COLD RESET Qualify Register (Configuration Of Behavior Of The Device)	Section 3.7.11
1B1h	SWOFF_STATUS	Switch Off Events for HW RESET Qualify Register	Section 3.7.12
1B2h	PMU_CONFIG	PMU Configuration Register	Section 3.7.13
1B4h	SPARE	SPARE Register	Section 3.7.14
1B7h	SW_REVISION	Software (SW) Revision Register	Section 3.7.15

3.7.1 DEV_CTRL Register (Address = 1A0h) [reset = 1h]

DEV_CTRL is shown in Figure 3-83 and described in Table 3-90.

Return to Summary Table.

Device Control Register
RESET register domain: SWORST

Figure 3-83. DEV_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				DEV_STATUS		SW_RST	DEV_ON
R-0h				R-0h		R/W-0h	R/W-1h

Table 3-90. DEV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-2	DEV_STATUS	R	0h	Device status 00: OFF 01: ACTIVE 10: Not applicable (ACTIVE) 11: SLEEP
1	SW_RST	R/W	0h	Software Reset (SW_RST) Writing 1 will restart the device (turn-off sequence followed by turn-on sequence) This bit is cleared automatically
0	DEV_ON	R/W	1h	Device ON enable 1: will maintain the device in ACTIVE mode 0: allow the device to go in OFF mode

3.7.2 POWER_CTRL Register (Address = 1A1h) [reset = 47h]

POWER_CTRL is shown in Figure 3-84 and described in Table 3-91.

Return to Summary Table.

Power control register
RESET register domain: SWORST

Figure 3-84. POWER_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						ENABLE1_MASK	NSLEEP_MASK
R-11h						R/W-1h	R/W-1h

Table 3-91. POWER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	11h	
1	ENABLE1_MASK	R/W	1h	Enable of the ENABLE1 line (mask) 0: ENABLE1 is not masked (allow control of the resource with ENABLE1 pin) 1: ENABLE1 is masked (does not affect resource control) (default)
0	NSLEEP_MASK	R/W	1h	Enable of the NSLEEP line (mask) 0: NSLEEP is not masked (allow control of the resource with NSLEEP pin) 1: NSLEEP is masked (does not affect resource control) (default)

3.7.3 VSYS_LO Register (Address = 1A2h) [reset = X]

VSYS_LO is shown in Figure 3-85 and described in Table 3-92.

Return to Summary Table.

VSYS Low threshold register
RESET register domain: HWRST

Figure 3-85. VSYS_LO Register

7	6	5	4	3	2	1	0
RESERVED			THRESHOLD				
R-0h			R-X				

Table 3-92. VSYS_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	THRESHOLD	R	X	VSYS_LO - System voltage falling edge threshold. When VCCx input falls below VSYS_LO, device enters OFF mode and is ready for start-up event. Configured by OTP bits. From 2.5V to 3.10V per 50mV step. 00000 = 2.300 V (Reserved) 00001 = 2.050 V (Reserved) 00010 = 2.100 V (Reserved) 00011 = 2.150 V (Reserved) 00100 = 2.200 V (Reserved) 00101 = 2.250 V (Reserved) 00110 = 2.300 V (Reserved) 00111 = 2.350 V (Reserved) 01000 = 2.400 V (Reserved) 01001 = 2.450 V (Reserved) 01010 = 2.500 V 01011 = 2.550 V 01100 = 2.600 V 01101 = 2.650 V 01110 = 2.700 V 01111 = 2.750 V 10000 = 2.800 V 10001 = 2.850 V 10010 = 2.900 V 10011 = 2.950 V 10100 = 3.000 V 10101 = 3.050 V 10110 = 3.100V 10111 = Reserved .. 11111 = Reserved

3.7.4 VSYS_MON Register (Address = 1A3h) [reset = X]

VSYS_MON is shown in Figure 3-86 and described in Table 3-93.

Return to Summary Table.

VSYS Monitoring register. This register is initialized by OTP memory. The software can overwrite this value by a new value (VSYS_MON - from 2.3V to 4.6V).
RESET register domain: SWORST

Figure 3-86. VSYS_MON Register

7	6	5	4	3	2	1	0
ENABLE	RESERVED	THRESHOLD					
R/W-0h	R-0h	R/W-X					

Table 3-93. VSYS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	0h	Enable VSYS monitoring (only in ACTIVE /SLEEP) 0: VSYS monitoring is not enabled 1: VSYS monitoring is enabled
6	RESERVED	R	0h	

Table 3-93. VSYS_MON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESHOLD	R/W	X	VSYS_HI Configured by OTP bits. By SW, from 2.3V to 4.6V per 50mV step. 000000 = 2.30 V 100000 = 3.60 V 000001 = 2.30 V 100001 = 3.65 V 000010 = 2.30 V 100010 = 3.70 V 000011 = 2.30 V 100011 = 3.75 V 000100 = 2.30 V 100100 = 3.80 V 000101 = 2.30 V 100101 = 3.85 V 000110 = 2.30 V 100110 = 3.90 V 000111 = 2.35 V 100111 = 3.95 V 001000 = 2.40 V 101000 = 4.00 V 001001 = 2.45 V 101001 = 4.05 V 001010 = 2.50 V 101010 = 4.10 V 001011 = 2.55 V 101011 = 4.15 V 001100 = 2.60 V 101100 = 4.20 V 001101 = 2.65 V 101101 = 4.25 V 001110 = 2.70 V 101110 = 4.30 V 001111 = 2.75 V 101111 = 4.35 V 010000 = 2.80 V 110000 = 4.40 V 010001 = 2.85 V 110001 = 4.45 V 010010 = 2.90 V 110010 = 4.50 V 010011 = 2.95 V 110011 = 4.55 V 010100 = 3.00 V 110100 = 4.60 V 010101 = 3.05 V 110101 = 4.60 V 010110 = 3.10 V 110110 = 4.60 V 010111 = 3.15 V 110111 = 4.60 V 011000 = 3.20 V 111000 = 4.60 V 011001 = 3.25 V 111001 = 4.60 V 011010 = 3.30 V 111010 = 4.60 V 011011 = 3.35 V 111011 = 4.60 V 011100 = 3.40 V 111100 = 4.60 V 011101 = 3.45 V 111101 = 4.60 V 011110 = 3.50 V 111110 = 4.60 V 011111 = 3.55 V 111111 = 4.60 V

3.7.5 WATCHDOG Register (Address = 1A5h) [reset = 7h]

WATCHDOG is shown in Figure 3-87 and described in Table 3-94.

Return to Summary Table.

Watch dog timer Register
RESET register domain: SWORST
NOTES:
The WATCHDOG.TIMER counter is initialized with the RESET_OUT=0
The WATCHDOG.TIMER counter starts as soon as RESET_OUT is released.

Figure 3-87. WATCHDOG Register

7	6	5	4	3	2	1	0
RESERVED		LOCK	ENABLE	MODE	TIMER		
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-7h		

Table 3-94. WATCHDOG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LOCK	R/W	0h	Access protection of the WATCHDOG.ENABLE, WATCHDOC.MODE and WATCHDOG.LOCK bits 0: No protection. R/W access to these register bits 1: Protection of these registers (Read only). This bit will reset (0b0) during SWITCH-OFF
4	ENABLE	R/W	0h	Selection of the Watchdog: 0: Watchdog is not selected (disable) (default) 1: Watchdog is elected (enabled)
3	MODE	R/W	0h	Select type of watchdog behavior: 0: Periodic (default) 1: Interrupt mode
2-0	TIMER	R/W	7h	Timer delay selection: 000: 1s 001: 2s 010: 4s 011: 8s 100: 16s 101: 32s 110: 64s 111: 128s (default)

3.7.6 BOOT_STATUS Register (Address = 1A6h) [reset = 0h]

BOOT_STATUS is shown in Figure 3-88 and described in Table 3-95.

Return to Summary Table.

BOOT status register. Provide a copy of the boot pins
RESET register domain: POR
NOTES: This register is updated during the power transition from NOSUPPLY to WAITON state.

Figure 3-88. BOOT_STATUS Register

7	6	5	4	3	2	1	0
RESERVED						BOOT1	BOOT0
R-0h						R-0h	R-0h

Table 3-95. BOOT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	BOOT1	R	0h	Provide a copy of the BOOT1 pin
0	BOOT0	R	0h	Provide a copy of the BOOT0 pin

3.7.7 VRTC_CTRL Register (Address = 1A8h) [reset = X]

VRTC_CTRL is shown in Figure 3-89 and described in Table 3-96.

Return to Summary Table.

VRTC Control Register
RESET register domain: HWRST

Figure 3-89. VRTC_CTRL Register

7	6	5	4	3	2	1	0
VRTC_18_15	VRTC_EN_SLP	VRTC_EN_OFF	VRTC_PWEN	RESERVED			
R-X	R/W-1h	R/W-1h	R/W-1h	R/W-Ah			

Table 3-96. VRTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VRTC_18_15	R	X	VRTC voltage selection. This bit will allow to decrease the power consumption in BACKUP mode by setting the VRCT at 1.5V. 0: 1.8V (default) 1: 1.5V
6	VRTC_EN_SLP	R/W	1h	0: VRTC is configured in the standard power mode configuration when device is in SLEEP state (biasing also in SLEEP state). 1: VRTC is configured in a low-power mode configuration when device is in SLEEP state (biasing also in SLEEP state) (default).
5	VRTC_EN_OFF	R/W	1h	0: VRTC is configured in the standard power mode configuration when device is in OFF state (biasing also in OFF state) 1: VRTC is configured in a low-power mode configuration when device is in OFF state (biasing also in OFF state) (default).
4	VRTC_PWEN	R/W	1h	0: VRTC is configured in a low-power mode configuration. 1: VRTC is configured in the standard power mode configuration (default)
3-0	RESERVED	R/W	Ah	

3.7.8 LONG_PRESS_KEY Register (Address = 1A9h) [reset = 3Ch]

LONG_PRESS_KEY is shown in Figure 3-90 and described in Table 3-97.

Return to Summary Table.

Long Press Key (LPK) configuration register
RESET register domain: HWRST

Figure 3-90. LONG_PRESS_KEY Register

7	6	5	4	3	2	1	0
LPK_LOCK	RESERVED	RESERVED	LPK_INT_CLR	LPK_TIME		RESERVED	
R/W-0h	R-0h	R-1h	R/W-1h	R/W-3h		R-0h	

Table 3-97. LONG_PRESS_KEY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LPK_LOCK	R/W	0h	Access protection of the LPK_TIME, LPK_EN and LPK_LOCK registers 0: No protection. R/W access to these register bits (default) 1: Protection of these registers (Read only). This bit will reset (0b0) during SWITCH-OFF
6	RESERVED	R	0h	
5	RESERVED	R	1h	
4	LPK_INT_CLR	R/W	1h	Interrupt clear behavior configuration. Interrupt clear will have two behavior based on bit configuration. 0: Switch OFF cannot be cancelled if both PWRON and RPWON are low. It mean if only PWRON is used and interrupt clears, Switch OFF is canceled. If RPWRON is high an PWRON is low, Switch OFF occurs only if interrupt is not cleared. 1: Switch OFF cannot be cancelled when PWRON maintains low (default).
3-2	LPK_TIME	R/W	3h	Long press key duration 00: 6 second 01: 8 second 10: 10 second 11: 12 second (default)
1-0	RESERVED	R	0h	

3.7.9 OSC_THERM_CTRL Register (Address = 1AAh) [reset = Ch]

OSC_THERM_CTRL is shown in Figure 3-91 and described in Table 3-98.

Return to Summary Table.

Oscillator and Thermal control register
RESET register domain: HWRST

Figure 3-91. OSC_THERM_CTRL Register

7	6	5	4	3	2	1	0
VANA_ON_IN_SLEEP	INT_MASK_IN_SLEEP	RC15MHZ_ON_IN_SLEEP	THERM_OFF_IN_SLEEP	THERM_HD_SEL		RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-3h		R/W-0h	

Table 3-98. OSC_THERM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VANA_ON_IN_SLEEP	R/W	0h	VANA LDO selection during SLEEP mode 0: VANA LDO is OFF in SLEEP mode (default) 1: VANA LDO is ON in SLEEP mode (In case some modules are used in SLEEP mode and need VANA (USB OTG, ILMON))
6	INT_MASK_IN_SLEEP	R/W	0h	INT masked selection during SLEEP mode (Released interrupt line only when DEVICE fully wake up) 0: INT is not masked in SLEEP mode (default) 1: INT is asserted when SLEEP2ACTIVE transition is completed (allow to wakeup platform before INT generation)
5	RC15MHZ_ON_IN_SLEEP	R/W	0h	RC15MHZ oscillator selection during SLEEP mode 0: RC15MHZ oscillator is OFF in SLEEP mode. Minimize consumption in SLEEP mode (default) 1: RC15MHZ oscillator is ON in SLEEP mode. It allow to make I2C/SPI access in SLEEP mode.
4	THERM_OFF_IN_SLEEP	R/W	0h	THERM selection during SLEEP mode (Minimization of the power consumption) 0: THERM is ON in SLEEP mode (default) 1: THERM is OFF in SLEEP mode
3-2	THERM_HD_SEL	R/W	3h	Hot die temperature detection selection: 00: 117 / 108 deg. 01: 121 / 112 deg. 10: 125 / 116 deg. 11: 130 / 120 deg. (default)
1-0	RESERVED	R/W	0h	

3.7.10 SWOFF_HWRST Register (Address = 1AFh) [reset = X]

SWOFF_HWRST is shown in Figure 3-92 and described in Table 3-99.

Return to Summary Table.

Qualify which switch off events generate a HW RESET (configuration of behavior of the device)
RESET register domain: HWRST

Figure 3-92. SWOFF_HWRST Register

7	6	5	4	3	2	1	0
PWRON_LPK	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

Table 3-99. SWOFF_HWRST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWRON_LPK	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
6	PWRDOWN	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
5	WTD	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
4	TSHUT	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
3	RESET_IN	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
2	SW_RST	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
1	VSYS_LO	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
0	GPADC_SHUTDOWN	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)

3.7.11 SWOFF_COLDRST Register (Address = 1B0h) [reset = X]

SWOFF_COLDRST is shown in Figure 3-93 and described in Table 3-100.

Return to Summary Table.

Qualify which switch off events generate a COLD RESET (configuration of behavior of the device)
RESET register domain: HWRST

Figure 3-93. SWOFF_COLDRST Register

7	6	5	4	3	2	1	0
WRON_LPKRVED	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 3-100. SWOFF_COLDRST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WRON_LPKRVED	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
6	PWRDOWN	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
5	WTD	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
4	TSHUT	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
3	RESET_IN	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
2	SW_RST	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
1	VSYS_LO	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
0	GPADC_SHUTDOWN	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)

3.7.12 SWOFF_STATUS Register (Address = 1B1h) [reset = 0h]

SWOFF_STATUS is shown in Figure 3-94 and described in Table 3-101.

Return to Summary Table.

Qualify which switch off events generate a HW RESET
RESET register domain: PORRST

Figure 3-94. SWOFF_STATUS Register

7	6	5	4	3	2	1	0
PWRON_LPK	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN
C-0h	C-0h	C-0h	C-0h	C-0h	C-0h	C-0h	C-0h

Table 3-101. SWOFF_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWRON_LPK	C	0h	
6	PWRDOWN	C	0h	
5	WTD	C	0h	
4	TSHUT	C	0h	
3	RESET_IN	C	0h	
2	SW_RST	C	0h	
1	VSYS_LO	C	0h	
0	GPADC_SHUTDOWN	C	0h	

3.7.13 PMU_CONFIG Register (Address = 1B2h) [reset = X]

PMU_CONFIG is shown in Figure 3-95 and described in Table 3-102.

Return to Summary Table.

PMU configuration
RESET register domain: HWRST

Figure 3-95. PMU_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	HIGH_VCC_SENSE	SPARE5	SPARE4	SWOFF_DLY		GATE_RESET_OUT	AUTODEVON
R-0h	R/W-0h	R/W-X	R/W-X	R/W-X		R/W-X	R/W-X

Table 3-102. PMU_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	HIGH_VCC_SENSE	R/W	0h	High VCC Sense (> 5V) selection 0: High VCC not enabled 1: High VCC enabled
5	SPARE5	R/W	X	
4	SPARE4	R/W	X	
3-2	SWOFF_DLY	R/W	X	Delay before to go to SWITCH-OFF to allow host processor to save his context (device will be maintained ACTIVE until delay expiration then SWITCH-OFF) 00: no delay 01: 1 second window (+/- 250ms) 10: 2 second window (+/- 250ms) 11: 4 second window (+/- 250ms)
1	GATE_RESET_OUT	R/W	X	Gating of RESET_OUT with Crystal oscillator status 0: RESET_OUT not gated 1: RESET_OUT released when crystal oscillator is ready
0	AUTODEVON	R/W	X	Selection of the feature Auto Device ON 0: Feature is inactive 1: Feature is active

3.7.14 SPARE Register (Address = 1B4h) [reset = X]

SPARE is shown in Figure 3-96 and described in Table 3-103.

Return to Summary Table.

SPARE register
RESET register domain: HWRST

Figure 3-96. SPARE Register

7	6	5	4	3	2	1	0
SPARE					REGEN2_OD	RESERVED	REGEN1_OD
R/W-X					R/W-X	R/W-X	R/W-X

Table 3-103. SPARE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	SPARE	R/W	X	SPARE register
2	REGEN2_OD	R/W	X	0: open drain not enable (Push-Pull enabled) 1: open drain enable (Push-Pull not enable)
1	RESERVED	R/W	X	
0	REGEN1_OD	R/W	X	0: open drain not enable (Push-Pull enabled) 1: open drain enable (Push-Pull not enable)

3.7.15 SW_REVISION Register (Address = 1B7h) [reset = X]

SW_REVISION is shown in Figure 3-97 and described in Table 3-104.

Return to Summary Table.

Software (SW) revision register
RESET register domain: HWRST

Figure 3-97. SW_REVISION Register

7	6	5	4	3	2	1	0
SW_REVISION							
R-X							

Table 3-104. SW_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SW_REVISION	R	X	Software (SW) revision register - This revision will be representative of the OTP version.

3.8 FUNC_RESOURCE Registers

Table 3-105 lists the memory-mapped registers for the FUNC_RESOURCE. All register offset addresses not listed in Table 3-105 should be considered as reserved locations and the register contents should not be modified.

Table 3-105. FUNC_RESOURCE Registers

Address	Acronym	Register Name	Section
1D4h	CLK32KGO1V8_CTRL	CLK32KGO1V8 Control Register	Section 3.8.1
1D5h	REGEN1_CTRL	REGEN1 Control Register	Section 3.8.2
1D6h	PLLEN_CTRL	PLLEN Control Register	Section 3.8.3
1D7h	SYSEN1_CTRL	SYSEN1 (GPIO_4 Secondary Function) Control Register	Section 3.8.4
1D8h	SYSEN2_CTRL	SYSEN1 (GPIO_6 Secondary Function) Control Register	Section 3.8.5
1D9h	NSLEEP_RES_ASSIGN	NSLEEP Resource Assignment Register	Section 3.8.6
1DAh	NSLEEP_SMPS_ASSIGN	NSLEEP Input Signal SMPS Resource Assignment Register	Section 3.8.7
1DBh	NSLEEP_LDO_ASSIGN1	NSLEEP Input Signal LDO Resource Assignment Register 1	Section 3.8.8
1DCh	NSLEEP_LDO_ASSIGN2	NSLEEP Input Signal LDO Resource Assignment Register 2	Section 3.8.9
1DDh	ENABLE1_RES_ASSIGN	ENABLE1 Resource Assignment Register	Section 3.8.10
1DEh	ENABLE1_SMPS_ASSIGN	ENABLE1 Input Signal SMPS Resource Assignment Register	Section 3.8.11
1DFh	ENABLE1_LDO_ASSIGN1	ENABLE1 Input Signal LDO Resource Assignment Register 1	Section 3.8.12
1E0h	ENABLE1_LDO_ASSIGN2	ENABLE1 Input Signal LDO Resource Assignment Register 2	Section 3.8.13
1E5h	REGEN2_CTRL	REGEN2 Control Register	Section 3.8.14

3.8.1 CLK32KGO1V8_CTRL Register (Address = 1D4h) [reset = X]

CLK32KGO1V8_CTRL is shown in Figure 3-98 and described in Table 3-106.

Return to Summary Table.

CLK32KGO1V8 control register
RESET register domain: SWORST

Figure 3-98. CLK32KGO1V8_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R-0h	R-0h	R/W-0h	R-0h	R/W-X

Table 3-106. CLK32KGO1V8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R	0h	CLK32KGO1V8 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	CLK32KGO1V8 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	X	CLK32KGO1V8 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.8.2 REGEN1_CTRL Register (Address = 1D5h) [reset = X]

REGEN1_CTRL is shown in Figure 3-99 and described in Table 3-107.

Return to Summary Table.

REGEN1 control register
RESET register domain: SWORST

Figure 3-99. REGEN1_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R-0h	R-0h	R/W-0h	R-0h	R/W-X

Table 3-107. REGEN1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R	0h	REGEN1 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	REGEN1 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	X	REGEN1 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.8.3 PLLEN_CTRL Register (Address = 1D6h) [reset = X]

PLLEN_CTRL is shown in Figure 3-100 and described in Table 3-108.

Return to Summary Table.

PLLEN control register
RESET register domain: SWORST

Figure 3-100. PLLEN_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X

Table 3-108. PLLEN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	STATUS	R/W	0h	PLLEN Status 0: OFF 1: ON
3	RESERVED	R/W	0h	
2	MODE_SLEEP	R/W	0h	PLLEN SLEEP Mode 0: OFF 1: ON
1	RESERVED	R/W	0h	
0	MODE_ACTIVE	R/W	X	PLLEN ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.8.4 SYSEN1_CTRL Register (Address = 1D7h) [reset = X]

SYSEN1_CTRL is shown in Figure 3-101 and described in Table 3-109.

Return to Summary Table.

SYSEN1 (GPIO_4 secondary function) control register
RESET register domain: SWORST

Figure 3-101. SYSEN1_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R/W-0h	R-0h	R/W-0h	R-0h	R/W-X

Table 3-109. SYSEN1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R/W	0h	SYSEN1 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	GPIO_4 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	X	GPIO_4 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.8.5 SYSEN2_CTRL Register (Address = 1D8h) [reset = X]

SYSEN2_CTRL is shown in Figure 3-102 and described in Table 3-110.

Return to Summary Table.

SYSEN1 (GPIO_6 secondary function) control register
RESET register domain: SWORST

Figure 3-102. SYSEN2_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R-0h	R-0h	R/W-0h	R-0h	R/W-X

Table 3-110. SYSEN2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R	0h	SYSEN2 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	GPIO_6 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	X	GPIO_6 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.8.6 NSLEEP_RES_ASSIGN Register (Address = 1D9h) [reset = 0h]

NSLEEP_RES_ASSIGN is shown in Figure 3-103 and described in Table 3-111.

Return to Summary Table.

NSLEEP resource assignment register
RESET register domain: HWRST

Figure 3-103. NSLEEP_RES_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED	REGEN2	CLK32KGO1V8	RESERVED	SYSEN2	SYSEN1	PLLEN	REGEN1
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-111. NSLEEP_RES_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	REGEN2	R/W	0h	0: NSLEEP has no effect on REGEN2 1: REGEN2 is controlled by NSLEEP
5	CLK32KGO1V8	R/W	0h	0: NSLEEP has no effect on CLK32KGO1V8 1: CLK32KGO1V8 is controlled by NSLEEP
4	RESERVED	R	0h	
3	SYSEN2	R/W	0h	0: NSLEEP has no effect on SYSEN2 1: SYSEN2 is controlled by NSLEEP
2	SYSEN1	R/W	0h	0: NSLEEP has no effect on SYSEN1 1: SYSEN1 is controlled by NSLEEP
1	PLLEN	R/W	0h	0: NSLEEP has no effect on PLLEN 1: PLLEN is controlled by NSLEEP
0	REGEN1	R/W	0h	0: NSLEEP has no effect on REGEN1 1: REGEN1 is controlled by NSLEEP

3.8.7 NSLEEP_SMPS_ASSIGN Register (Address = 1DAh) [reset = 0h]

NSLEEP_SMPS_ASSIGN is shown in Figure 3-104 and described in Table 3-112.

Return to Summary Table.

NSLEEP input signal SMPS resource assignment register
RESET register domain: HWRST

Figure 3-104. NSLEEP_SMPS_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-112. NSLEEP_SMPS_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SMPS9	R/W	0h	0: NSLEEP has no effect on SMPS9 1: SMPS9 is controlled by NSLEEP
5	SMPS8	R/W	0h	0: NSLEEP has no effect on SMPS8 1: SMPS8 is controlled by NSLEEP
4	SMPS7	R/W	0h	0: NSLEEP has no effect on SMPS7 1: SMPS7 is controlled by NSLEEP
3	SMPS6	R/W	0h	0: NSLEEP has no effect on SMPS6 1: SMPS6 is controlled by NSLEEP
2	SMPS45	R/W	0h	0: NSLEEP has no effect on SMPS45 1: SMPS45 is controlled by NSLEEP
1	SMPS3	R/W	0h	0: NSLEEP has no effect on SMPS3 1: SMPS3 is controlled by NSLEEP
0	SMPS12	R/W	0h	0: NSLEEP has no effect on SMPS12 1: SMPS12 is controlled by NSLEEP

3.8.8 NSLEEP_LDO_ASSIGN1 Register (Address = 1DBh) [reset = 0h]

NSLEEP_LDO_ASSIGN1 is shown in Figure 3-105 and described in Table 3-113.

Return to Summary Table.

NSLEEP input signal LDO resource assignment register #1
RESET register domain: HWRST

Figure 3-105. NSLEEP_LDO_ASSIGN1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	LDO4	LDO3	LDO2	LDO1
				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-113. NSLEEP_LDO_ASSIGN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	LDO4	R/W	0h	0: NSLEEP has no effect on LDO4 1: LDO4 is controlled by NSLEEP
2	LDO3	R/W	0h	0: NSLEEP has no effect on LDO3 1: LDO3 is controlled by NSLEEP
1	LDO2	R/W	0h	0: NSLEEP has no effect on LDO2 1: LDO2 is controlled by NSLEEP
0	LDO1	R/W	0h	0: NSLEEP has no effect on LDO1 1: LDO1 is controlled by NSLEEP

3.8.9 NSLEEP_LDO_ASSIGN2 Register (Address = 1DCh) [reset = 0h]

NSLEEP_LDO_ASSIGN2 is shown in Figure 3-106 and described in Table 3-114.

Return to Summary Table.

NSLEEP input signal LDO resource assignment register #2
RESET register domain: HWRST

Figure 3-106. NSLEEP_LDO_ASSIGN2 Register

7	6	5	4	3	2	1	0
RESERVED					LDOUSB	LDOLN	LDO9
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 3-114. NSLEEP_LDO_ASSIGN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	LDOUSB	R/W	0h	0: NSLEEP has no effect on LDOUSB 1: LDOUSB is controlled by NSLEEP
1	LDOLN	R/W	0h	0: NSLEEP has no effect on LDOLN 1: LDOLN is controlled by NSLEEP
0	LDO9	R/W	0h	0: NSLEEP has no effect on LDO9 1: LDO9 is controlled by NSLEEP

3.8.10 ENABLE1_RES_ASSIGN Register (Address = 1DDh) [reset = 0h]

ENABLE1_RES_ASSIGN is shown in Figure 3-107 and described in Table 3-115.

Return to Summary Table.

ENABLE1 resource assignment register
RESET register domain: HWRST

Figure 3-107. ENABLE1_RES_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED	REGEN2	CLK32KGO1V8	RESERVED	SYSEN2	SYSEN1	PLLEN	REGEN1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-115. ENABLE1_RES_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	REGEN2	R/W	0h	0: ENABLE1 has no effect on REGEN2 1: REGEN2 is controlled by ENABLE1
5	CLK32KGO1V8	R/W	0h	0: ENABLE1 has no effect on CLK32KGO1V8 1: CLK32KGO1V8 is controlled by ENABLE1
4	RESERVED	R/W	0h	
3	SYSEN2	R/W	0h	0: ENABLE1 has no effect on SYSEN2 1: SYSEN2 is controlled by ENABLE1
2	SYSEN1	R/W	0h	0: ENABLE1 has no effect on SYSEN1 1: SYSEN1 is controlled by ENABLE1
1	PLLEN	R/W	0h	0: ENABLE1 has no effect on PLLEN 1: PLLEN is controlled by ENABLE1
0	REGEN1	R/W	0h	0: ENABLE1 has no effect on REGEN1 1: REGEN1 is controlled by ENABLE1

3.8.11 ENABLE1_SMPS_ASSIGN Register (Address = 1DEh) [reset = 0h]

ENABLE1_SMPS_ASSIGN is shown in Figure 3-108 and described in Table 3-116.

Return to Summary Table.

ENABLE1 input signal SMPS resource assignment register
RESET register domain: HWRST

Figure 3-108. ENABLE1_SMPS_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED	SMPS9	SMPS8	SMPS7	SMPS6	SMPS45	SMPS3	SMPS12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-116. ENABLE1_SMPS_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	SMPS9	R/W	0h	0: ENABLE1 has no effect on SMPS9 1: SMPS9 is controlled by ENABLE1
5	SMPS8	R/W	0h	0: ENABLE1 has no effect on SMPS8 1: SMPS8 is controlled by ENABLE1
4	SMPS7	R/W	0h	0: ENABLE1 has no effect on SMPS7 1: SMPS7 is controlled by ENABLE1
3	SMPS6	R/W	0h	0: ENABLE1 has no effect on SMPS6 1: SMPS6 is controlled by ENABLE1
2	SMPS45	R/W	0h	0: ENABLE1 has no effect on SMPS45 1: SMPS45 is controlled by ENABLE1
1	SMPS3	R/W	0h	0: ENABLE1 has no effect on SMPS3 1: SMPS3 is controlled by ENABLE1
0	SMPS12	R/W	0h	0: ENABLE1 has no effect on SMPS12 1: SMPS12 is controlled by ENABLE1

3.8.12 ENABLE1_LDO_ASSIGN1 Register (Address = 1DFh) [reset = 0h]

ENABLE1_LDO_ASSIGN1 is shown in Figure 3-109 and described in Table 3-117.

Return to Summary Table.

ENABLE1 input signal LDO resource assignment register #1
RESET register domain: HWRST

Figure 3-109. ENABLE1_LDO_ASSIGN1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	LDO4	LDO3	LDO2	LDO1
				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-117. ENABLE1_LDO_ASSIGN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	LDO4	R/W	0h	0: ENABLE1 has no effect on LDO4 1: LDO4 is controlled by ENABLE1
2	LDO3	R/W	0h	0: ENABLE1 has no effect on LDO3 1: LDO3 is controlled by ENABLE1
1	LDO2	R/W	0h	0: ENABLE1 has no effect on LDO2 1: LDO2 is controlled by ENABLE1
0	LDO1	R/W	0h	0: ENABLE1 has no effect on LDO1 1: LDO1 is controlled by ENABLE1

3.8.13 ENABLE1_LDO_ASSIGN2 Register (Address = 1E0h) [reset = 0h]

ENABLE1_LDO_ASSIGN2 is shown in Figure 3-110 and described in Table 3-118.

Return to Summary Table.

ENABLE1 input signal LDO resource assignment register #2
RESET register domain: HWRST

Figure 3-110. ENABLE1_LDO_ASSIGN2 Register

7	6	5	4	3	2	1	0
RESERVED					LDOUSB	LDOLN	LDO9
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 3-118. ENABLE1_LDO_ASSIGN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	LDOUSB	R/W	0h	0: ENABLE1 has no effect on LDOUSB 1: LDOUSB is controlled by ENABLE1
1	LDOLN	R/W	0h	0: ENABLE1 has no effect on LDOLN 1: LDOLN is controlled by ENABLE1
0	LDO9	R/W	0h	0: ENABLE1 has no effect on LDO9 1: LDO9 is controlled by ENABLE1

3.8.14 REGEN2_CTRL Register (Address = 1E5h) [reset = X]

REGEN2_CTRL is shown in Figure 3-111 and described in Table 3-119.

Return to Summary Table.

REGEN2 control register
RESET register domain: SWORST
Note: In QFN configuration, this pin is not bounded. This register is still visible and it is recommanded to keep the defaut values (reset value)

Figure 3-111. REGEN2_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R-0h	R-0h	R/W-0h	R-0h	R/W-X

Table 3-119. REGEN2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R	0h	REGEN2 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	REGEN2 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	X	REGEN2 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.9 FUNC_PAD_CONTROL Registers

Table 3-120 lists the memory-mapped registers for the FUNC_PAD_CONTROL. All register offset addresses not listed in Table 3-120 should be considered as reserved locations and the register contents should not be modified.

Table 3-120. FUNC_PAD_CONTROL Registers

Address	Acronym	Register Name	Section
1F4h	PU_PD_INPUT_CTRL1	Pull-Up Pull-Down Control Register	Section 3.9.1
1F5h	PU_PD_INPUT_CTRL2	Pull-Up Pull-Down Control Register	Section 3.9.2
1F6h	PU_PD_INPUT_CTRL3	Pull-Up Pull-Down Control Register	Section 3.9.3
1F8h	OD_OUTPUT_CTRL	Open Drain Control Register	Section 3.9.4
1F9h	POLARITY_CTRL	Polarity Control Register	Section 3.9.5
1FAh	PRIMARY_SECONDARY_PAD1	PAD/PIN Function Register (Primary vs. Secondary)	Section 3.9.6
1FBh	PRIMARY_SECONDARY_PAD2	PAD/PIN Function Register (Primary vs. Secondary)	Section 3.9.7
1FCh	I2C_SPI	Validity Memory Register	Section 3.9.8
1FDh	PU_PD_INPUT_CTRL4	Pull-Up Pull-Down Control Register	Section 3.9.9

3.9.1 PU_PD_INPUT_CTRL1 Register (Address = 1F4h) [reset = X]

PU_PD_INPUT_CTRL1 is shown in Figure 3-112 and described in Table 3-121.

Return to Summary Table.

Pull-up Pull-down control register
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)

Figure 3-112. PU_PD_INPUT_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RESET_IN_PD	RESERVED			PWRDOWN_PD	NRESWARM_PU	RESERVED
R-0h	R/W-X	R-2h			R/W-X	R/W-1h	R-0h

Table 3-121. PU_PD_INPUT_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESET_IN_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled
5-3	RESERVED	R	2h	
2	PWRDOWN_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled
1	NRESWARM_PU	R/W	1h	0: Pull-up not enabled 1: Pull-up enabled (default)
0	RESERVED	R	0h	

3.9.2 PU_PD_INPUT_CTRL2 Register (Address = 1F5h) [reset = 86h]

PU_PD_INPUT_CTRL2 is shown in Figure 3-113 and described in Table 3-122.

Return to Summary Table.

Pull-up Pull-down control register
RESET register domain: HWRST

Figure 3-113. PU_PD_INPUT_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED				ENABLE1_PU	ENABLE1_PD	NSLEEP_PU	NSLEEP_PD
R-8h				R/W-0h	R/W-1h	R/W-1h	R/W-0h

Table 3-122. PU_PD_INPUT_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	8h	
3	ENABLE1_PU	R/W	0h	0: Pull-up not enabled (default) 1: Pull-up enabled
2	ENABLE1_PD	R/W	1h	0: Pull-down not enabled 1: Pull-down enabled (default)
1	NSLEEP_PU	R/W	1h	0: Pull-up not enabled 1: Pull-up enabled (default)
0	NSLEEP_PD	R/W	0h	0: Pull-down not enabled (default) 1: Pull-down enabled

3.9.3 PU_PD_INPUT_CTRL3 Register (Address = 1F6h) [reset = Fh]

PU_PD_INPUT_CTRL3 is shown in Figure 3-114 and described in Table 3-123.

Return to Summary Table.

Pull-up Pull-down control register
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)

Figure 3-114. PU_PD_INPUT_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		RESERVED		POWERHOLD_PD	RESERVED	
R-0h	R-0h		R-1h		R/W-1h	R-3h	

Table 3-123. PU_PD_INPUT_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	-
6-5	RESERVED	R	0h	
4-3	RESERVED	R	1h	
2	POWERHOLD_PD	R/W	1h	Secondary function of GPIO_7 0: Pull-down not enabled 1: Pull-down enabled (default)
1-0	RESERVED	R	3h	

3.9.4 OD_OUTPUT_CTRL Register (Address = 1F8h) [reset = 1h]

OD_OUTPUT_CTRL is shown in Figure 3-115 and described in Table 3-124.

Return to Summary Table.

Open Drain control register
RESET register domain: HWRST
Note: It is user responsibility to take care about the IO direction and type (Open drain / Push-Pull) versus the pull-up/pull-down selections

Figure 3-115. OD_OUTPUT_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	VBUSDET_OD	RESERVED		INT_OD	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-1h

Table 3-124. OD_OUTPUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	VBUSDET_OD	R/W	0h	Secondary function of GPIO_1 0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)
5-4	RESERVED	R/W	0h	
3	INT_OD	R/W	0h	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)
2	RESERVED	R/W	0h	
1	RESERVED	R/W	0h	
0	RESERVED	R/W	1h	

3.9.5 POLARITY_CTRL Register (Address = 1F9h) [reset = X]

POLARITY_CTRL is shown in Figure 3-116 and described in Table 3-125.

Return to Summary Table.

Polarity control register. This register allows to invert the initial polarity of the input or output pin.
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO polarity

Figure 3-116. POLARITY_CTRL Register

7	6	5	4	3	2	1	0
INT_POLARITY	RESERVED	ENABLE1_POLARITY	NSLEEP_POLARITY	RESET_IN_POLARITY	GPIO_3_POLARITY	POWERGOOD_POLARITY	PWRDOWN_POLARITY
R/W-0h	R-0h	R/W-0h	R/W-0h	R-X	R-X	R-X	R-X

Table 3-125. POLARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_POLARITY	R/W	0h	Select the polarity of the INT output line 0: Interrupt line (INT) is low when interrupt is pending (default) 1: Interrupt line (INT) is high when interrupt is pending
6	RESERVED	R	0h	
5	ENABLE1_POLARITY	R/W	0h	Select the polarity of the ENABLE1 input line 0: Resources will be enable when ENABLE1 is high (default) 1: Resources will be enable when ENABLE1 is low
4	NSLEEP_POLARITY	R/W	0h	Select the polarity of the NSLEEP input line 0: Resources will go in SLEEP mode when NSLEEP is low (default) 1: Resources will go in SLEEP mode when NSLEEP is high
3	RESET_IN_POLARITY	R	X	Select the polarity of the RESET_IN input line 0: Device is switch-off when RESET_IN is low (default) 1: Device is switch-off when RESET_IN is high
2	GPIO_3_POLARITY	R	X	Select the polarity of the GPIO_3 line This polarity change will apply to the primary and secondary function. 0: inversion not enable (default) 1: inversion is enabled
1	POWERGOOD_POLARITY	R	X	Select the polarity of the POWERGOOD output line This polarity change will apply to the primary and secondary function. 0: inversion not enable - active high (default) 1: inversion is enabled - active low
0	PWRDOWN_POLARITY	R	X	Select the polarity of the PWRDOWN input line 0: inversion not enable - active high (default) 1: inversion is enabled - active low

3.9.6 PRIMARY_SECONDARY_PAD1 Register (Address = 1FAh) [reset = X]

PRIMARY_SECONDARY_PAD1 is shown in Figure 3-117 and described in Table 3-126.

Return to Summary Table.

PAD/PIN function register (Primary vs. Secondary)
RESET register domain: HWRST

Figure 3-117. PRIMARY_SECONDARY_PAD1 Register

7	6	5	4	3	2	1	0
RESERVED		GPIO_2	RESERVED	GPIO_1	RESERVED		
R-0h		R/W-X	R-0h	R/W-X	R-0h		

Table 3-126. PRIMARY_SECONDARY_PAD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	GPIO_2	R/W	X	Selection primary or secondary function associated to GPIO_2 pin/pad 0: Primary function is selected (GPIO_2) 1: Secondary function is selected (REGEN2)
4	RESERVED	R	0h	
3	GPIO_1	R/W	X	Selection primary or secondary function associated to GPIO_1 pin/pad 0: Primary function is selected (GPIO_1) 1: Secondary function is selected (VBUSDET)
2-0	RESERVED	R	0h	

3.9.7 PRIMARY_SECONDARY_PAD2 Register (Address = 1FBh) [reset = X]

PRIMARY_SECONDARY_PAD2 is shown in Figure 3-118 and described in Table 3-127.

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PAD/PIN function register (Primary vs. Secondary)
RESET register domain: HWRST

Figure 3-118. PRIMARY_SECONDARY_PAD2 Register

7	6	5	4	3	2	1	0
RESERVED		GPIO_7	RESERVED	GPIO_6	GPIO_5		GPIO_4
R-0h		R/W-X	R-0h	R/W-X	R/W-X		R/W-X

Table 3-127. PRIMARY_SECONDARY_PAD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	GPIO_7	R/W	X	Selection primary or secondary function associated to GPIO_7 pin/pad 0: Primary function is selected (GPIO_7) 1: Secondary function is selected (POWERHOLD)
4	RESERVED	R	0h	
3	GPIO_6	R/W	X	Selection primary or secondary function associated to GPIO_6 pin/pad 0: Primary function is selected (GPIO_6) 1: Secondary function is selected (SYSEN2)
2-1	GPIO_5	R/W	X	Selection primary or secondary function associated to GPIO_5 pin/pad 00: Primary function is selected (GPIO_5) 01: Secondary function is selected (CLK32KGO1V8) 1x: Secondary function is selected (SYNCCLK)
0	GPIO_4	R/W	X	Selection primary or secondary function associated to GPIO_4 pin/pad 0: Primary function is selected (GPIO_4) 1: Secondary function is selected (SYSEN1)

3.9.8 I2C_SPI Register (Address = 1FCh) [reset = X]

I2C_SPI is shown in Figure 3-119 and described in Table 3-128.

Return to Summary Table.

Validity memory
RESET register domain: HWRST

Figure 3-119. I2C_SPI Register

7	6	5	4	3	2	1	0
I2C2OTP_EN	I2C2OTP_PAGESEL	ID_I2C2	I2C_SPI	ID_I2C1			
R/W-0h	R/W-0h	R/W-X	R-X	R/W-X			

Table 3-128. I2C_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C2OTP_EN	R/W	0h	I2C to OTP (I2C2OTP) feature selection (EVM purpose only) 0: I2C2OTP is disable 1: I2C2OTP is enabled
6	I2C2OTP_PAGESEL	R/W	0h	I2C to OTP (I2C2OTP) page selection (EVM purpose only) 0: page0 is selected (OTP-page0 (Test/Trim - reserved), OTP-page1 (Sequencer - LSB), OTP-page2 (Sequencer), OTP-page3 (Sequencer)) 1: page1 is selected (OTP-page4 (Sequencer - MSB), OTP-page5 (Config))
5	ID_I2C2	R/W	X	I2C_2 address for page access versus initial address (0H12) 0: Address 0H12 1: Address 0H22
4	I2C_SPI	R	X	Selection of the interface 0: I2C 1: SPI
3-0	ID_I2C1	R/W	X	I2C_1 address for page accesses versus initial address (0H48, 0H49, 0H4A, 0H4B (OTP)) I2C_1[0]=0: 0H48 I2C_1[0]=1: 0H58 I2C_1[1]=0: 0H49 I2C_1[1]=1: 0H59 I2C_1[2]=0: 0H4A I2C_1[2]=1: 0H5A I2C_1[3]=0: 0H4B I2C_1[3]=1: 0H5B

3.9.9 PU_PD_INPUT_CTRL4 Register (Address = 1FDh) [reset = 55h]

PU_PD_INPUT_CTRL4 is shown in Figure 3-120 and described in Table 3-129.

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Pull-up Pull-down control register
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)

Figure 3-120. PU_PD_INPUT_CTRL4 Register

7	6	5	4	3	2	1	0
RESERVED					DVFS1_DAT_PD	RESERVED	DVFS1_CLK_PD
R-Ah					R/W-1h	R-0h	R/W-1h

Table 3-129. PU_PD_INPUT_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	Ah	
2	DVFS1_DAT_PD	R/W	1h	Secondary function of I2C2_SDA_SDO 0: Pull-down not enabled 1: Pull-down enabled (default)
1	RESERVED	R	0h	
0	DVFS1_CLK_PD	R/W	1h	Secondary function of I2C2_SCL_SCE 0: Pull-down not enabled 1: Pull-down enabled

3.10 FUNC_INTERRUPT Registers

Table 3-130 lists the memory-mapped registers for the FUNC_INTERRUPT. All register offset addresses not listed in Table 3-130 should be considered as reserved locations and the register contents should not be modified.

Table 3-130. FUNC_INTERRUPT Registers

Address	Acronym	Register Name	Section
210h	INT1_STATUS	Interrupt Status Register 1	Section 3.10.1
211h	INT1_MASK	Interrupt Line Mask Register 1	Section 3.10.2
212h	INT1_LINE_STATE	Interrupt Source Line State Register 1	Section 3.10.3
215h	INT2_STATUS	Interrupt Status Register 2	Section 3.10.4
216h	INT2_MASK	Interrupt Line Mask Register 2	Section 3.10.5
217h	INT2_LINE_STATE	Interrupt Source Line State Register 2	Section 3.10.6
21Ah	INT3_STATUS	Interrupt Status Register 3	Section 3.10.7
21Bh	INT3_MASK	Interrupt Line Mask Register 3	Section 3.10.8
21Ch	INT3_LINE_STATE	Interrupt Source Line State Register 3	Section 3.10.9
21Fh	INT4_STATUS	Interrupt Status Register 4	Section 3.10.10
220h	INT4_MASK	Interrupt Line Mask Register 4	Section 3.10.11
221h	INT4_LINE_STATE	Interrupt Source Line State Register 4	Section 3.10.12
222h	INT4_EDGE_DETECT1	Interrupt Edge Detection Register 4.1	Section 3.10.13
223h	INT4_EDGE_DETECT2	Interrupt Edge Detection Register 4.2	Section 3.10.14
224h	INT_CTRL	Interrupt Control Register	Section 3.10.15

3.10.1 INT1_STATUS Register (Address = 210h) [reset = 0h]

INT1_STATUS is shown in Figure 3-121 and described in Table 3-131.

Return to Summary Table.

Interrupt Status Register #1
The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR)
RESET register domain: HWRST

Figure 3-121. INT1_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	VSYS_MON	HOTDIE	PWRDOWN	RPWRON	LONG_PRESS_KEY	PWRON	RESERVED
C-0h	C-0h	C-0h	C-0h	C-0h	C-0h	C-0h	C-0h

Table 3-131. INT1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	C	0h	
6	VSYS_MON	C	0h	VSYS_MON status bit register (internal event) 0: no detection 1: Rising or Falling edge are detected
5	HOTDIE	C	0h	HOTDIE status bit register (internal event) 0: no detection 1: Rising or Falling edge are detected
4	PWRDOWN	C	0h	PWRDOWN status bit register associated to PWRDOWN pin 0: no detection 1: Rising or Falling edge are detected
3	RPWRON	C	0h	RPWRON status bit register associated to RPWRON pin 0: no detection 1: Falling edge is detected
2	LONG_PRESS_KEY	C	0h	LONG_PRESS_KEY (Long Key Press duration) status bit 0: no detection 1: Falling edge is detected
1	PWRON	C	0h	PWRON status bit register associated to PWRON pin 0: no detection 1: Falling edge is detected
0	RESERVED	C	0h	

3.10.2 INT1_MASK Register (Address = 211h) [reset = X]

INT1_MASK is shown in Figure 3-122 and described in Table 3-132.

Return to Summary Table.

Interrupt Line Mask Register #1
RESET register domain: HWRST

Figure 3-122. INT1_MASK Register

7	6	5	4	3	2	1	0
RESERVED	VSYS_MON	HOTDIE	PWRDOWN	RPWRON	LONG_PRESS_KEY	PWRON	RESERVED
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 3-132. INT1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	
6	VSYS_MON	R/W	X	VSYS_MON Line Mask bit register 0: VSYS_MON line is enabled. An interrupt is generated on INT line 1: VSYS_MON line is masked. No interrupt is generated on INT line
5	HOTDIE	R/W	X	HOTDIE Line Mask bit register 0: HOTDIE line is enabled. An interrupt is generated on INT line 1: HOTDIE line is masked. No interrupt is generated on INT line
4	PWRDOWN	R/W	X	PWRDOWN Line Mask bit register 0: PWRDOWN line is enabled. An interrupt is generated on INT line 1: PWRDOWN line is masked. No interrupt is generated on INT line
3	RPWRON	R/W	X	RPWRON Line Mask bit register 0: RPWRON line is enabled. An interrupt is generated on INT line 1: RPWRON line is masked. No interrupt is generated on INT line
2	LONG_PRESS_KEY	R/W	X	LONG_PRESS_KEY Line Mask bit register 0: LONG_PRESS_KEY line is enabled. An interrupt is generated on INT line 1: LONG_PRESS_KEY line is masked. No interrupt is generated on INT line
1	PWRON	R/W	X	PWRON Line Mask bit register 0: PWRON line is enabled. An interrupt is generated on INT line 1: PWRON line is masked. No interrupt is generated on INT line
0	RESERVED	R/W	X	

3.10.3 INT1_LINE_STATE Register (Address = 212h) [reset = 0h]

INT1_LINE_STATE is shown in Figure 3-123 and described in Table 3-133.

Return to Summary Table.

Interrupt source line state Register #1
RESET register domain: HWRST

Figure 3-123. INT1_LINE_STATE Register

7	6	5	4	3	2	1	0
RESERVED	VSYS_MON	HOTDIE	PWRDOWN	RPWRON	LONG_PRESS_KEY	PWRON	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-133. INT1_LINE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	VSYS_MON	R	0h	VSYS_MON line state register 0: VSYS_MON line is equal to 0 1: VSYS_MON line is equal to 1
5	HOTDIE	R	0h	HOTDIE line state register 0: HOTDIE line is equal to 0 1: HOTDIE line is equal to 1
4	PWRDOWN	R	0h	PWRDOWN line state register 0: PWRDOWN line is equal to 0 1: PWRDOWN line is equal to 1
3	RPWRON	R	0h	RPWRON line state register 0: RPWRON line is equal to 0 1: RPWRON line is equal to 1
2	LONG_PRESS_KEY	R	0h	LONG_PRESS_KEY line state register 0: LONG_PRESS_KEY line is equal to 0 1: LONG_PRESS_KEY line is equal to 1
1	PWRON	R	0h	PWRON line state register 0: PWRON line is equal to 0 1: PWRON line is equal to 1
0	RESERVED	R	0h	

3.10.4 INT2_STATUS Register (Address = 215h) [reset = 0h]

INT2_STATUS is shown in Figure 3-124 and described in Table 3-134.

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Interrupt Status Register #2
The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR)
RESET register domain: HWRST

Figure 3-124. INT2_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	SHORT	RESERVED	RESET_IN	RESERVED	WDT	RTC_TIMER	RTC_ALARM
C-0h	C-0h	C-0h	C-0h	C-0h	C-0h	C-0h	C-0h

Table 3-134. INT2_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	C	0h	
6	SHORT	C	0h	SHORT status bit register associated (internal event). This bit is providing information on SHORT status (LDO and SMPS) and THERMAL status (SMPS only). Hence, normal behavior when you get a SHORT/over TEMPERATURE is: - An interrupt is generated - Interrupt routine will read interrupt status then SHORT /THERMAL status to know which resource is the source, which will clear the status (SHORT /THERMAL status register is cleared upon read) - Status is then cleared before the resource is re-enabled. 0: no detection 1: Rising or falling edge are detected
5	RESERVED	C	0h	
4	RESET_IN	C	0h	RESET_IN status bit register associated to RESET_IN pin 0: no detection 1: Rising edge is detected
3	RESERVED	C	0h	
2	WDT	C	0h	WDT status bit register (internal event) 0: no detection 1: Rising edge is detected
1	RTC_TIMER	C	0h	RTC_TIMER status bit register (internal event) 0: no detection 1: Rising edge is detected
0	RTC_ALARM	C	0h	RTC_ALARM status bit register (internal event) 0: no detection 1: Rising edge is detected

3.10.5 INT2_MASK Register (Address = 216h) [reset = X]

INT2_MASK is shown in Figure 3-125 and described in Table 3-135.

Return to Summary Table.

Interrupt Line Mask Register #2
RESET register domain: HWRST

Figure 3-125. INT2_MASK Register

7	6	5	4	3	2	1	0
RESERVED	SHORT	RESERVED	RESET_IN	RESERVED	WDT	RTC_TIMER	RTC_ALARM
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 3-135. INT2_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	
6	SHORT	R/W	X	SHORT Line Mask bit register 0: SHORT line is enabled. An interrupt is generated on INT line 1: SHORT line is masked. No interrupt is generated on INT line
5	RESERVED	R/W	X	
4	RESET_IN	R/W	X	RESET_IN Line Mask bit register 0: RESET_IN line is enabled. An interrupt is generated on INT line 1: RESET_IN line is masked. No interrupt is generated on INT line
3	RESERVED	R/W	X	
2	WDT	R/W	X	WDT (Watchdog) Line Mask bit register 0: WDT (Watchdog) line is enabled. An interrupt is generated on INT line 1: WDT (Watchdog) line is masked. No interrupt is generated on INT line
1	RTC_TIMER	R/W	X	RTC_TIMER Line Mask bit register 0: RTC_TIMER line is enabled. An interrupt is generated on INT line 1: RTC_TIMER line is masked. No interrupt is generated on INT line
0	RTC_ALARM	R/W	X	RTC_ALARM Line Mask bit register 0: RTC_ALARM line is enabled. An interrupt is generated on INT line 1: RTC_ALARM line is masked. No interrupt is generated on INT line

3.10.6 INT2_LINE_STATE Register (Address = 217h) [reset = 0h]

INT2_LINE_STATE is shown in Figure 3-126 and described in Table 3-136.

Return to Summary Table.

Interrupt source line state Register #2
RESET register domain: HWRST

Figure 3-126. INT2_LINE_STATE Register

7	6	5	4	3	2	1	0
RESERVED	SHORT	RESERVED	RESET_IN	RESERVED	WDT	RTC_TIMER	RTC_ALARM
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-136. INT2_LINE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SHORT	R	0h	SHORT line state register 0: SHORT line is equal to 0 1: SHORT line is equal to 1
5	RESERVED	R	0h	
4	RESET_IN	R	0h	RESET_IN line state register 0: RESET_IN line is equal to 0 1: RESET_IN line is equal to 1
3	RESERVED	R	0h	
2	WDT	R	0h	WDT line state register 0: WDT line is equal to 0 1: WDT line is equal to 1
1	RTC_TIMER	R	0h	RTC_TIMER line state register 0: RTC_TIMER line is equal to 0 1: RTC_TIMER line is equal to 1
0	RTC_ALARM	R	0h	RTC_ALARM line state register 0: RTC_ALARM line is equal to 0 1: RTC_ALARM line is equal to 1

3.10.7 INT3_STATUS Register (Address = 21Ah) [reset = 0h]

INT3_STATUS is shown in Figure 3-127 and described in Table 3-137.

Return to Summary Table.

Interrupt Status Register #3
The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR)
RESET register domain: HWRST

Figure 3-127. INT3_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0
C-0h					C-0h	C-0h	C-0h

Table 3-137. INT3_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	C	0h	
2	GPADC_EOC_SW	C	0h	GPADC_EOC_SW status bit register associated (internal event) 0: no detection 1: Rising or falling edge are detected
1	GPADC_AUTO_1	C	0h	GPADC_AUTO_1 status bit register (internal event) 0: no detection 1: Rising edge is detected
0	GPADC_AUTO_0	C	0h	GPADC_AUTO_0 status bit register (Internal event) 0: no detection 1: Rising edge is detected

3.10.8 INT3_MASK Register (Address = 21Bh) [reset = X]

INT3_MASK is shown in Figure 3-128 and described in Table 3-138.

Return to Summary Table.

Interrupt Line Mask Register #3
RESET register domain: HWRST

Figure 3-128. INT3_MASK Register

7	6	5	4	3	2	1	0
RESERVED					GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0
R/W-X					R/W-X	R/W-X	R/W-X

Table 3-138. INT3_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	X	
2	GPADC_EOC_SW	R/W	X	GPADC_EOC_SW Line Mask bit register (Internal event) 0: GPADC_EOC_SW line is enabled. An interrupt is generated on INT line 1: GPADC_EOC_SW line is masked. No interrupt is generated on INT line
1	GPADC_AUTO_1	R/W	X	GPADC_AUTO_1 Line Mask bit register (Internal event) 0: GPADC_AUTO_1 line is enabled. An interrupt is generated on INT line 1: GPADC_AUTO_1 line is masked. No interrupt is generated on INT line
0	GPADC_AUTO_0	R/W	X	GPADC_AUTO_0 Line Mask bit register (Internal event) 0: GPADC_AUTO_0 line is enabled. An interrupt is generated on INT line 1: GPADC_AUTO_0 line is masked. No interrupt is generated on INT line

3.10.9 INT3_LINE_STATE Register (Address = 21Ch) [reset = 0h]

INT3_LINE_STATE is shown in Figure 3-129 and described in Table 3-139.

Return to Summary Table.

Interrupt source line state Register #3
RESET register domain: HWRST

Figure 3-129. INT3_LINE_STATE Register

7	6	5	4	3	2	1	0
RESERVED					GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0
R-0h					R-0h	R-0h	R-0h

Table 3-139. INT3_LINE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	GPADC_EOC_SW	R	0h	GPADC_EOC_SW line state register (Internal event) 0: GPADC_EOC_SW line is equal to 0 1: GPADC_EOC_SW line is equal to 1
1	GPADC_AUTO_1	R	0h	GPADC_AUTO_1 line state register (internal event) 0: GPADC_AUTO_1 line is equal to 0 1: GPADC_AUTO_1 line is equal to 1
0	GPADC_AUTO_0	R	0h	GPADC_AUTO_0 line state register (Internal event) 0: GPADC_AUTO_0 line is equal to 0 1: GPADC_AUTO_0 line is equal to 1

3.10.10 INT4_STATUS Register (Address = 21Fh) [reset = 0h]

INT4_STATUS is shown in Figure 3-130 and described in Table 3-140.

Return to Summary Table.

Interrupt Status Register #4
The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR)
RESET register domain: HWRST

Figure 3-130. INT4_STATUS Register

7	6	5	4	3	2	1	0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
C-0h	C-0h	C-0h	C-0h	C-0h	C-0h	C-0h	C-0h

Table 3-140. INT4_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7	C	0h	GPIO_7 status bit register associated to GPIO_7 pin 0: no detection 1: Rising or Falling edge are detected
6	GPIO_6	C	0h	GPIO_6 status bit register associated to GPIO_6 pin 0: no detection 1: Rising or Falling edge are detected
5	GPIO_5	C	0h	GPIO_5 status bit register associated to GPIO_5 pin 0: no detection 1: Rising or Falling edge are detected
4	GPIO_4	C	0h	GPIO_4 status bit register associated to GPIO_4 pin 0: no detection 1: Rising or Falling edge are detected
3	GPIO_3	C	0h	GPIO_3 status bit register associated to GPIO_3 pin 0: no detection 1: Rising or Falling edge are detected
2	GPIO_2	C	0h	GPIO_2 status bit register associated to GPIO_2 pin 0: no detection 1: Rising or Falling edge are detected
1	GPIO_1	C	0h	GPIO_1 status bit register associated to GPIO_1 pin 0: no detection 1: Rising or Falling edge are detected
0	GPIO_0	C	0h	GPIO_0 status bit register associated to GPIO_0 pin 0: no detection 1: Rising or Falling edge are detected

3.10.11 INT4_MASK Register (Address = 220h) [reset = X]

INT4_MASK is shown in Figure 3-131 and described in Table 3-141.

Return to Summary Table.

Interrupt Line Mask Register #4
RESET register domain: HWRST

Figure 3-131. INT4_MASK Register

7	6	5	4	3	2	1	0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 3-141. INT4_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7	R/W	X	GPIO_7 Line Mask bit register 0: GPIO_7 line is enabled. An interrupt is generated on INT line 1: GPIO_7 line is masked. No interrupt is generated on INT line
6	GPIO_6	R/W	X	GPIO_6 Line Mask bit register 0: GPIO_6 line is enabled. An interrupt is generated on INT line 1: GPIO_6 line is masked. No interrupt is generated on INT line
5	GPIO_5	R/W	X	GPIO_5 Line Mask bit register 0: GPIO_5 line is enabled. An interrupt is generated on INT line 1: GPIO_5 line is masked. No interrupt is generated on INT line
4	GPIO_4	R/W	X	GPIO_4 Line Mask bit register 0: GPIO_4 line is enabled. An interrupt is generated on INT line 1: GPIO_4 line is masked. No interrupt is generated on INT line
3	GPIO_3	R/W	X	GPIO_3 Line Mask bit register 0: GPIO_3 line is enabled. An interrupt is generated on INT line 1: GPIO_3 line is masked. No interrupt is generated on INT line
2	GPIO_2	R/W	X	GPIO_2 Line Mask bit register 0: GPIO_2 line is enabled. An interrupt is generated on INT line 1: GPIO_2 line is masked. No interrupt is generated on INT line
1	GPIO_1	R/W	X	GPIO_1 Line Mask bit register 0: GPIO_1 line is enabled. An interrupt is generated on INT line 1: GPIO_1 line is masked. No interrupt is generated on INT line
0	GPIO_0	R/W	X	GPIO_0 Line Mask bit register 0: GPIO_0 line is enabled. An interrupt is generated on INT line 1: GPIO_0 line is masked. No interrupt is generated on INT line

3.10.12 INT4_LINE_STATE Register (Address = 221h) [reset = 0h]

INT4_LINE_STATE is shown in Figure 3-132 and described in Table 3-142.

Return to Summary Table.

Interrupt source line state Register #4
RESET register domain: HWRST

Figure 3-132. INT4_LINE_STATE Register

7	6	5	4	3	2	1	0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-142. INT4_LINE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7	R	0h	GPIO_7 line state register 0: GPIO_7 line is equal to 0 1: GPIO_7 line is equal to 1
6	GPIO_6	R	0h	GPIO_6 line state register 0: GPIO_6 line is equal to 0 1: GPIO_6 line is equal to 1
5	GPIO_5	R	0h	GPIO_5 line state register 0: GPIO_5 line is equal to 0 1: GPIO_5 line is equal to 1
4	GPIO_4	R	0h	GPIO_4 line state register 0: GPIO_4 line is equal to 0 1: GPIO_4 line is equal to 1
3	GPIO_3	R	0h	GPIO_3 line state register 0: GPIO_3 line is equal to 0 1: GPIO_3 line is equal to 1
2	GPIO_2	R	0h	GPIO_2 line state register 0: GPIO_2 line is equal to 0 1: GPIO_2 line is equal to 1
1	GPIO_1	R	0h	GPIO_1 line state register 0: GPIO_1 line is equal to 0 1: GPIO_1 line is equal to 1
0	GPIO_0	R	0h	GPIO_0 line state register 0: GPIO_0 line is equal to 0 1: GPIO_0 line is equal to 1

3.10.13 INT4_EDGE_DETECT1 Register (Address = 222h) [reset = FFh]

INT4_EDGE_DETECT1 is shown in Figure 3-133 and described in Table 3-143.

Return to Summary Table.

Interrupt Edge Detection Register #4.1
RESET register domain: HWRST

Figure 3-133. INT4_EDGE_DETECT1 Register

7	6	5	4	3	2	1	0
GPIO_3_RISING	GPIO_3_FALLING	GPIO_2_RISING	GPIO_2_FALLING	GPIO_1_RISING	GPIO_1_FALLING	GPIO_0_RISING	GPIO_0_FALLING
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 3-143. INT4_EDGE_DETECT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_3_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
6	GPIO_3_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
5	GPIO_2_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
4	GPIO_2_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
3	GPIO_1_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
2	GPIO_1_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
1	GPIO_0_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
0	GPIO_0_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)

3.10.14 INT4_EDGE_DETECT2 Register (Address = 223h) [reset = FFh]

INT4_EDGE_DETECT2 is shown in Figure 3-134 and described in Table 3-144.

Return to Summary Table.

Interrupt Edge Detection Register #4.2
RESET register domain: HWRST

Figure 3-134. INT4_EDGE_DETECT2 Register

7	6	5	4	3	2	1	0
GPIO_7_RISING	GPIO_7_FALLING	GPIO_6_RISING	GPIO_6_FALLING	GPIO_5_RISING	GPIO_5_FALLING	GPIO_4_RISING	GPIO_4_FALLING
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 3-144. INT4_EDGE_DETECT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
6	GPIO_7_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
5	GPIO_6_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
4	GPIO_6_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
3	GPIO_5_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
2	GPIO_5_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
1	GPIO_4_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
0	GPIO_4_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)

3.10.15 INT_CTRL Register (Address = 224h) [reset = 0h]

INT_CTRL is shown in Figure 3-135 and described in Table 3-145.

Return to Summary Table.

Interrupt control register
RESET register domain: HWRST

Figure 3-135. INT_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					INT_PENDING	RESERVED	INT_CLEAR
R-0h					R/W-0h	R-0h	R/W-0h

Table 3-145. INT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	INT_PENDING	R/W	0h	Pending interrupt latching feature selection (interrupt latched in case of new event before clearing on same line) 0: Enabled (default) 1: Not enabled
1	RESERVED	R	0h	
0	INT_CLEAR	R/W	0h	Select the way to clear the interrupt bits (will be apply to ALL the bits) 0: Clear-on-Write - Interrupts cleared by writing 1. This method is bit based (default) 1: Clear-on-Read - Interrupts cleared on read

3.11 FUNC_ID Registers

Table 3-146 lists the memory-mapped registers for the FUNC_ID. All register offset addresses not listed in Table 3-146 should be considered as reserved locations and the register contents should not be modified.

Table 3-146. FUNC_ID Registers

Address	Acronym	Register Name	Section
24Fh	VENDOR_ID_LSB	Vendor ID Register (LSB)	Section 3.11.1
250h	VENDOR_ID_MSB	Vendor ID Register (MSB)	Section 3.11.2
251h	PRODUCT_ID_LSB	Product ID Register (LSB)	Section 3.11.3
252h	PRODUCT_ID_MSB	Product ID Register (MSB)	Section 3.11.4

3.11.1 VENDOR_ID_LSB Register (Address = 24Fh) [reset = 51h]

VENDOR_ID_LSB is shown in Figure 3-136 and described in Table 3-147.

Return to Summary Table.

Vendor ID Register (LSB)
RESET register domain: HWRST

Figure 3-136. VENDOR_ID_LSB Register

7	6	5	4	3	2	1	0
VENDOR_ID							
R-51h							

Table 3-147. VENDOR_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VENDOR_ID	R	51h	Texas Instruments USB Vendor ID (8 LSBs) - Default value: 0x51

3.11.2 VENDOR_ID_MSB Register (Address = 250h) [reset = 4h]

VENDOR_ID_MSB is shown in Figure 3-137 and described in Table 3-148.

Return to Summary Table.

Vendor ID Register (MSB)
RESET register domain: HWRST

Figure 3-137. VENDOR_ID_MSB Register

7	6	5	4	3	2	1	0
VENDOR_ID							
R-4h							

Table 3-148. VENDOR_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VENDOR_ID	R	4h	Texas Instruments USB Vendor ID (8 MSBs) - Default value: 0x04

3.11.3 PRODUCT_ID_LSB Register (Address = 251h) [reset = 39h]

PRODUCT_ID_LSB is shown in Figure 3-138 and described in Table 3-149.

Return to Summary Table.

Product ID Register (LSB)
RESET register domain: HWRST

Figure 3-138. PRODUCT_ID_LSB Register

7	6	5	4	3	2	1	0
PRODUCT_ID							
R-39h							

Table 3-149. PRODUCT_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRODUCT_ID	R	39h	Texas Instruments Product ID (8 LSBs) - Default value: 0x39

3.11.4 PRODUCT_ID_MSB Register (Address = 252h) [reset = 90h]

PRODUCT_ID_MSB is shown in Figure 3-139 and described in Table 3-150.

Return to Summary Table.

Product ID Register (MSB)
RESET register domain: HWRST

Figure 3-139. PRODUCT_ID_MSB Register

7	6	5	4	3	2	1	0
PRODUCT_ID							
R-90h							

Table 3-150. PRODUCT_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRODUCT_ID	R	90h	Texas Instruments Product ID (8 MSBs) - Default value: 0x90

3.12 FUNC_GPIO Registers

Table 3-151 lists the memory-mapped registers for the FUNC_GPIO. All register offset addresses not listed in Table 3-151 should be considered as reserved locations and the register contents should not be modified.

Table 3-151. FUNC_GPIO Registers

Address	Acronym	Register Name	Section
280h	GPIO_DATA_IN	GPIO Data Input Register	Section 3.12.1
281h	GPIO_DATA_DIR	GPIO Data Direction Register	Section 3.12.2
282h	GPIO_DATA_OUT	GPIO Data Output Register	Section 3.12.3
283h	GPIO_DEBOUNCE_EN	GPIO Debounce Enable Register	Section 3.12.4
284h	GPIO_CLEAR_DATA_OUT	GPIO Clear Data Out Register	Section 3.12.5
285h	GPIO_SET_DATA_OUT	GPIO Set Data Out Register	Section 3.12.6
286h	PU_PD_GPIO_CTRL1	Pull-Up Pull-Down Control Register 1	Section 3.12.7
287h	PU_PD_GPIO_CTRL2	Pull-Up Pull-Down Control Register 2	Section 3.12.8
288h	OD_OUTPUT_GPIO_CTRL	Open Drain Control Register	Section 3.12.9

3.12.1 GPIO_DATA_IN Register (Address = 280h) [reset = 0h]

GPIO_DATA_IN is shown in Figure 3-140 and described in Table 3-152.

Return to Summary Table.

GPIO Data input register
RESET register domain: HWRST

Figure 3-140. GPIO_DATA_IN Register

7	6	5	4	3	2	1	0
GPIO_7_IN	GPIO_6_IN	GPIO_5_IN	GPIO_4_IN	GPIO_3_IN	GPIO_2_IN	GPIO_1_IN	GPIO_0_IN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-152. GPIO_DATA_IN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7_IN	R	0h	Data read value (in) of the GPIO_7
6	GPIO_6_IN	R	0h	Data read value (in) of the GPIO_6
5	GPIO_5_IN	R	0h	Data read value (in) of the GPIO_5
4	GPIO_4_IN	R	0h	Data read value (in) of the GPIO_4
3	GPIO_3_IN	R	0h	Data read value (in) of the GPIO_3
2	GPIO_2_IN	R	0h	Data read value (in) of the GPIO_2
1	GPIO_1_IN	R	0h	Data read value (in) of the GPIO_1
0	GPIO_0_IN	R	0h	Data read value (in) of the GPIO_0

3.12.2 GPIO_DATA_DIR Register (Address = 281h) [reset = 0h]

GPIO_DATA_DIR is shown in Figure 3-141 and described in Table 3-153.

Return to Summary Table.

GPIO data direction
RESET register domain: HWRST

Figure 3-141. GPIO_DATA_DIR Register

7	6	5	4	3	2	1	0
GPIO_7_DIR	GPIO_6_DIR	GPIO_5_DIR	GPIO_4_DIR	GPIO_3_DIR	GPIO_2_DIR	GPIO_1_DIR	GPIO_0_DIR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-153. GPIO_DATA_DIR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
6	GPIO_6_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
5	GPIO_5_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
4	GPIO_4_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
3	GPIO_3_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
2	GPIO_2_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
1	GPIO_1_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
0	GPIO_0_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration

3.12.3 GPIO_DATA_OUT Register (Address = 282h) [reset = 0h]

GPIO_DATA_OUT is shown in Figure 3-142 and described in Table 3-154.

Return to Summary Table.

GPIO Data output register
RESET register domain: HWRST

Figure 3-142. GPIO_DATA_OUT Register

7	6	5	4	3	2	1	0
GPIO_7_OUT	GPIO_6_OUT	GPIO_5_OUT	GPIO_4_OUT	GPIO_3_OUT	GPIO_2_OUT	GPIO_1_OUT	GPIO_0_OUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-154. GPIO_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7_OUT	R/W	0h	Data write value (out) of the GPIO_7
6	GPIO_6_OUT	R/W	0h	Data write value (out) of the GPIO_6
5	GPIO_5_OUT	R/W	0h	Data write value (out) of the GPIO_5
4	GPIO_4_OUT	R/W	0h	Data write value (out) of the GPIO_4
3	GPIO_3_OUT	R/W	0h	Data write value (out) of the GPIO_3
2	GPIO_2_OUT	R/W	0h	Data write value (out) of the GPIO_2
1	GPIO_1_OUT	R/W	0h	Data write value (out) of the GPIO_1
0	GPIO_0_OUT	R/W	0h	Data write value (out) of the GPIO_0

3.12.4 GPIO_DEBOUNCE_EN Register (Address = 283h) [reset = 0h]

GPIO_DEBOUNCE_EN is shown in Figure 3-143 and described in Table 3-155.

Return to Summary Table.

GPIO Debounce enable register
RESET register domain: HWRST

Figure 3-143. GPIO_DEBOUNCE_EN Register

7	6	5	4	3	2	1	0
GPIO_7_DEBOUNCE_EN	GPIO_6_DEBOUNCE_EN	GPIO_5_DEBOUNCE_EN	GPIO_4_DEBOUNCE_EN	GPIO_3_DEBOUNCE_EN	GPIO_2_DEBOUNCE_EN	GPIO_1_DEBOUNCE_EN	GPIO_0_DEBOUNCE_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-155. GPIO_DEBOUNCE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
6	GPIO_6_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
5	GPIO_5_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
4	GPIO_4_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
3	GPIO_3_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
2	GPIO_2_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
1	GPIO_1_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
0	GPIO_0_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled

3.12.5 GPIO_CLEAR_DATA_OUT Register (Address = 284h) [reset = 0h]

GPIO_CLEAR_DATA_OUT is shown in Figure 3-144 and described in Table 3-156.

Return to Summary Table.

GPIO Clear Data Out Register
RESET register domain: HWRST

Figure 3-144. GPIO_CLEAR_DATA_OUT Register

7	6	5	4	3	2	1	0
GPIO_7_CLEAR_DATA_OUT	GPIO_6_CLEAR_DATA_OUT	GPIO_5_CLEAR_DATA_OUT	GPIO_4_CLEAR_DATA_OUT	GPIO_3_CLEAR_DATA_OUT	GPIO_2_CLEAR_DATA_OUT	GPIO_1_CLEAR_DATA_OUT	GPIO_0_CLEAR_DATA_OUT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 3-156. GPIO_CLEAR_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_7 bit 1: CLEAR GPIO_7 bit
6	GPIO_6_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_6 bit 1: CLEAR GPIO_6 bit
5	GPIO_5_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_5 bit 1: CLEAR GPIO_5 bit
4	GPIO_4_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_4 bit 1: CLEAR GPIO_4 bit
3	GPIO_3_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_3 bit 1: CLEAR GPIO_3 bit
2	GPIO_2_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_2 bit 1: CLEAR GPIO_2 bit
1	GPIO_1_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_1 bit 1: CLEAR GPIO_1 bit
0	GPIO_0_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_0 bit 1: CLEAR GPIO_0 bit

3.12.6 GPIO_SET_DATA_OUT Register (Address = 285h) [reset = 0h]

GPIO_SET_DATA_OUT is shown in Figure 3-145 and described in Table 3-157.

Return to Summary Table.

GPIO Set Data Out Register
RESET register domain: HWRST

Figure 3-145. GPIO_SET_DATA_OUT Register

7	6	5	4	3	2	1	0
GPIO_7_SET_DATA_OUT	GPIO_6_SET_DATA_OUT	GPIO_5_SET_DATA_OUT	GPIO_4_SET_DATA_OUT	GPIO_3_SET_DATA_OUT	GPIO_2_SET_DATA_OUT	GPIO_1_SET_DATA_OUT	GPIO_0_SET_DATA_OUT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 3-157. GPIO_SET_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_7_SET_DATA_OUT	W	0h	0: no action on GPIO_7 bit 1: SET GPIO_7 bit
6	GPIO_6_SET_DATA_OUT	W	0h	0: no action on GPIO_6 bit 1: SET GPIO_6 bit
5	GPIO_5_SET_DATA_OUT	W	0h	0: no action on GPIO_5 bit 1: SET GPIO_5 bit
4	GPIO_4_SET_DATA_OUT	W	0h	0: no action on GPIO_4 bit 1: SET GPIO_4 bit
3	GPIO_3_SET_DATA_OUT	W	0h	0: no action on GPIO_3 bit 1: SET GPIO_3 bit
2	GPIO_2_SET_DATA_OUT	W	0h	0: no action on GPIO_2 bit 1: SET GPIO_2 bit
1	GPIO_1_SET_DATA_OUT	W	0h	0: no action on GPIO_1 bit 1: SET GPIO_1 bit
0	GPIO_0_SET_DATA_OUT	W	0h	0: no action on GPIO_0 bit 1: SET GPIO_0 bit

3.12.7 PU_PD_GPIO_CTRL1 Register (Address = 286h) [reset = X]

PU_PD_GPIO_CTRL1 is shown in Figure 3-146 and described in Table 3-158.

Return to Summary Table.

Pull-up Pull-down control register
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the GPIO direction and type (Open drain / Push-Pull)

Figure 3-146. PU_PD_GPIO_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_3_PD	GPIO_2_PU	GPIO_2_PD	GPIO_1_PU	GPIO_1_PD	RESERVED	GPIO_0_PD
R-0h	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R-0h	R/W-X

Table 3-158. PU_PD_GPIO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_3_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled
5	GPIO_2_PU	R/W	X	0: Pull-up not enabled 1: Pull-up enabled
4	GPIO_2_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled
3	GPIO_1_PU	R/W	X	0: Pull-up not enabled 1: Pull-up enabled
2	GPIO_1_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled
1	RESERVED	R	0h	
0	GPIO_0_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)

3.12.8 PU_PD_GPIO_CTRL2 Register (Address = 287h) [reset = X]

PU_PD_GPIO_CTRL2 is shown in Figure 3-147 and described in Table 3-159.

Return to Summary Table.

Pull-up Pull-down control register
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the GPIO direction and type (Open drain / Push-Pull)

Figure 3-147. PU_PD_GPIO_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_7_PD	GPIO_6_PU	GPIO_6_PD	GPIO_5_PU	GPIO_5_PD	GPIO_4_PU	GPIO_4_PD
R-0h	R/W-X	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h

Table 3-159. PU_PD_GPIO_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_7_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)
5	GPIO_6_PU	R/W	0h	0: Pull-up not enabled (default) 1: Pull-up enabled
4	GPIO_6_PD	R/W	1h	0: Pull-down not enabled 1: Pull-down enabled (default)
3	GPIO_5_PU	R/W	0h	0: Pull-up not enabled (default) 1: Pull-up enabled
2	GPIO_5_PD	R/W	1h	0: Pull-down not enabled 1: Pull-down enabled (default)
1	GPIO_4_PU	R/W	0h	0: Pull-up not enabled (default) 1: Pull-up enabled
0	GPIO_4_PD	R/W	1h	0: Pull-down not enabled 1: Pull-down enabled (default)

3.12.9 OD_OUTPUT_GPIO_CTRL Register (Address = 288h) [reset = 0h]

OD_OUTPUT_GPIO_CTRL is shown in Figure 3-148 and described in Table 3-160.

Return to Summary Table.

Open Drain control register
RESET register domain: HWRST
Note: It is user responsibility to take care about the GPIO direction and type (Open drain / Push-Pull) versus the pull-up/pull-down selections

Figure 3-148. OD_OUTPUT_GPIO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO_5_OD	RESERVED	RESERVED	GPIO_2_OD	GPIO_1_OD	RESERVED
R-0h	R-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h	R-0h

Table 3-160. OD_OUTPUT_GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	GPIO_5_OD	R/W	0h	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	GPIO_2_OD	R/W	0h	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)
1	GPIO_1_OD	R/W	0h	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)
0	RESERVED	R	0h	

3.13 FUNC_GPADC Registers

Table 3-161 lists the memory-mapped registers for the FUNC_GPADC. All register offset addresses not listed in Table 3-161 should be considered as reserved locations and the register contents should not be modified.

Table 3-161. FUNC_GPADC Registers

Address	Acronym	Register Name	Section
2C0h	GPADC_CTRL1	GPADC Control Register	Section 3.13.1
2C2h	GPADC_FLUSH	GPADC FLUSH Register	Section 3.13.2
2C3h	GPADC_AUTO_CTRL	GPADC Automatic Control Register (Periodic)	Section 3.13.3
2C4h	GPADC_STATUS	GPADC Status Register	Section 3.13.4
2C5h	GPADC_FLUSH_EN	GPADC FLUSH Enable Register	Section 3.13.5
2C7h	GPADC_STUCK	GPADC Stuck Status Register	Section 3.13.6
2C8h	GPADC_AUTO_SELECT	GPADC Automatic (Periodic) Channel Selection Register	Section 3.13.7
2C9h	GPADC_AUTO_CONV0_LSB	GPADC Data Results of the Automatic (Periodic) Conversion Register 0 (LSB)	Section 3.13.8
2CAh	GPADC_AUTO_CONV0_MSB	GPADC Data Results of the Automatic (Periodic) Conversion Register 0 (MSB)	Section 3.13.9
2CBh	GPADC_AUTO_CONV1_LSB	GPADC Data Results of the Automatic (Periodic) Conversion Register 1 (LSB)	Section 3.13.10
2CCh	GPADC_AUTO_CONV1_MSB	GPADC Data Results of the Automatic (Periodic) Conversion Register 1 (MSB)	Section 3.13.11
2CDh	GPADC_SW_SELECT	GPADC Software Channel Selection Register for Conversion 0	Section 3.13.12
2CEh	GPADC_SW_CONV0_LSB	GPADC Data Results of the Software Conversion Register 0 (LSB)	Section 3.13.13
2CFh	GPADC_SW_CONV0_MSB	GPADC Data Results of the Software Conversion Register 0 (MLSB)	Section 3.13.14
2D0h	GPADC_THRES_CONV0_LSB	LSB of Threshold Reference Register (To be Compared to the Conversion 0 Results)	Section 3.13.15
2D1h	GPADC_THRES_CONV0_MSB	MSB of Threshold Reference Register (To be Compared to the Conversion 0 Results)	Section 3.13.16
2D2h	GPADC_THRES_CONV1_LSB	LSB of Threshold Reference Register (To be Compared to the Conversion 1 Results)	Section 3.13.17
2D3h	GPADC_THRES_CONV1_MSB	MSB of Threshold Reference Register (To be Compared to the Conversion 1 Results)	Section 3.13.18
2D4h	GPADC_SMPS_ILMONITOR_EN	GPADC SMPS Selection Register for Current Measurement	Section 3.13.19
2D5h	GPADC_SMPS_VSEL_MONITORING	GPADC SMPS Voltage Monitoring Register	Section 3.13.20

3.13.1 GPADC_CTRL1 Register (Address = 2C0h) [reset = 0h]

GPADC_CTRL1 is shown in Figure 3-149 and described in Table 3-162.

Return to Summary Table.

GPADC Control Register
RESET register domain: HWRST

Figure 3-149. GPADC_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	CURRENT_SRC_CH3		CURRENT_SRC_CH0		RESERVED	GPADC_FORCE
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h

Table 3-162. GPADC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	RESERVED	R/W	0h	
5-4	CURRENT_SRC_CH3	R/W	0h	Current Source selection for GPADC Channel 3 input 00: 0uA 01: 10uA 10: 400uA 11: 800uA
3-2	CURRENT_SRC_CH0	R/W	0h	Current Source selection for GPADC Channel 0 input 00: 0uA (default) 01: 5uA 10: 15uA 11: 20uA
1	RESERVED	R/W	0h	
0	GPADC_FORCE	R/W	0h	Force GPADC module to active (Always On) 0: GPADC OFF. The GPADC is controlled by conversion request in all modes (default) 1: GPADC ON (Always ON - will allow conversion latency)

3.13.2 GPADC_FLUSH Register (Address = 2C2h) [reset = 0h]

GPADC_FLUSH is shown in Figure 3-150 and described in Table 3-163.

Return to Summary Table.

GPADC FLUSH Register
RESET register domain: HWRST

Figure 3-150. GPADC_FLUSH Register

7	6	5	4	3	2	1	0
RESERVED						EXTEND_DELAY	FLUSH
R-0h						R/W-0h	R/W-0h

Table 3-163. GPADC_FLUSH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	EXTEND_DELAY	R/W	0h	Extend delay before SW conversion. 0: 0 µs (default) 1: 450 µs
0	FLUSH	R/W	0h	Flush the conversion result of the GPADC when it is stuck in a busy state. This bit can be toggled to 1 and back to 0 to recover the GPADC operation.

3.13.3 GPADC_AUTO_CTRL Register (Address = 2C3h) [reset = 0h]

GPADC_AUTO_CTRL is shown in Figure 3-151 and described in Table 3-164.

Return to Summary Table.

GPADC Automatic Control register (Periodic)
RESET register domain: HWRST

Figure 3-151. GPADC_AUTO_CTRL Register

7	6	5	4	3	2	1	0
SHUTDOWN_CONV1	SHUTDOWN_CONV0	AUTO_CONV1_EN	AUTO_CONV0_EN	COUNTER_CONV			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

Table 3-164. GPADC_AUTO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SHUTDOWN_CONV1	R/W	0h	Shut down control based on Auto conversions (only for CONV1) 0: shut down not enabled (default) 1: enable shut down of the platform if interrupt is not clear within delay time
6	SHUTDOWN_CONV0	R/W	0h	Shut down control based on Auto conversions (only for CONV0) 0: shut down not enabled (default) 1: enable shut down of the platform if interrupt is not clear within delay time
5	AUTO_CONV1_EN	R/W	0h	Automatic Conversion 1 enabling 0: Automatic Conversion 1 is not enable (defaults) 1: Automatic Conversion 1 is enabled
4	AUTO_CONV0_EN	R/W	0h	Automatic Conversion 0 enabling 0: Automatic Conversion 0 is not enable (defaults) 1: Automatic Conversion 0 is enabled
3-0	COUNTER_CONV	R/W	0h	Time slot between conversions (RT and SW modes) or two consecutive conversions (Auto mode) 0000: 1/32s (default) 0001: 1/16s 0010: 1/8s 1110: 512s 1111: 1024s

3.13.4 GPADC_STATUS Register (Address = 2C4h) [reset = 10h]

GPADC_STATUS is shown in Figure 3-152 and described in Table 3-165.

Return to Summary Table.

GPADC Status Register
RESET register domain: HWRST

Figure 3-152. GPADC_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			GPADC_AVAILABLE	RESERVED			
R-0h			R-1h	R-0h			

Table 3-165. GPADC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	GPADC_AVAILABLE	R	1h	GPADC status 0: Conversions not completed. GPADC not available (busy) 1: Conversions completed. GPADC available
3-0	RESERVED	R	0h	

3.13.5 GPADC_FLUSH_EN Register (Address = 2C5h) [reset = 0h]

GPADC_FLUSH_EN is shown in Figure 3-153 and described in Table 3-166.

Return to Summary Table.

GPADC FLUSH Enable register
RESET register domain: HWRST

Figure 3-153. GPADC_FLUSH_EN Register

7	6	5	4	3	2	1	0
FLUSH_EN	RESERVED			RESERVED			
R/W-0h	R-0h			R/W-0h			

Table 3-166. GPADC_FLUSH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLUSH_EN	R/W	0h	GPADC Flush Enable
6-4	RESERVED	R	0h	
3-0	RESERVED	R/W	0h	

3.13.6 GPADC_STUCK Register (Address = 2C7h) [reset = 0h]

GPADC_STUCK is shown in Figure 3-154 and described in Table 3-167.

Return to Summary Table.

GPADC stuck status
RESET register domain: HWRST

Figure 3-154. GPADC_STUCK Register

7	6	5	4	3	2	1	0
RESERVED			STUCK	RESERVED			
R-0h			R-0h	R-0h			

Table 3-167. GPADC_STUCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STUCK	R	0h	GPADC stuck status
3-0	RESERVED	R	0h	

3.13.7 GPADC_AUTO_SELECT Register (Address = 2C8h) [reset = 0h]

GPADC_AUTO_SELECT is shown in Figure 3-155 and described in Table 3-168.

Return to Summary Table.

GPADC Automatic (Periodic) Channel selection for Conversion 0 and Conversion 1
RESET register domain: HWRST
Note: All Selected channels are queued and converted from channel 0 to 11
The first (lower) converted channel results is placed in GPADC_AUTO_CONV0 register and the second one is placed in GPADC_AUTO_CONV1 register. It is why it is recommended to put the lower channel to convert in AUTO_CONV0_SEL and the higher channel to convert in AUTO_CONV1_SEL.

Figure 3-155. GPADC_AUTO_SELECT Register

7	6	5	4	3	2	1	0
AUTO_CONV1_SEL				AUTO_CONV0_SEL			
R/W-0h				R/W-0h			

Table 3-168. GPADC_AUTO_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	AUTO_CONV1_SEL	R/W	0h	Channel selection for Conversion 1 in Automatic mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 1110: GPADC Channel 14 1111: GPADC Channel 15
3-0	AUTO_CONV0_SEL	R/W	0h	Channel selection for Conversion 0 in Automatic mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 1110: GPADC Channel 14 1111: GPADC Channel 15

3.13.8 GPADC_AUTO_CONV0_LSB Register (Address = 2C9h) [reset = 0h]

GPADC_AUTO_CONV0_LSB is shown in Figure 3-156 and described in Table 3-169.

Return to Summary Table.

GPADC data results of the Automatic (Periodic) conversion 0 (LSB)
RESET register domain: HWRST

Figure 3-156. GPADC_AUTO_CONV0_LSB Register

7	6	5	4	3	2	1	0
AUTO_CONV0_LSB							
R-0h							

Table 3-169. GPADC_AUTO_CONV0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_CONV0_LSB	R	0h	AUTO Conversion 0 data result (LSB) <7:0>

3.13.9 GPADC_AUTO_CONV0_MSB Register (Address = 2CAh) [reset = 0h]

GPADC_AUTO_CONV0_MSB is shown in Figure 3-157 and described in Table 3-170.

Return to Summary Table.

GPADC data results of the Automatic (Periodic) conversion 0 (MSB)
RESET register domain: HWRST

Figure 3-157. GPADC_AUTO_CONV0_MSB Register

7	6	5	4	3	2	1	0
RESERVED				AUTO_CONV0_MSB			
R-0h				R-0h			

Table 3-170. GPADC_AUTO_CONV0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	AUTO_CONV0_MSB	R	0h	AUTO Conversion 0 data result (MSB) <11:8>

3.13.10 GPADC_AUTO_CONV1_LSB Register (Address = 2CBh) [reset = 0h]

GPADC_AUTO_CONV1_LSB is shown in Figure 3-158 and described in Table 3-171.

Return to Summary Table.

GPADC data results of the Automatic (Periodic) conversion 1 (LSB)
RESET register domain: HWRST

Figure 3-158. GPADC_AUTO_CONV1_LSB Register

7	6	5	4	3	2	1	0
AUTO_CONV1_LSB							
R-0h							

Table 3-171. GPADC_AUTO_CONV1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_CONV1_LSB	R	0h	AUTO Conversion 1 data result (LSB) <7:0>

3.13.11 GPADC_AUTO_CONV1_MSB Register (Address = 2CCh) [reset = 0h]

GPADC_AUTO_CONV1_MSB is shown in Figure 3-159 and described in Table 3-172.

Return to Summary Table.

GPADC data results of the Automatic (Periodic) conversion 1 (MSB)
RESET register domain: HWRST

Figure 3-159. GPADC_AUTO_CONV1_MSB Register

7	6	5	4	3	2	1	0
RESERVED				AUTO_CONV1_MSB			
R-0h				R-0h			

Table 3-172. GPADC_AUTO_CONV1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	AUTO_CONV1_MSB	R	0h	AUTO Conversion 1 data result (MSB) <11:8>

3.13.12 GPADC_SW_SELECT Register (Address = 2CDh) [reset = 0h]

GPADC_SW_SELECT is shown in Figure 3-160 and described in Table 3-173.

Return to Summary Table.

GPADC Software Channel selection for Conversion 0
RESET register domain: HWRST

Figure 3-160. GPADC_SW_SELECT Register

7	6	5	4	3	2	1	0
SW_CONV_EN	RESERVED		SW_START_CONV0	SW_CONV0_SEL			
R/W-0h	R-0h		R/W-0h	R/W-0h			

Table 3-173. GPADC_SW_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_CONV_EN	R/W	0h	Software Conversion enabling 0: Software Conversion is not enable (defaults) 1: Software Conversion is enabled
6-5	RESERVED	R	0h	
4	SW_START_CONV0	R/W	0h	Toggle bit used by host processor to start a conversion (Conversion0) on selected channel by SW_CONV0_SEL Writing logical 0 in this bit has no effect
3-0	SW_CONV0_SEL	R/W	0h	Channel selection for Conversion 0 in SW mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 1110: GPADC Channel 14 1111: GPADC Channel 15

3.13.13 GPADC_SW_CONV0_LSB Register (Address = 2CEh) [reset = 0h]

GPADC_SW_CONV0_LSB is shown in Figure 3-161 and described in Table 3-174.

Return to Summary Table.

GPADC data results of the Software conversion 0 (LSB)
RESET register domain: HWRST

Figure 3-161. GPADC_SW_CONV0_LSB Register

7	6	5	4	3	2	1	0
SW_CONV0_LSB							
R-0h							

Table 3-174. GPADC_SW_CONV0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SW_CONV0_LSB	R	0h	SW Conversion 0 data result (LSB) <7:0>

3.13.14 GPADC_SW_CONV0_MSB Register (Address = 2CFh) [reset = 0h]

GPADC_SW_CONV0_MSB is shown in Figure 3-162 and described in Table 3-175.

Return to Summary Table.

GPADC data results of the Software conversion 0 (MSB)
RESET register domain: HWRST

Figure 3-162. GPADC_SW_CONV0_MSB Register

7	6	5	4	3	2	1	0
RESERVED				SW_CONV0_MSB			
R-0h				R-0h			

Table 3-175. GPADC_SW_CONV0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	SW_CONV0_MSB	R	0h	SW Conversion 0 data result (MSB) <11:8>

3.13.15 GPADC_THRES_CONV0_LSB Register (Address = 2D0h) [reset = 0h]

GPADC_THRES_CONV0_LSB is shown in Figure 3-163 and described in Table 3-176.

Return to Summary Table.

LSB of Threshold reference to be compared to the Conversion 0 results
RESET register domain: HWRST

Figure 3-163. GPADC_THRES_CONV0_LSB Register

7	6	5	4	3	2	1	0
THRES_CONV0_LSB							
R/W-0h							

Table 3-176. GPADC_THRES_CONV0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRES_CONV0_LSB	R/W	0h	Threshold value for Conversion 0 (LSB) <7:0>

3.13.16 GPADC_THRES_CONV0_MSB Register (Address = 2D1h) [reset = 0h]

GPADC_THRES_CONV0_MSB is shown in Figure 3-164 and described in Table 3-177.

Return to Summary Table.

MSB of Threshold reference to be compared to the Conversion 0 results
RESET register domain: HWRST

Figure 3-164. GPADC_THRES_CONV0_MSB Register

7	6	5	4	3	2	1	0
THRES_CONV0_POL	RESERVED			THRES_CONV0_MSB			
R/W-0h	R-0h			R/W-0h			

Table 3-177. GPADC_THRES_CONV0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THRES_CONV0_POL	R/W	0h	Threshold conversion 0 polarity 0: Interrupt generated if Conversion0 result is above threshold 1: Interrupt generated if Conversion0 result is below threshold
6-4	RESERVED	R	0h	
3-0	THRES_CONV0_MSB	R/W	0h	Threshold value for Conversion 0 (MSB) <11:8>

3.13.17 GPADC_THRES_CONV1_LSB Register (Address = 2D2h) [reset = 0h]

GPADC_THRES_CONV1_LSB is shown in Figure 3-165 and described in Table 3-178.

Return to Summary Table.

LSB of Threshold reference to be compared to the Conversion 1 results
RESET register domain: HWRST

Figure 3-165. GPADC_THRES_CONV1_LSB Register

7	6	5	4	3	2	1	0
THRES_CONV1_LSB							
R/W-0h							

Table 3-178. GPADC_THRES_CONV1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRES_CONV1_LSB	R/W	0h	Threshold value for Conversion 1 (LSB) <7:0>

3.13.18 GPADC_THRES_CONV1_MSB Register (Address = 2D3h) [reset = 0h]

GPADC_THRES_CONV1_MSB is shown in Figure 3-166 and described in Table 3-179.

Return to Summary Table.

MSB of Threshold reference to be compared to the Conversion 1 results
RESET register domain: HWRST

Figure 3-166. GPADC_THRES_CONV1_MSB Register

7	6	5	4	3	2	1	0
THRES_CONV1_POL	RESERVED			THRES_CONV1_MSB			
R/W-0h	R-0h			R/W-0h			

Table 3-179. GPADC_THRES_CONV1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THRES_CONV1_POL	R/W	0h	Threshold conversion 1 polarity 0: Interrupt generated if Conversion0 result is above threshold 1: Interrupt generated if Conversion0 result is below threshold
6-4	RESERVED	R	0h	
3-0	THRES_CONV1_MSB	R/W	0h	Threshold value for Conversion 1 (MSB) <11:8>

3.13.19 GPADC_SMPS_ILMONITOR_EN Register (Address = 2D4h) [reset = 7h]

GPADC_SMPS_ILMONITOR_EN is shown in Figure 3-167 and described in Table 3-180.

Return to Summary Table.

GPADC SMPS selection for current measurement
RESET register domain: HWRST

Figure 3-167. GPADC_SMPS_ILMONITOR_EN Register

7	6	5	4	3	2	1	0
RESERVED	SMPS_COMPMODE	SMPS_ILMON_EN	SMPS_ILMON_VADC_MEAS_EN	SMPS_ILMON_SEL			
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-7h			

Table 3-180. GPADC_SMPS_ILMONITOR_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SMPS_COMPMODE	R/W	0h	ILMON comparator enable. This bit can be written 1 ONLY if SMPS_ILMON_EN bit is already 1. If SMPS_ILMON_EN is written with 0, ILMON_COMPMODE bit will be automatically written with 0 too. 0: ILMON Comparator is disabled 1: ILMON Comparator is enabled
5	SMPS_ILMON_EN	R/W	0h	Selection of GPADC ILMONITOR feature 0: Feature not enabled (default) 1: Feature is enabled
4	SMPS_ILMON_VADC_MEAS_EN	R/W	0h	Provide the capability to implement an external resistor on TESTV (secondary pad function) for the I Load Monitoring measurement (ILMONITORING) 0: Feature not enable (default) 1:External resistor on TESTV pad Allow monitoring of the SMPS load current profile including 100us peaks, for SW development purposes by using VPROG pin (without external resistor). In this mode also offset and gain compensation by trimming are included. 0: Feature not enable (default) 1 :Feature is enabled
3-0	SMPS_ILMON_SEL	R/W	7h	SMPS I Load Monitor selection (exclusive) 0000: SMPS12 / SMPS123, no more default 0001: SMPS3 0010: SMPS45 / SMPS457 0011: SMPS6 0100: SMPS7 0101: SMPS8 - Reserved as not supported 0110: SMPS9 - Reserved as not supported 0111: No SMPS selection (default) Others: No SMPS selection (default)

3.13.20 GPADC_SMPS_VSEL_MONITORING Register (Address = 2D5h) [reset = 0h]

GPADC_SMPS_VSEL_MONITORING is shown in Figure 3-168 and described in Table 3-181.

Return to Summary Table.

GPADC SMPS voltage monitoring related to ILMONITORING measurement
RESET register domain: HWRST

Figure 3-168. GPADC_SMPS_VSEL_MONITORING Register

7	6	5	4	3	2	1	0
ACTIVE_PHASE	SMPS_VSEL_MONITORING						
R-0h	R-0h						

Table 3-181. GPADC_SMPS_VSEL_MONITORING Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ACTIVE_PHASE	R	0h	Specify the number of active phases during measurements 0: One phase 1: Multi-phases (more than one)
6-0	SMPS_VSEL_MONITORING	R	0h	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register

3.14 FUNC_DESIGNREV Registers

Table 3-182 lists the memory-mapped registers for the FUNC_DESIGNREV. All register offset addresses not listed in Table 3-182 should be considered as reserved locations and the register contents should not be modified.

Table 3-182. FUNC_DESIGNREV Registers

Address	Acronym	Register Name	Section
357h	DESIGNREV	Silicon Version Number Register	Section 3.14.1

3.14.1 DESIGNREV Register (Address = 357h) [reset = X]

DESIGNREV is shown in Figure 3-169 and described in Table 3-183.

Return to Summary Table.

Silicon version number register
RESET register domain: POR

Figure 3-169. DESIGNREV Register

7	6	5	4	3	2	1	0
RESERVED				DESIGNREV			
R-0h				R-X			

Table 3-183. DESIGNREV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	DESIGNREV	R	X	Value depending on silicon version number (From metal bits) 0000 - Silicon Revision 1.0 0001 - Silicon Revision 1.1 0010 - Silicon Revision 1.2 0011 - Silicon Revision 1.3 0100 - Silicon Revision 1.4

3.15 FUNC_OSCILLATOR Registers

Table 3-184 lists the memory-mapped registers for the FUNC_OSCILLATOR. All register offset addresses not listed in Table 3-184 should be considered as reserved locations and the register contents should not be modified.

Table 3-184. FUNC_OSCILLATOR Registers

Address	Acronym	Register Name	Section
0x3C1	OSCILLATOR_BYPASS	Oscillator Bypass	Section 3.15.1

3.15.1 OSCILLATOR_BYPASS Register (Address = 0x3C1) [reset = X]

OSCILLATOR_BYPASS is shown in Figure 3-170 and described in Table 3-185.

Return to Summary Table.

Oscillator bypass register.
RESET register domain: POR

Figure 3-170. OSCILLATOR_BYPASS Register

7	6	5	4	3	2	1	0
RESERVED							OSC16M_CFG
R-0h							R-X

Table 3-185. OSCILLATOR_BYPASS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	OSC16M_CFG	R	X	Bypass the 16-MHz oscillator. 0: 16-MHz oscillator is enabled, and external 16.384-MHz crystal is required. 1: Oscillator is bypassed

3.16 FUNC_TRIM_GPADC Registers

Table 3-186 lists the memory-mapped registers for the FUNC_TRIM_GPADC. All register offset addresses not listed in Table 3-186 should be considered as reserved locations and the register contents should not be modified.

Table 3-186. FUNC_TRIM_GPADC Registers

Address	Acronym	Register Name	Section
3CDh	GPADC_TRIM1	RESET register domain: POR	Section 3.16.1
3CEh	GPADC_TRIM2	RESET register domain: POR	Section 3.16.2
3CFh	GPADC_TRIM3	RESET register domain: POR	Section 3.16.3
3D0h	GPADC_TRIM4	RESET register domain: POR	Section 3.16.4
3D3h	GPADC_TRIM7	RESET register domain: POR	Section 3.16.5
3D4h	GPADC_TRIM8	RESET register domain: POR	Section 3.16.6

3.16.1 GPADC_TRIM1 Register (Address = 3CDh) [reset = X]

GPADC_TRIM1 is shown in Figure 3-171 and described in Table 3-187.

Return to Summary Table.

RESET register domain: POR

Figure 3-171. GPADC_TRIM1 Register

7	6	5	4	3	2	1	0
GPADC_IN0_IN1_D1							GPADC_IN0_IN1_D1_SIGN
R-X							R-X

Table 3-187. GPADC_TRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	GPADC_IN0_IN1_D1	R	X	GPADC Input Channels 0 and 1 Calibration Value D1
0	GPADC_IN0_IN1_D1_SIGN	R	X	Sign bit of the GPADC Input Channels 0 and 1 Calibration Value D1 0: Positive 1: Negative

3.16.2 GPADC_TRIM2 Register (Address = 3CEh) [reset = X]

GPADC_TRIM2 is shown in Figure 3-172 and described in Table 3-188.

Return to Summary Table.

RESET register domain: POR

Figure 3-172. GPADC_TRIM2 Register

7	6	5	4	3	2	1	0
GPADC_IN0_IN1_D2							GPADC_IN0_IN1_D2_SIGN
R-X							R-X

Table 3-188. GPADC_TRIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	GPADC_IN0_IN1_D2	R	X	GPADC Input Channels 0 and 1 Calibration Value D2
0	GPADC_IN0_IN1_D2_SIGN	R	X	Sign bit of the GPADC Input Channels 0 and 1 Calibration Value D2 0: Positive 1: Negative

3.16.3 GPADC_TRIM3 Register (Address = 3CFh) [reset = X]

GPADC_TRIM3 is shown in Figure 3-173 and described in Table 3-189.

Return to Summary Table.

RESET register domain: POR

Figure 3-173. GPADC_TRIM3 Register

7	6	5	4	3	2	1	0
GPADC_IN2_D1							GPADC_IN2_D1_SIGN
R-X							R-X

Table 3-189. GPADC_TRIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	GPADC_IN2_D1	R	X	GPADC Input Channel 2 Calibration Value D1
0	GPADC_IN2_D1_SIGN	R	X	Sign bit of the GPADC Input Channel 2 Calibration Value D1 0: Positive 1: Negative

3.16.4 GPADC_TRIM4 Register (Address = 3D0h) [reset = X]

GPADC_TRIM4 is shown in Figure 3-174 and described in Table 3-190.

Return to Summary Table.

RESET register domain: POR

Figure 3-174. GPADC_TRIM4 Register

7	6	5	4	3	2	1	0
GPADC_IN2_D2							GPADC_IN2_D2_SIGN
R-X							R-X

Table 3-190. GPADC_TRIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	GPADC_IN2_D2	R	X	GPADC Input Channel 2 Calibration Value D2
0	GPADC_IN2_D2_SIGN	R	X	Sign bit of the GPADC Input Channel 2 Calibration Value D2 0: Positive 1: Negative

3.16.5 GPADC_TRIM7 Register (Address = 3D3h) [reset = X]

GPADC_TRIM7 is shown in Figure 3-175 and described in Table 3-191.

Return to Summary Table.

RESET register domain: POR

Figure 3-175. GPADC_TRIM7 Register

7	6	5	4	3	2	1	0
VCC_D1							VCC_D1_SIGN
R-X							R-X

Table 3-191. GPADC_TRIM7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	VCC_D1	R	X	GPADC Input Channel 7 Calibration Value D1
0	VCC_D1_SIGN	R	X	Sign bit of the GPADC Input Channel 7 Calibration Value D1 0: Positive 1: Negative

3.16.6 GPADC_TRIM8 Register (Address = 3D4h) [reset = X]

GPADC_TRIM8 is shown in Figure 3-176 and described in Table 3-192.

Return to Summary Table.

RESET register domain: POR

Figure 3-176. GPADC_TRIM8 Register

7	6	5	4	3	2	1	0
VCC_D2							VCC_D2_SIGN
R-X							R-X

Table 3-192. GPADC_TRIM8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	VCC_D2	R	X	GPADC Input Channels 0 and 1 Calibration Value D2
0	VCC_D2_SIGN	R	X	Sign bit of the GPADC Input Channels 0 and 1 Calibration Value D2 0: Positive 1: Negative

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2015) to A Revision	Page
• Changed the GPADC_FLUSH Register	170
• Added the FUNC_OSCILLATOR registers	191
• Added the *FUNC_TRIM_GPADC* registers	193

Changes from A Revision (April 2017) to B Revision	Page
• Added Silicon Revision 1.4	190

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