# TPS650932 Simple and Flexible Wide Input Voltage PMIC for Computing

## 1 Device Overview

### 1.1 Features

- 5 Reconfigurable Voltage Regulators:
  - 4 Step-Down Controllers Using External Power MOSFETs:
    - $V_{IN}$ Range from 4.5 V to 24 V
    - Continuous Output Current 20 A+ Using External Power MOSFETs
    - Frequency Selectable for Highest Efficiency or Ultra-Small Layout
  - 1 Step-Down Converter with Internal Power MOSFETs:
    - $V_{IN}$ Range from 3 V to 3.6 V
    - Up to 2.7 A of Continuous Output Current
  - Differential Output-Voltage Sensing
  - Individual Enables and Power Goods for Flexible Sequence
  - Sleep-Mode Dynamic-Voltage Scaling and Decay to 0-V Feature
  - Ultra-Low Quiescent Current Mode (ULQ)
- 3 Fixed LDO Voltage Regulators:
  - LDO1: Fixed Output Voltage LDO for DDRx VTT ($V_{OUT}$ = VINLDO1S/2)
    - Up to 1 A of Continuous Output Current, DC+AC Accuracy ±5%, 2-A peak
  - LDO3: 3.3-V Always-On Fixed Output Voltage LDO, DC Accuracy ±1%, < 40 mA
    - 3.3-V Load Switch for EC_VCC or ADC Rail
  - LDO5: 5-V Always-On Fixed Output Voltage LDO, DC Accuracy ±1%, < 100 mA
    - Automatic Switch to 5-V Regulator for Higher Efficiency
- 7 Power Good Comparators and Sequence Logic for External Voltage Regulators, Load Switches, or LDOs
- Power-Button With Programmable Response Time
- 3 General-Purpose Level Shifters
- Backup Battery and LDO Selector for RTC Domain
- Power-Source Monitoring for Adapter and 2 Batteries
- Board Temperature Monitoring
- 1-Hz EC-Wake Clock Output
- Advanced System-Reset Control
- $I^2C$ Interface: Standard-Mode (100 kHz), Fast-Mode (400 kHz), Fast-Mode Plus (1000 kHz)

### 1.2 Applications

- NVDC or Non-NVDC; 2, 3, or 4 Series-Cell Li Battery-Powered Products
- Tablet, Ultrabook, 2-in-1, and Notebook Computers
- Mobile PCs, All-In-Ones, Mobile Internet Devices, and Industrial Computing

### 1.3 Description

The TPS650932 device is a single-chip solution, power-management IC (PMIC) designed specifically for the latest Intel Cannon Lake processors targeted for tablets, ultrabooks, and notebooks with NVDC or non-NVDC power architectures, using 2S, 3S, or 4S Lithium-Ion battery packs. The device can provide a power solution based on Intel Reference Designs.

Five highly-efficient step-down voltage regulators (VRs) and a sink-source LDO are used along with power-up sequence logic managing external load switches to provide the proper power rails, sequencing, and protection—including DDR3 and DDR4 memory power. The regulators support dynamic voltage scaling (DVS) for maximum efficiency including connected standby. The high-frequency voltage regulators use small inductors and capacitors to achieve a small solution size. Output power is adjustable on the controllers to scale across processor skews and applications. An $I^2C$ interface allows simple control by the embedded controller (EC).

The device is available in a 7×7 nFBGA package (ZAJ). The ZAJ package can be used in Type-4 PCB boards for the smallest area implementation.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS650932 | nFBGA (168) | 7.00 mm x 7.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 1.4 Simplified System Diagram

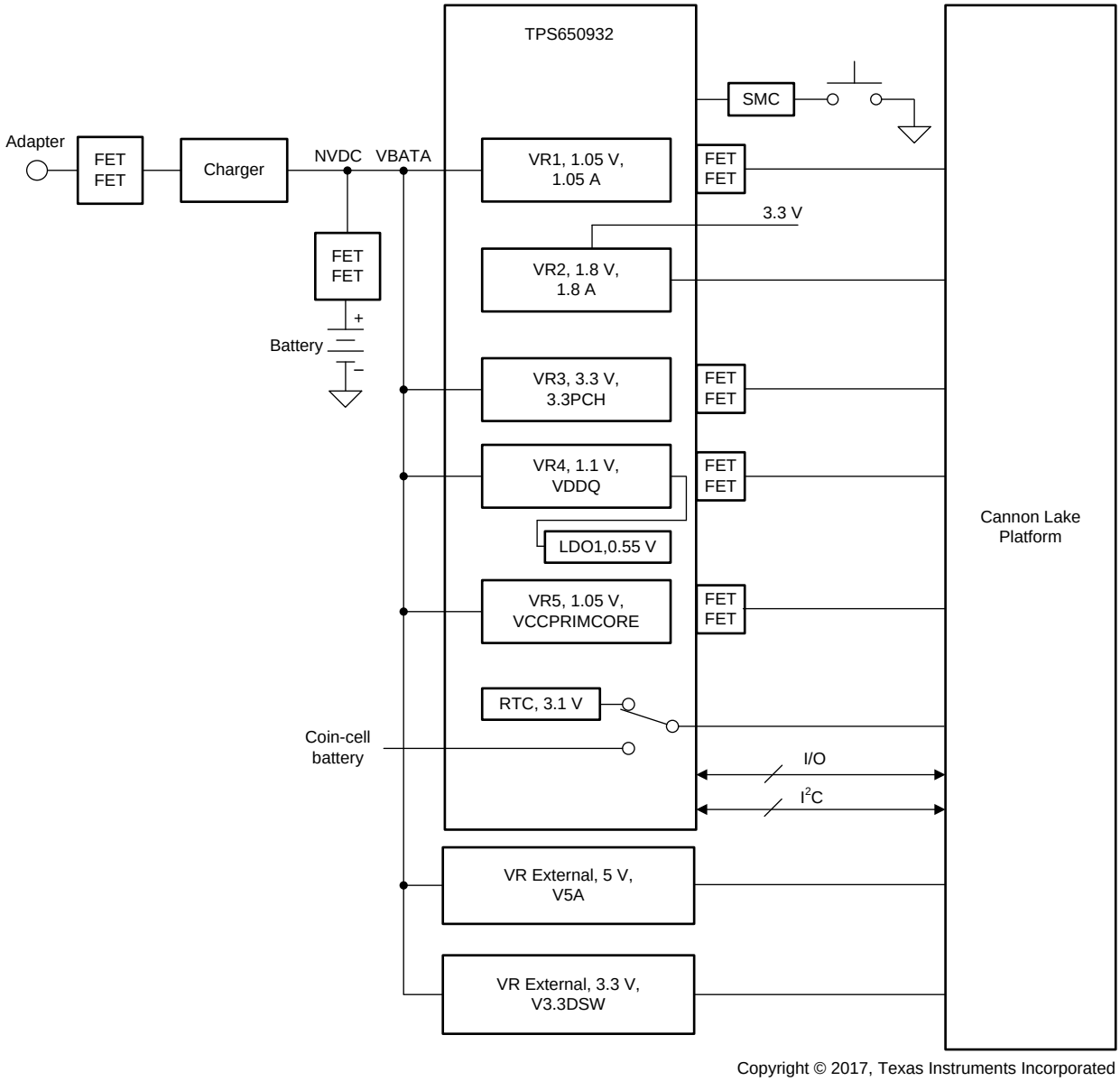





**Figure 1-1. Simplified System Diagram**

# Table of Contents



## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| August 2017 | * | Initial release. |

# 3 Voltage Regulator and Power-Good Comparator Logic Assignment

Table 3-1 lists the voltage regulator and power-good comparator logic assignments for Cannon Lake Platforms.

**Table 3-1. Voltage Regulator and Power-Good Comparator Logic Assignment for Cannon Lake Platforms**

| REGULATOR OR COMPARATOR | PREMIUM (SPLIT LOW VOLTAGE RAILS) | | POWER-GOOD OUTPUT SETTING(1) |
|---|---|---|---|
| | Cannon Lake PLATFORM POWER-SYSTEM VOLTAGE RAIL | OUTPUT VOLTAGE ( $V_O$) OR COMPARATOR INPUT | |
| VR1 | V1.05A | 1.05 V | PP |
| VR2 | V1.8A | 1.8 V | PP |
| VR3 | 3.3PCH | 3.3 V | PP |
| VR4 | VDDQ | 1.2 V, 1.35 V, 1.1 V | OD |
| VR5 | VCCPRIMCORE | 1.05 V | PP |
| LDO1 | VTT | ½ of VDDQ | — |
| External regulator A | VCCIO (optional) | 0.95 V | — |
| External regulator B | V5A_DS3 | — | — |
| Power-good comparator logic A | V3.3A_DSW enable<br>Sense external-load switch | 3.3 V | PP |
| Power-good comparator logic B | V1.8U_2.5U enable<br>Sense external-load switch | 1.8 V | PP |
| Power-good comparator logic C | V5A_DS3 enable<br>Sense external regulator B | 5 V | PP |
| Power-good comparator logic D | VCCIO enable<br>Sense external load switch | Level mode 0.85 V | PP |
| Power-good comparator logic E | V3.3S sense external-load switch | 3.3 V | PP |
| Power-good comparator logic F | V1.8S sense external-load switch | Output of VR2 | PP |
| Power-good comparator logic G | V1.05S sense external-load switch | Output of VR1 | OD |
| Power-good comparator logic H | Unavailable<br>Used in level-shifter mode | Window mode 1.2V | OD |

(1) PP = Push pull, OD = Open drain

# 4 Pin Configuration and Functions

Figure 4-1 shows the 168-pin ZAJ New Fine-Pitch Ball-Grid Array package.

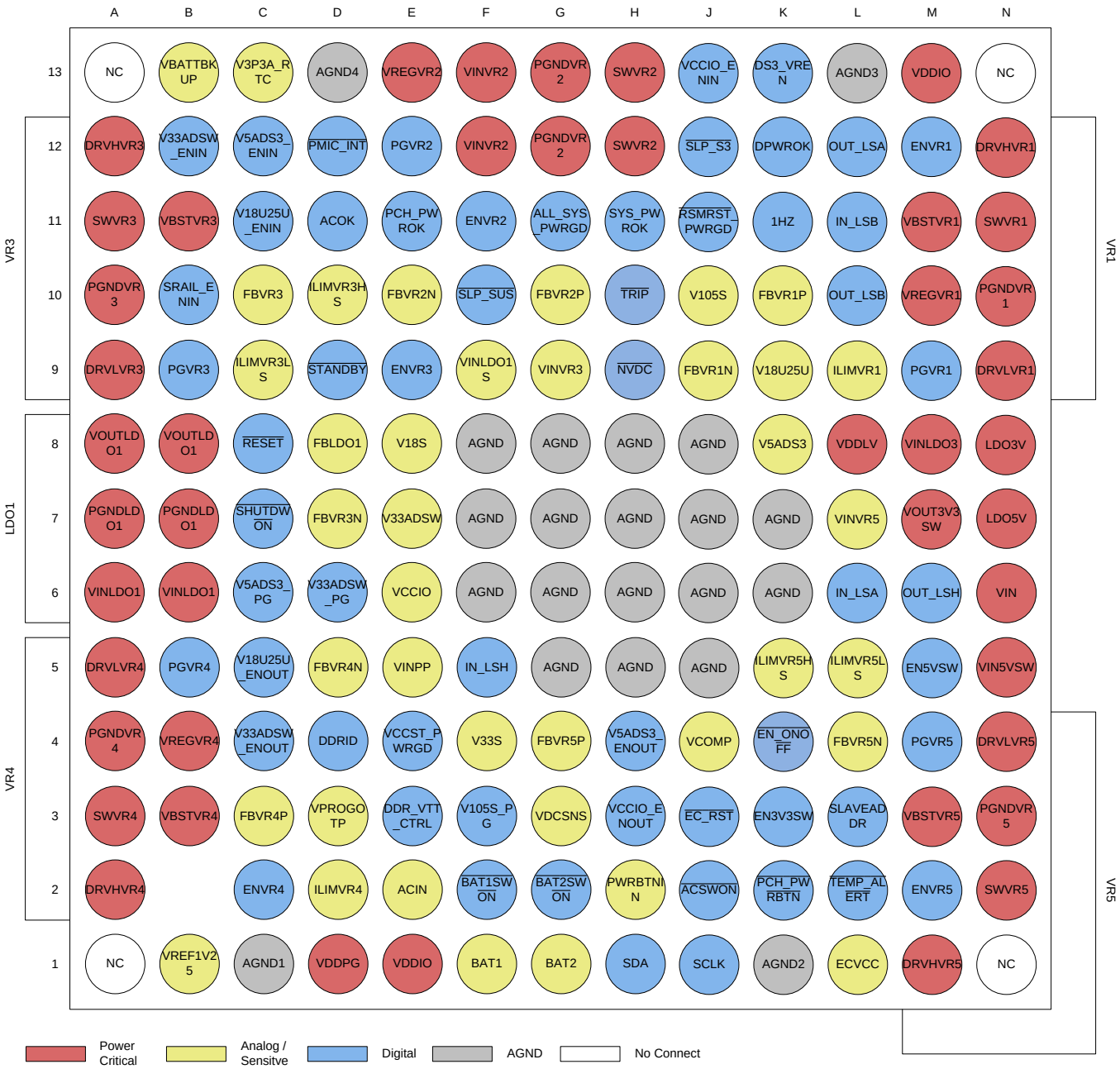



**Figure 4-1. 168-Pin ZAJ nFBGA (Top View)**

## 4.1 Pin Attributes

**Pin Attributes—ZAJ Package**

| PIN | | I/O | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| A1 | NC | NC | — | No connect pin. Solder this pin to the PCB for mechanical strength. |
| A2 | DRVHVR4 | O | VR | VR4 high-side gate-drive output for the external-power FET |
| A3 | SWVR4 | I | VR | VR4 switch-node connection |
| A4 | PGNDVR4 | — | VR | VR4 power ground |
| A5 | DRVLVR4 | O | VR | VR4 Low side gate drive output for the external-power FET |
| A6 | VINLDO1 | I | VR | LDO1 input supply |
| A7 | PGNDLDO1 | — | VR | LDO1 power ground |
| A8 | VOUTLDO1 | O | VR | LDO1 output voltage. The voltage of this pin equals ½ × VINLDO1SNS. |
| A9 | DRVLVR3 | O | VR | VR3 Low side gate drive output for the external-power FET |
| A10 | PGNDVR3 | — | VR | VR3 power ground |
| A11 | SWVR3 | I | VR | VR3 switch-node connection |
| A12 | DRVHVR3 | O | VR | VR3 high-side gate-drive output for the external-power FET |
| A13 | NC | NC | — | No connect pin. Solder this pin to the PCB for mechanical strength. |
| B1 | VREF1V25 | O | AS | Decoupling capacitor connection for the internal voltage reference |
| B3 | VBSTVR4 | I | VR | VR4 bootstrap pin |
| B4 | VREGVR4 | I | VR | VR4 5-V drive-supply input. This pin is shorted on the PCB with LDO5V and is shared with VR3. |
| B5 | PGVR4 | O | D | VR4 power-good comparator output. This pin is an open-drain output. |
| B6 | VINLDO1 | I | VR | LDO1 input supply |
| B7 | PGNDLDO1 | — | VR | LDO1 power ground |
| B8 | VOUTLDO1 | O | VR | LDO1 output voltage. The voltage of this pin equals ½ × VINLDO1SNS. |
| B9 | PGVR3 | O | D | VR3 power-good comparator output. This pin is a push-pull output. |
| B10 | SRAIL_ENIN | I | D | Enable for power-good comparators E, F and G, which monitor the S rails: V33S, V18S, and V105S |
| B11 | VBSTVR3 | I | VR | VR3 bootstrap pin |
| B12 | V33ADSW_ENIN | I | D | Enable for power-good comparator A, which monitors V33ADSW |
| B13 | VBATTBKUP | I | AS | RTC backup battery-supply connection |
| C1 | AGND1 | — | A | Analog ground 1. Tie this pin directly to the ground plane. |
| C2 | ENVR4 | I | D | VR4 enable |
| C3 | FBVR4P | I | AS | VR4 positive-feedback remote sense. Connect this pin to the output voltage of VR4 at the output-load capacitor. |
| C4 | V33A_DSW_ENOUT | O | D | Qualified enable for external V33A_DSW rail. |
| C5 | V18U25U_ENOUT | O | D | V18U_25U enable to the PoL load switch or regulator (push-pull to VDDPG) |
| C6 | V5ADS3_PG | O | D | Power-good comparator C output for V5A_DS3 (push-pull to VDDPG) |
| C7 | $\overline{\text{SHUTDOWN}}$ | I | D | Set shutdown mode (all supplies off). This pin is active low. |
| C8 | $\overline{\text{RESET}}$ | O | D | Global disable output for external converters and power tree. This pin is active low. |
| C9 | ILIMVR3LS | I | AS | VR3 current-limit setting, low-side FET valley-current limit |
| C10 | FBVR3P | I | AS | VR3 positive-feedback remote sense. Connect this pin to the output voltage of VR3 at the output-load capacitor. |
| C11 | V18U25U_ENIN | I | D | Enable for power-good comparator B, which monitors V18U_25U |
| C12 | V5A_DS3 _ENIN | I | D | Enable for power-good comparator C, which monitors V5A_DS3 |
| C13 | V3P3A_RTC | O | AS | PCH RTC power supply |
| D1 | VDDPG | I | VR | PGx supply. This pin sets the output level for the PG pins for A-H if the PG pin is configured as a push-pull pin. |
| D2 | ILIMVR4 | I | AS | VR4 current-limit setting, low-side FET valley-current limit |

(1) VR = VR critical, AS = Analog sensitive, D = Digital, A = AGND

**Pin Attributes—ZAJ Package (continued)**

| PIN | | I/O | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| D3 | VPROGOTP | I | AS | Always connect this pin to the LDO5V pin. This pin is the supply voltage for OTP programming (must be connected to the LDO5V pin in normal operation). |
| D4 | DDRID | I | D | VR4 output voltage selection pin. Set this pin low for 1.2-V operation, high for 1.35-V operation, or floating for 1.1-V operation. |
| D5 | FBVR4N | I | AS | VR4 negative-feedback remote sense. Connect this pin to the GND of VR4 at the output-load capacitor. |
| D6 | V33ADSW_PG | O | D | Power good comparator A output for V33A_DSW rail. |
| D7 | FBVR3N | I | AS | VR3 negative-feedback remote sense. Connect this pin to the GND of VR3 at the output-load capacitor. |
| D8 | FBLDO1 | I | AS | LDO1 feedback-voltage kelvin sense. Connect this pin to the output voltage of the LDO1 pin at the output-load capacitor. |
| D9 | $\overline{\text{STANDBY}}$ | I | D | Set rails in standby when this pin is low (low-power mode) |
| D10 | ILIMVR3HS | I | AS | VR3 current-limit setting, high-side FET peak-current limit |
| D11 | ACOK | I | D | ACOK input |
| D12 | $\overline{\text{PMIC\_INT}}$ | O | D | PMIC to EC interrupt. This pin is an open-drain output and is active low. |
| D13 | AGND4 | — | A | Analog ground 4. Tie this pin directly to the ground plane. |
| E1 | VDDIO | I | VR | Voltage supply input for the I/O buffers. The VDDIO pin should be tied to the LDO3V (3.3 V) pin. |
| E2 | ACIN | I | AS | AC adaptor voltage sense |
| E3 | DDR_VTT_CTRL | I | D | LDO1 enable and DVS control of VR4 |
| E4 | VCCST_PWRGD | O | D | VCCST power good .This pin is an open-drain output. |
| E5 | VINPP | I | AS | VIN for the power-path domain. Connect this pin to the external diode or from AC, BAT1, or BAT2. |
| E6 | VCCIO | I | AS | Power good comparator D input and discharge path for VCCIO rail |
| E7 | V33ADSW | I | AS | Power Good comparator A Input and discharge path for the V33A_DSW_rail |
| E8 | V18S | I | AS | Power-good comparator F input and discharge path for the V18S rail |
| E9 | ENVR3 | I | D | VR3 enable |
| E10 | FBVR2N | I | AS | VR2 negative-feedback remote sense. Connect this pin to the GND of VR2 at the output-load capacitor. |
| E11 | PCH_PWROK | O | D | Core and non-core power-good pin. This pin is the delayed version of the ALL_SYS_PWRGD pin. This pin is an open-drain output. |
| E12 | PGVR2 | O | D | VR2 power-good comparator output. This pin is a push-pull output. |
| E13 | VREGVR2 | I | VR | VR2 5-V drive-supply input. This pin is shorted on the PCB with LDO5V. |
| F1 | BAT1 | I | AS | Battery 1 voltage-sense input |
| F2 | $\overline{\text{BAT1SWON}}$ | O | D | Battery 1 switch-on power path. This pin is an open-drain output and is active low. |
| F3 | V105S_PG | O | D | Power-good comparator G output for V105S. This pin is an open-drain output. |
| F4 | V33S | I | AS | Power-good comparator E input and discharge path for the V33A rail |
| F5 | IN_LSH | I | AS | Input for level shifter H |
| F6 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| F7 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| F8 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| F9 | VINLDO1S | I | AS | LDO1 input voltage-reference sense. Connect this pin to the output voltage of the VR4 pin at the output-load capacitor. |
| F10 | $\overline{\text{SLP\_SUS}}$ | I | D | Input for $\overline{\text{SLP\_SUS}}$ signal for the power-good tree |
| F11 | ENVR2 | I | D | VR2 enable |
| F12 | VINVR2 | I | VR | VR2 power input voltage. Connect this pin to a 3.3-V voltage regulator, such as the V3.3A_DSW. |
| F13 | VINVR2 | I | VR | VR2 power input voltage. Connect this pin to a 3.3-V voltage regulator, such as the V3.3A_DSW. |
| G1 | BAT2 | I | AS | Battery 2 voltage-sense input |

## Pin Attributes—ZAJ Package (continued)

| PIN | | I/O | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| G2 | $\overline{\text{BAT2SWON}}$ | O | D | Battery 2 switch-on power path. This pin is an open-drain output and is active low. |
| G3 | VDCSNS | I | AS | VDC voltage monitor |
| G4 | FBVR5P | I | AS | VR5 positive-feedback remote sense. Connect this pin to the output voltage of VR5 at the output-load capacitor. |
| G5 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| G6 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| G7 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| G8 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| G9 | VINVR3 | I | AS | VR3 input-voltage sense and high-side current-sense. Kelvin connect this pin to the drain of high-side FET. |
| G10 | FBVR2P | I | AS | VR2 positive-feedback remote sense. Connect this pin to the output voltage of VR2 at the output-load capacitor. |
| G11 | ALL_SYS_PWRGD | O | D | Non-core rails power-good pin. Power-good pin for all PMIC and specified monitored VRs. This pin is an open-drain output. |
| G12 | PGNDVR2 | — | VR | VR2 power ground |
| G13 | PGNDVR2 | — | VR | VR2 power ground |
| H1 | SDA | I/O | D | $I^2C$ data |
| H2 | PWRBTNIN | I | AS | Power-button input (internal pullup to LDO3V). This pin is active low. |
| H3 | VCCIO_ENOUT | O | D | Qualified enable for VCCIO rail. |
| H4 | V5ADS3_ENOUT | O | D | Power-good comparator F output for V18S or V33A_PCH and enable to the PoL load switch or regulator (push-pull to VDDPG) |
| H5 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| H6 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| H7 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| H8 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| H9 | $\overline{\text{NVDC}}$ | I | D | NVDC select. This pin has two levels: low = NVDC, high = non-NVDC. Connect the $\overline{\text{NVDC}}$ pin to ground for NVDC. Connect the $\overline{\text{NVDC}}$ pin to the LDO3V pin for non-NVDC. |
| H10 | $\overline{\text{TRIP}}$ | O | D | VCOMP comparator push-pull output. This pin is active low. |
| H11 | SYS_PWROK | O | D | Delayed version of the ALL_SYS_PWRGD pin. This pin is an open-drain output. |
| H12 | SWVR2 | I | VR | VR2 switch-node connection |
| H13 | SWVR2 | I | VR | VR2 switch-node connection |
| J1 | SCLK | I | D | $I^2C$ clock |
| J2 | $\overline{\text{ACSWON}}$ | O | D | AC adaptor switch-on power path. This pin is an open-drain output and is active low. |
| J3 | $\overline{\text{EC\_RST}}$ | O | D | EC reset. This pin is an open-drain output and is active low. |
| J4 | VCOMP | I | AS | VCOMP comparator input |
| J5 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| J6 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| J7 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| J8 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| J9 | FBVR1N | I | AS | VR1 negative-feedback remote sense. Connect this pin to the GND of the VR1 pin at the output-load capacitor. |
| J10 | V105S | I | AS | Power-good comparator G input and discharge path for the V105S rail |
| J11 | $\overline{\text{RSMRST}}$_PWRGD | O | D | Resume-reset power good. This pin is an open-drain output and is active low. |
| J12 | $\overline{\text{SLP\_S3}}$ | I | D | Input for $\overline{\text{SLP\_SUS}}$ signal for the power-good tree |
| J13 | VCCIO_ENIN | I | D | Enable for power good comparator D which is V33A_DSW |
| K1 | AGND2 | — | A | Analog ground 2. Tie this pin directly to the ground plane. |
| K2 | $\overline{\text{PCH\_PWRBTN}}$ | O | D | Power-button signal to PCH. This pin is an open-drain output and is active low. |
| K3 | EN3V3SW | I | D | Enable for load switch from the LDO3V pin to the VOUT3V3SW output pin |

## Pin Attributes—ZAJ Package (continued)

| PIN | | I/O | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| K4 | $\overline{\text{EC\_ONOFF}}$ | O | D | Debounced version of PWRBTNIN. This pin is an open-drain output and is active low. |
| K5 | ILIMVR5HS | I | AS | VR5 current-limit setting, high-side FET peak-current limit |
| K6 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| K7 | AGND | — | A | Analog ground. Tie this pin directly to the ground plane. |
| K8 | V5A_DS3 | I | AS | Power-good comparator C input and discharge path for the V5A_DS3 rail |
| K9 | V18U25U | I | AS | Power-good comparator B input and discharge path for the V18U_25U rail |
| K10 | FBVR1P | I | AS | VR1 positive-feedback remote sense. Connect this pin to the output voltage of VR1 at the output-load capacitor. |
| K11 | 1Hz | O | D | 1-Hz clock output for waking up the embedded controller (EC). |
| K12 | DPWROK | O | D | Delayed version of V3.3A_DSW_PG. This pin is an open-drain output. |
| K13 | DS3_VREN | O | D | DS3 VR enable. This pin enables the external power switches. This pin is a push-pull output. |
| L1 | ECVCC | I | AS | EC VCC supply |
| L2 | $\overline{\text{TEMP\_ALERT}}$ | O | D | Open-drain output of the silicon temperature sensor. This pin is the input to the power-monitor unit (PMU). Connect this pin to the to $\overline{\text{PROCHOT}}$ pin of the system. This pin is active low. TI recommends connecting a 50-Ω pullup resistor from this pin to the V1.00S pin. |
| L3 | SLAVEADDR | I | D | $I^2C$ slave-address select (low = 0x30, high = 0x32, open = float = 0x34). This pin keeps the same connection during operation. |
| L4 | FBVR5N | I | AS | VR5 negative-feedback remote sense. Connect this pin to the GND of VR5 at the output-load capacitor. |
| L5 | ILIMVR5LS | I | AS | VR5 Current-limit setting, low-side FET valley-current limit |
| L6 | IN_LSA | I | D | Input of level shifter A |
| L7 | VINVR5 | I | AS | VR5 input-voltage sense and high-side current-sense. Kelvin connect this pin to the drain of high-side FET. |
| L8 | VDDLV | I | VR | LVx buffer supply. This pin sets the output level for the level shifter pins. |
| L9 | ILIMVR1 | I | AS | VR1 current-limit setting, low-side FET valley-current limit |
| L10 | OUT_LSB | O | D | Output of level shifter B |
| L11 | IN_LSB | I | D | Input of level shifter B |
| L12 | OUT_LSA | O | D | Output of level shifter A |
| L13 | AGND3 | — | A | Analog ground 3. Tie this pin directly to the ground plane. |
| M1 | DRVHVR5 | O | VR | VR5 high-side gate-drive output for the external-power FET |
| M2 | ENVR5 | I | D | VR5 enable |
| M3 | VBSTVR5 | I | VR | VR5 bootstrap pin |
| M4 | PGVR5 | O | D | VR5 power-good comparator output. This pin is a push-pull output. |
| M5 | EN5VSW | I | D | Enable internal-load switch from the 5-V switching regulator to the LDO5V output through the VIN5VSW pin. Connect this pin to power-good of the 5-V switching regulator. |
| M6 | OUT_LSH | O | D | Output of level shifter H |
| M7 | VOUT3V3SW | O | VR | EC domain load-switch output and discharge path from LDO3V |
| M8 | VINLDO3 | I | VR | LDO3V input supply |
| M9 | PGVR1 | O | D | VR1 power-good comparator output. This pin is a push-pull output. |
| M10 | VREGVR1 | I | VR | 5-V drive-supply input. This pin is shorted on the PCB with LDO5V. This pin is the supply for VR1 and VR5. |
| M11 | VBSTVR1 | I | VR | VR1 bootstrap pin |
| M12 | ENVR1 | I | D | VR1 enable |
| M13 | VDDIO | I | VR | Voltage supply input for the I/O buffers. The VDDIO pin should be tied to the LDO3V (3.3 V) pin. |
| N1 | NC | NC | — | No connect pin. Solder this pin to the PCB for mechanical strength. |
| N2 | SWVR5 | I | VR | VR5 switch-node connection |

**Pin Attributes—ZAJ Package (continued)**

| PIN | | I/O | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| N3 | PGNDVR5 | — | VR | VR5 power ground |
| N4 | DRVLVR5 | O | VR | VR5 Low side gate drive output for the external-power FET |
| N5 | VIN5VSW | I | VR | Internal load switch from the 5-V switching regulator to the LDO5V output. Connect the VIN5VSW pin to the 5-V switching regulator output. |
| N6 | VIN | I | VR | Device input voltage |
| N7 | LDO5V | O | AS | 5-V internal supply used primarily for the gate drives |
| N8 | LDO3V | O | AS | 3.3-V LDO used as a reference voltage and as a pullup supply |
| N9 | DRVLVR1 | O | VR | VR1 Low side gate drive output for the external-power FET |
| N10 | PGNDVR1 | — | VR | VR1 power ground |
| N11 | SWVR1 | I | VR | VR1 switch-node connection |
| N12 | DRVHVR1 | O | VR | VR1 high-side gate-drive output for the external-power FET |
| N13 | NC | NC | — | No connect pin. Solder this pin to the PCB for mechanical strength. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **CHIP** | | | | |
| Power input pins | VIN, VINLDO3 | –0.3 | 28 | V |
| Analog ground pins | AGND1, AGND2, AGND3, AGND4, AGND (16 center pins) | –0.3 | 0.3 | V |
| **SWITCHING REGULATORS** | | | | |
| Input pins, controllers | VINVR3, VINVR5 | –0.3 | 28 | V |
| Switch pins, controllers | SWVR1 , SWVR3 , SWVR4 , SWVR5 | –1 | 28 | V |
| | SWVR1 , SWVR3 , SWVR4 , SWVR5 (transient <10ns) | –2 | 28 | V |
| High-drive pins, controllers | DRVHVR1, DRVHVR3, DRVHVR4, DRVHVR5 | –0.3 | 32 | V |
| Low-drive pins, controllers | DRVLVR1, DRVLVR3, DRVLVR4, DRVLVR5 | –0.3 | 7 | V |
| Bootstrap pins, controllers | VBSTVR1, VBSTVR3, VBSTVR4, VBSTVR5 | –0.3 | 32 | V |
| | Differential voltage between VBSTVRx and SWVRx | –0.3 | 7 | V |
| Input pin, converter | VINVR2 | –0.3 | 3.6 | V |
| Switch pins, converter | SWVR2 | –1 | 4.0 | V |
| | SWVR2 (transient <10ns) | –2 | 5.5 | V |
| Power-ground pins | PGNDVR1, PGNDVR2, PGNDVR3, PGNDVR4, PGNDVR5 | –0.3 | 0.3 | V |
| Enable pins | ENVR1, ENVR2, ENVR3, ENVR4, ENVR5 | –0.3 | 3.6 | V |
| NVDC select pin | $\overline{\text{NVDC}}$ | –0.3 | 3.6 | V |
| Positive remote-feedback pins | FBVR1P, FBVR2P, FBVR3P, FBVR4P | –0.3 | 3.6 | V |
| | FBVR5P | –0.3 | 5.7 | V |
| Negative remote-feedback pins | FBVR1N, FBVR2N, FBVR3N, FBVR4N, FBVR5N | –0.3 | 0.3 | V |
| Gate-drive regulator input-power pins | VREGVR1, VREGVR2, VREGVR4 | –0.3 | 5.7 | V |
| Low-side current limit | ILIMVR1, ILIMVR3LS, ILIMVR4, ILMVR5LS | –0.3 | 3.6 | V |
| High-side current limit | ILMVR3HS, ILMVR5HS | –0.3 | 3.6 | V |
| **LDO REGULATOR** | | | | |
| Input pin | VINLDO1 | –0.3 | 3.6 | V |
| Output pin | VOUTLDO1 | –0.3 | 3.6 | V |
| Power ground pin | PGNDLDO1 | –0.3 | 0.3 | V |
| Input feedback pin | VINLDO1S | –0.3 | 3.6 | V |
| Output feedback pin | FBLDO1 | –0.3 | 3.6 | V |
| **$I^2C$** | | | | |
| SCLK, SDAT, SLAVEADDR | | –0.3 | 3.6 | V |
| **POWER-GOOD COMPARATOR LOGIC** | | | | |
| Power-good (push-pull) supply for input pins | VDDPG | –0.3 | 3.6 | V |
| Power-good input-voltage sense pins | V33ADSW, V5ADS3, V18U25U, VCCIO, V105S, V33S, V18S | –0.3 | 5.7 | V |
| Power-good enable pins | $\overline{\text{V33ADSW\_ENIN}}$, V18U25U_ENIN, V5ADS3_ENIN, VCCIO_ENIN, $\overline{\text{SLP\_SUS}}$, $\overline{\text{SLP\_S3}}$, SRAIL_ENIN | –0.3 | 3.6 | V |
| Power-good output pins | V33ADSW_PG, V18U25U_ENOUT, V5ADS3_PG, VCCIO_ENOUT, V33ADSW_ENOUT, V5ADS3_ENOUT, V105S_PG | –0.3 | 3.6 | V |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## Absolute Maximum Ratings *(continued)*

Over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **POWER-GOOD TREE LOGIC** | | | | |
| Open-drain outputs | DPWROK, $\overline{\text{RSMRST}}$_PWRGD, VCCST_PGOOD, SYS_PWROK, ALL_SYS_PWRGD, $\overline{\text{PCH\_PWROK}}$ | –0.3 | 3.6 | V |
| **DDR CONTROL** | | | | |
| Input pins | DDR_VTT_CTRL, DDRID | –0.3 | 3.6 | V |
| **LEVEL SHIFTERS** | | | | |
| Level-shifter (push-pull) supply input pin | VDDLV | –0.3 | 3.6 | V |
| Level-shifter enable input pins | IN_LSA, IN_LSB, IN_LSH | –0.3 | 3.6 | V |
| Level-shifter output pins | OUT_LSA,OUT_LSB,OUT_LSH | –0.3 | 3.6 | V |
| **POWER-PATH LOGIC** | | | | |
| Power-path comparator input voltage sense pins | VCOMP, BAT1, BAT2, ACIN | –0.3 | 7 | V |
| Power-path comparator open-drain output pins | $\overline{\text{BAT1SWON}}$, $\overline{\text{BAT2SWON}}$, $\overline{\text{ACSWON}}$ | –0.3 | 28 | V |
| PTC overtemperature comparator open-drain output pin | $\overline{\text{TRIP}}$ | –0.3 | 3.6 | V |
| Power-path domain diode OR input pin | VINPP | –0.3 | 28 | V |
| **POWER BUTTON** | | | | |
| PWRBNTIN, $\overline{\text{PCH\_PWRBTN}}$, $\overline{\text{EC\_ONOFF}}$ | | –0.3 | 3.6 | V |
| **RESETS** | | | | |
| ECVCC, $\overline{\text{RESET}}$, $\overline{\text{EC\_RST}}$ | | –0.3 | 3.6 | V |
| **CLOCKS** | | | | |
| EC 1-Hz wake clock | | –0.3 | 3.6 | V |
| **POWER MΩNITOR** | | | | |
| VDCSNS | | –0.3 | 28 | V |
| $\overline{\text{TEMP\_ALERT}}$ | | –0.3 | 3.6 | V |
| ACOK | | –0.3 | 12 | V |
| **REFERENCE** | | | | |
| LDO output pins | LDO5V | –0.3 | 7 | V |
| | VREF1V25, LDO3V | –0.3 | 3.6 | V |
| 3.3-V load-switch enable pin | EN3V3SW | –0.3 | 3.6 | V |
| 3.3-V load-switch output pin | VOUT3V3SW | –0.3 | 3.6 | V |
| 5V- load-switch enable pin | EN5VSW | –0.3 | 3.6 | V |
| 5-V load-switch input pin | VIN5VSW | –0.3 | 6 | V |
| **BACKUP BATTERY RTC SELECTOR** | | | | |
| VBATTBKUP, V3P3A_RTC | | –0.3 | 3.6 | V |
| **MISCELLANEOUS PINS** | | | | |
| Input control pins | $\overline{\text{STANDBY}}$, $\overline{\text{SHUTDOWN}}$ | –0.3 | 3.6 | V |
| Output interrupt pin | $\overline{\text{PMIC\_INT}}$ | –0.3 | 3.6 | V |
| Output DS3 VR enable pin | DS3_VREN | –0.3 | 3.6 | V |
| Buffer-supply input pin | VDDIO | –0.3 | 3.6 | V |
| VPROGOTP | | –0.3 | 7 | V |
| **GENERAL** | | | | |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±1500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101 (2) | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **CHIP** | | | | |
| Power input pins | VIN, VINLDO3 | –0.3 | 21 | V |
| Analog ground pins | AGND1, AGND2, AGND3, AGND4, AGND (16 center pins) | –0.3 | 0.3 | V |
| **SWITCHING REGULATORS** | | | | |
| Input pins, controllers | VINVR3, VINVR5 | –0.3 | 21 | V |
| Switch pins, controllers | SWVR1 , SWVR3 , SWVR4 , SWVR5 | –1 | 21 | V |
| High-drive pins, controllers | DRVHVR1, DRVHVR3, DRVHVR4, DRVHVR5 | –0.3 | 26 | V |
| Low-drive pins, controllers | DRVLVR1, DRVLVR3, DRVLVR4, DRVLVR5 | –0.3 | 5 | V |
| Bootstrap pins, controllers | VBSTVR1, VBSTVR3, VBSTVR4, VBSTVR5 | –0.3 | 26 | V |
| | Differential voltage between VBSTVRx and SWVRx | –0.3 | 5 | V |
| Input pin, converter | VINVR2 | –0.3 | 3.3 | V |
| Switch pins, converter | SWVR2 | –1 | 3.3 | V |
| Power-ground pins | PGNDVR1, PGNDVR2, PGNDVR3, PGNDVR4, PGNDVR5 | –0.3 | 0.3 | V |
| Enable pins | ENVR1, ENVR2, ENVR3, ENVR4, ENVR5 | –0.3 | 3.3 | V |
| NVDC select pin | $\overline{\text{NVDC}}$ | –0.3 | 3.3 | V |
| Positive remote-feedback pins | FBVR1P, FBVR2P, FBVR3P, FBVR4P | –0.3 | 3.3 | V |
| | FBVR5P | –0.3 | 5 | V |
| Negative remote-feedback pins | FBVR1N, FBVR2N, FBVR3N, FBVR4N, FBVR5N | –0.3 | 0.3 | V |
| Gate-drive regulator input power pins | VREGVR1, VREGVR2, VREGVR4 | –0.3 | 5 | V |
| Low-side current limit | ILIMVR1, ILIMVR3LS, ILIMVR4, ILMVR5LS | –0.3 | 3.3 | V |
| High-side current limit | ILMVR3HS, ILMVR5HS | –0.3 | 3.3 | V |
| **LDO REGULATOR** | | | | |
| Input pin | VINLDO1 | –0.3 | 3.3 | V |
| Output pin | VOUTLDO1 | –0.3 | 1.65 | V |
| Power-ground pin | PGNDLDO1 | –0.3 | 0.3 | V |
| Input feedback pin | VINLDO1S | –0.3 | 3.3 | V |
| Output feedback pin | FBLDO1 | –0.3 | 1.65 | V |
| **$I^2C$** | | | | |
| SCLK, SDAT, SLAVEADDR | | –0.3 | 3.3 | V |
| **POWERGOOD COMPARATOR LOGIC** | | | | |
| Power-good (push-pull) supply for input pins | VDDPG | –0.3 | 3.3 | V |
| Power-good input voltage sense pins | V33ADSW, V5ADS3, V18U25U, VCCIO, V105S,V33S, V18S | –0.3 | 5 | V |
| Power-good enable pins | V33ADSW_ENIN, V18U25U_ENIN, V5ADS3_ENIN, VCCIO_ENIN, $\overline{\text{SLP\_SUS}}$, $\overline{\text{SLP\_S3}}$, SRAIL_ENIN | –0.3 | 3.3 | V |
| Power-good output pins | V33ADSW_PG, V18U25U_ENOUT, V5ADS3_PG, VCCIO_ENOUT, V33ADSW_ENOUT, V5ADS3_ENOUT, V105S_PG | –0.3 | 3.3 | V |
| **POWER-GOOD TREE LOGIC** | | | | |
| Open-drain outputs | DPWROK, $\overline{\text{RSMRST}}$_PWRGD, VCCST_PGOOD, SYS_PWROK, ALL_SYS_PWRGD, PCH_PWROK | –0.3 | 3.3 | V |

## Recommended Operating Conditions *(continued)*

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **DDR CONTROL** | | | | |
| Input pins | DDR_VTT_CTRL, DDRID | –0.3 | 3.3 | V |
| **LEVEL SHIFTERS** | | | | |
| Level-shifter (push-pull) supply input pin | VDDLV | –0.3 | 3.3 | V |
| Level-shifter enable input pins | NU | –0.3 | 3.3 | V |
| Level-shifter output pins | BC_ACOK | –0.3 | 3.3 | V |
| **POWER-PATH LOGIC** | | | | |
| Power-path comparator input voltage sense pins | VCOMP, BAT1, BAT2, ACIN | –0.3 | 5 | V |
| Power-path comparator open-drain output pins | $\overline{\text{BAT1SWON}}$, $\overline{\text{BAT2SWON}}$, $\overline{\text{ACSWON}}$ | –0.3 | 21 | V |
| PTC overtemperature comparator open-drain output pin | $\overline{\text{TRIP}}$ | –0.3 | 3.3 | V |
| Power-path domain diode or input pin | VINPP | –0.3 | 21 | V |
| **POWER BUTTON** | | | | |
| PWRBNTIN, $\overline{\text{PCH\_PWRBTN}}$, $\overline{\text{EC\_ONOFF}}$ | | –0.3 | 3.3 | V |
| **RESETS** | | | | |
| ECVCC, $\overline{\text{RESET}}$, $\overline{\text{EC\_RST}}$ | | –0.3 | 3.3 | V |
| **CLOCKS** | | | | |
| EC 1-Hz wake clock | | –0.3 | 3.3 | V |
| **POWER MΩNITOR** | | | | |
| VDCSNS | | –0.3 | 21 | V |
| $\overline{\text{TEMP\_ALERT}}$ | | –0.3 | 3.3 | V |
| ACOK | | –0.3 | 3.3 | V |
| **REFERENCE** | | | | |
| LDO output pins | LDO5V | –0.3 | 5 | V |
| | VREF1V25, LDO3V | –0.3 | 3.3 | V |
| 3.3-V load-switch enable pin | EN3V3SW | –0.3 | 3.3 | V |
| 3.3-V load-switch output pin | VOUT3V3SW | –0.3 | 3.3 | V |
| 5-V load-switch enable pin | EN5VSW | –0.3 | 3.3 | V |
| 5-V load-switch input pin | VIN5VSW | –0.3 | 5 | V |
| **BACKUP BATTERY RTC SELECTOR** | | | | |
| VBATTBKUP, V3P3A_RTC | | –0.3 | 3.3 | V |
| **MISCELLANEOUS PINS** | | | | |
| Input control pins | $\overline{\text{STANDBY}}$, $\overline{\text{SHUTDOWN}}$ | –0.3 | 3.3 | V |
| Output interrupt pin | $\overline{\text{PMIC\_INT}}$ | –0.3 | 3.3 | V |
| Output DS3 VR enable pin | DS3_VREN | –0.3 | 3.3 | V |
| Buffer-supply input pin | VDDIO | –0.3 | 3.3 | V |
| VPROGOTP | | –0.3 | 5 | V |
| **GENERAL** | | | | |
| Operating free air temperature, $T_A$ | | –40 | 85 | °C |
| Operating junction temperature, $T_J$ | | –40 | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | TPS650932 ZAJ (nFBGA) 168 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 37.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 15.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 11.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 11.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics: Control

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SYSTEM** | | | | | | |
| $V_{IN}$ | System input voltage | Parametric and functional | 5.4 | 7.4 | 21 | V |
| | | Functional | 5.4 | 7.4 | 24 | V |
| $I_Q$ | System quiescent current (includes IDDQ for LDO5V, LDO3V, and VREF1.25V, all registers are default setting) | Measured at VIN = 7.4 V | | 95 | 150 | µA |
| $V_{UVLO\_5V\_Main}$ | System undervoltage lockout threshold - All IC functionality including 5VLDO, except LDO3V and internal reference system | $V_{VIN}$ voltage decreasing - measured at VIN (falling edge) | 4.95 | 5.1 | 5.25 | V |
| $V_{Hys\_5V\_Main}$ | System undervoltage lockout threshold hysteresis | $V_{VIN}$ voltage increasing - measured at VIN | | 200 | | mV |
| **INTERNAL REFERENCES** | | | | | | |
| $V_{O(VLDO5)}$ | LDO5V output | VIN = 5.4 V to 21 V, 10-mA load | 4.9 | 5.0 | 5.1 | V |
| Line regulation $V_{O(LDO5V)}$ | Line regulation for regulator over operating voltage range | VIN = 5.4 V to 21 V, Measured as (?$V_{O(LDO5V)}$/$V_{O(LDO5V)}$) over this operating range with 40mA load current. measured at LDO5V pin with respect to AGND pin | | | 0.5% | |
| Load regulation $V_{O(LDO5V)}$ | Load regulation for regulator over operating current range | VIN = 5.4V to 21V Measured as (?$V_{O(LDO5V)}$/$V_{O(LDO5V)}$) over this operating range with 10mA to 100mA load current. measured at LDO5V pin with respect to AGND pin | | | 2% | |
| $I_{SC\ (LDO5V)}$ | Over current protection | Measured at 90% of the regulation voltage | 115 | | | mA |
| $C_{O\ (LDO5V)}$ | External output capacitance range after derating | Actual capacitance after derating. ex: 2.7-µF capacitance, then use a 4.7-µF capacitor with 60% derating at 5 V | 2.7 | 4.7 | 10 | µF |
| $V_{O(VREF1V25)}$ | VREF1V25 output - Internal buffered bandgap output | See below for output capacitance. measured at VREF1V25 pin with respect to AGND pin | 1.244 | 1.25 | 1.256 | V |
| $C_{O\ (VREF1V25)}$ | External output capacitance range after derating | Actual capacitance after derating. ex: 0.27-µF capacitance, then use a 0.47-µF capacitor with 60% derating at 1.25 V | 0.2 | | 1 | µF |
| $V_{I(LDO3V)}$ | LDO3V input | Parametric and functional | 5.4 | 7.4 | 21 | V |
| $V_{I(LDO3V)}$ | LDO3V input | Functional | 3.45 | 7.4 | 24 | V |
| $V_{O(LDO3V)}$ | LDO3V output | VIN = 7.4 V, 1mA load | 3.267 | 3.3 | 3.333 | V |
| $I_{O\ (LDO3V)}$ | Output current | Maximum current for external user is limited 40mA | | | 40 | mA |

## Electrical Characteristics: Control *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SC\ (LDO3V)}$ | Output circuit current limit | Measured at 90% of the regulation voltage | 75 | | | mA |
| Line regulation $V_{O(LDO3V)}$ | Line regulation for regulator over operating voltage range | VIN = 5.4 V to 21 V, Measured as (?$V_{O(LDO3V)}$/$V_{O(LDO3V)}$) over the operating range with 20mA load current. measured at LDO3V pin with respect to AGND pin | | | 0.5% | |
| Load regulation $V_{O(LDO3V)}$ | Load regulation for regulator over operating current range | VIN = 7.4 Measured as (?$V_{O(LDO3V)}$/$V_{O(LDO3V)}$) over this operating range with 0mA to 50mA load current. measured at LDO3V pin with respect to AGND pin | | | 0.5% | |
| $C_{O\ (LDO3V)}$ | External output capacitance range after derating | Actual capacitance after derating, for example: 2.7-µF capacitance, then use a 4.7uF capacitor with 60% derating at 3.3 V | 2.2 | 4.7 | 10 | µF |
| $t_{r\ (LDO3V)}$ | Rise time | Measured from 5% to 95% of the output voltage with 2.2 µF | 300 | | 450 | µs |
| **I/O BUFFER, DDR_VTT_CTRL** | | | | | | |
| $V_{IL\_DDR\_VTT\_CTRL}$ | DDR_VTT_CTRL input-low voltage | Input-low voltage threshold | | | 0.49 | V |
| $V_{IH\_DDR\_VTT\_CTRL}$ | DDR_VTT_CTRL input-high voltage | Input-high voltage threshold | 0.61 | | | V |
| $V_{HYST\_DDR\_VTT\_CTRL}$ | DDR_VTT_CTRL hysteresis voltage | Hysteresis voltage | | 70 | | mV |
| $I_{leakage\_DDR\_VTT\_CTRL}$ | DDR_VTT_CTRL input current | Input current, Clamped to 1 V | | 0.01 | 0.2 | µA |
| **INPUT TTL BUFFERS (ALL INPUT PINS), (DEFAULT: $\overline{\text{SHUTDOWN}}$, $\overline{\text{STANDBY}}$, NU, EN3V3SW, EN5VSW, ENVR1, ENVR2, ENVR3, ENVR4, ENVR5, V33APCH_ENIN, V18U25U_ENIN, ENC, V5ADS3_ENIN, VCCIO_ENIN, V33ADSW_ENIN, SLP_SUS, SLP_S3, SRAIL_ENIN, INB, NU)** | | | | | | |
| $V_{IL\_INPUTS}$ | Input-low voltage | | | | 0.4 | V |
| $V_{IH\_INPUTS}$ | Input-high voltage | | 1.2 | | | V |
| $V_{HYST\_INPUTS}$ | Hysteresis voltage | | | 300 | | mV |
| $I_{leakage\_INPUTS}$ | Input current | Clamped on 3.3 V | | 0.01 | 0.3 | µA |
| $V_{IL\_PWRBTNZ}$ | Input-low voltage for PWRBTNZ | | | | 0.4 | V |
| $V_{IH\_PWRBTNZ}$ | Input-high voltage for PWRBTNZ | Internal 5-kΩ pullup resistor between PWRBTNZ pin and VDDIO | 1.6 | | | V |
| $V_{HYST\_PWRBTNZ}$ | Hysteresis voltage for PWRBTNZ | | | 580 | | mV |
| $I_{Output\_PWRBTNZ}$ | Output current for PWRBTNZ when power button is pressed to close and pulling PWRBTNZ to GND | PWRBTNZ = GND, Internal 5kΩ pullup resistor between PWRBTNZ pin and VDDIO | | 660 | 790 | µA |
| $t_{\overline{EC\_ONOFF}\_Debouinc\_0e}$ | $\overline{\text{EC\_ONOFF}}$ debounce time, 0-ms setting | Time set to 0 ms, Measured from 0.5% PWBTNZ rising to 5% of the $\overline{\text{EC\_ONOFF}}$ output | | 0 | | ms |
| $t_{\overline{EC\_ONOFF}\_Debouinc\_30e}$ | $\overline{\text{EC\_ONOFF}}$ debounce time, 30-ms setting | Time set to 30 ms, Measured from 0.5% PWBTNZ rising to 5% of the $\overline{\text{EC\_ONOFF}}$ output | | 30 | | ms |
| **VDDIO DOMAIN PUSH-PULL OUTPUTS, ($\overline{\text{RESET}}$, 1Hz, DS3_VREN, PGVR1, PGVR2, PGVR3, PGVR5)** | | | | | | |
| $V_{PP}$ | Pullup output voltage supply | Pulled up to VDDIO pin which should by tied to LDO3V pin = 3.3 V | | VDDIO | | V |
| $V_{OL\_PP}$ | Low-level output voltage | $I_{OL}$ = 3 mA | | | 0.6 | V |
| $V_{OH\_PP}$ | High-level output voltage | $I_{OH}$ = 3 mA | VDDIO – 0.6 | | | V |

## Electrical Characteristics: Control *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VDDPG DOMAIN PUSH-PULL OUTPUTS, (V33APCH_PG, V18U25U_ENOUT, PGC, VCCIO_ENOUT, V33APCH_ENOUT, V18S_PG, V5ADS3_PG, V5ADS3_ENOUT, V33SDSW_ENOUT)** | | | | | | |
| $V_{PP}$ | Pullup output voltage supply | Pulled up to VDDPG pin | | VDDPG | | V |
| $V_{OL\_PP}$ | Low-level output voltage | $I_{OL}$ = 3 mA | | | 0.6 | V |
| $V_{OH\_PP}$ | High-level output voltage | $I_{OH}$ = 3 mA | VDDPG – 0.6 | | | V |
| **GENERAL OPEN-DRAIN OUTPUTS, ($\overline{\text{ACSWON}}$, $\overline{\text{BAT1SWON}}$, $\overline{\text{BAT2SWON}}$, VCCST_PWRGD, SYS_PWROK, PCH_PWROK, RSMRST_PWRGD, ALL_SYS_PWRGD, $\overline{\text{PMIC\_INT}}$, $\overline{\text{EC\_RST}}$, PCH_PWRBTN, $\overline{\text{EC\_ONOFF}}$, DPWROK, V105S_PG, PGVR4, BC_ACOK)** | | | | | | |
| $V_{OL\_OD1}$ | OD output voltage | $I_{OL}$ = 2 mA | | | 0.4 | V |
| $I_{LK\_OD1}$ | OD leakage current | $V_{(PIN)}$ = 3.3 V | | | 0.45 | µA |
| **OPEN-DRAIN OUTPUT (TEMP_ALERT)** | | | | | | |
| $V_{OL\_OD}$ | Open-drain low level output voltage | $I_{OL}$ = 15 mA, with 75-Ω pullup resistor to 1 V | | | 0.165 | V |
| $I_{LK\_OD}$ | Open-drain leakage current | $V_{(PIN)}$ = 3.3 V, with 75-Ω pullup resistor to 1 V | | | 0.35 | µA |
| **TRISTATE INPUT BUFFER (SLAVEADDR, DDRID)** | | | | | | |
| $V_{IL\_TRISTATE}$ | Low-level input voltage | $I_{OL}$ = 6 µA | | | 0.33 | V |
| $V_{IH\_TRISTATE}$ | High-level input voltage | $I_{OH}$ = 6 µA | 1.8 | | | V |
| $I_{TRISTATE}$ | $I_{TRISTATE}$ current | Maximum allowable current in or out of pin when floating to maintain FLOAT logic state | –0.650 | | 0.675 | µA |
| $I_{TRISTATE\_TOTAL\_PIN\_GND}$ | Total current drawn when pin connected to GND | VINLDO3 current when TRISTATE pin = GND | | | 6 | µA |
| $I_{TRISTATE\_TOTAL\_PIN\_3.3V}$ | Total current drawn when pin connected to 3.3 V | VINLDO3 current when TRISTATE pin = LDO3V = 3.3 V | | | 6 | µA |
| $I_{TRISTATE\_TOTAL\_PIN\_FLOAT}$ | Total current drawn when pin floating | VINLDO3 current when TRISTATE pin = Floating | | | 4.5 | µA |
| **EXTERNAL RAIL POWER GOOD COMPARATORS (V33APCH, V18U25U, VSC, V5ADS3, VCCIO, V33ADSW, V33S, V18S, V105S, INH)** | | | | | | |
| | VSx input voltage range | When VSx configured as voltage sense input | 0.7 | | 5 | V |
| | VSx input leakage current | When VSx configured as voltage sense input, VSx = 5.7V | 0 | | 9 | µA |
| | Power-good exit threshold high, VSx | VSx rising out of power-good. When VSx configured as voltage sense input and power-good window comparator. | 106% | 108% | 110% | |
| | Power-good threshold high, VSx hysteresis | VSx falling into power-good. When VSx configured as voltage sense input and power-good window comparator. | | –3% | | |
| | Power-good exit threshold low, VSx | VSx falling out of power-good. When VSx configured as voltage sense input and power-good window comparator. | 90% | 92% | 94% | |
| | Power-good threshold low, VSx hystersis | VSx rising into power-good. When VSx configured as voltage sense input and power-good window comparator. | | 3% | | |
| $T_{VSx\_POWERGOOD\_DEGLITCH}$ | Power-good deglitch time for both rising and falling edges | VSx voltage must cross power-good threshold and stay for at least this time to change power-good output state.Measured from VSx into or out of power-good threshold, until PGx toggles, for both rising and falling edges. | 27 | 30 | 33 | µs |

## 5.6 Electrical Characteristics: Embedded Controller Reset

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL\_OD}$ | $\overline{EC\_RST}$ output-low voltage | $I_{OL}$ = 2 mA, $V_{EC\_RST}$ = 3.3 V | | | 0.4 | V |
| $I_{LKG\_OD}$ | $\overline{EC\_RST}$ leakage current | Output buffer in open-drain mode, $V_{EC\_RST}$ = 3.3 V | | 0.01 | 0.2 | µA |
| $t_{RST}$ | EC_RST time duration | Reset-timer register value: 00b | | 20 | | ms |
| | | Reset-timer register value: 01b | | 40 | | |
| | | Reset-timer register value: 10b | | 80 | | |
| | | Reset-timer register value: 11b (default | | 200 | | |
| $I_{LK}$ | ECVCC input quiescent current | | | | 3 | µA |
| $V_{TH}$ | ECVCC voltage threshold | Reset-voltage threshold register value: 000b | 1.344 | 1.4 | 1.456 | V |
| | | Reset-voltage threshold register value: 001b | 1.44 | 1.5 | 1.56 | |
| | | Reset-voltage threshold register value: 010b | 1.536 | 1.6 | 1.664 | |
| | | Reset-voltage threshold register value: 011b | 1.632 | 1.7 | 1.768 | |
| | | Reset-voltage threshold register value: 100b | 2.304 | 2.4 | 2.496 | |
| | | Reset-voltage threshold register value: 101b | 2.496 | 2.6 | 2.704 | |
| | | Reset-voltage threshold register value: 110b | 2.688 | 2.8 | 2.912 | |
| | | Reset-voltage threshold register value: 111b | 2.88 | 3.0 | 3.12 | |

## 5.7 Electrical Characteristics: Power-Path Comparators and Critical Supply Voltage

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ACIN, BAT1, BAT2, VDCSNS** | | | | | | |
| | Output-low saturation voltage for open-drain logic output pin ($\overline{TRIP}$) | Comparator input voltage > internal reference voltage, Output pulling low, Sink current = 5 mA | | | 0.5 | V |
| | Internal current source, IOUT VCOMP | Current out of the VCOMP pin when IOUT VCOMP enabled | 9.5 | 10 | 10.6 | µA |
| | Internal reference voltage, VREF_VCOMP_rising | $\overline{Rising}$ voltage at VCOMP pin, changes $\overline{TRIP}$ to logic low | 1.211 | 1.223 | 1.235 | V |
| | Internal hysteresis voltage, VHYST VCOMPFalling | $\overline{Falling}$ voltage at VCOMP pin, changes $\overline{TRIP}$ to logic high | | 61 | | mV |
| | Output-low saturation voltage for open-drain logic output pin ($\overline{ACSWON}$, $\overline{BAT1SWON}$, $\overline{BAT2SWON}$) | Comparator input voltage > internal reference voltage, Output pulling low, Sink current = 5 mA | | | 0.5 | V |
| $I_{LKG}$ | ACIN, BAT1, BAT2 - Current leakage | Current into the ACIN, BAT1, or BAT2 pins from 5.4 V to 24 V (when pin is below, at, or above 6V internal protection switch.) | | | 0.1 | µA |
| $V_{REF\_PP}$ | Internal reference voltage, VREF_ACIN_rising | $\overline{Rising}$ voltage at ACIN pin, makes $\overline{ACSWON}$ trigger low | 1.2365 | 1.25 | 1.2645 | V |
| $V_{HYST\_PP}$ | Internal hysteresis voltage, VHYST_ACIN_falling | Falling voltage with respect to $\overline{VREF\_ACIN}$ at ACIN pin, makes $\overline{ACSWON}$ trigger high | | 125 | | mV |

## Electrical Characteristics: Power-Path Comparators and Critical Supply Voltage *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REF\_PP}$ | Internal reference voltage, VREF_BAT1_rising | Rising voltage at BAT1 pin, makes BAT1SWON trigger low | 1.2365 | 1.25 | 1.2645 | V |
| $V_{HYST\_PP}$ | Internal hysteresis voltage, VHYST_BAT1_falling | Falling voltage with respect to VREF_BAT1 at BAT1 pin, makes BAT1SWON trigger high | | 125 | | mV |
| $V_{REF\_PP}$ | Internal reference voltage, VREF_BAT2_rising | Rising voltage at BAT2 pin, makes BAT2SWON trigger low | 1.2365 | 1.25 | 1.2645 | V |
| $V_{HYST\_PP}$ | Internal hysteresis voltage, VHYST_BAT2_falling | Falling voltage with respect to VREF_BAT2 at BAT1 pin, makes BAT2SWON trigger high | | 125 | | mV |
| | Critical supply voltage (VDCSNS) falling threshold | Critical supply voltage threshold register value VDLMTCRT[3:0] = 0101b, Supply voltage decreasing. With a resistor divider from VDC to VDCSNS with 4R top, R bottom, VDC = 6 V when VDCSNS pin = 1.12 V. | 1.10 | 1.12 | 1.14 | V |
| | Critical supply voltage (VDCSNS) rising threshold hysteresis | Supply voltage increasing, With a resistor divider from VDC to VDCSNS with 4R top, R bottom, VDC_hyst = 100 mV when VDCSNS_hyst pin = 20 mV | | 20 | | mV |
| | Critical supply voltage (VDCSNS) input current | VDCSNS = 1.2 V to 1.75 V | | 0.01 | 0.1 | µA |
| **INTERNAL RAMP COMPARATOR** | | | | | | |
| Vramp_comp_VIN_rising | Rising voltage at VIN pin, makes internal ramp compensation of all controllers slightly smaller | | 10.5 | 11 | 11.5 | V |
| Vramp_comp_VIN_falling_hyst | Falling voltage hysteresis at VIN pin, makes the internal ramp compensation of all controllers slightly bigger | | | 1.1 | | V |

## 5.8 Electrical Characteristics: AC-Adapter Detection

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | ACOK input-low voltage | | | | 0.4 | V |
| $V_{IH}$ | ACOK input-high voltage | | 1.2 | | | V |
| | ACOK input current | ACOK = 3.3 V | | 0.01 | 0.1 | µA |
| | Adapter detection debounce time | ACOKDB register value: 00b | 50 | 61 | 95 | µs |
| | | ACOKDB register value: 01b | 7 | 10 | 13 | ms |
| | | ACOKDB register value: 10b | 15 | 20 | 25 | |
| | | ACOKDB register value: 11b (default) | 24 | 30 | 36 | |

## 5.9 Electrical Characteristics: Emergency Reset Shutdown

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{UVLO\_shutdown}$ | UVLO low shutdown time | Time from VIN < UVLO5 low threshold until shutdown | | | 1 | µs |
| $t_{\overline{SHUTDOWN}\_shutdown}$ | $\overline{SHUTDOWN}$ low shutdown time | Time from $\overline{SHUTDOWN}$ pin falling-edge until shut down. | | | 1 | µs |
| $t_{PWRGD\_Fault\_shutdown}$ | PWRGD fault shutdown time | Time from PWRGD fault detected including deglitch time until shut down. Output voltage is overvoltage or undervoltage | 27 | 30 | 33 | µs |
| $t_{CRIT\_Temp\_shutdown}$ | CRITICAL temperature high shutdown time | Time from $T_J > T_{CRIT\_Temp}$ including deglitch time until shut down, Deglitch time can be changed from 5 µs to 300 µs | | | 5 | µs |
| $t_{SDWNCTRL\_bit\_shutdown}$ | SDWNCTRL bit set to 1 shutdown time | Time from SDWNCTRL register (0x49) bit 0 set to 1b until shutdown, Time after SDWNCTRL register is written to by $I^2C$ | | | 1 | µs |

## 5.10 Electrical Characteristics: Voltage Regulators (VR1, VR3, VR4, VR5)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| $V_{IN}$ | Input voltage | Parametric and functional | 5.4 | 7.4 | 21 | V |
| | | Functional | 5.4 | 7.4 | 24 | |
| $t_{SS\_total}$ | Soft-Start total turnon time (start-up time + output ramp-up time) | Time to start switching from enable to 95% of $V_{OUT}$, Continuous slope (no slope reversal) | 770 | 876 | 1000 | µs |
| $t_{SS\_delay}$ | Soft-start delay time | Delay time from enable to first switching pulse | 120 | 136 | 150 | µs |
| $t_{SS}$ | Soft-start ramp-up time | From first switching pulse to 95% of $V_{OUT}$, Continuous slope (no slope reversal) | 650 | 740 | 850 | µs |
| $SS_{PG\_Mask}$ | Power-good mask time during & after soft-start ramp-up time | | 9 | 10 | 11 | ms |
| $PG_{Threshold}$ | Power-good exit threshold | Percentage of nominal $V_{OUT}$ | ±5.5% | ±8% | ±10.5% | |
| $PG_{HYS}$ | Power-good hysteresis | Percentage of nominal $V_{OUT}$ | | 3% | | |
| $PG_{deglitch}$ | Power-good deglitch time | Time measured from FBVRxP crossing power good threshold to PGVRx toggling\ (for both rising and falling edges) | 27 | 30 | 33 | µs |
| $DRVH_{Rout\_H}$ | DRVH resistance, high | Source, IDRVH = –50 mA | | 3.0 | 4.5 | Ω |
| $DRVH_{Rout\_L}$ | DRVH resistance, low | Sink, IDRVH = 50 mA | | 2.0 | 3.5 | Ω |
| $DRVL_{Rout\_H}$ | DRVL resistance, high | Source, IDRVL = –50 mA | | 3.0 | 4.5 | Ω |
| $DRVL_{Rout\_L}$ | DRVL resistance, low | Sink, IDRVL = 50 mA | | 0.8 | 2.0 | Ω |
| $t_{dead\_fall}$ | Dead time, fall | DRVH off to DRVL on | | 10 | | ns |
| $t_{dead\_rise}$ | Dead time, rise | DRVL off to DRVH on | | 20 | | ns |
| $t_{ON\_min}$ | High-side driver minimum on-time | DRVH on | 65 | 80 | 105 | ns |
| $t_{OFF\_min}$ | High-side driver minimum off-time | DRVH off | 235 | 260 | 285 | ns |
| $Force\_PWM_{PWM-PFM\ Transition}$ | Time that PWM is forced to remain on once zero crossing comparator detects PWM to PFM transition | Cycles is the number of pulses on the switch node | 16 | 16 | 16 | cycles |
| **CURRENT LIMIT** | | | | | | |
| $I_{TRIP}$ | Current limit pin source current | $T_A$ = 25°C | 45 | 50 | 55 | µA |
| $TC_{ILIM\_LS}$ | External low-side FET $R_{DSon}$ current limit temperature coefficient | $T_A$ = 25°C | | 4780 | | ppm/°C |

## Electrical Characteristics: Voltage Regulators (VR1, VR3, VR4, VR5) *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $TC_{ILIM\_HS}$ | External high-side FET $R_{DSon}$ current limit temperature coefficient | $T_A$ = 25°C | | 3300 | | ppm/°C |
| $V_{ILIM}$ | Current-limit pin setting voltage range | $V_{ILIM} = R_{CS} \times I_{TRIP}$ (usable voltage range across the operating temperature range) | 0.2 | | 2 | V |
| **DVS AND DECAY** | | | | | | |
| $t_{DVS\_total}$ | DVS total fall and rise time (delay time + output ramp time) | Time to start switching from enable to 5% of $V_{OUT}$, Continuous slope (no slope reversal), For $V_{OUT}$ change = 300 mV | 56 | 61.25 | 68.5 | µs |
| $t_{DVS\_delay}$ | DVS delay time for falling and rising edge | DVS delay time from when $\overline{STANDBY}$ changes from High to Low, until the output voltage begins to fall. | 1 | 1.25 | 1.5 | µs |
| $t_{DVS\_ramp}$ | DVS ramp time for falling and rising edge | From first switching pulse to 5% of $V_{OUT}$, Continuous slope (no slope reversal), Total ramp time = (($V_{OUT}$ – $V_{OUT}$ change) / slew rate), For $V_{OUT}$ change = 300 mV | 55 | 60 | 67 | µs |
| $DVS_{slew\ rate}$ | DVS slew rate for falling and rising edge | DVS falling edge slew rate for $V_{OUT}$ to change from the upper target to the lower target after $\overline{STANDBY}$ ($\overline{SLP\_S0}$) changes from high to low | 4.5 | 5 | 5.5 | mV/µs |
| $t_{decay\_total}$ | Decay exit total turnon time (delay time + output ramp-up time) | time to start switching from enable to 95% of $V_{OUT}$, Continuous slope (no slope reversal). For $V_{OUT}$ target = 0.95 V | 69 | 79 | 99 | µs |
| $t_{decay\_delay}$ | Decay exit delay time for rising edge | Decay delay time from when $\overline{STANDBY}$ changes from low to high, until the output voltage begins to rise. | 10 | 12 | 16 | µs |
| $t_{decay\_ramp}$ | Decay exit ramp time for rising edge | From first switching pulse to 95% of $V_{OUT}$, Continuous slope (no slope reversal). Total ramp time = (($V_{OUT}$ – 0 V) / slew rate). For $V_{OUT}$ target = 0.95 V | 59 | 67 | 83 | µs |
| $Exit\ Decay_{slew\ rate}$ | Decay exit slew rate for rising edge | Decay rising edge slew rate for $V_{OUT}$ to change from the lower target to the upper target after $\overline{STANDBY}$ changes from low to high | 12 | 15 | 17 | µs |
| $DVS_{PG\_Mask}$ | Power good mask time during DVS ramp | | $t_{DVS\_ramp}$ + 90 | $t_{DVS\_ramp}$ + 100 | $t_{DVS\_ramp}$ + 110 | µs |
| $Force\_PWM_{DVS}$ | Time that PWM is forced to remain on after DVS ramp | | $t_{DVS\_ramp}$ + 9 | $t_{DVS\_ramp}$ + 10 | $t_{DVS\_ramp}$ + 11 | µs |
| **OUTPUT DISCHARGE** | | | | | | |
| $R_{VRdis}$ | Output auto discharge resistance | Discharge register value: 00b (default) | 1000 | | | kΩ |
| | | Discharge register value: 01b | 90 | 125 | 160 | Ω |
| | | Discharge register value: 10b | 170 | 225 | 315 | |
| | | Discharge register value: 11b | 450 | 550 | 690 | |
| $FB_{Rin}$ | Controller feedback input resistance | Controller enabled | | 1 | 2.25 | MΩ |
| $R_{internal\_Boot}$ | Bootstrap internal-switch on resistance ($R_{DSon}$) | –40°C = $T_A$ = 125°C | | 15 | 25 | Ω |
| **VR1 CONTROLLER** | | | | | | |
| $V_{OUT}$ | Output voltage | Power-save mode disabled ($\overline{STANDBY}$ = high, and V105ACNT[5:4] = 00b [default]) | | 1.05 | | V |
| | VR1 maximum line regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VIN}$ = 5.4 V to 21 V, $I_{OUT}$ = 6 A | -0.5% | | 0.5% | |

## Electrical Characteristics: Voltage Regulators (VR1, VR3, VR4, VR5) *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | VR1 maximum load regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VIN}$ = 7.4 V, $I_{OUT}$ = 0 A to 10 A, | -0.5% | | 0.61% | |
| | VR1 switching frequency | $V_{IN}$ = 7.4 V, PWM mode ($\overline{NVDC}$ = 3.3 V = programmed to low switching frequency) | | 625 | | kHz |
| | | $V_{IN}$ = 7.4 V, PWM mode ($\overline{NVDC}$ = GND = programmed to high switching frequency) | | 1000 | | kHz |
| **VR3 CONTROLLER** | | | | | | |
| $V_{OUT}$ | Output voltage | Power-save mode disabled ($\overline{STANDBY}$ = high, and VCCIOCNT[5:4] = 00b [default]) | | 3.3 | | V |
| | VR3 maximum line regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VIN}$ = 5.4 V to 21 V, $I_{OUT}$ = 6 A | -0.5% | | 0.65% | |
| | VR3 maximum load regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VIN}$ = 7.4 V, $I_{OUT}$ = 0 A to 10 A | -0.5% | | 0.55% | |
| | VR3 switching frequency | $V_{IN}$ = 7.4 V, PWM mode ($\overline{NVDC}$ = 3.3 V = programmed to low switching frequency) | | 625 | | kHz |
| | | $_{IN}$ = 7.4 V, PWM mode ($\overline{NVDC}$ = GND = programmed to high switching frequency) | | 1000 | | kHz |
| **VR4 CONTROLLER** | | | | | | |
| $V_{OUT}$ | Output voltage | Power-save mode disabled (DDR_VTT_CTRL = low, and V12UCNT[5:4] = 00b) | | 1.2 | | V |
| | | Power-save mode disabled (DDR_VTT_CTRL = high, and V12UCNT[5:4] = 00b) | | 1.35 | | |
| | | Power-save mode disabled (DDR_VTT_CTRL = float, and V12UCNT[5:4] = 00b) | | 1.1 | | |
| | VR4 maximum line regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VIN}$ = 5.4 V to 21 V, $I_{OUT}$ = 6 A | –0.5% | | 0.5% | |
| | VR4 maximum load regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VIN}$ = 7.4 V, $I_{OUT}$ = 0 A to 10 A | –0.5% | | 0.65% | |
| | VR4 switching frequency | $V_{IN}$ = 7.4 V, PWM mode ($\overline{NVDC}$ = 3.3 V = programmed to low switching frequency) | | 625 | | kHz |
| | | $V_{IN}$ = 7.4 V, PWM mode ($\overline{NVDC}$ = GND = programmed to high switching frequency) | | 1000 | | kHz |
| **VR5 CONTROLLER** | | | | | | |
| $V_{OUT}$ | Output voltage | Power-save mode disabled ($\overline{STANDBY}$ = high, and VPRIMCORECNT[5:4] = 00b) | | 1.05 | | V |
| | VR5 maximum line regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VIN}$ = 5.4 V to 21 V, $I_{OUT}$ = 6 A | –0.5% | | 1.05% | |
| | VR5 maximum load regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VIN}$ = 7.4 V, $I_{OUT}$ = 0 A to 10 A | –0.5% | | 0.75% | |
| | VR5 switching frequency | $V_{IN}$ = 7.4 V, PWM mode ($\overline{NVDC}$ = 3.3 V = programmed to low switching frequency) | | 625 | | kHz |
| | | $V_{IN}$ = 7.4 V, PWM Mode ($\overline{NVDC}$ = GND = programmed to high switching frequency) | | 1000 | | kHz |

## 5.11 Electrical Characteristics: VR2 Converter

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER** | | | | | | |
| $V_{IN}$ | $V_{VINVR2}$ power input voltage | Parametric and functional, $V_{VIN}$ = 5.4 V to 21 V | 3.135 | 3.3 | 3.465 | V |
| | | Functional, $V_{VIN}$ = 5.4 V to 24 V | 2.97 | 3.3 | 3.63 | |
| $V_{OUT}$ | Output voltage | Power-save mode disabled ($\overline{STANDBY}$ = high and V18ACNT[5:4] = 10b) | | 1.8 | | V |
| $I_{OUT}$ | Maximum average output current range | $V_{VINVR2}$ = 2.97 V to 3.63 V | 2500 | | | mA |
| $I_{LIM}$ | Low-side valley cycle-by-cycle positive current limit | $V_{VINVR2}$ = 2.97 V to 3.63 V | 2260 | | 3360 | mA |
| $I_{nLIM}$ | Low-side valley cycle-by-cycle negative current limit | $V_{VINVR2}$ = 2.97 V to 3.63 V | 1400 | | 1875 | mA |
| $HS\_R_{DSon}$ | High-side switch on resistance | $V_{VINVR2}$ = 3.3 V, 100% duty cycle | 30 | | 105 | mO |
| $LS\_R_{DSon}$ | Low-side switch on resistance | $V_{VINVR2}$ = 3.3 V, 0% duty cycle | 30 | | 95 | mO |
| | Maximum line regulation | With respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VINVR2}$ = 2.97 V to 3.63 V, $I_{OUT}$ = $I_{max}$, All output voltages, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P – FBVR2N). | –0.5% | | 0.5% | |
| | Maximum load regulation | PWM mode with respect to nominal $V_{OUT}$ ULQ/auto mode, $V_{VINVR2}$ = 2.97 V to 3.63 V, $I_{OUT}$ = 0 A to $I_{max}$, All output voltages, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P – FBVR2N). | –0.5% | | 0.5% | |
| | | AUTO mode with respect to nominal $V_{OUT}$ ULQ/auto Mode, $V_{VINVR2}$ = 2.97 V to 3.63 V, $I_{OUT}$ = 0 A to $I_{max}$, All output voltages, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P – FBVR2N). | –0.65% | | 1% | |
| $f_{SW}$ | Switching frequency | PWM mode, $I_{OUT}$ = 2 A | 1700 | 2000 | 2300 | KHz |
| $t_{on}$ | Soft-Start total turnon time (start-up time + output ramp-up time) | Time to start switching from enable to 95% of $V_{O(min)}$, Continuous slope (no slope reversal) | 730 | 800 | 1050 | µs |
| $t_{delay}$ | Enable delay time | Delay time from enable to first switching pulse. | 120 | 135 | 150 | µs |
| $t_{SS}$ | Soft-Start ramp-up time | From first switching pulse to 95% of $V_{O(min)}$, Continuous slope (no slope reversal) | 610 | 665 | 900 | µs |
| $SS_{PG\_Mask}$ | Power-good mask time during and after soft-start ramp-up time | | 9 | 10 | 11 | ms |
| $t_{DVS\_total}$ | DVS total fall and rise time (delay time + output ramp time) | Time to start switching from enable to 5% of $V_{OUT}$, Continuous slope (no slope reversal), For $V_{OUT}$ change = 300 mV) | 56 | 61.25 | 68.5 | µs |
| $t_{DVS\_delay}$ | DVS delay time for falling and rising edge | DVS delay time from when $\overline{STANDBY}$ changes from high to Low, until the output voltage begins to fall | 1 | 1.25 | 1.5 | µs |

## Electrical Characteristics: VR2 Converter *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{DVS\_ramp}$ | DVS ramp time for falling and rising edge | From first switching pulse to 5% of $V_{OUT}$, Continuous slope (no slope reversal), Total ramp time = ([$V_{OUT}$ – $V_{OUT}$ change] / slew rate). For $V_{OUT}$ change = 300 mV | 55 | 60 | 67 | µs |
| $DVS_{slew\ rate}$ | DVS slew rate for falling and rising edge | DVS falling edge slew rate for $V_{OUT}$ to change from the upper target to the lower target after $\overline{STANDBY}$ (SLP_S0) changes from high to low. | 4.5 | 5 | 5.5 | mV/µs |
| $DVS_{PG\_Mask}$ | Power-good mask time during DVS ramp | | $t_{DVS\_ramp}$ + 90 | $t_{DVS\_ramp}$ + 100 | $t_{DVS\_ramp}$ + 110 | µs |
| $Forced\_PWM_{DVS}$ | Time that PWM is forced to remain on after DVS ramp | | $t_{DVS\_ramp}$ + 9 | $t_{DVS\_ramp}$ + 10 | $t_{DVS\_ramp}$ + 11 | µs |
| $R_{VRdis}$ | Output auto discharge resistance | Discharge register value, DISCHGCNT3[7:6] = 00b | 250 | 860 | 1450 | kΩ |
| | | Discharge register value, DISCHGCNT3[7:6] = 01b | 80 | 100 | 120 | Ω |
| | | Discharge register value, DISCHGCNT3[7:6] = 10b | 160 | 200 | 240 | |
| | | Discharge register value, DISCHGCNT3[7:6] = 11b (default) | 400 | 500 | 600 | |
| $FB_{Rin}$ | Feedback input resistance | Enabled | | | 3 | MΩ |
| $Iq\_VR2_{LDO3V\_VREGVR2}$ | Quiescent current on LDO3V and VREGVR2 with converter when enabled | $I_{OUT}$ = 0 mA, enabled, at $T_A$= 25°C, Not switching, Measured at LDO3V, VREGVR2 | | 30 | 55 | µA |
| $I_{SD}$ | Shutdown current into VIN, Currents from LDO3V, VREGVR2 and 1V25 supplies | $V_{VINVR2}$ = 3.63 V, disabled, at $T_A$= 25°C | | | 3 | µA |
| **CONTROL** | | | | | | |
| $PG_{Threshold}$ | Power-good exit threshold | Percentage of nominal $V_{OUT}$ | ±5.5% | ±8% | ±10.5% | |
| $PG_{HYS}$ | Power-good hysteresis | Percentage of nominal $V_{OUT}$ | | 3% | | |
| $PG_{deglitch}$ | Power-good deglitch time | Time measured from FBVRxP crossing power-good threshold to PGVRx toggling (for both rising and falling edges) | 27 | 30 | 33 | µs |
| $T_{HOT}$ | Overtemperature protection Hot Warning | | 120 | | 140 | °C |
| $T_{HOT\_hys}$ | Overtemperature hysteresis Hot Warning | | | 10 | | °C |
| $T_{SHUTDOWN}$ | Overtemperature protection Shutdown | | 130 | | 160 | °C |
| $T_{SHUTDOWN\_hys}$ | Overtemperature hysteresis Shutdown | | | 10 | | °C |

## 5.12 Electrical Characteristics: LDO1 Regulator

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER** | | | | | | |
| $V_{OUT}$ | Output voltage | DDRID = 0 V, VOUTLDO1 = (VINLDO1S) / 2, VINLDO1S = 1.2 V | | 0.6 | | V |
| | | DDRID = 3.3 V, VOUTLDO1 = (VINLDO1S) / 2, VINLDO1S = 1.35 V | | 0.675 | | |
| | | DDRID = Open, VOUTLDO1 = (VINLDO1S) / 2, VINLDO1S = 1.1 V | | 0.55 | | |
| $V_{OUT\_Trans}$ | Output voltage tolerance, AC and DC transient load | $I_{OUT}$ = 1 A, VINLDO1 = 1.2 V, (FBLDO1 – FBVR4N) = Output voltage relative to (VINLDO1S – FBVR4N) / 2, where VINLDO1S connected to FBVR4P on the board, Load transient from 0 mA to 70% × 1 A, dI/dt = 2.5 A/µs | –30 | | 30 | mV |
| $I_{Leak}$ | Leakage current | $T_A$ = 25°C, VIN13 = 1.2 V, LDO1 disabled | | | 5 | µA |
| $I_{Bias}$ | Bias current at VINLDO1S | $T_A$ = 25°C, Bias current measured when VINLDO1S is at 1.2 V | | | 40 | µA |
| $VLDO1_{Max\_Load}$ | Sink and source load current | Maximum current sink or source from LDO without exceeding load regulation | 1000 | | | mA |
| $VLDO1_{SC\_Limit}$ | Sink and source short-circuit current limit | Measured when $V_{OUT}$ = (1.1 ╫ nominal $V_{OUT}$) for source. Measured when $V_{OUT}$ = (0.9 × nominal $V_{OUT}$) for source | 2000 | | | mA |
| $VLDO1_{Load\_Reg}$ | Maximum load regulation | $V_{VIN}$ = 1.1 V, 1.2 V and 1.35 V, $I_{OUT}$ = 0 A to 1 A | –4.5% | | 4.5% | |
| $t_{on}$ | Total turnon time (enable + ramp) | Measure from LDO enable to $V_{OUT}$ stable, Time to ramp from 0.3 V to $V_{O(min)}$. Continuous slope (no slope reversal). Assumes $V_{VIN}$ is present, with 2 22-µF output capacitors | | | 35 | µs |
| $C_{OUT}$ | External output capacitor | Minimum actual capacitance after derating | 38 | | | µF |
| $C_{IN}$ | External input capacitor | Minimum actual capacitance after derating | 8 | | | µF |
| $R_{LDO1dis}$ | Output auto-discharge resistance | Discharge register value: 0b | 1000 | | | kΩ |
| $R_{LDO1dis}$ | Output auto-discharge resistance | Discharge register value: 1b | 60 | 80 | 100 | Ω |
| $FB_{Rin}$ | FBLDO1 input impedance | LDO1 Enabled | 20 | 25 | | MΩ |
| $I_{Q(VIN)}$ | Quiescent current into VINLDO1 | VINLDO1 = 1.35 V, $I_{LDO1}$ = 0 mA, LDO1 enabled | | 3.5 | 5 | µA |
| $I_{Q(LDO3V)}$ | Quiescent current from 3.3-V reference LDO when LDO1 is enabled | $V_{VINLDO1}$ = 1.35 V, Enabled | | | 250 | µA |
| **CONTROL** | | | | | | |
| $PG_{Threshold}$ | Power-good exit threshold | Percentage of nominal $V_{OUT}$ | ±8% | ±10% | ±12% | |
| $PG_{HYS}$ | Power-good hysteresis | Percentage of nominal $V_{OUT}$ | | ±5% | | |
| $PG_{deglitch}$ | Power-good deglitch time | Time measured from FBLDO1 crossing power good threshold to PG for LDO1 toggling. (for both rising and falling edges) | 27 | 30 | 33 | µs |
| $OVP_{temp}$ | Overtemperature protection | | 130 | 145 | 160 | °C |
| $OVP_{hys}$ | Overtemperature hysteresis | | | 10 | | °C |

## 5.13 Electrical Characteristics: Input Power Source Detection

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AC-ADAPTER DETECTION** | | | | | | |
| $V_{IL}$ | ACOK input-low voltage | | | | 0.4 | V |
| $V_{IH}$ | ACOK input-high voltage | | 1.2 | | | V |
| | ACOK input current | ACOK = 3.3 V | | 0.01 | 0.1 | µA |
| | Adapter detection debounce time | ACOKDB register value: 00b | 50 | 61 | 95 | µs |
| | | ACOKDB register value: 01b | 7 | 10 | 13 | ms |
| | | ACOKDB register value: 10b | 15 | 20 | 25 | |
| | | ACOKDB register value: 11b | 24 | 30 | 36 | |
| **POWER MONITORING (1-Hz CLOCK TO 1-Hz CLOCK - PULLED UP TO ECVCC INTERNAL PULLUP RAIL = ECVCC = 1.8 V OR 3.3 V)** | | | | | | |
| | Clock frequency (1) | | 0.8 | 1 | 1.2 | Hz |
| | Duty cycle | | | 50% | | |
| $V_{PP}$ | Pullup output voltage supply | Pulled up to ECVCC pin which should be tied to 3.3-V LDO3V pin, can also have EC_VCC pullup to 1.8 V instead of 3.3 V | | EC_VCC | | V |
| $V_{OL\_PP}$ | Low-level output voltage | $I_{OL}$ = 3 mA | | | 0.66 | V |
| $V_{OH\_PP}$ | High-level output voltage | $I_{OH}$ = 3 mA | EC_VCC – 0.66 | | | V |
| **COIN-CELL SELECTOR** | | | | | | |
| $V_{3v1LDO}$ | 3V1 LDO RTC regulation voltage | VDCIN > UVLO, LDO3V and LDO5V on, Measured at the V3P3A_RTC pin with respect to AGND. Place a 1-µF capacitor at V3P3A_RTC. (Do not exceed 2-µF actual capacitance). | 3 | 3.1 | 3.2 | V |
| $I_{3v1LDO}$ | Maximum 3V1 LDO RTC output current | Maximum output current out of 3V3RTC. | | | 1 | mA |
| $I_{Q\_bkup\_no\_VIN}$ | VBATTBKUP quiescent current, when no adapter and no main battery connected to system, automatically VBATTBKUP internally selected. internal 3.1-V LDO automatically off | $V_{VDC}$ < UVLO, $V_{BBC}$ = 2 V to 3 V, $V_{VDC}$ = 0 V | | 0.03 | 0.45 | µA |
| $I_{Q\_bkup\_with\_VIN}$ | VBATTBKUP quiescent current, when adapter or main battery connected to system, automatically VBATTBKUP internally not selected, internal 3.1-V LDO automatically on and selected. | $V_{VDC}$ > UVLO, $V_{BBC}$ = 2 V to 3 V, $V_{VDC}$ = 7.4 V | | 0.15 | 0.85 | µA |
| $R_{ext\_bkup}$ | External resistor in series with backup battery | Place between backup battery and VBATTBKUP pin, for limiting current out of backup battery | | 1 | | kΩ |

(1) All values referred to $V_{IH}$ min and $V_{IH}$ maximum levels.

## 5.14 Electrical Characteristics: I²C Interface

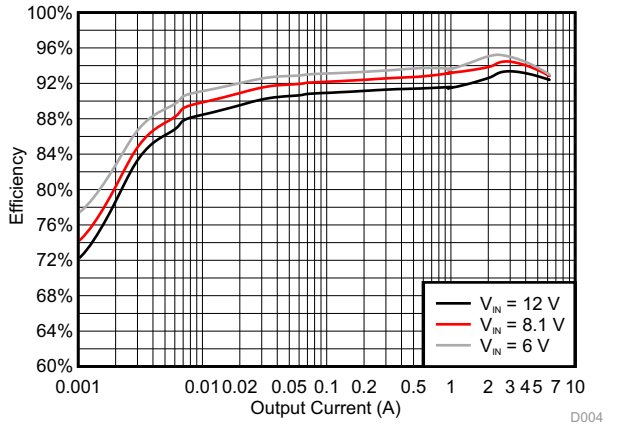
Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | SDA, SCL input-low voltage | | | | 0.4 | V |
| $V_{IH}$ | SDA, SCL input-high voltage | | 1.2 | | | V |
| | SDA, SCL input current | Clamped on 3.3 V | | 0.01 | 0.3 | µA |
| | SDA output-low voltage | $I_{SDA}$ = 5 mA (using a 354-Ω or larger external pullup resistor) | | 0.04 | 0.4 | V |
| $C_b$ | Capacitive load for SDA and SCL | | | | 400 | pF |

## 5.15 Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| I²C INTERFACE | | | | | | |
| $t_{I2C\_Rdy}$ | Minimum time for I2C to be ready after VIN > UVLO5V rising | Time after VIN rising above > $V_{UVLO\_5V\_Main}$ + $V_{Hys_5V_Main}$until OTP is loaded and I2C is ready to communicate | | | 1 | ms |
| $f_{(SCL)}$ | SCL clock frequency | Standard-mode | | | 100 | kHz |
| | | Fast-mode | | | 400 | |
| | | Fast-mode Plus | | | 1000 | |
| $t_{BUF}$ | Bus free time between a STOP and START condition | Standard-mode | 4.7 | | | µs |
| | | Fast-mode | 1.3 | | | |
| | | Fast-mode Plus | 0.5 | | | |
| $t_{HD;\ STA}$ | Hold time (repeated) START condition | Standard-mode | 4 | | | µs |
| | | Fast-mode | 600 | | | ns |
| | | Fast-mode Plus | 260 | | | ns |
| $t_{SU;\ STA}$ | Setup time for a repeated START condition | Standard-mode | 4.7 | | | µs |
| | | Fast-mode | 600 | | | ns |
| | | Fast-mode Plus | 260 | | | ns |
| $t_{SU;\ DAT}$ | Data setup time | Standard-mode | 250 | | | ns |
| | | Fast-mode | 100 | | | |
| | | Fast-mode Plus | 50 | | | |
| $t_{HD;\ DAT}$ | Data hold time | Standard-mode | 0 | | 3.45 | µs |
| | | Fast-mode | 0 | | 0.9 | µs |
| | | Fast-mode Plus | 0 | | | ns |
| $t_{rCL}$ | Rise time of SCL signal | Standard-mode | | | 1000 | ns |
| | | Fast-mode | 20 | | 300 | |
| | | Fast-mode Plus | | | 120 | |
| $t_{rDA}$ | Rise time of SDA signal | Standard-mode (using a 2.95 kΩ or smaller external pullup resistor) | | | 1000 | ns |
| | | Fast-mode (using an 885 Ω or smaller external pullup resistor) | 20 | | 300 | |
| | | Fast-mode Plus (using a 354 Ω or smaller external pullup resistor) | | | 120 | |
| $t_{fDA}$ | Fall time of SDA signal | Standard-mode | | | 300 | ns |
| | | Fast-mode | 20 x ($V_{DD}$ / 5.5 V) | | 300 | |
| | | Fast-mode Plus | 20 x ($V_{DD}$ / 5.5 V) | | 120 | |
| $t_{SU;\ STO}$ | Setup time for STOP condition | Standard-mode | 4 | | | µs |
| | | Fast-mode | 600 | | | ns |
| | | Fast-mode Plus | 260 | | | ns |

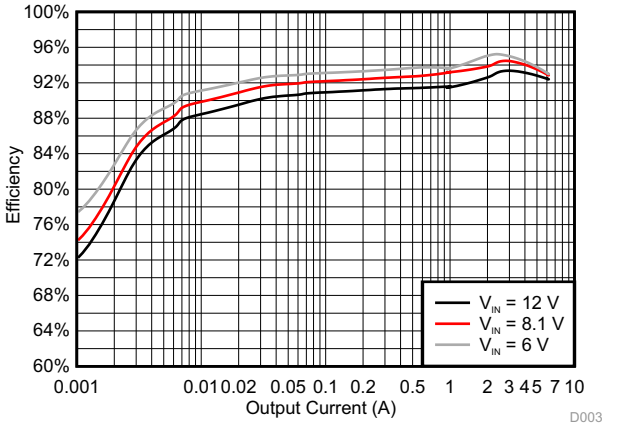
## 5.16 Typical Characteristics




Inductor: XEL4020-561ME FETs: CSD87330Q3D

$f_{SW}$ = 1 MHz

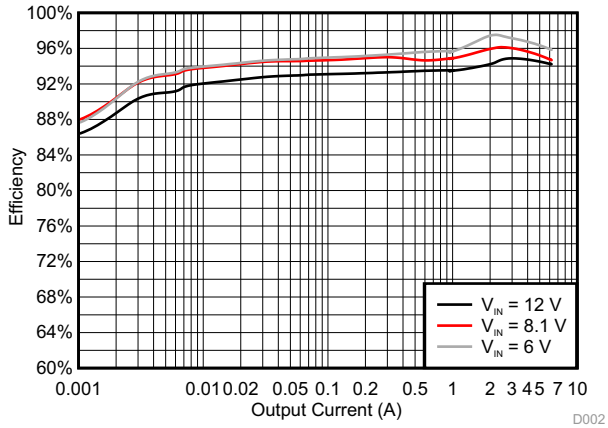
**Figure 5-1. Controller Efficiency vs Load at 1.05-V Output**




Inductor: CMLE051H-1R0MS FETs: CSD87330Q3D

$f_{SW}$ = 1 MHz

**Figure 5-2. Controller Efficiency vs Load at 3.3-V Output**




Inductor: CMLE051H-1R0MS FETs: CSD87330Q3D

$f_{SW}$ = 1 MHz

**Figure 5-3. Controller Efficiency vs Load at 5-V Output**

# 6 Detailed Description

## 6.1 Overview

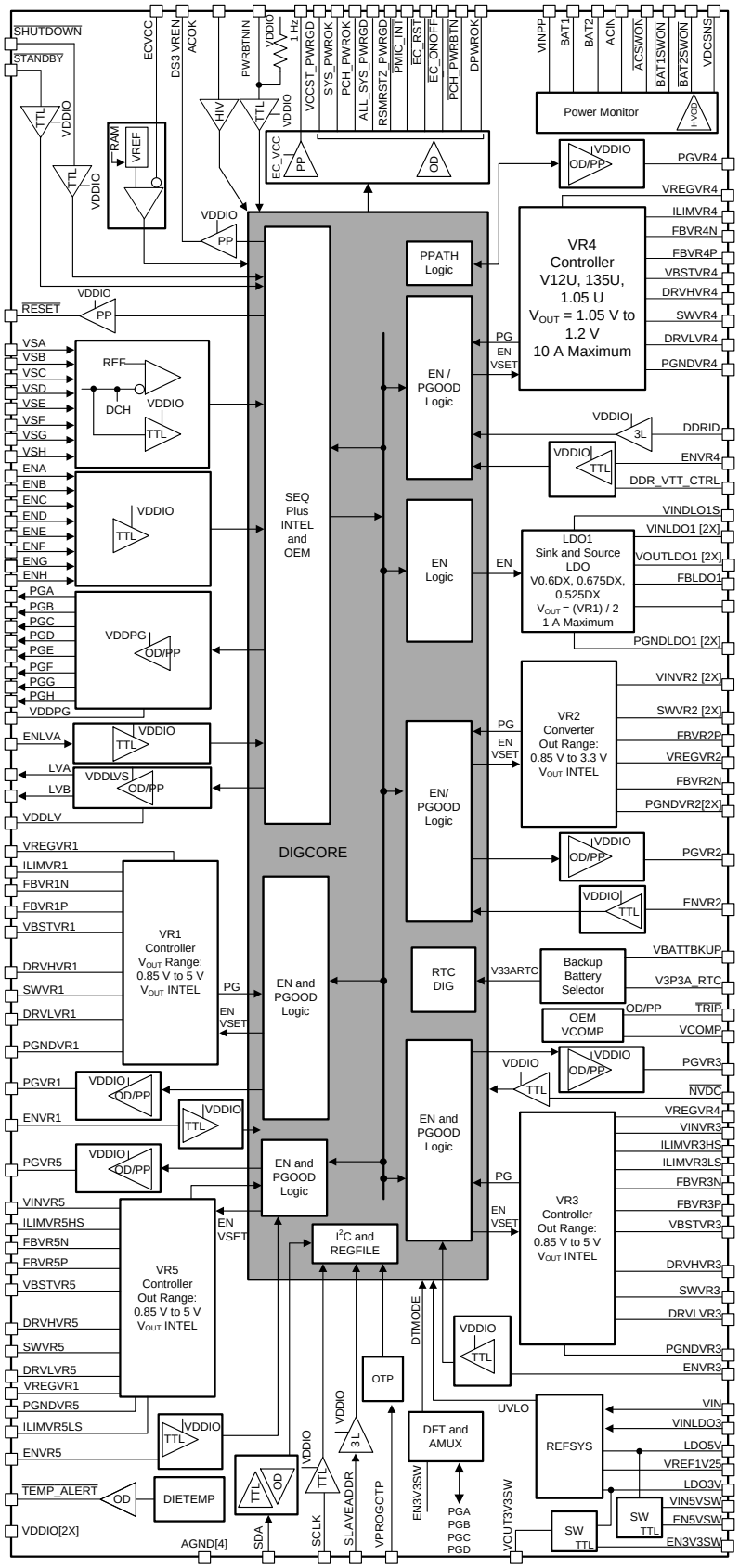
The TPS650932 device is a single-chip solution PMIC designed specifically for the latest Intel processors targeted for tablets, ultrabooks, and notebooks with NVDC or non-NVDC power architectures, using 2S, 3S Lithium-Ion battery packs.

The TPS650932 device can provide a power solution based on the Intel reference designs. Five highly efficient, step-down voltage regulators (VRs), a sink-source LDO, and power-up sequence logic that manages the external load switches are used to provide the proper power rails, sequencing, and protection, including DDR3 and DDR4 memory power. The regulators support dynamic-voltage scaling (DVS) for maximum efficiency including connected standby. The high-frequency voltage regulators use small inductors and capacitors to achieve a small solution size. Output power is adjustable on four VR controllers. An $I^2C$ interface allows simple control by the embedded controller (EC). The device is available in a 7-mm by 7-mm nFBGA packagewhich can be used in Type-4 PCB boards for the smallest area implementation

The power-good comparator logic allows controlling and monitoring of up to eight external load switches within the sequence. All the VRs and load-switch power good signals are used in the power-good tree to determine the system-level power goods including the ALL_SYS_PWRGD pin. Enable inputs allow connecting externally to set the sequence, and it also allows using various sleep-mode state signals. The $\overline{\text{STANDBY}}$ state allows entering a deep sleep mode, in which the output voltages of the voltage regulators can be reduced to save power by DVS.

The power monitoring comparators are used to detect and monitor up to three input power sources (adapter, battery1, battery2, or any other combination). Overtemperature detection of the PMIC self-protects, and outputs a status output, TEMPALERTZ. A dedicated comparator also monitors system overtemperature conditions with multiple stacked PTC thermistors, or an NTC thermistor. The PMIC automatically switches between an internal 3.1-V LDO when a power source is connected; or to a backup battery (coin cell) when all power sources are removed. This output RTC rail is used to maintain the always-on RTC rails for critical register data.

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Converters

The PMIC has five built-in DC-DC converters. The voltage regulators are highly configurable with regard to voltage and current. Of the five voltage regulators, four voltage regulators have an external power stage with a programmable current limit (programmed by an external resistor). This programmable current limit allows for optimal selection of external passive components based on the desired system load. VR2 has a completely integrated power stage, except for the required passive components. To maintain high efficiency, the converters are implemented as synchronous step-down converters.

One additional voltage regulator is a low dropout (LDO) linear regulator is integrated as part of the PMIC. The LDO1 regulator is capable of sinking and sourcing current that regulates from the step-down controller (for DDR memory). This LDO regulator is designed to specifically provide the VTT power to DDR memory. The LDO1 output voltage tracks the output voltage of the step-down controller and is set to regulate to half of the voltage of the step-down controller voltage.

#### 6.3.1.1 Power-Save Mode

At medium and heavy loads, the converter and the controllers operate in pulse-width modulation (PWM) mode. As soon as the inductor current becomes discontinuous, which indicates that the output current is lower than half of the inductor ripple current, the converters enter power-save mode. In power-save mode, the switching frequency decreases linearly with the load current and maintains a high efficiency. By default, the converters and controller operate in auto pulse-frequency modulation (AutoPFM) mode such that the transition into and out of power-save mode happens within the entire regulation scheme and is seamless in both directions.

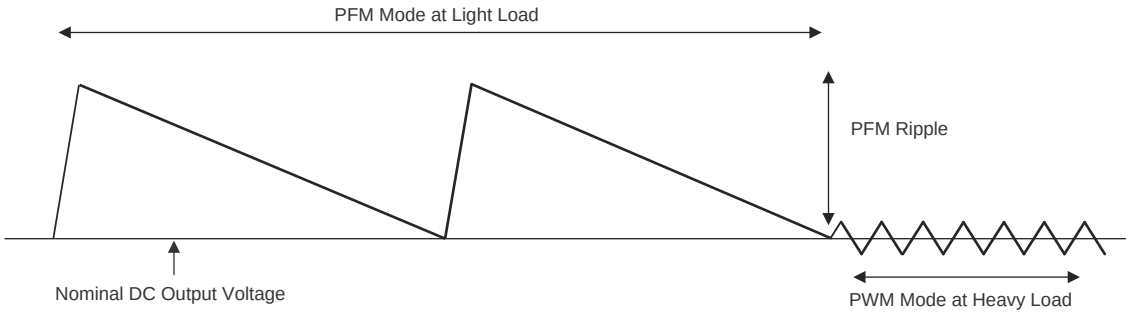



**Figure 6-1. PFM and PWM Mode Operation**

Figure 6-1 shows the converter and controller operation in PFM and PWM mode. In PFM mode, the minimum voltage to which the output falls is the programmed regulation voltage. The output voltage ripple in PFM mode is determined based on the external passive components (L and C). The regulator ensures that the minimum voltage during PFM mode is the same as the programmed regulation voltage (within the AC and DC tolerance).

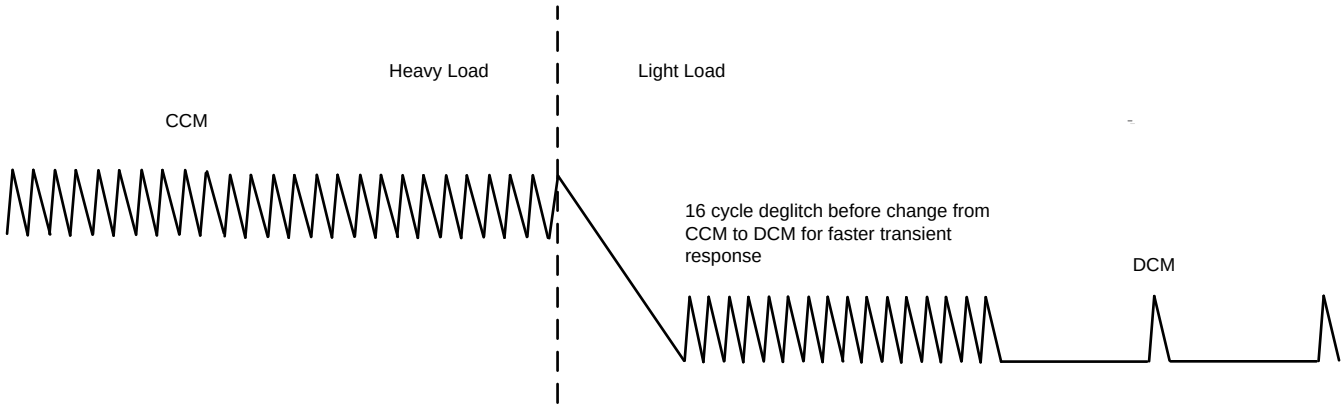



**Figure 6-2. Operation During Load Step Transient: CCM to DCM Transition**

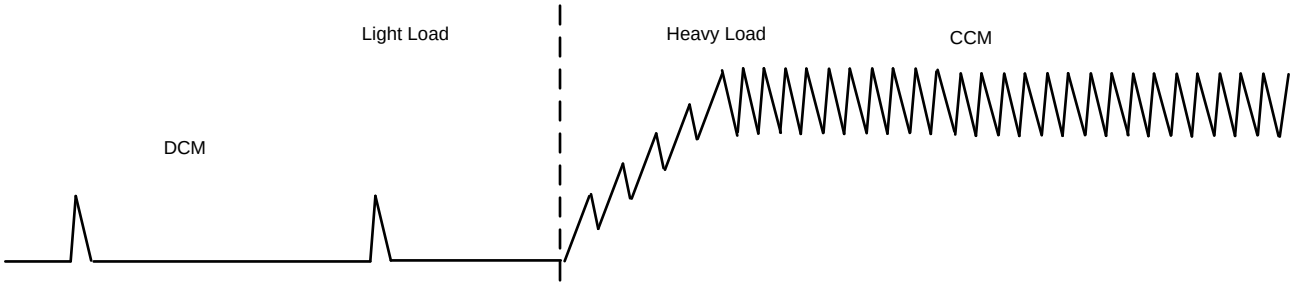
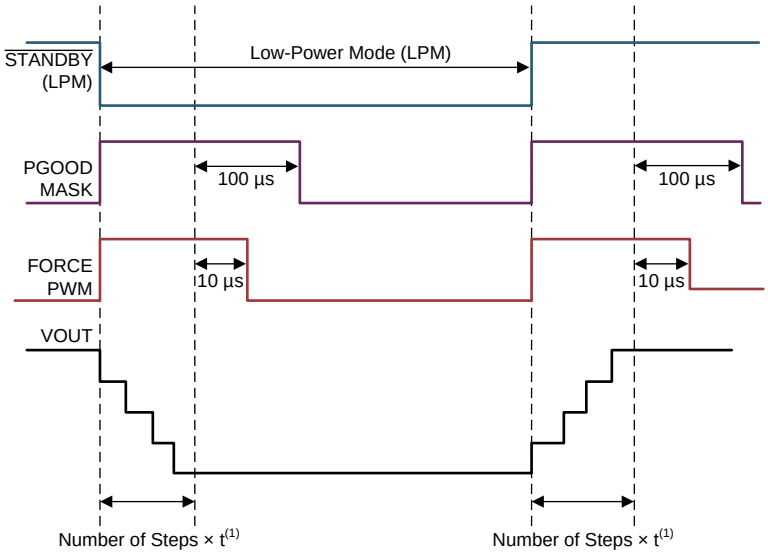



**Figure 6-3. Operation During Load Step Transient: DCM to CCM Transition**

Figure 6-2 and Figure 6-3 shows the inductor current of the controller during a load transient as it transitions in and out of continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM). CCM is often referred to as pulse-width modulation (PWM) mode, and DCM is referred to as pulse-frequency mode (PFM) mode. When the load step falls, a 16-cycle deglitch time passes, going from CCM to DCM. This time allows for a fast transient response and tighter peak-to-peak ripple voltage. When the load step rises, no deglitch time passes and therefore the controller goes directly from DCM to CCM in a quick-response characteristic of CCM.

#### 6.3.1.2 Dynamic Voltage Scaling

The dynamic-voltage scaling (DVS) timing is controlled by stepping the internal reference up or down. The total ramp-up or ramp-down transition time is equal to the step time multiplied by the number of steps. The number of steps is equal to the VOUT_hi voltage minus the VOUT_lo voltage, divided by 25 mV for each step. The step time of 5 μs for each 25-mV step ensures a time less than 70 μs for a 300-mV voltage change. The controller is forced into PWM from the $\overline{\text{STANDBY}}$ (LPM) transition until 10 μs after the reference ramp-up or ramp-down ends. This feature helps ensure a fast response. Similarly, the power-good signal for that rail is masked from the $\overline{\text{STANDBY}}$ (LPM) transition until 100 μs after the internal reference ramp-up or ramp-down ends. This feature ensures that no turnoff of the false power-good fault happens during DVS. In most cases the undershoot or overshoot is negligible.




(1) Where:
number of steps = (VOUT_hi – VOUT_lo) / 25 mV per step
t = 3 µs, 5 µs, 6 µs, or 7 µs per step.

**Figure 6-4. DVS Transition Timing**

#### 6.3.1.3 Voltage Regulator Startup

All of the voltage regulators, including the VTT LDO1, can be enabled using either pin enables or $I^2C$ commands. The default setting uses the pin enable option. The VTT LDO1 can be enabled using the DDR_VTT_CTRL discrete input. The VTT LDO1 can also be enabled by bit 7 and bit 6 in the MISC_BITS register (address 0xE9). Bit 7 masks the DDR_VTT_CTRL pin, and bit 6 enables the VTT LDO1. All system power-good pin should be high to enable the VTT LDO. Each voltage regulator can be enabled by the enable pin (ENAVRx) or by $I^2C$ Register (xCNT). The voltage should not be changed by register at the exact same time the voltage regulator is enabled. If a different voltage other than the default is required at power-up, the register (xCNT) should program the voltage first, and then a separate command should enable the register separately. DVS can be performed any time after power-up.

Each of the voltage regulators, except for the VTT LDO1, are controlled by an internal soft-start function to ensure the output voltage ramps up gently and does not cause huge inrush current during startup to prevent droop on the input. The VTT LDO1 startup time is driven by the DDR memory requirements for the VTT voltage rail, which requires that the ramp-up on voltage is faster than 35 µs.

#### 6.3.1.4 Power Good and Power Fault

During operation, when the voltage regulators are enabled, the output voltage for each rail is monitored to assess if the output voltage is within a specified voltage range. A power-good status bit is generated and stored in the PGOOD_STAT1 and PGOOD_STAT2 registers. If the output voltage is within the specified voltage range, the respective power-good status bit is set to a logic high. If the output voltage falls below or goes above the specified voltage range, the power-good status bit is set to a logic low.

By default, if any of the output voltage rails experience a power-fault condition, the PMIC automatically shuts down to help protect the system unless the power fault is masked. If a power fault happens, the source of the power fault is maintained in the PWRSTAT1 and PWRSTAT2 registers which are maintained in the RTC domain. The voltage thresholds for each of the power-good comparators is a percentage relative to the nominal voltage setting of the output voltage. For the nominal value of each comparator, see Table 3-1. For the upper and lower limits of each comparator, see Section 5.5.

Figure 6-5 shows the power-good tree logic.

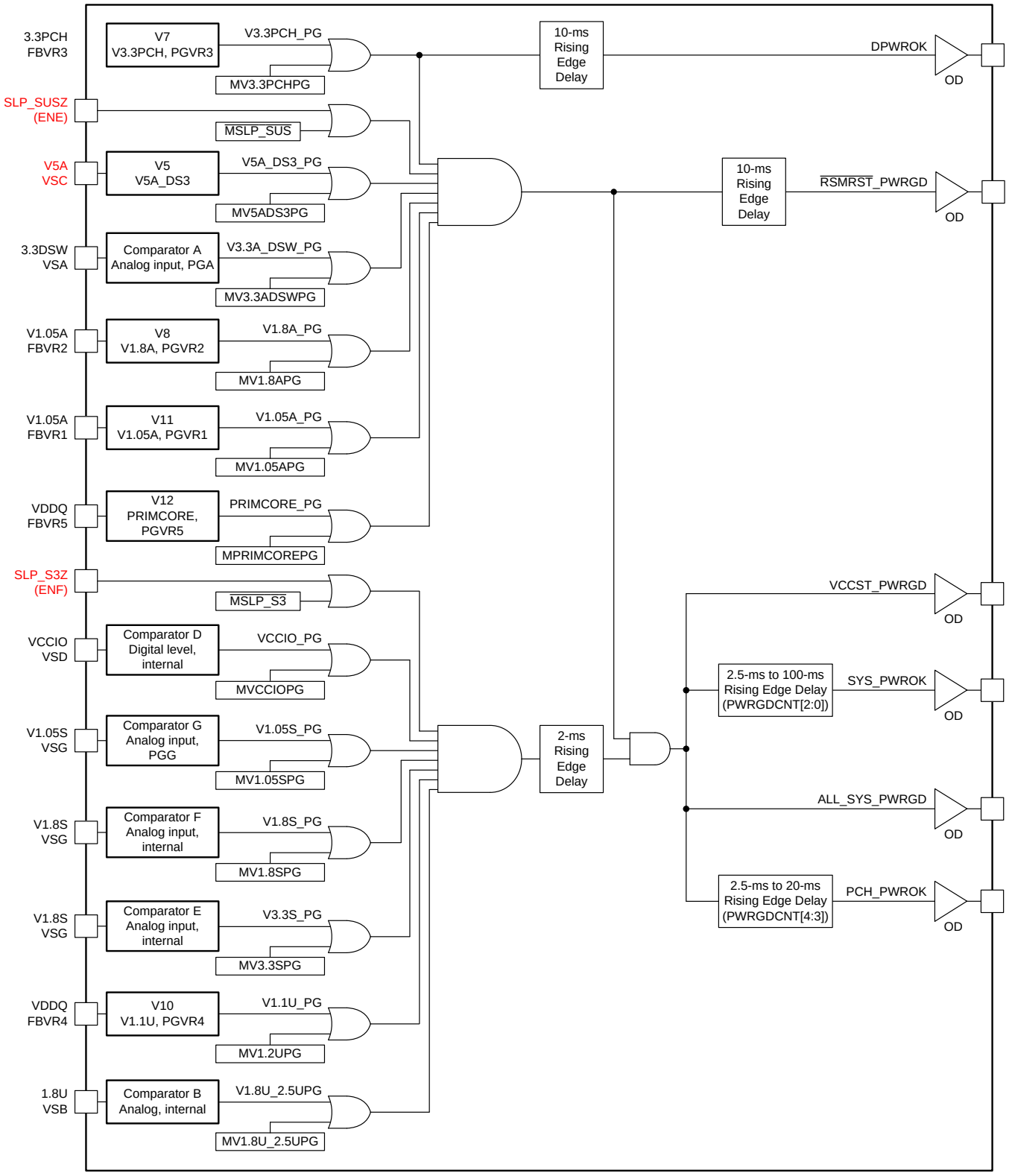



**Figure 6-5. Power-Good Tree Logic**

If a particular voltage rail is not critical to the performance of the overall system, the respective power-good output can be masked using the PGMASK1 and PGMASK2 registers. The masking of a power fault prevents an automatic PMIC shutdown. This masking can be also very helpful for debug purposes in case of system failure to isolate the voltage regulator with the sensitive output voltage.

To avoid an erroneous power fault during the turnon of the voltage regulators, the power fault is masked for 10 ms relative to the enable whether it be from the discrete signal or from an $I^2C$ command. The power-good comparator is also masked when coming out of the SLEEP (S3 state) for 100 µs after the ALL_SYS_PWRGD pin goes high to ensure that no false triggering of the power-good comparators happens.

#### 6.3.1.5 Current Limit

All voltage regulators are current limited. The current limit can be set based on the application load current using an external resistor for all VRs except for VR2. which has an internally-set current limit because it has an integrated power stage. The current limit controls the maximum output current. If the maximum current is reached, the output voltage starts to droop because the load can no longer be supplied with sufficient power. If the voltage drops below the power-good threshold, the power fault status is set to a logic high, and, if the power fault is not masked, the PMIC automatically shuts down in a controlled manner to protect the system.

For voltage regulators with an externally programmable current limit, see Section 7.2.2.1.4 to calculate the desired resistor value to prevent inductor saturation under nominal operation. A scaling factor of 1.5 is considered to account for the inductor variation (±20%) and temperature coefficient differences between the reference current ($I_{REF}$) and the FET $R_{DSON}$.

#### 6.3.1.6 Output Discharge Feature

All of the voltage regulators have a built-in, output discharge feature. The output discharge feature consists of the ability to configure register bits to enable a discharge resistor that is only active when the voltage regulator is disabled. The discharge resistors for each of the voltage regulators can be configured using the DISCHCNT1, DISCHCNT2, DISCHCNT3, and DISCHCNT4 registers. The discharge resistors are disconnected when the voltage regulators are enabled to minimize any losses within the PMIC.

#### 6.3.1.7 Output Voltage Control

All voltage regulators are designed to regulate a fixed-output voltage. To achieve high accuracy, the output voltage for the converters and controller is sensed using a separate feedback pin. For each of the voltage rails, except for the VTT LDO, the output voltage can be changed to slightly higher or lower values by changing the default setting in the voltage-regulator control registers. This function can be used to save power when supplying the connected load at the lowest possible supply voltage or to compensate for voltage drops during load transients by programming it slightly higher.

#### 6.3.1.8 Converter LPM Operation

To optimize low-power operation, the output voltage of the converters can be set to a specific value. The low-power output voltage is set by the xxLVsel bits in the VR5 (0x31), VR3 (0x32), VR4 (0x36), and VR1 (0x37) registers. Entering LPM is accomplished by asserting the $\overline{\text{SLP\_S0}}$ signal to a logic low. In LPM, the power-good function remains active and is not affected by the transition from normal-operation mode to LPM, and from LPM to normal-operation mode.

#### 6.3.1.9 Controller LPM Operation

To optimize low-power operation, the output voltage of the controllers can be set to a specific value. The low-power output voltage is set by the V18ALVSEL[1:0] bit in the V18ACNT register. Entering the low-power mode is accomplished by asserting the DDR_VTT_CTRL pin or the $\overline{\text{STANDBY}}$ pin to a logic low. In this low-power mode, the power-good function remains active and is not affected by the transition from normal-operation mode to the LPM, and from LPM to normal-operation mode. The DDR_VTT_CTRL pin asserts DVS on VR4 and the $\overline{\text{STANDBY}}$ pin asserts DVS on VR1, VR2, VR3, and VR5, as defined by the CNT registers. In cases where the output current demand from the controller is very small, the controller is automatically placed in an ultra-low quiescent (ULQ) mode to reduce power consumption and increase the efficiency.

#### 6.3.1.10 Controller Internal-Ramp Comparator

The controllers have an internal ramp characteristic of the DCAP2 control architecture which provides improved performance with low-ESR output capacitors. This internal ramp provides ramp compensation that helps maintain a relatively constant frequency during CCM and better stability for designs with very-low ESR on the output capacitors. The ramp height can be optimized and is a function of the input voltage to provide proportional feed-forward. At very high voltages, the ramp may exceed the operating window of the PWM comparator and may overpower the natural ripple of the output. Therefore a smaller ramp must be used. Because the ramp was already becoming large, switching to a smaller size is helpful. To switch to a smaller size, a comparator monitors the input voltage at the VIN pin. When input voltage rises and exceeds 11 V, it changes the ramp to a slightly smaller value. The smaller ramp has a wide 1.1-V hysteresis, so at approximately 9.9 V as the input voltage falls, the ramp returns to the slightly bigger size. In most cases this difference is negligible.

#### 6.3.1.11 Undervoltage Lockout

An undervoltage-lockout (UVLO) function prevents the PMIC from operating if the supply voltage on the VIN pin of the PMIC is lower than the UVLO threshold (see Section 5.5). During operation, if the supply voltage on the VIN pin drops below the UVLO threshold, the system or PMIC shuts down.

### *6.3.2 Power-Good Comparators for Cannon Lake Platform*

For the Cannon Lake power-map implementation, the five voltage regulators and LDO1 of the PMIC are assigned with the low-voltage rails which are either merged or split according to the configuration.

Figure 6-6 and Figure 6-7 show the operation of the window mode for the comparators. In window mode, the comparators have both high and low thresholds for detection of power good logic and power fail. In level mode, only the low threshold is present. For the voltage regulators and power good comparator logic assignments supporting the Cannon Lake platform, see Table 3-1.

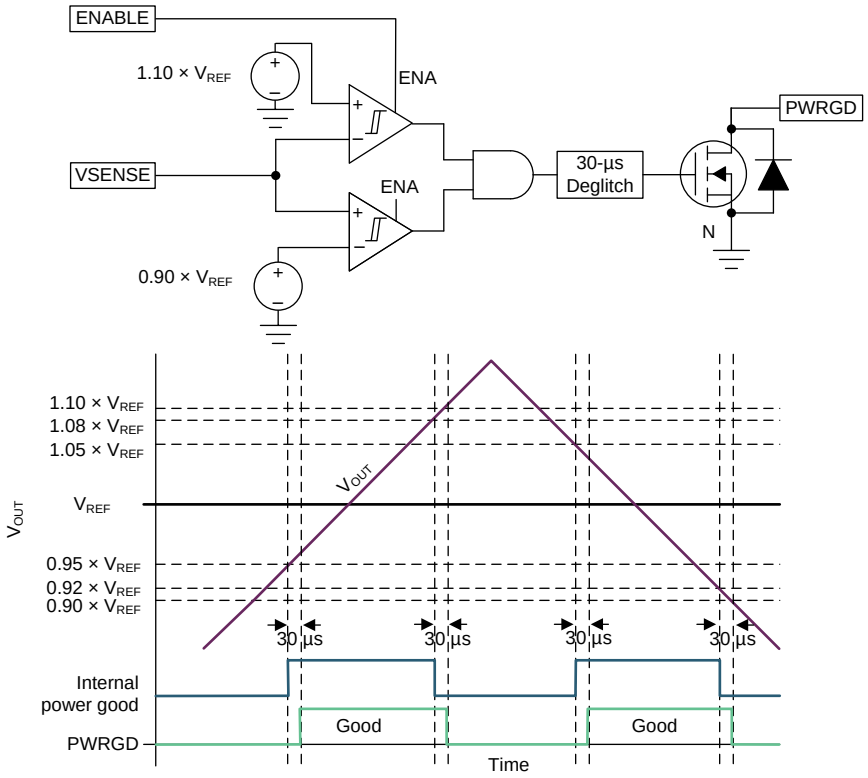



**Figure 6-6. Power-Good Window Comparator With Open-Drain Output**

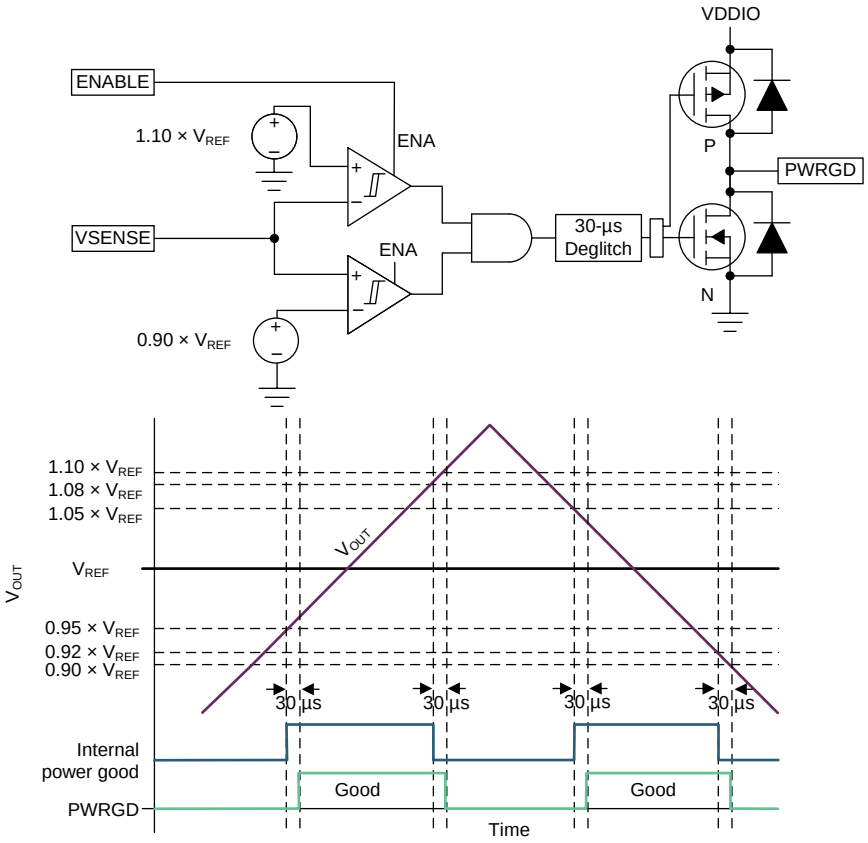



**Figure 6-7. Power-Good Window Comparator With Push-Pull Output**

#### 6.3.2.1 Internal VR Power-Good Comparators

All power-good comparators (converter and controllers) can be configured for either open-drain outputs or push-pull outputs. For VR PG configuration settings, see Table 3-1. The power-good comparators monitor the output voltage to ensure it is within the power-good threshold ($PG_{Threshold}$) of the nominal target voltage. A deglitch time ($PG_{deglitch}$) exists on the output of all the power-good comparators. The open-drain output requires an external pullup resistor (typically in the 100-kΩ range). Open-drain outputs can be combined to create an AND logic function. For push-pull outputs, the output internally pulls up to VDDIO pin rail.

#### 6.3.2.2 External VR Power-Good Comparators

The power-good comparators can be configured for either open-drain outputs or push-pull outputs. For VR PG configuration settings, see Table 3-1. The power-good comparators monitor the output voltage to ensure it is within the power-good threshold ($PG_{Threshold}$) of the nominal target voltage. A deglitch time ($PG_{deglitch}$) exists on the output of all the power-good comparators. The open-drain output requires an external pullup resistor (typically in the 100-kΩ range). Open-drain outputs can be combined to create an AND logic function. For push-pull outputs, the output internally pulls up to VDDPG pin rail.

### 6.3.3 LDO3V and 3V3SW Load Switch

The LDO3V LDO regulator powers up when the VINLDO3V pin voltage is greater than the UVLO3V threshold. The LDO3V LDO regulator powers the internal digital blocks and analog blocks of the PMIC. This LDO regulator is also used as the positive rail of the power-good comparator and level-shifter outputs. The 3V3SW load switch can optionally connect or disconnect the VOUT3V3SW output to a load. The 3V3SW load switch is enabled by the EN3V3SW pin. Figure 6-8 shows the block diagram for the load switch.

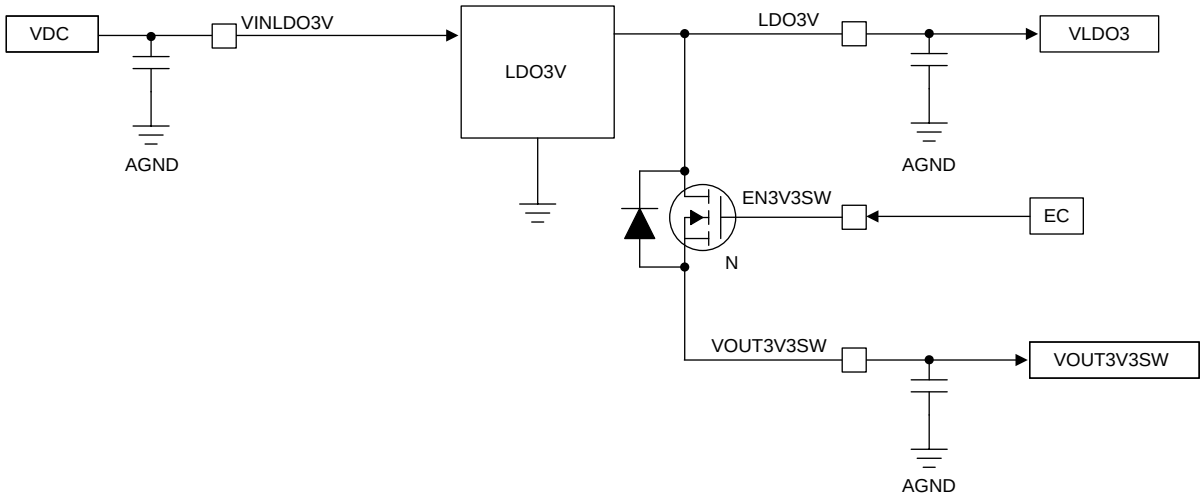





**Figure 6-8. LDO3V and 3V3SW Load Switch**

### 6.3.4 LDO5V and 5VSW Load Switch

The LDO5V LDO regulator powers up when the VIN pin voltage is greater than the UVLO5V threshold. The LDO5V LDO regulator powers the gate drives for all the five VRs of the PMIC. The 5VSW load switch is used to switch the gate-drive source from the internal LDO5V LDO to the 5-V voltage regulator output as soon as the V5A switching regulator power-good signal goes high. Because the switching regulator is used instead of LDO5V, it significantly improves the efficiency of the VRs whose effect is more significant

at lower VR load current and higher VR input voltage. The load switch is enabled by the EN5VSW pin. Connect the V5A_PG signal to the EN5VSW pin. When the EN5VSW pin is high, the LDO5-V internal reference drops to 4.5 V to ensure the 5-V VR drives all the gate drive current, but also to ensure the gate drive never falls below 4.5 V. When the EN5VSW pin is low, the LDO resumes to the 5-V internal reference and the load switch is turned off to disconnect the 5-V VR.

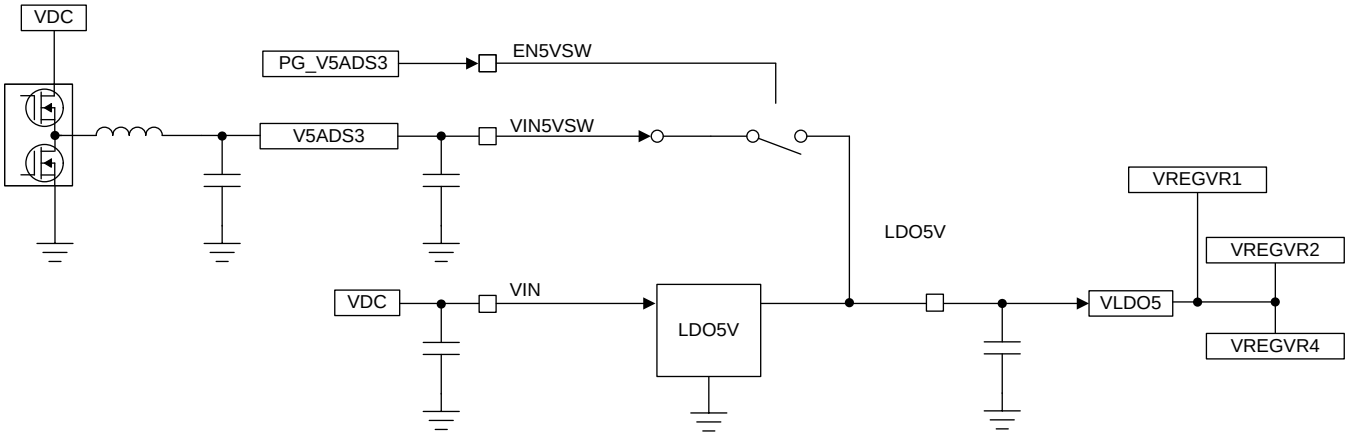





**Figure 6-9. LDO5V and 5VSW Load Switch**

### 6.3.5 RTC Selector and 3.1-V LDO

The RTC selector is used to select from the coin-cell backup battery and the internal 3.3-V LDO to power the 3P3A_RTC output rail for the RTC domain rail. If the VIN voltage is less than the $V_{UVLO\_5V\_Main}$ threshold, the coin-cell battery is selected. If the VIN voltage is greater than the UVLO5V threshold, then the internal 3.1-V LDO is selected. The selector logic for the backup battery selector has a very-low current draw when the battery is selected to extend the charge life of the backup battery. This rail allows keeping the data of the RTC registers even when the adapter and main battery are removed from the system. If the coin-cell voltage falls below the $V_{bkup\_UVLO}$ threshold, the RTC registers reset to the default values, as long as the VIN voltage is not also present. The 3.1-V LDO is set to 3.1 V to ensure the PCH voltage is always below 3.2 V (maximum) to help protect the PCH.

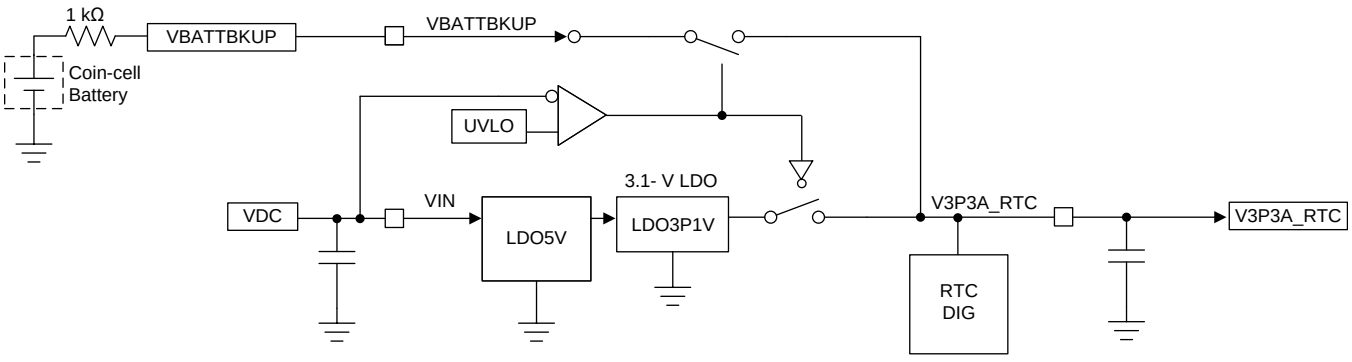





**Figure 6-10. RTC Selector and 3.1-V LDO**

### 6.3.6 Power-Path Comparators

The power-path comparators are comparators rated for a high voltage. The input pins of the power-path comparators are rated for high voltage. Both the voltage-sense and comparator-output pins are independent from the rest of the PMIC. These comparators can be used when the PMIC is powered down, as long as the VINPP pin is above the UVLO5V threshold. Connect a resistor divider from the source to set the $V_{REF\_PP}$ trigger threshold. These comparators can be used to detect an adapter and up to two batteries. An open-drain pin can detect the status, and a status register reports the status in the $I^2C$ registers using the ACOK, LOWBAT1, and LOWBAT2 bits. These bits can issue an interrupt to the EC if the interrupt mask bit is set appropriately at the MACOK, MLOWBAT1, and MLOWBAT2 bits. The high-voltage-rated outputs can be used to turn on the external P-channel power MOSFETs to control the power source path. Figure 6-11 shows an example of how to use the power-path comparators. A diode OR connection from all the power sources in use is recommended to ensure the VINPP pin is up when a source is available. If these comparators are not used, tie the VINPP pin to the VIN and VIN_LDO3 pins. Do not ground the VINPP pin when the VIN pin is powered up. These comparators can also be used as general-purpose comparators for numerous other applications.

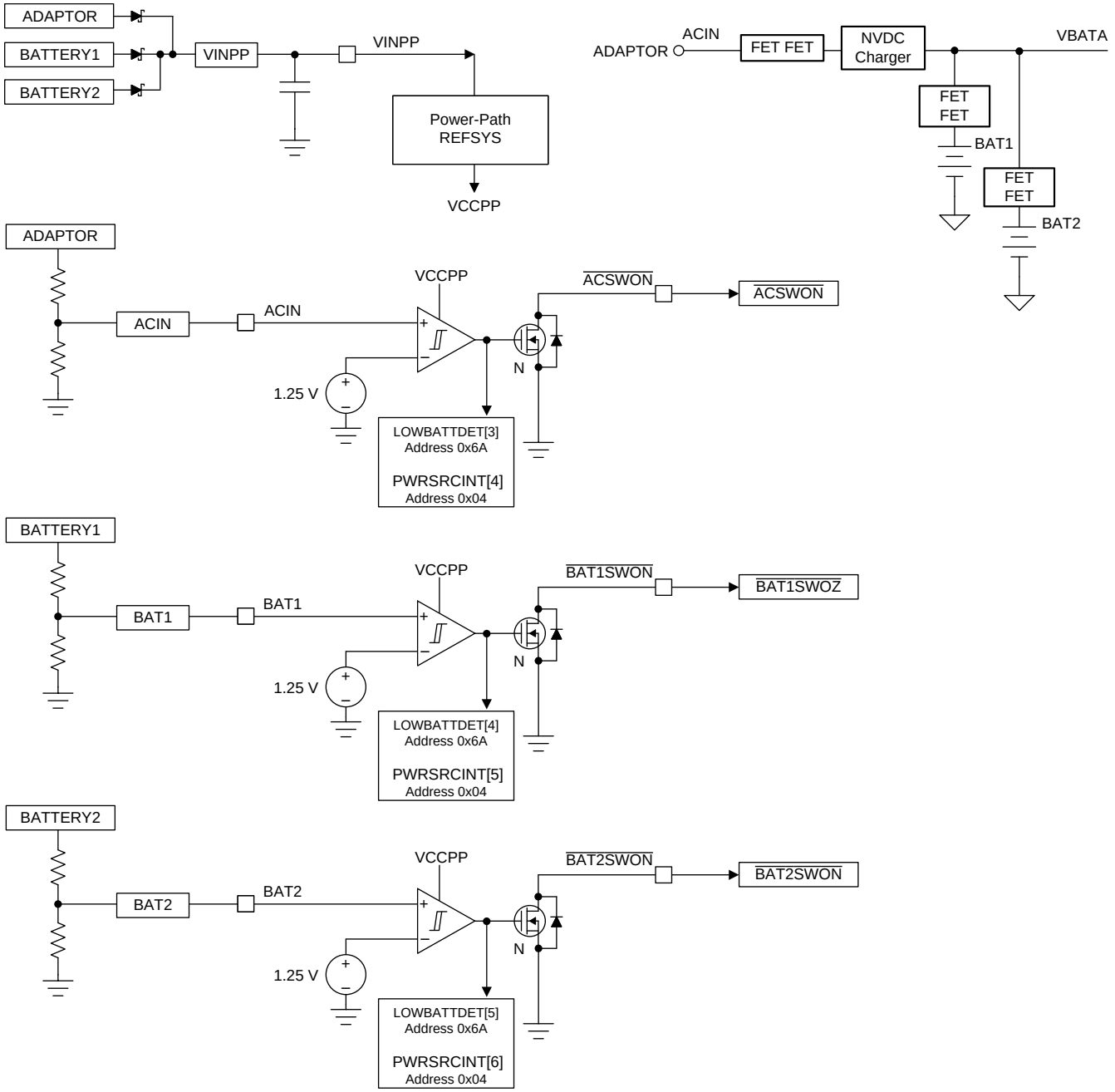





**Figure 6-11. Power-Path Comparators**

### 6.3.7 UVLO Comparators

The UVLO and VDCSNS comparators are high-voltage comparators rated for a 28-V input. The comparators are powered by the VIN pin for the LDO5V and 1.25-V LDO, and the VINLDO3V pin for the LDO3V. The VDCSNS input is also a high-voltage input pin to detect if the VIN voltage is above a programmable voltage. The VIN and VINLDO3V pins are tied directly to the VIN. The VDCSNS pin requires a resistor divider to set the proper detection gain.

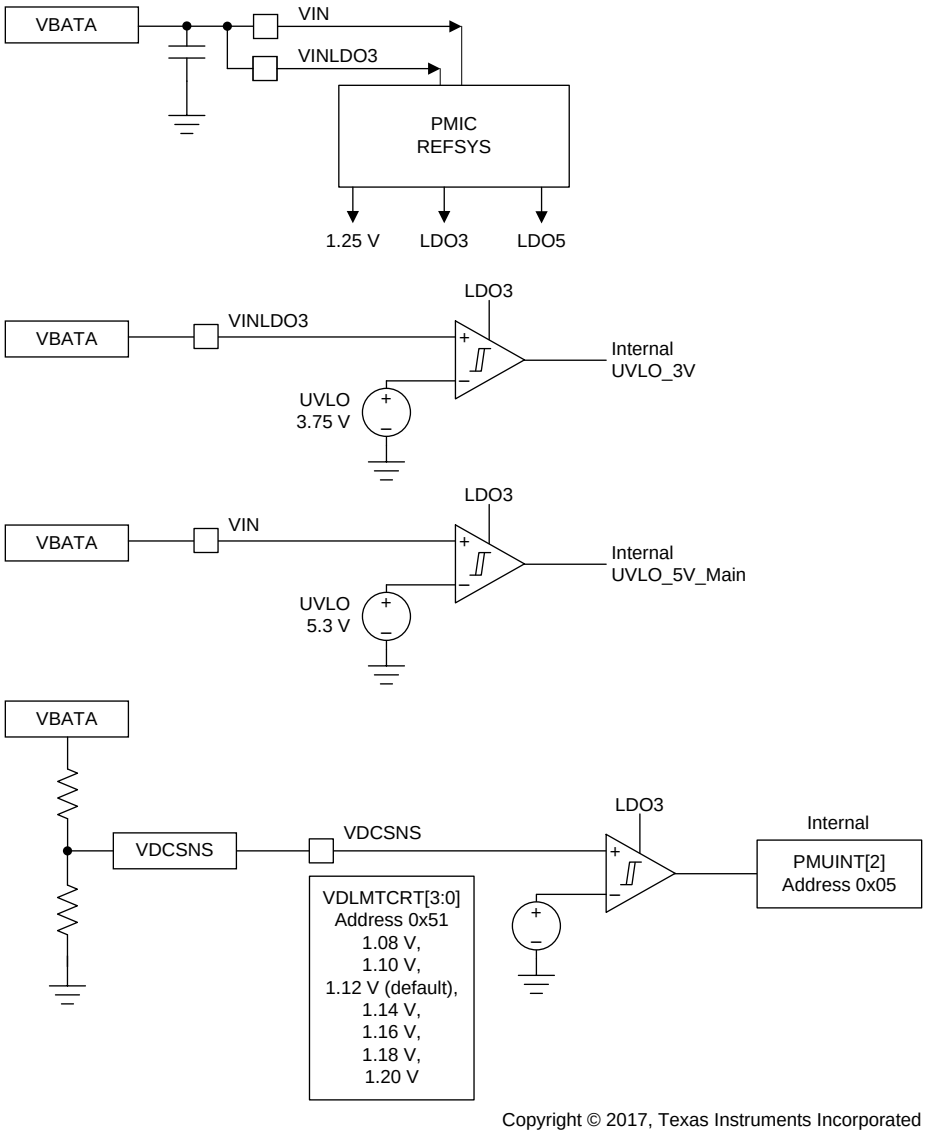





**Figure 6-12. UVLO Comparators**

### *6.3.8 Board Temperature Monitor*

The temperature comparator is used to detect either several PTC thermistors stacked in a series string or a single NTC thermistor. The PTC thermistors allow for an inexpensive overtemperature detection of any fault throughout several points on the motherboard, with each PTC thermistor selected to have its own temperature-threshold trigger point. An internal current source can be enabled to drive the PTC thermistors to minimize noise sensitivity. The current source can be disabled to drive with a voltage source, such as the LDO3V, to allow for tighter accuracy. Only a single NTC thermistor can be detected at a time, but the NTC allows tracking several temperature profiles. This comparator can also be used as a general-purpose comparator for numerous other applications.

The VCOMP comparator is on by default with the 10-µA current source also on. To completely disable the 10-µA current source or the comparator, write to the EN_VCOMP_10U and VCOMPEN bits.

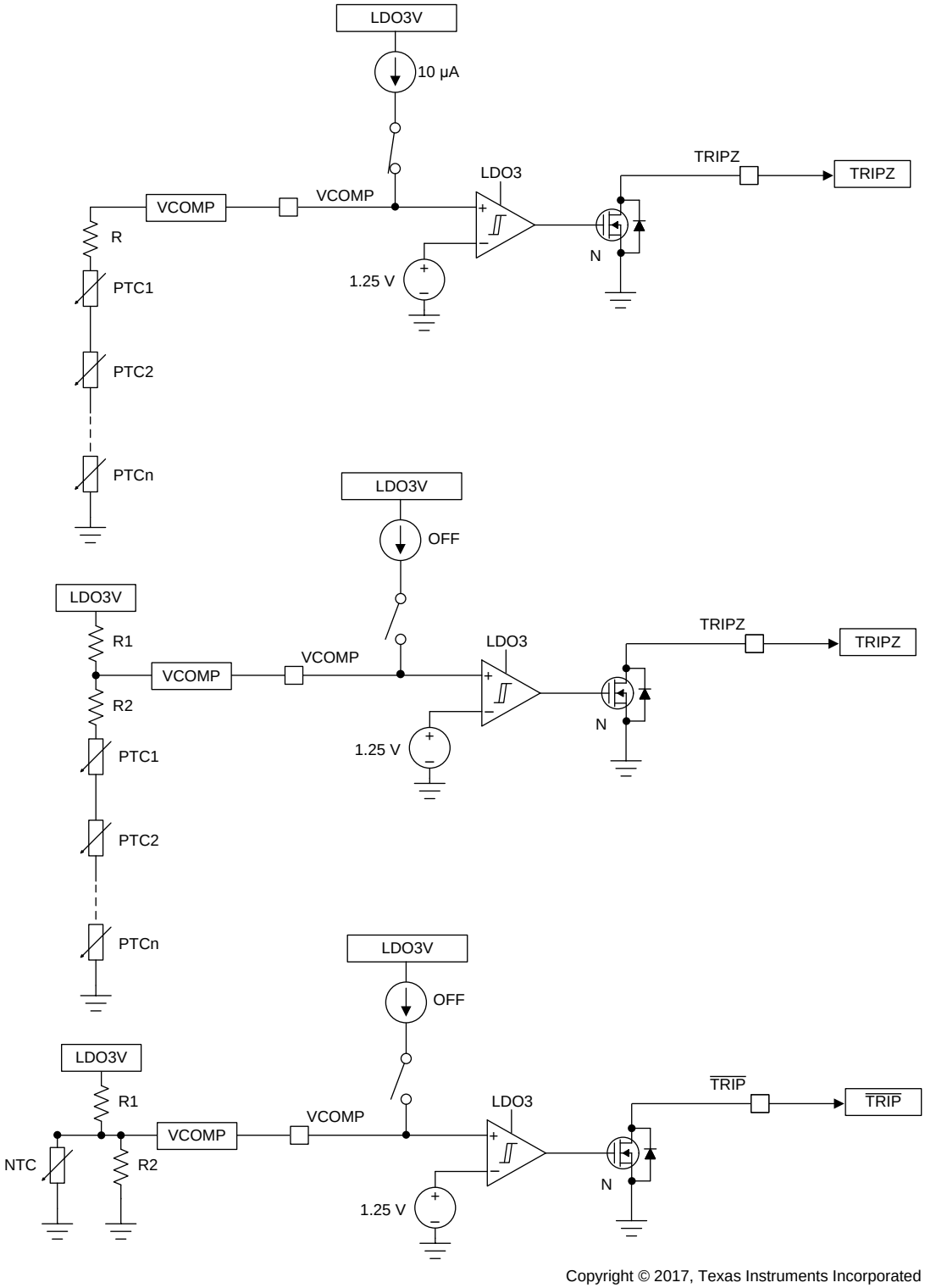





**Figure 6-13. Temperature Comparator**

### 6.3.9 Low-Power Mode (LPM), Connected Standby, Instant Go of VRs

The voltage regulators from the PMIC can be programmed by a register to change the voltage in active mode, or to change to a lower voltage or decay in the low-power mode (LPM). This feature can be used to conserve system power and extend battery life. This capability is useful to help meet the Connected Standby and Instant Go specifications. The $\overline{\text{STANDBY}}$ pin triggers low-power mode (LPM) when low. The $\overline{\text{STANDBY}}$ pin triggers active mode when high. Connect the $\overline{\text{SLP\_S0}}$ signal from the processor core (PCH) to the $\overline{\text{STANDBY}}$ pin to trigger LPM. The default settings can be changed by the user with the $I^2C$ register at any time.

In LPM, DVS and decay modes are enabled on the rails that were programmed for change in the VxxxCNT registers (address 0x30 through 0x38). The VCCIOCNT register is different because decay mode is enabled instead of DVS and therefore, only the CSDECAYEN bit is used.

For more information on DVS and decay, see Section 6.3.1.8 and Section 6.3.1.9.

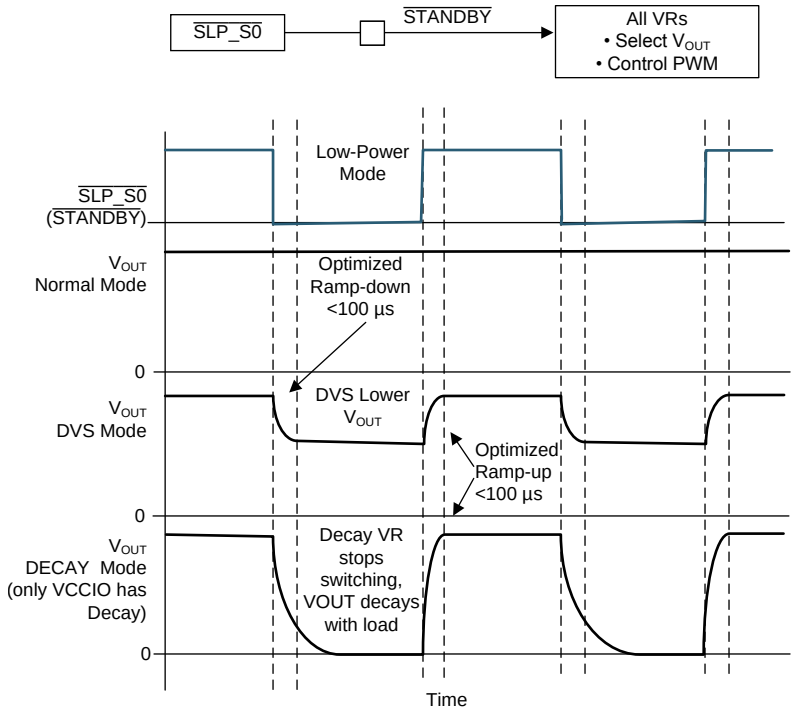



**Figure 6-14. Low-Power Mode (LPM), Connected Standby, and Instant Go of VRs**

### 6.3.10 VR4 VDDQ and LDO1 VTT Enabling

The VDDQ VR is enabled by the ENVR4 pin and the LDO1 VTT push-pull LDO is enabled by the DDR_VTT_CTRL pin. The DDR_VTT_CTRL pin is often connected to the $\overline{\text{SLP\_S0}}$ pin to turn off the VTT rail during sleep mode. The DDRID pin is a tri-level pin that sets the VR4 VDDQ voltage to either 1.2 V, 1.35 V, or 1.1 V. The DDR_VTT_CTRL pin is also used for DVS control of VR4, as defined by the V1P2UCNT register (0x36).

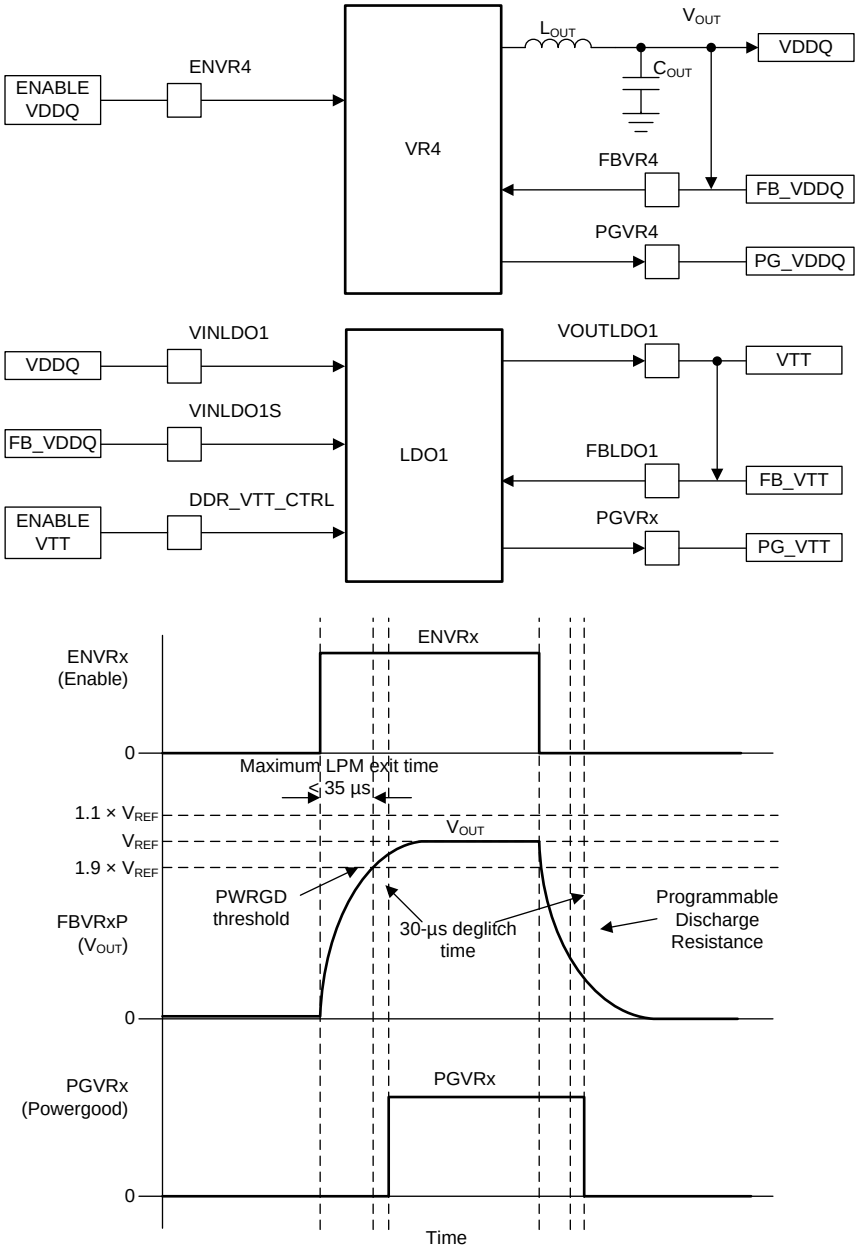



**Figure 6-15. VR4 VDDQ and LDO1 VTT Enabling**

### *6.3.11 RTC Power Path and LDO*

In case the main system battery is removed and no alternate power source is available, the RTC data, configuration and status registers, oscillator, and timekeeping path of the RTC block are backed up by either a super capacitor or a coin-cell battery. If the coin-cell or super-capacitor battery voltage falls below the minimum operational voltage and no input voltage is present (AC-DC voltage greater than the PMIC UVLO), the RTC data registers are invalid. Because the Intel RTC cannot support a maximum voltage greater than 3.2 V, when an AC-DC voltage is present and is higher than the UVLO threshold, the RTC is supplied by the AC-DC voltage instead of from the coin-cell battery. Supplying the RTC from the AC-DC voltage maximizes the stored charge in the coin-cell battery. When an AC-DC voltage is present, the internal coin-cell selector selects the higher voltage from either the coin-cell voltage or the AC-DC voltage. When the AC-DC voltage is selected as a source, the coin-cell LDO is driven from the 5-V PMIC LDO to regulate the output voltage at a fixed 3.1 V to ensure the maximum voltage remains below 3.2 V.

When the main system battery ($V_{DC}$) is greater than 5.4 V, the main power source for the RTC LDO is the 5-V internal LDO of the PMIC. The RTC LDO is bypassed and the RTC supply is powered by the coin-cell when the $V_{DC}$ falls below this threshold to maximize the life of the coin-cell battery. The coin-cell battery is used only if other options have failed. All power routing of the source selection for the RTC power happens internally and no external connections other than the coin-cell battery or super capacitor is required.

## 6.4 Device Functional Modes

### 6.4.1 OFF State (No VIN and No Backup Battery)

If the VIN voltage and the VBATTBKUP battery are both lower than their respective UVLO thresholds then the device is in the OFF state. In this state, the device cannot turn on or enable any VRs or discrete load switches and regulators. The clock and $I^2C$ are not active in this state.

In the OFF state, only the ACIN, BAT1, and BAT2 power-path switch comparators are available for use. To use these comparators, the VINPP pin must be supplied with the highest of the three input voltages from either the AC, BAT1, and BAT2 pin. In all other states, the VINPP must be supplied from the same source as the VIN pin.

### 6.4.2 STARTUP State

The device enters the STARTUP state when the VIN voltage is greater than the UVLO threshold. In the STARTUP state, the LDO3V, LDO5V, and VREF1V25 pins ramp-up. When the LDO3V and LDO5V pins both reach their nominal voltage and their power-good pins assert HIGH, the OTP memory loads into the $I^2C$ registers. After the LDO5V_PG pin asserts HIGH, the RTC LDO turns on and the V3.3A_RTC is regulated to 3.1 V, powered from the LDO5V. When the OTP memory is loaded and the RTC LDO is regulated to 3.1 V the device enters the READY state.

### 6.4.3 READY State

The device is considered to be in the READY state when all of the internal supplies and RTC are regulated, and the OTP memory is loaded into the registers. In this state, the device is ready for enable commands. The comparators, level shifters, and all other blocks are available for use.

### 6.4.4 STANDBY State

The device enters the STANDBY state when the $\overline{\text{STANDBY}}$ pin transitions from HIGH to LOW only if the ALL_SYS_PWRGD pin is HIGH. Only the VRs that have the DVS feature by default or through $I^2C$ register definition in registers 0x30 through 0x38 enter the STANDBY state.

### 6.4.5 Emergency Shutdown

An emergency shutdown is a protection feature for system loads. This feature reduces the risk of reverse bias in the processor or other devices from one rail to another. When an emergency shutdown is initiated, the DPWROK pin is pulled LOW, discharge resistors are enabled for all rails, and all rails are disabled at the same time. The PMIC remains in emergency shutdown mode until any of the following happens:

- A PWRBTNIN falling edge is detected.
- The ACOK pin transitions from LOW to HIGH.
- The VIN voltage is less than the UVLO threshold.

The PMIC only causes an emergency power shutdown of the rails for the following conditions:

- The is VIN pin voltage is less than the UVLO5V threshold or the VINLDO3V pin voltage is equal to or less than the UVLO3V threshold. In this case, read bit 2 in the IRQLVL1 register to determine if a VIN voltage < UVLO caused shutdown.
- A VR fault is detected. In this case, read the RESETIRQ1 register to determine if a VR fault caused shutdown.

- The junction temperature equals the critical temperature which casus a die thermal fault. In this case, read the RESETIRQ2 register to determine if thermal fault caused shutdown.
- The hardware forces shutdown. In this case, the SHUTDOWNZ pin is forced low.
- The software forces shutdown. In this case, read the SDWNCTRL register (address 0x49).
- The PWRBTN bit is held longer than the time defined by the FLT[5:0] bit. In this case, read the RESETIRQ1 register to determine if the push button caused shutdown.

The PMIC monitors each rail and ensures no faults are present. All rails are monitored for fault protection. Notice also that the current limit does not directly cause a shutdown. Instead, an overcurrent condition could cause a shutdown indirectly by means of a power fault. The overcurrent condition limits the maximum possible output current, such that if the load current exceeds the current limit, then the voltage drops until the lower output voltage causes a power fault if it is below the power-good threshold for more than the $PG_{deglitch}$ time (30 µs). An emergency power shutdown causes all rails to immediately power down. The LDO3, LDO5, and VREF1.25V remain on if the input voltage is greater than the UVLO3 and UVLO5 thresholds.

### 6.4.6 Backup Battery, G3 (No VIN)

G3 is an Intel defined state where the VIN voltage is greater than the UVLO threshold to the device and a valid backup battery is present on the VBATTBKUP pin. In this state, the backup battery is passed to the RTC output and the RTC-domain $I^2C$ register values are saved. When the VIN voltage is greater than the UVLO threshold these register retain their value and can be read when $I^2C$ is ready.

In this state, all VRs and internal LDOs are off and $I^2C$ access is not available.

## 6.5 Programming

### 6.5.1 I²C Interface

I²C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor) (refer to the I²C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller (MCU) or a digital-signal processor (DSP), controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the start and stop of data transfer. A slave device receives, transmits, or receives and transmits data on the bus under control of the master device.

The TPS650932 works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the power-supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when voltage is applied to the TPS650932 device that is higher than the UNVLO threshold. The I²C interface is running from an internal oscillator that is automatically enabled when an access to the interface is available.

The data transfer protocol for standard and fast modes is exactly the same, and, therefore, they are referred to as F/S-mode.

The TPS650932 device supports 7-bit addressing. The device does not support 10-bit addressing and general-call address. The default device address is defined by the status of the SLAVEADDR pin. Three different slave addresses are possible: 0x30 (SLAVEADDR, 0 V), 0x32 (SLAVEADDR, 3.3 V), and 0x34 (SLAVEADDR, floating).

All registers are set to their default value when the supply voltage is less than the UVLO threshold.

#### 6.5.1.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 6-16. All I²C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read-write direction bit, R/W, on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 6-17. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge*, see Figure 6-18, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 6-16. This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address

Attempting to read data from register addresses not listed in this section results in FFh being read out. F/S I²C operation does not support repeated start.

### 6.5.1.2 Diagrams of I²C Protocol

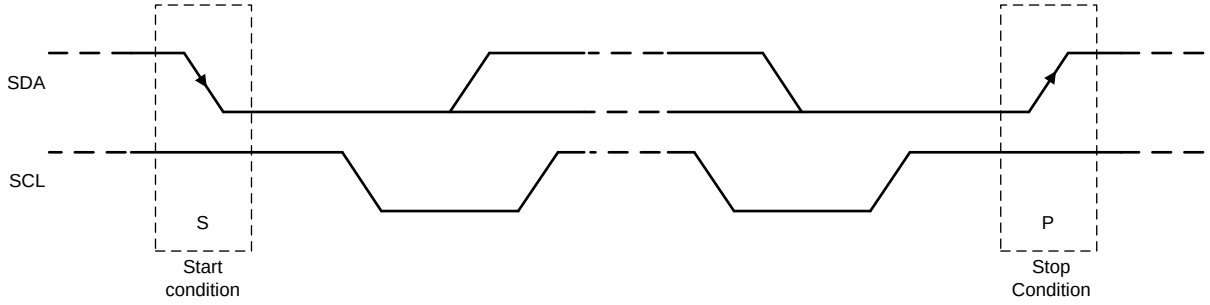



**Figure 6-16. Start and Stop Conditions**

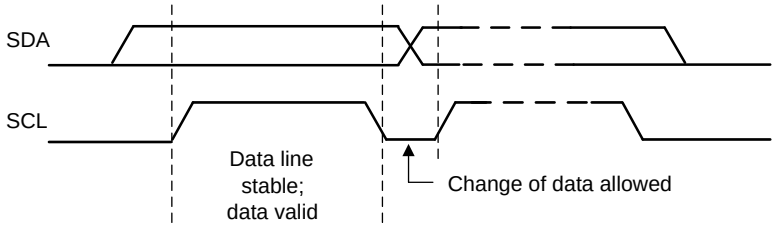



**Figure 6-17. Bit Transfer on the I²C-bus**

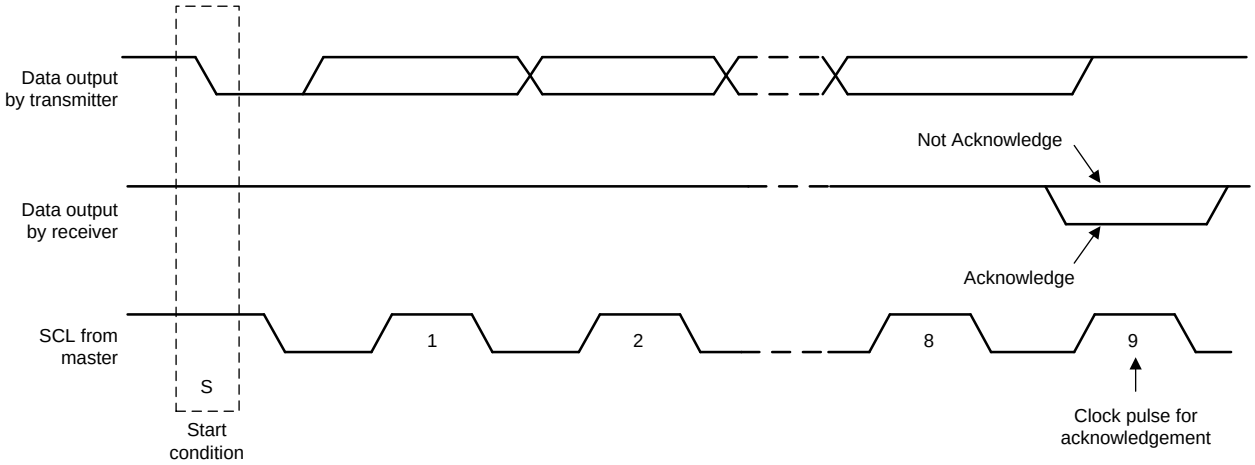



**Figure 6-18. Acknowledge on the I²C-Bus**

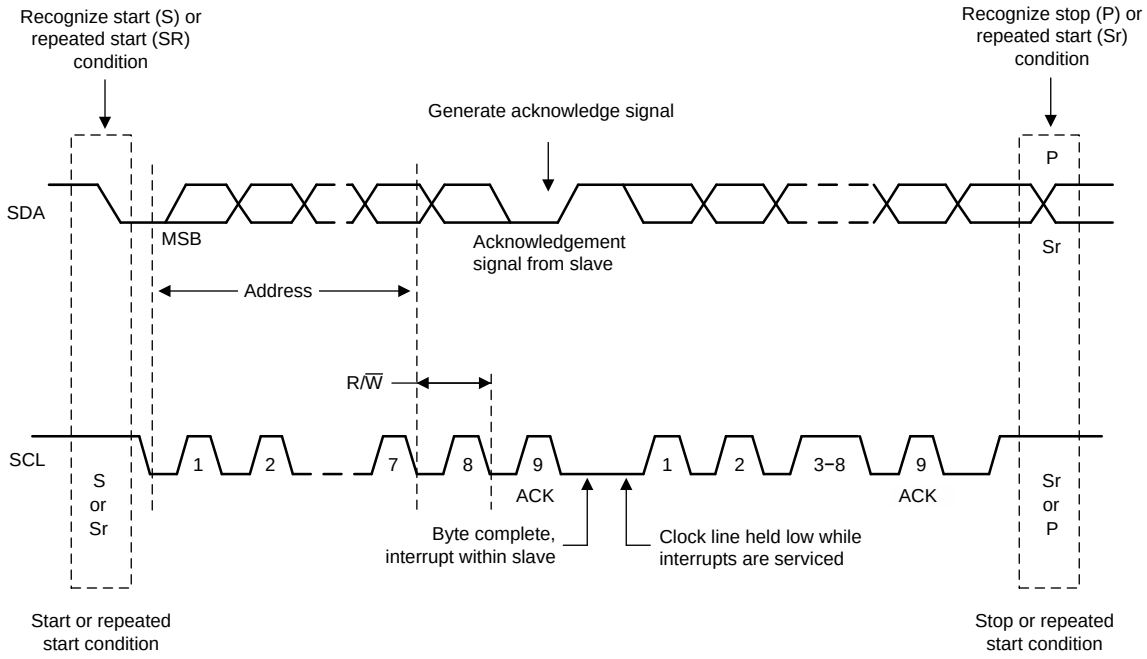



**Figure 6-19. Bus Protocol**

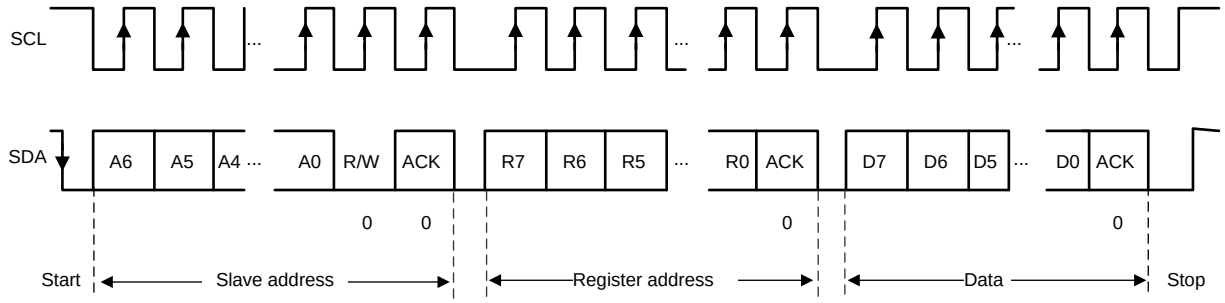



**Figure 6-20. I²C Interface Write to Device in F/S Mode**

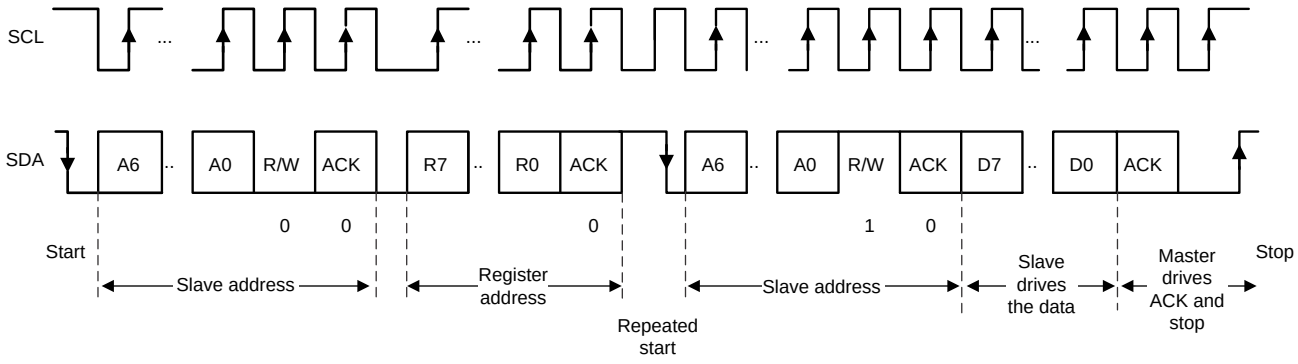



**Figure 6-21. I²C Interface Read from Device in F/S Mode**

## 6.6 Register Maps

Table 6-1 lists the memory-mapped registers for the TPS650932. All register offset addresses not listed in Table 6-1 should be considered as reserved locations and the register contents should not be modified.

**Table 6-1. Register Summary**

| Address | Acronym | Register Name | Domain | Section |
|---|---|---|---|---|
| 0x00 | VENDORID | Code that indicated a Texas Instruments' PMIC device | RESET | Go |
| 0x01 | REVID | Code to identify device revision and programming revision | RESET | Go |
| 0x02 | IRQLVL1 | Top level interrupts | RTC | Go |
| 0x04 | PWRSRCINT | Input power interrupts | RTC | Go |
| 0x05 | PMUINT | PMU interrupts | RTC | Go |
| 0x08 | RESETIRQ1 | Emergency shutdown interrupts | RTC | Go |
| 0x09 | RESETIRQ2 | Emergency shutdown interrupts | RTC | Go |
| 0x0B | MPMUINT | Mask PMU interrupts | RTC | Go |
| 0x0C | MPWRSRCNT | Mask input power interrupts | RTC | Go |
| 0x11 | RESETIRQ1MASK | Mask emergency shutdown interrupts | RTC | Go |
| 0x12 | RESETIRQ2MASK | Mask emergency shutdown interrupts | RTC | Go |
| 0x13 | IRQLVL1MSK | Mask top level interrupt | RTC | Go |
| 0x14 | PBCONFIG | Power button configuration | RTC | Go |
| 0x15 | PBSTATUS | Power button status | RTC | Go |
| 0x16 | PWRSTAT1 | VR fault reporting | RTC | Go |
| 0x17 | PWRSTAT2 | VR fault reporting | RTC | Go |
| 0x18 | PGMASK1 | Mask VR PGs from system power good tree | RTC | Go |
| 0x19 | PGMASK2 | Mask VR PGs from system power good tree | RTC | Go |
| 0x30 | VCCIOCNT | VCCIO control | RESET | Go |
| 0x31 | VPRIMCORECNT | PRIMCORE control | RESET | Go |
| 0x32 | V33ADSWCNT | V3.3A_DSW control | RESET | Go |
| 0x33 | V33APCHCNT | V3.3A_PCH (PGE) control | RESET | Go |
| 0x34 | V18ACNT | V1.8A control | RESET | Go |
| 0x35 | V18U25UCNT | V1.8U_2.5U (PGB) control | RESET | Go |
| 0x36 | VDDQCNT | VDDQ / VDDQ (VR4) control | RESET | Go |
| 0x37 | V105ACNT | V1.05A (VR1) control | RESET | Go |
| 0x38 | V5ACNT | V5A control | RESET | Go |
| 0x3B | VRMODECTRL | Force low power mode | RESET | Go |
| 0x3C | DISCHCNT1 | Discharge resistors settings | RESET | Go |
| 0x3D | DISCHCNT2 | Discharge resistors settings | RESET | Go |
| 0x3E | DISCHCNT3 | Discharge resistors settings | RESET | Go |
| 0x3F | DISCHCNT4 | Discharge resistors settings | RESET | Go |
| 0x40 | PWRGDCNT1 | System level power goods | RESET | Go |
| 0x41 | VREN | Deep sleep enable | RESET | Go |
| 0x42 | REGLOCK | Lock for control registers 0x30 through 0x38 | RESET | Go |
| 0x43 | VRENPINMASK | Mask hardware enable pins | RESET | Go |
| 0x48 | RSTCTRL | Reset control | RTC | Go |
| 0x49 | SDWNCTRL | Software force shutdown | RESET | Go |
| 0x51 | VDLMTCRT | VDCSNS settings | RESET | Go |
| 0x69 | ACOKDBDM | ACOK settings | RESET | Go |
| 0x6A | LOWBATTDET | Battery detection settings | RESET | Go |
| 0x6F | SPWRSRCINT | Input power statuses | RESET | Go |
| 0xD0 | CLKCTRL1 | Clock control | RTC | Go |

**Table 6-1. Register Summary (continued)**

| Address | Acronym | Register Name | Domain | Section |
|---|---|---|---|---|
| 0xDD | COMPA_REF | Comparator A settings | RESET | Go |
| 0xDE | COMPB_REF | Comparator B settings | RESET | Go |
| 0xDF | RESERVED | Reserved | — | |
| 0xE0 | RESERVED | Reserved | — | |
| 0xE1 | RESERVED | Reserved | — | |
| 0xE2 | RESERVED | Reserved | — | |
| 0xE3 | RESERVED | Reserved | — | |
| 0xE4 | RESERVED | Reserved | — | |
| 0xE5 | PWRFAULT_MASK1 | Mask VR faults from emergency shutdown | RESET | Go |
| 0xE6 | PWRFAULT_MASK2 | Mask VR Faults from emergency shutdown | RESET | Go |
| 0xE7 | PGOOD_STAT1 | VR PGs statuses | RESET | Go |
| 0xE8 | PGOOD_STAT2 | VR PGs statuses | RESET | Go |
| 0xE9 | MISC_BITS | Miscellaneous bits | RESET | Go |
| 0xEA | STDY_CTRL | VCOMP and standby control | RTC | Go |
| 0xEB | TEMPCRIT | VR critical temperature | RTC | Go |
| 0xEC | TEMPHOT | VR hot temperature | RTC | Go |
| 0xEE | VREN_PIN_OVR | VR enable override with software | RESET | Go |

Complex bit access types are encoded to fit into small table cells. Table 6-2 shows the codes that are used for access types in this section.

**Table 6-2. Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| Read Type | | |
| R | R | Read |
| R-0 | R<br>-0 | Read<br>Returns 0s |
| R-1 | R<br>-1 | Read<br>Returns 1s |
| Write Type | | |
| W | W | Write |
| W1C | W<br>1C | Write<br>1 to clear |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### *6.6.1 VENDORID Register (address = 0x00) [reset = 0x22]*

VENDORID is shown in Figure 6-22 and described in Table 6-3.

Return to Summary Table.

Register domain: RESET

**Figure 6-22. VENDORID Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VENDORID[7:0] | | | | | | | |
| R/W-22h | | | | | | | |

**Table 6-3. VENDORID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | VENDORID[7:0] | R/W | 22h | Vendor ID |

### 6.6.2 REVID Register (address = 0x01) [reset = 0x00]

REVID is shown in Figure 6-23 and described in Table 6-4.

Return to Summary Table.

Register domain: RESET

**Figure 6-23. REVID Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DNUM[3:0] | | | | OTPREV[1:0] | | REVID[1:0] | |
| R/W-0h | | | | R/W-0h | | R/W-0h | |

**Table 6-4. REVID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | DNUM[3:0] | R/W | 0h | Major revision ID<br>0h = A<br>1h = B<br>2h = C<br>3h = D<br>4h = E<br>5h = F |
| 3-2 | OTPREV[1:0] | R/W | 0h | Minor revision ID<br>0h = 0<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7 |
| 1-0 | REVID[1:0] | R/W | 0h | Minor revision ID<br>0h = 0<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7 |

### 6.6.3 IRQLVL1 Register (address = 0x02) [reset = 0x00]

IRQLVL1 is shown in Figure 6-24 and described in Table 6-5.

Return to Summary Table.

Register domain: RTC

**Figure 6-24. IRQLVL1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESET | RESERVED2 | PMU | RESERVED1[1:0] | | PWRSRC | RESERVED | PWRBTN |
| R/W-0h | R-0h | R/W-0h | R-0h | | R/W-0h | R-0h | R/W1C-0h |

**Table 6-5. IRQLVL1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESET | R | 0h | RESET interrupt<br>0h = Not asserted<br>1h = Asserted |
| 6 | RESERVED2 | R | 0h | |
| 5 | PMU | R | 0h | Power monitor interrupt<br>0h = Not asserted<br>1h = Asserted |
| 4-3 | RESERVED1[1:0] | R | 0h | |
| 2 | PWRSRC | R | 0h | Power source interrupt<br>0h = Not asserted<br>1h = Asserted |
| 1 | RESERVED | R | 0h | |
| 0 | PWRBTN | R/W1C | 0h | Power button interrupt<br>0h = Not asserted<br>1h = Asserted, write 1 to clear |

### 6.6.4 PWRSRCINT Register (address = 0x04) [reset = 0x00]

PWRSRCINT is shown in Figure 6-25 and described in Table 6-6.

Return to Summary Table.

Register domain: RTC

**Figure 6-25. PWRSRCINT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED1_ PWRSRCINT | LOWBATT2 | LOWBATT1 | ACOK | PMICHOT | RESERVED[2:0] | | |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | |

**Table 6-6. PWRSRCINT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED1_PWRSRCINT | R | 0 | |
| 6 | LOWBATT2 | R/W | 0 | Low battery2 interrupt (rising-edge detect threshold = 1.25 V; falling-edge hysteresis = 125 mV)<br>0h = No battery2 detected<br>1h = Battery2 detected |
| 5 | LOWBATT1 | R/W | 0 | Low battery1 interrupt (rising-edge detect threshold = 1.25 V; falling-edge hysteresis = 125 mV)<br>0h = No battery1 detected<br>1h = Battery1 detected |
| 4 | ACOK | R/W | 0 | AC/DC adapter detection interrupt (rising-edge detect threshold = 1.25 V; falling-edge hysteresis = 125 mV)<br>0h = No adapter detected<br>1h = Adapter detected |
| 3 | PMICHOT | R/W | 0 | PMIC internal temperature interrupt<br>0h = PMIC temperature normal<br>1h = PMIC temperature hot |
| 2-0 | RESERVED[2:0] | R | 000 | |

### 6.6.5 PMUINT Register (address = 0x05) [reset = 0x00]

PMUINT is shown in Figure 6-26 and described in Table 6-7.

Return to Summary Table.

Register domain: RTC

**Figure 6-26. PMUINT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED2[2:0] | | | PMUACOK | RESERVED1_ PMUINT | PMUVDC | RESERVED_PMUINT[1:0] | |
| R-0h | | | R/W-0h | R-0h | R/W-0h | R-0h | |

**Table 6-7. PMUINT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | | R | 0h | |
| 4 | PMUACOK | R/W | 0h | Adapter detection interrupt<br>0h = No interrupt pending<br>1h = AC adapter removed (SACOK goes from H to L) |
| 3 | RESERVED1_PMUINT | R | 0h | |
| 2 | PMUVDC | R/W | 0h | Power monitor critical supply voltage interrupt<br>0h = Critical supply voltage over threshold limit<br>1h = Critical supply voltage below threshold limit |
| 1-0 | RESERVED_PMUINT[1:0] | R | 0h | |

### 6.6.6 RESETIRQ1 Register (address = 0x08) [reset = 0x00]

RESETIRQ1 is shown in Figure 6-27 and described in Table 6-8.

Return to Summary Table.

Register domain: RTC

**Figure 6-27. RESETIRQ1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED1_RESETIRQ1[1:0] | | FCO | VRFAULT | RESERVED[3:0] | | | |
| R-0h | | R/W-0h | R/W-0h | R-0h | | | |

**Table 6-8. RESETIRQ1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED1_RESETIRQ1[1:0] | R | 0h | |
| 5 | FCO | R/W | 0h | Power button triggered reset interrupt<br>0h = Power button counter has not forced an emergency reset<br>1h = Power button counter has forced an emergency reset |
| 4 | VRFAULT | R/W | 0h | Voltage regulator triggered reset interrupt<br>0h = Voltage regulator fault has not triggered an emergency reset<br>1h = Voltage regulator fault has triggered an emergency reset |
| 3-0 | RESERVED[3:0] | R | 0h | |

### 6.6.7 RESETIRQ2 Register (address = 0x09) [reset = 0x00]

RESETIRQ2 is shown in Figure 6-28 and described in Table 6-9.

Return to Summary Table.

Register domain: RTC

**Figure 6-28. RESETIRQ2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED1[5:0] | | | | | | CRITTEMP | RESERVED_RESETIRQ2 |
| R-0h | | | | | | R/W-0h | R-0h |

**Table 6-9. RESETIRQ2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED1[5:0] | R | 0h | |
| 1 | CRITTEMP | R/W | 0h | Temperature triggered reset interrupt<br>0h = Critical temperature not reached<br>1h = Critical temperature reached, forcing emergency shutdown |
| 0 | RESERVED_RESETIRQ2 | R | 0h | |

### 6.6.8 MPMUINT Register (address = 0x0B) [reset = 0x14]

MPMUINT is shown in Figure 6-29 and described in Table 6-10.

Return to Summary Table.

Register domain: RTC

**Figure 6-29. MPMUINT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED2_MPMUINT[2:0] | | | MPMUACOK | RESERVED1_MPMUINT | MPMUVDC | RESERVED_MPMUINT[1:0] | |
| R-0h | | | R/W-1h | R-0h | R/W-1h | R-0h | |

**Table 6-10. MPMUINT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | RESERVED2_MPMUINT[2:0] | R | 0h | |
| 4 | MPMUACOK | R/W | 1h | Power monitor critical supply voltage (adapter) mask interrupt<br>0h = Not masked<br>1h = Masked |
| 3 | RESERVED1_MPMUINT | R | 0h | |
| 2 | MPMUVDC | R/W | 1h | Power monitor critical supply voltage mask interrupt<br>0h = Not masked<br>1h = Masked |
| 1-0 | RESERVED_MPMUINT[1:0] | R | 0h | |

### 6.6.9 MPWRSRCINT Register (address = 0x0C) [reset = 0x078]

MPWRSRCINT is shown in Figure 6-30 and described in Table 6-11.

Return to Summary Table.

Register domain: RTC

**Figure 6-30. MPWRSRCINT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED1_ MPWRSRCINT | MLOWBAT2 | MLOWBAT1 | MACOK | MPMICHOT | RESERVED_MPWRSRCINT[2:0] | | |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R-0h | | |

**Table 6-11. MPWRSRCINT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED1_MPWRSRCINT | R | 0h | |
| 6 | MLOWBAT2 | R/W | 1h | Low battery voltage mask interrupt<br>0h = Not masked<br>1h = Masked |
| 5 | MLOWBAT1 | R/W | 1h | Low battery voltage mask interrupt<br>0h = Not masked<br>1h = Masked |
| 4 | MACOK | R/W | 1h | AC/DC adapter detection mask interrupt<br>0h = Not masked<br>1h = Masked |
| 3 | MPMICHOT | R/W | 1h | PMIC internal temperature mask interrupt<br>0h = Not masked<br>1h = Masked |
| 2-0 | RESERVED_MPWRSRCINT[2:0] | R | 0h | |

### 6.6.10 RESETIRQ1MASK Register (address = 0x11) [reset = 0x30]

RESETIRQ1MASK is shown in Figure 6-31 and described in Table 6-12.

Return to Summary Table.

Register domain: RTC

**Figure 6-31. RESETIRQ1MASK Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED1_RESETIRQ1MASK[1:0] | | MFCO | MVRFAULT | RESERVED_RESETIRQ1MASK[3:0] | | | |
| R-0h | | R/W-1h | R/W-1h | R-0h | | | |

**Table 6-12. RESETIRQ1MASK Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED1_RESETIRQ1MASK[1:0] | R | 0h | |
| 5 | MFCO | R/W | 1h | Power button triggered reset mask interrupt<br>0h = Not masked<br>1h = Masked |
| 4 | MVRFAULT | R/W | 1h | Voltage regulator triggered reset mask interrupt<br>0h = Not masked<br>1h = Masked |
| 3-0 | RESERVED_RESETIRQ1MASK[3:0] | R | 0h | |

### 6.6.11 RESETIRQ2MASK Register (address = 0x12) [reset = 0x02]

RESETIRQ2MASK is shown in Figure 6-32 and described in Table 6-13.

Return to Summary Table.

Register domain: RTC

**Figure 6-32. RESETIRQ2MASK Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED1_RESETIRQ2MASK[5:0] | | | | | | MCRITTEMP | RESERVED_RESETIRQ2 MASK |
| R-0h | | | | | | R/W-1h | R-0h |

**Table 6-13. RESETIRQ2MASK Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED1_RESETIRQ2MASK[5:0] | R | 0h | |
| 1 | MCRITTEMP | R/W | 1h | Temperature triggered reset mask interrupt<br>0h = Not masked<br>1h = Masked |
| 0 | RESERVED_RESETIRQ2 MASK | R | 0h | |

### 6.6.12 IRQLVL1msK Register (address = 0x13) [reset = 0xA5]

IRQLVL1msK is shown in Figure 6-33 and described in Table 6-14.

Return to Summary Table.

Register domain: RTC

**Figure 6-33. IRQLVL1msK Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MRESET | RESERVED2_IRQLVL1msK | MPMU | RESERVED1_IRQLVL1msK[1:0] | | MPWRSRC | RESERVED_IRQLVL1msK | MPWRBTN |
| R/W-1h | R-0h | R/W-1h | R-0h | | R/W-1h | R-0h | R/W-1h |

**Table 6-14. IRQLVL1msK Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MRESET | R/W | 1h | RESET mask interrupt<br>0h = Not masked<br>1h = Masked |
| 6 | RESERVED2_IRQLVL1msK | R | 0h | |
| 5 | MPMU | R/W | 1h | Power monitor mask interrupt<br>0h = Not masked<br>1h = Masked |
| 4-3 | RESERVED1_IRQLVL1msK[1:0] | R | 0h | |
| 2 | MPWRSRC | R/W | 1h | Power source mask interrupt<br>0h = Not masked<br>1h = Masked |
| 1 | RESERVED_IRQLVL1msK | R | 0h | |
| 0 | MPWRBTN | R/W | 1h | Power button mask interrupt<br>0h = Not masked<br>1h = Masked |

### 6.6.13 PBCONFIG Register (address = 0x14) [reset = 0x1F]

PBCONFIG is shown in Figure 6-34 and described in Table 6-15.

Return to Summary Table.

Register domain: RTC

**Figure 6-34. PBCONFIG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWRBTNDBN | CLRHT | FLT[5:0] | | | | | |
| R/W-0h | R/W-0h | R/W-1Fh | | | | | |

**Table 6-15. PBCONFIG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PWRBTNDBN | R/W | 0h | Power button debounce<br>0h = 30 ms<br>1h = 0 ms (no debounce) |
| 6 | CLRHT | R/W | 0h | Reset of power button timer logic<br>0h = No action<br>1h = Reset of HT, bit is self clearing |
| 5-0 | FLT[5:0] | R/W | 1Fh | Time that the button must be held to force an emergency reset<br>0h: 0 s<br>1h: 1 s<br>2h: 2 s<br>3h: 3 s<br>4h: 4 s<br>5h = 5 s<br>6h: 6 s<br>7h: 7 s<br>8h: 8 s<br>9h: 9 s<br>Ah: 10 s<br>...<br>1Fh: 31 s<br>...<br>3Ch: 60 s<br>3Dh: 61 s<br>3Eh: 62 s<br>3Fh: 63 s |

### 6.6.14 PBSTATUS Register (address = 0x15) [reset = 0x00]

PBSTATUS is shown in Figure 6-35 and described in Table 6-16.

Return to Summary Table.

Register domain: RTC

**Figure 6-35. PBSTATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_PBSTATUS | LVL | HT[5:0] | | | | | |
| R-0h | R-0h | R-0h | | | | | |

**Table 6-16. PBSTATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED_PBSTATUS | R | 0h | |
| 6 | LVL | R | 0h | Power button present level<br>0h = Power button held<br>1h = Power button released |
| 5-0 | HT[5:0] | R | 0h | Time that the button has been held<br>0h = Disabled<br>1h = Disabled<br>2h = 2 s<br>3h = 3 s<br>4h = 4 s<br>5h = 5 s<br>6h = 6 s<br>7h = 7 s<br>8h = 8 s<br>9h = 9 s<br>Ah = 10 s<br>...<br>3Ch = 60 s<br>3Dh = 61 s<br>3Eh = 62 s<br>3Fh = 63 s |

### 6.6.15 PWRSTAT1 Register (address = 0x16) [reset = 0x00]

PWRSTAT1 is shown in Figure 6-36 and described in Table 6-17.

Return to Summary Table.

Register domain: RTC

**Figure 6-36. PWRSTAT1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VCCIO_FAULT | V5A_FAULT | V33A_PCH_FAULT | V33A_DSW_FAULT | V18A_FAULT | V18U_25U_FAULT | VDDQ_FAULT | V06DX_FAULT |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 6-17. PWRSTAT1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VCCIO_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |
| 6 | V5A_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |
| 4 | V33A_PCH_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |
| 5 | V33A_DSW_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |
| 3 | V18A_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |
| 2 | V18U_25U_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |
| 1 | VDDQ_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |
| 0 | V06DX_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |

### 6.6.16 PWRSTAT2 Register (address = 0x17) [reset = 0x00]

PWRSTAT2 is shown in Figure 6-37 and described in Table 6-18.

Return to Summary Table.

Register domain: RTC

**Figure 6-37. PWRSTAT2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED[5:0] | | | | | | V105A_FAULT | VPRIMCORE_FAULT |
| R-0h | | | | | | R/W-0h | R/W-0h |

**Table 6-18. PWRSTAT2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED[5:0] | R | 0h | |
| 1 | V105A_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |
| 0 | VPRIMCORE_FAULT | R/W | 0h | These bits indicate that the VR has lost regulation<br>0h = Clears register<br>1h = Indicates power fault |

### 6.6.17 PGMASK1 Register (address = 0x18) [reset = 0x00]

PGMASK1 is shown in Figure 6-38 and described in Table 6-19.

Return to Summary Table.

Register domain: RTC

**Figure 6-38. PGMASK1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MVCCIOPG | MVPRIMCOREPG | MV105APG | MV18APG | MV33ADSWPG | MV5APG | MV33APCHPG | MV105SPG |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 6-19. PGMASK1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MVCCIOPG | R/W | 0h | VCCIO PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 6 | MVPRIMCOREPG | R/W | 0 h | V0.85A PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 5 | MV105APG | R/W | 0h | V105A PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 4 | MV18APG | R/W | 0h | V1.8A PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 3 | MV33ADSWPG | R/W | 0h | V3.3A DSW PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 2 | MV5APG | R/W | 0h | V5AA DS3 PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 1 | MV33APCHPG | R/W | 0h | V3.3A PCH PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 0 | MV105SPG | R/W | 0h | V105S PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |

### 6.6.18 PGMASK2 Register (address = 0x19) [reset = 0x00]

PGMASK2 is shown in Figure 6-39 and described in Table 6-20.

Return to Summary Table.

Register domain: RTC

**Figure 6-39. PGMASK2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_PGMASK2[3:0] | | | | V18U25UPG | MVDDQPG | MV33SPG | MV18SPG |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 6-20. PGMASK2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED_PGMASK2[3:0] | R | 0h | |
| 3 | V18U25UPG | R/W | 0h | V1.8_2.5U PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 2 | MVDDQPG | R/W | 0h | VDDQ PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 1 | MV33SPG | R/W | 0h | V3.3S PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |
| 0 | MV18SPG | R/W | 0h | V1.8S PG is part of the power good tree<br>0h = Power good function is enabled<br>1h = Power good function is masked and set to 1 (not part of the power good tree) |

### 6.6.19 VCCIOCNT Register (address = 0x30) [reset = 0x1Ah]

VCCIOCNT is shown in Figure 6-40 and described in Table 6-21.

Return to Summary Table.

Register domain: RESET

**Figure 6-40. VCCIOCNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_VCCIOCNT | CSDECAYEN | RESERVED_VCCIOVSEL | | RESERVED | | CTLVVCCIO[1:0] | |
| R-0h | R/W-0h | R-1h | | R-2h | | R/W-2h | |

**Table 6-21. VCCIOCNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED_VCCIOCNT | R | 0h | |
| 6 | CSDECAYEN | R/W | 0h | Enables VCCIO decay when $\overline{\text{SLP\_S0}}$ is asserted.<br>Wait 2 µs after removing FPWM, before entering DECAY mode. Direct FPWM to DECAY by $\overline{\text{SLP\_S0}}$ may cause ringing. Decay exit time within 100 µs not ensured for $V_{OUT}$ > 1 V.)<br>0h = VCCIO stays at voltage set by VCCIOVSEL independent of state of $\overline{\text{SLP\_S0}}$<br>1h = VCCIO decays to 0 V, PGOOD is maintained when $\overline{\text{SLP\_S0}}$ is asserted (low) |
| 5-4 | RESERVED_VCCIOVSEL | R | 1h | |
| 3-2 | RESERVED | R | 2h | |
| 1-0 | CTLVVCCIO[1:0] | R/W | 2h | Mode control (VCCIO)<br>0h = Converter disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |

### 6.6.20 VPRIMCORECNT Register (address = 0x31) [reset = 0x4A]

VPRIMCORECNT is shown in Figure 6-41 and described in Table 6-22.

Return to Summary Table.

Register domain: RESET

**Figure 6-41. VPRIMCORECNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VPRIMCORELVSEL[1:0] | | VPRIMCOREVSEL[1:0] | | AOACCNTVPRIMCORE[1:0] | | CTLVPRIMCORE[1:0] | |
| R/W-1h | | R/W-0h | | R/W-2h | | R/W-2h | |

**Table 6-22. VPRIMCORECNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | VPRIMCORELVSEL[1:0] | R/W | 1h | VPRIMCORE low power mode output voltage set point<br>Set at assertion of $\overline{\text{SLP\_S0}}$<br>0h = Disabled, voltage stays at value set by VPRIMCOREVSEL[1:0]<br>1h = 0.75 V<br>2h = 0.8 V<br>3h = 0.85 V |
| 5-4 | VPRIMCOREVSEL[1:0] | R/W | 0h | Output voltage select<br>0h = 0.95 V<br>1h = 0.9 V<br>2h = 0.85 V<br>3h = 0.8 V |
| 3-2 | AOACCNTVPRIMCORE[1:0] | R/W | 2h | Mode control for exit standby (rising edge of $\overline{\text{SLP\_S0}}$)<br>Changes bits on exit<br>0h = No change in bits; fast change mode disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |
| 1-0 | CTLVPRIMCORE[1:0] | R/W | 2h | Mode control (VPRIMCORE)<br>0h = Converter disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |

### 6.6.21 V33ADSWCNT Register (address = 0x32) [reset = 0x2A]

V33ADSWCNT is shown in Figure 6-42 and described in Table 6-23.

Return to Summary Table.

Register domain: RESET

**Figure 6-42. V33ADSWCNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| V33ADSWLVSEL[1:0] | | V33ADSWVSEL[1:0] | | AOACCNTV33ADSW[1:0] | | CTLV33ADSW[1:0] | |
| R/W-0h | | R/W-2h | | R/W-2h | | R/W-2h | |

**Table 6-23. V33ADSWCNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | V33ADSWLVSEL[1:0] | R/W | 0h | V33A_DSW low power mode output voltage set point - set at assertion of SLP_S0<br>0h = Disabled, voltage stays at value set by V33ADSWVSEL[1:0]<br>1h = Vnom – 4%<br>2h = Vnom – 3%<br>3h = Vnom – 2% |
| 5-4 | V33ADSWVSEL[1:0] | R/W | 2h | Output voltage select<br>0h = Vnom + 3 %<br>1h = Vnom + 2 %<br>2h = Vnom<br>3h = Vnom – 2 % |
| 3-2 | AOACCNTV33ADSW[1:0] | R/W | 2h | Mode control for exit standby (rising edge of SLP_S0) Changes bits on exit<br>0h = No change in bits; fast change mode disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |
| 1-0 | CTLV33ADSW[1:0] | R/W | 2h | Mode control (V33ADSW)<br>0h = Converter disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |

### 6.6.22 V33APCHCNT Register (address = 0x33) [reset = 0x0A]

V33APCHCNTis shown in Figure 6-43 and described in Table 6-24.

Return to Summary Table.

Register domain: RESET

**Figure 6-43. V33APCHCNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_V33APCHCNT[3:0] | | | | RESERVED | | CTLV33APCH[1:0] | |
| R/W-0h | | | | R/W-2h | | R/W-2h | |

**Table 6-24. V33APCHCNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED_V33APCHCNT[3:0] | R/W | 0h | |
| 3-2 | RESERVED | R | 2h | |
| 1-0 | CTLV33APCH[1:0] | R/W | 2h | Mode control (V33APCH)<br>0h = Disabled<br>1h = Enabled<br>2h = Enabled<br>3h = Enabled |

### 6.6.23 V18ACNT Register (address = 0x34) [reset = 0x2A]

V18ACNT is shown in Figure 6-44 and described in Table 6-25.

Return to Summary Table.

Register domain: RESET

**Figure 6-44. V18ACNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| V18ALVSEL[1:0] | | V18AVSEL[1:0] | | AOACCNTV18A[1:0] | | CTLV18A[1:0] | |
| R/W-0h | | R/W-2h | | R/W-2h | | R/W-2h | |

**Table 6-25. V18ACNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | V18ALVSEL[1:0] | R/W | 0h | V18A low power mode output voltage set point<br>Set at assertion of $\overline{\text{SLP\_S0}}$<br>0h = Disabled, voltage stays at value set by V18AVSEL[1:0]<br>1h = Vnom – 4%<br>2h = Vnom – 3%<br>3h = Vnom – 2% |
| 5-4 | V18AVSEL[1:0] | R/W | 2h | Output voltage select<br>0h = Vnom + 3 %<br>1h = Vnom + 2 %<br>2h = Vnom<br>3h = Vnom – 2 % |
| 3-2 | AOACCNTV18A[1:0] | R/W | 2h | Mode control for exit standby (rising edge of $\overline{\text{SLP\_S0}}$)<br>Changes bits on exit<br>0h = No change in bits; fast change mode disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |
| 1-0 | CTLV18A[1:0] | R/W | 2h | Mode control (V18A)<br>0h = Converter disabled<br>1h = Auto Mode, (automatic transition from PFM to PWM)<br>2h = Auto Mode, (automatic transition from PFM to PWM)<br>3h = Forced PWM operation |

### 6.6.24 V18U25UCNT Register (address = 0x35) [reset = 0x0A]

V18U25UCNT is shown in Figure 6-45 and described in Table 6-26.

Return to Summary Table.

Register domain: RESET

**Figure 6-45. V18U25UCNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_V18U25UCNT[3:0] | | | | RESERVED_AOACCNTV18U25U | | CTLV18U25U[1:0] | |
| R-0h | | | | R-2h | | R/W-2h | |

**Table 6-26. V18U25UCNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED_V18U25UCNT[3:0] | R | 0h | |
| 3-2 | RESERVED_AOACCNTV18U25U | R | 2h | |
| 1-0 | CTLV18U25U[1:0] | R/W | 2h | Mode control (V18U25U)<br>0h = Disabled<br>1h = Enabled<br>2h = Enabled<br>3h = Enabled |

### 6.6.25 VDDQCNT Register (address = 0x36) [reset = 0x3A]

VDDQCNT is shown in Figure 6-46 and described in Table 6-27.

Return to Summary Table.

Register domain: RESET

**Figure 6-46. VDDQCNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VDDQLVSEL | VDDQVSEL[2:0] | | | AOACCNTVDDQ[1:0] | | CTLVDDQ[1:0] | |
| R/W-0h | R/W-3h | | | R/W-2h | | R/W-2h | |

**Table 6-27. VDDQCNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VDDQLVSEL | R/W | 0h | VDDQ low power mode output voltage set point - set at assertion of SLP_S0<br>0h = Disabled, voltage stays at value set by VDDQVSEL<br>1h = Vnom – 3% |
| 6-4 | VDDQVSEL[2:0] | R/W | 3h | Output voltage select<br>0h = Vnom + 3%<br>1h = Vnom + 2%<br>2h = Vnom + 1%<br>3h = Vnom + 0%<br>4h = Vnom – 1%<br>5h = Vnom – 2%<br>6h = Vnom – 3%<br>7h = Vnom – 4% |
| 3-2 | AOACCNTVDDQ[1:0] | R/W | 2h | Mode control for exit standby (rising edge of $\overline{\text{SLP\_S0}}$)<br>Changes bits on exit<br>0h = no change in bits; fast change mode disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = forced PWM operation |
| 1-0 | CTLVDDQ[1:0] | R/W | 2h | Mode control (VDDQ)<br>0h = Converter disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |

### 6.6.26 V105ACNT Register (address = 0x37) [reset = 0x0A]

V105ACNT is shown in Figure 6-47 and described in Table 6-28.

Return to Summary Table.

Register domain: RESET

**Figure 6-47. V105ACNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| V105ALVSEL[1:0] | | V105AVSEL[1:0] | | AOACCNTV105A[1:0] | | CTLV105A[1:0] | |
| R/W-0h | | R/W-0h | | R/W-2h | | R/W-2h | |

**Table 6-28. V105ACNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | V105ALVSEL[1:0] | R/W | 0h | V105A low power mode output voltage set point<br>Set at assertion of $\overline{\text{SLP\_S0}}$<br>0h = Disabled, voltage stays at value set by V105AVSEL[1:0]<br>1h = Vnom – 4%<br>2h = Vnom – 3%<br>3h = Vnom – 2% |
| 5-4 | V105AVSEL[1:0] | R/W | 0h | Output voltage select<br>0h = Vnom + 5 % (1.05 V)<br>1h = Vnom (1 V)<br>2h = Vnom -2.5 % (0.975 V)<br>3h = Vnom – 5 % (0.95 V) |
| 3-2 | AOACCNTV105A[1:0] | R/W | 2h | Mode control for exit standby (rising edge of $\overline{\text{SLP\_S0}}$)<br>Changes bits on exit<br>0h = No change in bits D[1:0], fast change mode disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |
| 1-0 | CTLV105A[1:0] | R/W | 2h | Mode control (V105A)<br>0h = Converter disabled<br>1h = Auto Mode, automatic transition from PFM to PWM<br>2h = Auto Mode, automatic transition from PFM to PWM<br>3h = Forced PWM operation |

### 6.6.27 V5ACNT Register (address = 0x38) [reset = 0x2A]

V5ACNT is shown in Figure 6-48 and described in Table 6-29.

Return to Summary Table.

Register domain: RESET

**Figure 6-48. V5ACNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_V5ALVSEL[1:0] | | RESERVED_V5AVSEL[1:0] | | RESERVED_AOACCNTV5A[1:0] | | RESERVED_CTLV5A[1:0] | |
| R-0h | | R-2h | | R-2h | | R-2h | |

**Table 6-29. V5ACNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED_V5ALVSEL[1:0] | R | 0h | V5A low power mode output voltage set point<br>Set at assertion of $\overline{\text{SLP\_S0}}$<br>0h = Disabled, voltage stays at value set by V5AVSEL[1:0]<br>1h = Vnom – 4%<br>2h = Vnom – 3%<br>3h = Vnom – 2% |
| 5-4 | RESERVED_V5AVSEL[1:0] | R | 2h | Output voltage select<br>0h = Vnom + 3 %<br>1h = Vnom + 2 %<br>2h = Vnom<br>3h = Vnom – 2 % |
| 3-2 | RESERVED_AOACCNTV5A[1:0] | R | 2h | Mode control for exit standby (rising edge of $\overline{\text{SLP\_S0}}$)<br>Changes bits on exit<br>0h = No change in bits; fast change mode disabled<br>1h = Auto Mode, (automatic transition from PFM to PWM)<br>2h = Auto Mode, (automatic transition from PFM to PWM)<br>3h = Forced PWM operation |
| 1-0 | RESERVED_CTLV5A[1:0] | R | 2h | Mode control (V5A)<br>0h = Converter disabled<br>1h = Auto Mode, (automatic transition from PFM to PWM)<br>2h = Auto Mode, (automatic transition from PFM to PWM)<br>3h = Forced PWM operation |

### 6.6.28 VRMODECTRL Register (address = 0x3B) [reset = 0x3F]

VRMODECTRL is shown in Figure 6-49 and described in Table 6-30.

Return to Summary Table.

Register domain: RESET

**Figure 6-49. VRMODECTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_VRMODECTRL[1:0] | | V33APCH_LPM | RESERVED_VCCIO_LPM | RESERVED_V5A_LPM | VDDQ_LPM | V105A_LPM | VPRIMCORE_LPM |
| R-0h | | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

**Table 6-30. VRMODECTRL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED_VRMODECTRL[1:0] | R | 0h | |
| 5 | V33APCH_LPM | R/W | 1h | Force low power mode (Auto mode). This feature is only used if forcing PWM in the CTLV33APCH[1:0] bits of the V33APCHCNT register.<br>0h = Force Auto mode when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$) is asserted (low). This overrides the setting of the V33APCHCNT register, bits CTLV33APCH[1:0] when $\overline{\text{STANDBY}}$ is low.<br>1h = Mode set by CTLV33APCH[1:0] bits when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$). Does what is setting of register bits CTLV33APCH[1:0] when $\overline{\text{STANDBY}}$ is low. |
| 4 | RESERVED_VCCIO_LPM | R | 1h | Force low power mode (Auto mode). This is only used if forcing PWM in CTLVCCIO[1:0] bits of VCCIOCNT register.<br>0h = Force Auto mode when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$) is asserted (low). This overrides the setting of the VCCIOCNT register, bits CTLVCCIO[1:0] when $\overline{\text{STANDBY}}$ is low.<br>1h = Mode set by CTLVCCIO[1:0] bits when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$). Does what is setting of register bits CTLVCCIO[1:0] when $\overline{\text{STANDBY}}$ is low. |
| 3 | RESERVED_V5A_LPM | R | 1h | Force low power mode (Auto mode). This is only used if forcing PWM in CTLVPRIMCORE[1:0] register.<br>0h = Force Auto mode when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$) is asserted (low). This overrides the setting of the VPRIMCORECNT register, bits CTLVPRIMCORE[1:0] when $\overline{\text{STANDBY}}$ is low.<br>1h = Mode set by CTLVPRIMCORE[1:0] bits when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$). Does what is setting of register bits CTLVPRIMCORE[1:0] when $\overline{\text{STANDBY}}$ is low. |
| 2 | VDDQ_LPM | R/W | 1h | Force low power mode (Auto mode). This is only used if forcing PWM in CTLVDDQ[1:0] bits in VDDQCNT register.<br>0h = Force Auto mode when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$) is asserted (low). This overrides the setting of the VDDQCNT register, bits CTLVDDQ[1:0] when $\overline{\text{STANDBY}}$ is low}<br>1h = Mode set by CTLVDDQ[1:0] bits when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$). Does what is setting of register bits CTLVDDQ[1:0] when $\overline{\text{STANDBY}}$ is low. |

**Table 6-30. VRMODECTRL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 1 | V105A_LPM | R/W | 1h | Force low power mode (Auto mode). This is only used if forcing PWM in CTLV105A [1:0] bits in V105ACNTregister.<br>0h = Force Auto mode when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$) is asserted (low). This overrides the setting of the V105ACNT register, bits CTLV105A [1:0] when $\overline{\text{STANDBY}}$ is low.<br>1h = Mode set by CTLV105A [1:0] bits when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$). Does what is setting of register bits CTLV105A[1:0] when $\overline{\text{STANDBY}}$ is low. |
| 0 | VPRIMCORE_LPM | R/W | 1h | Force low power mode (Auto mode). This is only used if forcing PWM in CTLV5A [1:0] bits in V5ACNT register.<br>0h = Force Auto mode when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$) is asserted (low). This overrides the setting of the V5A register, CNT bits CTLVV33ADSW[1:0] when $\overline{\text{STANDBY}}$ is low.<br>1h = Mode set by CTLV5A [1:0] bits when $\overline{\text{STANDBY}}$ ($\overline{\text{SLP\_S0}}$). Does what is setting of register bits CTLV5A [1:0] when $\overline{\text{STANDBY}}$ is low. |

### 6.6.29 DISCHCNT1 Register (address = 0x3C) [reset = 0x00]

DISCHCNT1 is shown in Figure 6-50 and described in Table 6-31.

Return to Summary Table.

Register domain: RESET

**Figure 6-50. DISCHCNT1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_DISCHCNT1[5:0] | | | | | | VCCIODISCHG[1:0] | |
| R-0h | | | | | | R/W-0h | |

**Table 6-31. DISCHCNT1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED_DISCHCNT1[5:0] | R | 0h | |
| 1-0 | VCCIODISCHG[1:0] | R/W | 0h | VCCIO discharge resistance<br>0h = >1000 kΩ<br>1h = 125 Ω<br>2h = 225 Ω<br>3h = 550 Ω |

### 6.6.30 DISCHCNT2 Register (address = 0x3D) [reset = 0x00]

DISCHCNT2 is shown in Figure 6-51 and described in Table 6-32.

Return to Summary Table.

Register domain: RESET

**Figure 6-51. DISCHCNT2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| V5ADISCHG[1:0] | | V33APCHDISCHG[1:0] | | V33PCHDISCHG[1:0] | | V18ADISCH[1:0] | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 6-32. DISCHCNT2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | V5ADISCHG[1:0] | R/W | 0h | V5A discharge resistance<br>0h = No discharge<br>1h = 100 Ω<br>2h = 200 Ω<br>3h = 500 Ω |
| 5-4 | V33APCHDISCHG[1:0] | R/W | 0h | V33A_PCH discharge resistance<br>0h = No discharge<br>1h = 100 Ω<br>2h = 200 Ω<br>3h = 500 Ω |
| 3-2 | V33PCHDISCHG[1:0] | R/W | 0h | V33A_PCH discharge resistance at VSA<br>0h = No discharge<br>1h = 100 Ω<br>2h = 200 Ω<br>3h = 500 Ω |
| 1-0 | V18ADISCH[1:0] | R/W | 0h | V18A discharge resistance<br>0h = 860 Ω<br>1h = 100 Ω<br>2h = 200 Ω<br>3h = 500 Ω |

### 6.6.31 DISCHCNT3 Register (address = 0x3E) [reset = 0x00]

DISCHCNT3 is shown in Figure 6-52 and described in Table 6-33.

Return to Summary Table.

Register domain: RESET

**Figure 6-52. DISCHCNT3 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| V18U25UDISCHG[1:0] | | VDDQDISCHG[1:0] | | V105ADISCHG[1:0] | | VPRIMCOREDISCH[1:0] | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 6-33. DISCHCNT3 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | V18U25UDISCHG[1:0] | R/W | 0h | V1.8U_2.5U discharge resistance at VSB<br>0h = No discharge<br>1h = 100 Ω<br>2h = 200 Ω<br>3h = 500 Ω |
| 5-4 | VDDQDISCHG[1:0] | R/W | 0h | VDDQ discharge resistance at FBVR4P<br>0h = >1000 kΩ<br>1h = 125 Ω<br>2h = 225 Ω<br>3h = 550 Ω |
| 3-2 | V105ADISCHG[1:0] | R/W | 0h | V105A discharge resistance at FBVR1P<br>0h = >1000 kΩ<br>1h = 125 Ω<br>2h = 225 Ω<br>3h = 550 Ω |
| 1-0 | VPRIMCOREDISCH[1:0] | R/W | 0h | VPRIMCORE discharge resistance<br>0h = >1000 kΩ<br>1h = 150 Ω<br>2h = 250 Ω<br>3h = 575 Ω |

### 6.6.32 DISCHCNT4 Register (address = 0x3F) [reset = 0x00]

DISCHCNT4 is shown in Figure 6-53 and described in Table 6-34.

Return to Summary Table.

Register domain: RESET

**Figure 6-53. DISCHCNT4 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_DISCHCNT4[1:0] | | V33SDISCHG[1:0] | | V18SDISCHG[1:0] | | V105SDISCH[1:0] | |
| R-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**Table 6-34. DISCHCNT4 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED_DISCHCNT4[1:0] | R | 0h | |
| 5-4 | V33SDISCHG[1:0] | R/W | 0h | V3.3S discharge resistance at VSE<br>0h = No discharge<br>1h = 100 Ω<br>2h = 200 Ω<br>3h = 500 Ω |
| 3-2 | V18SDISCHG[1:0] | R/W | 0h | V18S discharge resistance at VSF<br>0h = No discharge<br>1h = 100 Ω<br>2h = 200 Ω<br>3h = 500 Ω |
| 1-0 | V105SDISCH[1:0] | R/W | 0h | V105S discharge resistance at VSG<br>0h = No discharge<br>1h = 100 Ω<br>2h = 200 Ω<br>3h = 500 Ω |

### 6.6.33 PWRGDCNT1 Register (address = 0x40) [reset = 0x5F]

PWRGDCNT1 is shown in Figure 6-54 and described in Table 6-35.

Return to Summary Table.

Register domain: RESET

**Figure 6-54. PWRGDCNT1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_PWRGDCNT1 | RSMRSTN_PWRGD[1:0] | | PCH_PWROK[1:0] | | DEL_ALL_SYS_PWRGD[2:0] | | |
| R-0h | R/W-2h | | R/W-3h | | R/W-7h | | |

**Table 6-35. PWRGDCNT1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED_PWRGDCNT1 | R | 0h | |
| 6-5 | RSMRSTN_PWRGD[1:0] | R/W | 2h | Delay of RSMRSTN_PWRGD (RTC = 30.5 µs ± 10%)<br>0h = No Delay<br>1h = 164x RTC (5.5 ms)<br>2h = 360x RTC (11 ms)<br>3h = 721x RTC (22 ms) |
| 4-3 | PCH_PWROK[1:0] | R/W | 3h | Delay of PCH_PWROK compared to ALL_SYS_PWRGD (RTC = 30.5 µs ± 10%)<br>0h = 82x RTC (2.5 ms)<br>1h = 164x RTC (5 ms)<br>2h = 328x RTC (10 ms)<br>3h = 656x RTC (20 ms) |
| 2-0 | DEL_ALL_SYS_PWRGD[2:0] | R/W | 7h | Delay of SYS_PWR_OK compared to ALL_SYS_PWRGD (RTC = 30.5 µs ± 10%)<br>0h = 82x RTC (2.5 ms)<br>1h = 164x RTC (5 ms)<br>2h = 328x RTC (10 ms)<br>3h = 492x RTC (15 ms)<br>4h = 656x RTC (20 ms)<br>5h = 1640x RTC (50 ms)<br>6h = 2460x RTC (75 ms)<br>7h = 3280x RTC (100 ms) |

### 6.6.34 VREN Register (address = 0x41) [reset = 0x00]

VREN is shown in Figure 6-55 and described in Table 6-36.

Return to Summary Table.

Register domain: RESET

**Figure 6-55. VREN Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_VREN[5:0] | | | | | | EC_SLP_S4 | EC_DS4 |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

**Table 6-36. VREN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED_VREN[5:0] | R/W | 0h | |
| 1 | EC_SLP_S4 | R/W | 0h | 0h = Disable<br>1h = Enable |
| 0 | EC_DS4 | R/W | 0h | 0h = Disable<br>1h = Enable |

### 6.6.35 REGLOCK Register (address = 0x42) [reset = 0x00]

REGLOCK is shown in Figure 6-56 and described in Table 6-37.

Return to Summary Table.

Register domain: RESET

**Figure 6-56. REGLOCK Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED[6:0] | | | | | | | CNTLOCK |
| R-0h | | | | | | | R/W-0h |

**Table 6-37. REGLOCK Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED[6:0] | R | 0h | |
| 0 | CNTLOCK | R/W | 0h | Locks all VxCNT registers<br>0h = All VxCNT registers are unlocked and can be overwritten<br>1h = All VxCNT registers are locked and cannot be overwritten |

### 6.6.36 VRENPINMASK Register (address = 0x43) [reset = 0x00]

VRENPINMASK is shown in Figure 6-57 and described in Table 6-38.

Return to Summary Table.

Register domain: RESET

**Figure 6-57. VRENPINMASK Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MVPRIMCOREEN | MV105AEN | MVDDQEN | MV18U25UEN | MV18AEN | MV33APCHEN | MV5AEN | MVCCIOEN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 6-38. VRENPINMASK Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MVPRIMCOREEN | R/W | 0h | VPRIMCORE enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |
| 6 | MV105AEN | R/W | 0h | V105A enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |
| 5 | MVDDQEN | R/W | 0h | VDDQ enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |
| 4 | MV18U25UEN | R/W | 0h | V18U25U enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |
| 3 | MV18AEN | R/W | 0h | V18A enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |
| 2 | MV33APCHEN | R/W | 0h | V33APCH enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |
| 1 | MV5AEN | R/W | 0h | V5A enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |
| 0 | MVCCIOEN | R/W | 0h | VCCIO enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |

### 6.6.37 RSTCTRL Register (address = 0x48) [reset = 0x1C]

RSTCTRL is shown in Figure 6-58 and described in Table 6-39.

Return to Summary Table.

Register domain: RTC

**Figure 6-58. RSTCTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_RSTCTRL[2:0] | | | TRST[1:0] | | VTHRST[2:0] | | |
| R-0h | | | R/W-3h | | R/W-4h | | |

**Table 6-39. RSTCTRL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | RESERVED_RSTCTRL[2:0] | R | 0h | |
| 4-3 | TRST[1:0] | R/W | 3h | Reset time duration<br>0h = 20 ms<br>1h = 40 ms<br>2h = 80 ms<br>3h = 200 ms |
| 2-0 | VTHRST[2:0] | R/W | 4h | Reset voltage threshold<br>0h = 1.4 V<br>1h = 1.5 V<br>2h = 1.6 V<br>3h = 1.7 V<br>4h = 2.4 V<br>5h = 2.6 V<br>6h = 2.8 V<br>7h = 3 V |

### 6.6.38 SDWNCTRL Register (address = 0x49) [reset = 0x00]

SDWNCTRL is shown in Figure 6-59 and described in Table 6-40.

Return to Summary Table.

Register domain: RESET

**Figure 6-59. SDWNCTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_SDWNCTRL[6:0] | | | | | | | SDWN |
| R-0h | | | | | | | R/W-0h |

**Table 6-40. SDWNCTRL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED_SDWNCTRL[6:0] | R | 0h | |
| 0 | SDWN | R/W | 0h | Forced emergency reset, bit is self clearing<br>0h = No action<br>1h = Force emergency reset |

### 6.6.39 VDLMTCRT Register (address = 0x51) [reset = 0x05]

VDLMTCRT is shown in Figure 6-60 and described in Table 6-41.

Return to Summary Table.

Register domain: RESET

**Figure 6-60. VDLMTCRT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_VDLMTCRT | VDLMTCOMP | TDBNCVDLMTCRT[1:0] | | VDLMTCRTH[3:0] | | | |
| R/W-0h | R/W-0h | R/W-0h | | R/W-5h | | | |

**Table 6-41. VDLMTCRT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED_VDLMTCRT | R/W | 0h | |
| 6 | VDLMTCOMP | R/W | 0h | Critical supply voltage comparator for VDCSNS pin input voltage sense. Connect voltage divider resistors from VIN to detect when input voltage is low<br>0h = disable<br>1h = enable |
| 5-4 | TDBNCVDLMTCRT[1:0] | R/W | 0h | Supply voltage monitor debounce of VDCSNS input voltage sense pin<br>0h = No Deglitch<br>1h = 10 µs<br>2h = 1x RTC (30 µs)<br>3h = 2x RTC (60 µs) |
| 3-0 | VDLMTCRTH[3:0] | R/W | 5h | Critical supply voltage falling threshold on VDCSNS pin. Connect voltage divider resistors from VIN to detect when input voltage is low. For 2S should be 4X top resistor, X bottom resistor. (rising hysteresis = 20 mV)<br>0h = No limit<br>1h = 1.2 V<br>2h = 1.18 V<br>3h = 1.16 V<br>4h = 1.14 V<br>5h = 1.12 V<br>6h = 1.1 V<br>7h = 1.08 V<br>8h to Fh = Not applicable |

### 6.6.40 ACOKDBDM Register (address = 0x69) [reset = 0x0F]

ACOKDBDM is shown in Figure 6-61 and described in Table 6-42.

Return to Summary Table.

Register domain: RESET

**Figure 6-61. ACOKDBDM Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_ACOKDBDM[3:0] | | | | ACOKDB[1:0] | | ACOKDM[1:0] | |
| R/W-0h | | | | R/W-3h | | R/W-3h | |

**Table 6-42. ACOKDBDM Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED_ACOKDBDM[3:0] | R/W | 0h | |
| 3-2 | ACOKDB[1:0] | R/W | 3h | Adapter detection debounce time<br>0h = 81 µs<br>1h = 10 ms<br>2h = 20 ms<br>3h = 30 ms |
| 1-0 | ACOKDM[1:0] | R/W | 3h | Adapter detection mode<br>0h = reserved<br>1h = low-to-high<br>2h = high-to-low<br>3h = both, low-to-high and high-to-low |

### 6.6.41 LOWBATTDET Register (address = 0x6A) [reset = 0xF8]

LOWBATTDET is shown in Figure 6-62 and described in Table 6-43.

Return to Summary Table.

Register domain: RESET

**Figure 6-62. LOWBATTDET Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LOWBATTDB[1:0] | | LOWBATT2_EN | LOWBATT1_EN | ACIN_EN | RESERVED_LOWBATTDET[2:0] | | |
| R/W-3h | | R/W-1h | R/W-1h | R/W-1h | R/W-0h | | |

**Table 6-43. LOWBATTDET Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | LOWBATTDB[1:0] | R/W | 3h | Low battery detection debounce time<br>0h = 4 RTC periods (120 µs)<br>1h = 32 RTC periods (960 µs)<br>2h = 64 RTC periods (1920 µs)<br>3h = 128 RTC periods (3840 µs) |
| 5 | LOWBATT2_EN | R/W | 1h | Low battery two detection enable<br>0h = Disable<br>1h = Enable |
| 4 | LOWBATT1_EN | R/W | 1h | Low battery One detection Enable<br>0h = Disable<br>1h = Enable |
| 3 | ACIN_EN | R/W | 1h | AC IN Comparator<br>0h = Disable<br>1h = Enable |
| 2-0 | RESERVED_LOWBATTDET[2:0] | R/W | 0h | |

### 6.6.42 SPWRSRCINT Register (address = 0x6F) [reset = 0x00]

SPWRSRCINT is shown in Figure 6-63 and described in Table 6-44.

Return to Summary Table.

Register domain: RESET

**Figure 6-63. SPWRSRCINT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED1_SPWRSRCINT | SLOWBATT2 | SLOWBATT1 | SACOK | RESERVED_SPWRSRCINT[3:0] | | | |
| R-0h | R-0h | R-0h | R-0h | R-0h | | | |

**Table 6-44. SPWRSRCINT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED1_SPWRSRCINT | R | 0h | |
| 6 | SLOWBATT2 | R | 0h | LOWBATT2 detection status<br>0h = BATT2 above threshold<br>1h = BATT2 below threshold |
| 5 | SLOWBATT1 | R | 0h | LOWBATT1 detection status<br>0h = BATT1 above threshold<br>1h = BATT1 below threshold |
| 4 | SACOK | R | 0h | AC adapter (ACOK) detection status<br>0h = Adapter removed<br>1h = Adapter inserted |
| 3-0 | RESERVED_SPWRSRCINT[3:0] | R | 0h | |

### 6.6.43 CLKCTRL1 Register (address = 0xD0) [reset = 0x00]

CLKCTRL1 is shown in Figure 6-64 and described in Table 6-45.

Return to Summary Table.

Register domain: RTC

**Figure 6-64. CLKCTRL1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_CLKCTRL1[6:0] | | | | | | | ECWAKEEN |
| R/W-0h | | | | | | | R/W-0h |

**Table 6-45. CLKCTRL1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED_CLKCTRL1[6:0] | R/W | 0h | |
| 0 | ECWAKEEN | R/W | 0h | 1-Hz clock<br>0h = Clock OFF<br>1h = Clock ON |

### 6.6.44 COMPA_REF Register (address = 0xDD) [reset = 0xB6]

COMPA_REF is shown in Figure 6-65 and described in Table 6-46.

Return to Summary Table.

Register domain: RESET

**Figure 6-65. COMPA_REF Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COMPA_Mode | COMPA_DVS[3:0] | | | | COMPA_VSEL[2:0] | | |
| R/W-1h | R/W-6h | | | | R/W-6h | | |

**Table 6-46. COMPA_REF Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | COMPA_Mode | R/W | 1h | Comparator mode:<br>0h = PGOOD mode<br>1h = Comparator mode |
| 6-3 | COMPA_DVS[3:0] | R/W | 6h | Comparator window voltage shifting:<br>% deviation from VSEL if VSEL ≠ 1 V or second voltage option if VSEL = 1 V<br>0h = + 3% or 1.05 V<br>1h = + 2% or 1 V<br>2h = + 1% or 0.975 V<br>3h = + 0% or 0.95 V<br>4h = – 1% or 0.9 V<br>5h = – 2% or 0.875 V<br>6h = – 3% or 0.85 V<br>7h = – 4% or 0.8 V<br>8h = 0.75 V<br>9h = 0.7 V |
| 2-0 | COMPA_VSEL[2:0] | R/W | 6h | Comparator window voltage select:<br>0h = 1 V<br>1h = 1.2 V<br>2h = 1.5 V<br>3h = 1.8 V<br>4h = 1.1 V<br>5h = 1.35 V<br>6h = 3.3 V<br>7h = 2.5 V |

### 6.6.45 COMPB_REF Register (address = 0xDE) [reset = 0x1B]

COMPB_REF is shown in Figure 6-66 and described in Table 6-47.

Return to Summary Table.

Register domain: RESET

**Figure 6-66. COMPB_REF Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COMPB_Mode | COMPB_DVS[3:0] | | | | COMPB_VSEL[2:0] | | |
| R/W-0h | R/W-3h | | | | R/W-3h | | |

**Table 6-47. COMPB_REF Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | COMPB_Mode | R/W | 0h | Comparator mode:<br>0h = PGOOD mode<br>1h = Comparator mode |
| 6-3 | COMPB_DVS[3:0] | R/W | 3h | Comparator window voltage shifting: % deviation from VSEL if VSEL ? 1 V or second voltage option if VSEL = 1 V<br>0h = + 3% or 1.05 V<br>1h = + 2% or 1 V<br>2h = + 1% or 0.975 V<br>3h = + 0% or 0.95 V<br>4h = – 1% or 0.9 V<br>5h = – 2% or 0.875 V<br>6h = – 3% or 0.85 V<br>7h = – 4% or 0.8 V<br>8h = 0.75 V<br>9h = 0.7 V |
| 2-0 | COMPB_VSEL[2:0] | R/W | 3h | Comparator window voltage select:<br>0h = 1 V<br>1h = 1.2 V<br>2h = 1.5 V<br>3h = 1.8 V<br>4h = 1.1 V<br>5h = 1.35 V<br>6h = 3.3 V<br>7h = 2.5 V |

### 6.6.46 PWFAULT_MASK1 Register (address = 0xE5) [reset = 0x01]

PWFAULT_MASK1 is shown in Figure 6-67 and described in Table 6-48.

Return to Summary Table.

Register domain: RESET

**Figure 6-67. PWFAULT_MASK1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VCCIO_FLTmsK | V5A_FLTmsK | V33APCHFLTmsk | V33ADSWFLTmsk | V18A_FLTmsK | V18U25U_FLTmsK | VDDQ_FLTmsK | V13_FLTmsK |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h |

**Table 6-48. PWFAULT_MASK1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VCCIO_FLTmsK | R/W | 0h | VCCIO power fault masked<br>0h = Not masked<br>1h = Masked |
| 6 | V5A_FLTmsK | R/W | 0h | V5A power fault masked<br>0h = Not masked<br>1h = Masked |
| 5 | V33APCHFLTmsk | R/W | 0h | V33APCH power fault masked<br>0h = Not masked<br>1h = Masked |
| 4 | V33ADSWFLTmsk | R/W | 0h | V33ADSW power fault masked<br>0h = Not masked<br>1h = Masked |
| 3 | V18A_FLTmsK | R/W | 0h | V18A power fault masked<br>0h = Not masked<br>1h = Masked |
| 2 | V18U25U_FLTmsK | R/W | 0h | V18U25U power fault masked<br>0h = Not masked<br>1h = Masked |
| 1 | VDDQ_FLTmsK | R/W | 0h | VDDQ power fault masked<br>0h = Not masked<br>1h = Masked |
| 0 | V13_FLTmsK | R/W | 1h | V13 power fault masked<br>0h = Not masked<br>1h = Masked |

### 6.6.47 PWFAULT_MASK2 Register (address = 0xE6) [reset = 0x00]

PWFAULT_MASK2 is shown in Figure 6-68 and described in Table 6-49.

Return to Summary Table.

Register domain: RESET

**Figure 6-68. PWFAULT_MASK2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_PWFAULT_MASK2[5:0] | | | | | | V105A_FLTmsK | VPRIMCORE_FLTmsK |
| R-0h | | | | | | R/W-0h | R/W-0h |

**Table 6-49. PWFAULT_MASK2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED_PWFAULT_MASK2[5:0] | R-1 | 0h | Read always returns 1 |
| 1 | V105A_FLTmsK | R/W | 0h | V105A power fault masked<br>0h = Not masked<br>1h = Masked |
| 0 | VPRIMCORE_FLTmsK | R/W | 0h | VPRIMCORE power fault masked<br>0h = Not masked<br>1h = Masked |

### 6.6.48 PGOOD_STAT1 Register (address = 0xE7) [reset = 0x00]

PGOOD_STAT1 is shown in Table 6-50 and described in Table 6-51.

Return to Summary Table.

Register domain: RESET

**Table 6-50. PGOOD_STAT1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| V13_PGOOD | VDDQ_PGOOD | V18U25U_PGOOD | V18A_PGOOD | V33ADSW_PGOOD | V33APCH_PGOOD | VPRIMCORE_PGOOD | VCCIO_PGOOD |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

**Table 6-51. PGOOD_STAT1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | V13_PGOOD | R | 0h | V13 power-good status<br>0h = Fail<br>1h = Pass |
| 6 | VDDQ_PGOOD | R | 0h | VDDQ power-good status<br>0h = Fail<br>1h = Pass |
| 5 | V18U25U_PGOOD | R | 0h | V18U25U power-good status<br>0h = Fail<br>1h = Pass |
| 4 | V18A_PGOOD | R | 0h | V18A power-good status<br>0h = Fail<br>1h = Pass |
| 3 | V33ADSW_PGOOD | R | 0h | V33ADSW power-good status<br>0h = Fail<br>1h = Pass |
| 2 | V33APCH_PGOOD | R | 0h | V33APCH power-good status<br>0h = Fail<br>1h = Pass |
| 1 | VPRIMCORE_PGOOD | R | 0h | VPRIMCORE power-good status<br>0h = Fail<br>1h = Pass |
| 0 | VCCIO_PGOOD | R | 0h | VCCIO power-good status<br>0h = Fail<br>1h = Pass |

### 6.6.49 PGOOD_STAT2 Register (address = 0xE8) [reset = 0x00]

PGOOD_STAT2 is shown in Figure 6-69 and described in Table 6-52.

Return to Summary Table.

Register domain: RESET

**Figure 6-69. PGOOD_STAT2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_PGOOD_STAT2[2:0] | | | V5A_PG | V105A_PGOOD | V105A_SPGD | V18A_SPGD | V33ADSW_SPGD |
| R-0h | | | R-0h | R-0h | R-0h | R-0h | R-0h |

**Table 6-52. PGOOD_STAT2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | RESERVED_PGOOD_STAT2[2:0] | R-1 | 0h | Read always returns 1 |
| 4 | V5A_PG | R | 0h | V5A power-good status<br>0h = Fail<br>1h = Pass |
| 3 | V105A_PGOOD | R | 0h | V105A power-good status<br>0h = Fail<br>1h = Pass |
| 2 | V105A_SPGD | R | 0h | V105AS power-good status<br>0h = Fail<br>1h = Pass |
| 1 | V18A_SPGD | R | 0h | V18AS power-good status<br>0h = Fail<br>1h = Pass |
| 0 | V33ADSW_SPGD | R | 0h | V33ADSWS power-good status<br>0h = Fail<br>1h = Pass |

### 6.6.50 MISC_BITS Register (address = 0xE9) [reset = 0x02]

MISC_BITS is shown in Figure 6-70 and described in Table 6-53.

Return to Summary Table.

Register domain: RESET

**Figure 6-70. MISC_BITS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| V13_PIN_OVR | MV13EN | V33APCH_PIN_OVR | MV33APCHEN | msLP_S3ZPG | msLP_SUSZPG | BC_ACOK_EN | V13DISCHG |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-0h |

**Table 6-53. MISC_BITS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | V13_PIN_OVR | R/W | 0h | V13 ENABLE pin override<br>0h = V13 is OFF if MV13EN is 1<br>1h = V13 is ON if MV13EN is 1 |
| 6 | MV13EN | R/W | 0h | V13 enable pin mask<br>0h = DDR_VT_CTRL pin controls V13<br>1h = V13_EN_PIN bit controls V13 |
| 5 | V33APCH_PIN_OVR | R/W | 0h | V33APCH ENABLE pin override<br>0h = V33ADSW pin controls V33ADSW<br>1h = V33ADSW is ON if VREN PIN MASK = 0 |
| 4 | MV33APCHEN | R/W | 0h | V33APCH enable pin mask<br>0h = VR enable pin controls VR enable<br>1h = VR enable pin masked VxCTLV controls VR enable |
| 3 | msLP_S3ZPG | R/W | 0h | SLP_S3Z is part of the power good tree<br>0h = SLP_S3Z is part of power good tree<br>1h = SLP_S3Z is masked and set to 1 (not part of the power good tree) |
| 2 | msLP_SUSZPG | R/W | 0h | SLP_SUSZ is part of the power good tree<br>0h = SLP_SUSZ is part of power good tree<br>1h = SLP_SUSZ is masked and set to 1 (not part of the power good tree) |
| 1 | BC_ACOK_EN | R/W | 1h | Enables BC_ACOK output out of LVA pin. The input is ACOK pin, instead of ENLVA pin.<br>0h = LVA pin is not BC_ACOK, and ENLVA is the input for LVA output, behaving as a general purpose level shifter.<br>1h = LVA pin is BC_ACOK, and ACOK is the input, and ENLVA is not functional. BC_ACOK is a level shifted version of ACOK. |
| 0 | V13DISCHG | R/W | 0h | V0.6DX discharge resistance (V13)<br>0h = no discharge<br>1h = 100 Ω |

### 6.6.51 STDBY_CTRL Register (address = 0xEA) [reset = 0xFE]

STDBY_CTRL is shown in Figure 6-71 and described in Table 6-54.

Return to Summary Table.

Register domain: RTC

**Figure 6-71. STDBY_CTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_STDBY_CTRL[4:0] | | | | | EN_VCOMP_10U | QLSLPS0_ACTIVE | QLSLPS0_ACTIVE |
| R-Fh | | | | | R/W-1h | R/W-1h | R/W-0h |

**Table 6-54. STDBY_CTRL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | RESERVED_STDBY_CTRL[4:0] | R | 1Fh | Read always returns 1 |
| 2 | EN_VCOMP_10U | R/W | 1h | VCOMP current source control bit:<br>0h = Disable<br>1h = Enable |
| 1 | VCOMPEN | R/W | 1h | VCOMP enable control bit:<br>0h = Disable<br>1h = Enable |
| 0 | QLSLPS0_ACTIVE | R/W | 0h | SLP_S0 and DDR_VTT_CTRL detect logic control<br>0h = Normal Operation DELAY_ALL_SYS_PG is used in QSTANDBY (SLP_S0)<br>1h = DELAY_ALL_SYS_PG is ignored for QSTANDBY (SLP_S0) |

### 6.6.52 TEMPCRIT Register (address = 0xEB) [reset = 0x00]

TEMPCRIT is shown in Figure 6-72 and described in Table 6-55.

Return to Summary Table.

Register domain: RTC

**Figure 6-72. TEMPCRIT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_TEMPCRIT[1:0] | | LDO1_CRIT | VR5_CRIT | VR4_CRIT | VR3_CRIT | VR2_CRIT | VR1_CRIT |
| R-0h | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

**Table 6-55. TEMPCRIT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED_TEMPCRIT[1:0] | R | 0h | Read always returns 0 |
| 5 | LDO1_CRIT | R/W1C | 0h | LDO1 critical temperature<br>0h = Not asserted<br>1h = Asserted, regulator at critical temperature, write 1 to clear |
| 4 | VR5_CRIT | R/W1C | 0h | VR5 critical temperature<br>0h = Not asserted<br>1h = Asserted, regulator at critical temperature, write 1 to clear |
| 3 | VR4_CRIT | R/W1C | 0h | VR4 critical temperature<br>0h = Not asserted<br>1h = Asserted, regulator at critical temperature, write 1 to clear |
| 2 | VR3_CRIT | R/W1C | 0h | VR3 critical temperature<br>0h = Not asserted<br>1h = Asserted, regulator at critical temperature, write 1 to clear |
| 1 | VR2_CRIT | R/W1C | 0h | VR2 critical temperature<br>0h = Not asserted<br>1h = Asserted, regulator at critical temperature, write 1 to clear |
| 0 | VR1_CRIT | RR/W1C | 0h | VR1 critical temperature<br>0h = Not asserted<br>1h = Asserted, regulator at critical temperature, write 1 to clear |

### 6.6.53 TEMPHOT Register (address = 0xEC) [reset = 0x00]

TEMPHOT is shown in Figure 6-73 and described in Table 6-56.

Return to Summary Table.

Register domain: RTC

**Figure 6-73. TEMPHOT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED_TEMPHOT[1:0] | | LDO1_HOT | VR5_HOT | VR4_HOT | VR3_HOT | VR2_HOT | VR1_HOT |
| R-0h | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

**Table 6-56. TEMPHOT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED_TEMPHOT[1:0] | R | 0h | Read always returns 0 |
| 5 | LDO1_HOT | R/W1C | 0h | LDO1 hot temperature<br>0h = Not asserted<br>1h = Asserted, write 1 to clear |
| 4 | VR5_HOT | R/W1C | 0h | VR5 hot temperature<br>0h = Not asserted<br>1h = Asserted, write 1 to clear |
| 3 | VR4_HOT | R/W1C | 0h | VR4 hot temperature<br>0h = Not asserted<br>1h = Asserted, write 1 to clear |
| 2 | VR3_HOT | R/W1C | 0h | VR3 hot temperature<br>0h = Not asserted<br>1h = Asserted, write 1 to clear |
| 1 | VR2_HOT | R/W1C | 0h | VR2 hot temperature<br>0h = Not asserted<br>1h = Asserted, write 1 to clear |
| 0 | VR1_HOT | R/W1C | 0h | VR1 hot temperature<br>0h = Not asserted<br>1h = Asserted, write 1 to clear |

### 6.6.54 VREN_PIN_OVR Register (address = 0xEE) [reset = 0x0]

VREN_PIN_OVR is shown in Figure 6-74 and described in Table 6-57.

Return to Summary Table.

Register domain: RESET

**Figure 6-74. VREN_PIN_OVR Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VPRIMCORE_PIN_OVR | V105A_PIN_OVR | VDDQ_PIN_OVR | V18U25U_PIN_OVR | V18A_PIN_OVR | V33APCH_PIN_OVR | V5A_PIN_OVR | VCCIO_PIN_OVR |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 6-57. VREN_PIN_OVR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VPRIMCORE_PIN_OVR | R/W | 0h | VPRIMCORE ENABLE pin override<br>0h = VPRIMCORE pin controls VPRIMCORE<br>1h = VPRIMCORE is ON if VREN PIN MASK = 0 |
| 6 | V105A_PIN_OVR | R/W | 0h | V105A ENABLE pin override<br>0h = V105A pin controls V105A<br>1h = V105A is ON if VREN PIN MASK = 0 |
| 5 | VDDQ_PIN_OVR | R/W | 0h | VDDQ ENABLE pin override<br>0h = VDDQ pin controls VDDQ<br>1h = VDDQ is ON if VREN PIN MASK = 0 |
| 4 | V18U25U_PIN_OVR | R/W | 0h | V18U25U ENABLE pin override<br>0h = V18U25U pin controls V18U25U<br>1h = V18U25U is ON if VREN PIN MASK = 0 |
| 3 | V18A_PIN_OVR | R/W | 0h | V18A ENABLE pin override<br>0h = V18A Pin controls V18A<br>1h = V18A is ON if VREN PIN MASK = 0 |
| 2 | V33APCH_PIN_OVR | R/W | 0h | V33APCH ENABLE pin override<br>0h = V33APCH pin controls V33APCH<br>1h = V33APCH is ON if VREN PIN MASK = 0 |
| 1 | V5A_PIN_OVR | R/W | 0h | V5A ENABLE pin override<br>0h = V5A pin controls V5A<br>1h = V5A is ON if VREN PIN MASK = 0 |
| 0 | VCCIO_PIN_OVR | R/W | 0h | VCCIO ENABLE pin override<br>0h = VCCIO pin controls VCCIO<br>1h = VCCIO is ON if VREN PIN MASK = 0 |

# 7 Applications, Implementation, and Layout

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Application Information

The TPS650932 can be used in several different applications from computing to industrial interfacing and more. This section describes the general application information and provides a detailed description of powering the Intel Cannon Lake system with the TPS650932 device.

## 7.2 Typical Application

The TPS650932 can be used in any system that requires multiple voltage rails. A DC supply voltage from 5.4 V to 21 V is required. If the supply voltage is less than this range, then a small boost can be added to the system to supply the VIN and VINLDO3.

Along with the five DC-DCs and one LDO, the TPS650932 device has eight general-purpose comparators, two level shifters, one board temperature-monitoring system, and three power-path comparators. The temperature-monitoring system and power-path comparators can be used as simple comparators if desired, increasing the total number of comparators available for use on the TPS650932 to 12.

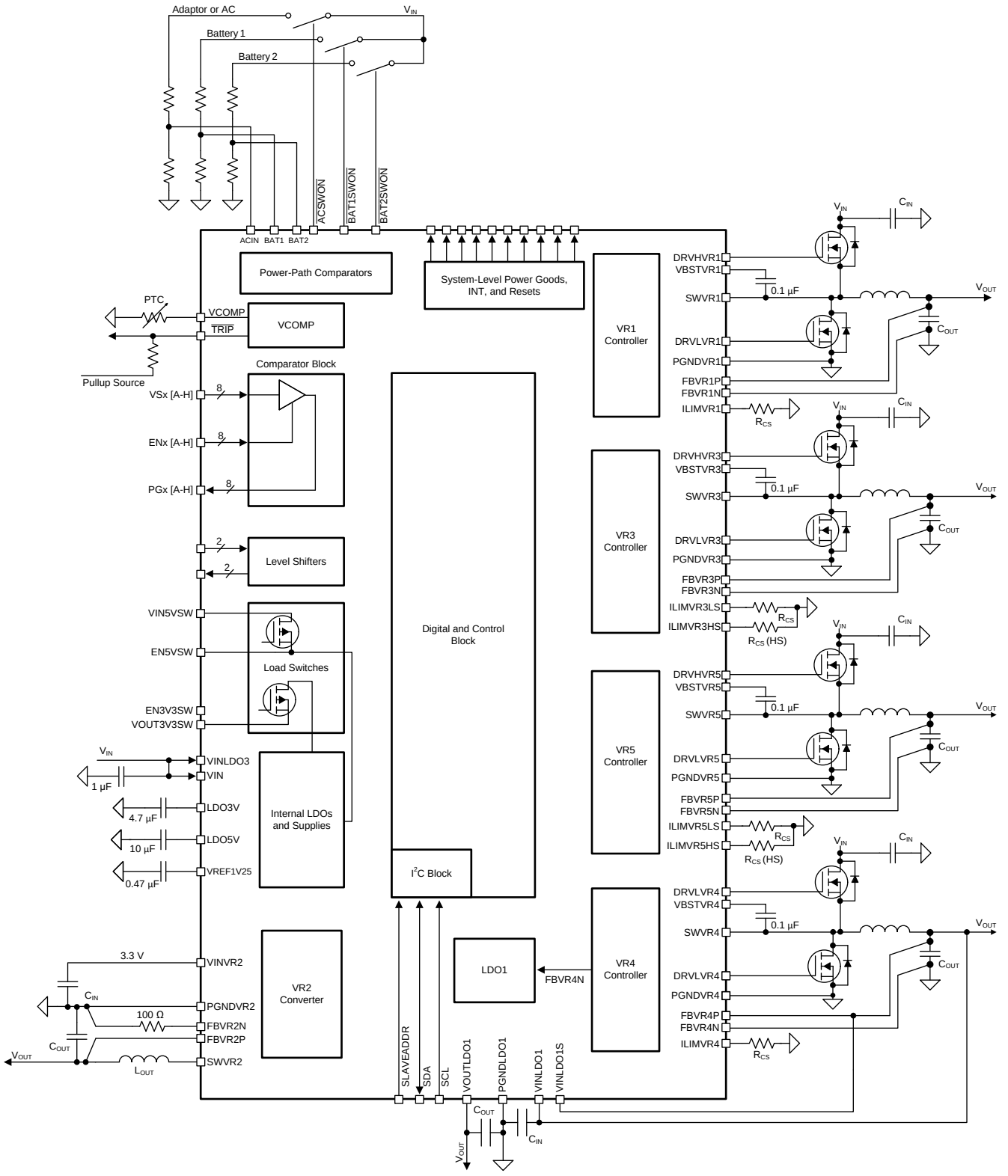





**Figure 7-1. Simplified General Block Diagram**

### 7.2.1 Design Requirements

The TPS650932 device requires decoupling capacitors on the supply pins. Follow the specifications in the *Section 5.14* table for the recommended capacitance on these supplies.

The controllers, converter, LDO, and some other features can be adjusted to meet the application requirements. The *Section 7.2.2* section describes how to design and adjust the external components to achieve the desired performance.

### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Controller Design Procedure

Designing the controller is performed in several steps: designing the output filter, selecting the FETs, bootstrap capacitor, and input capacitors, and setting the current limits.

The VR1 and VR4 controllers require the VREG supply and capacitors. The VREG pin should be connected to the 5-V LDO. A 1-µF, X5R, 20%, 10-V or similar capacitor should be used for decoupling.

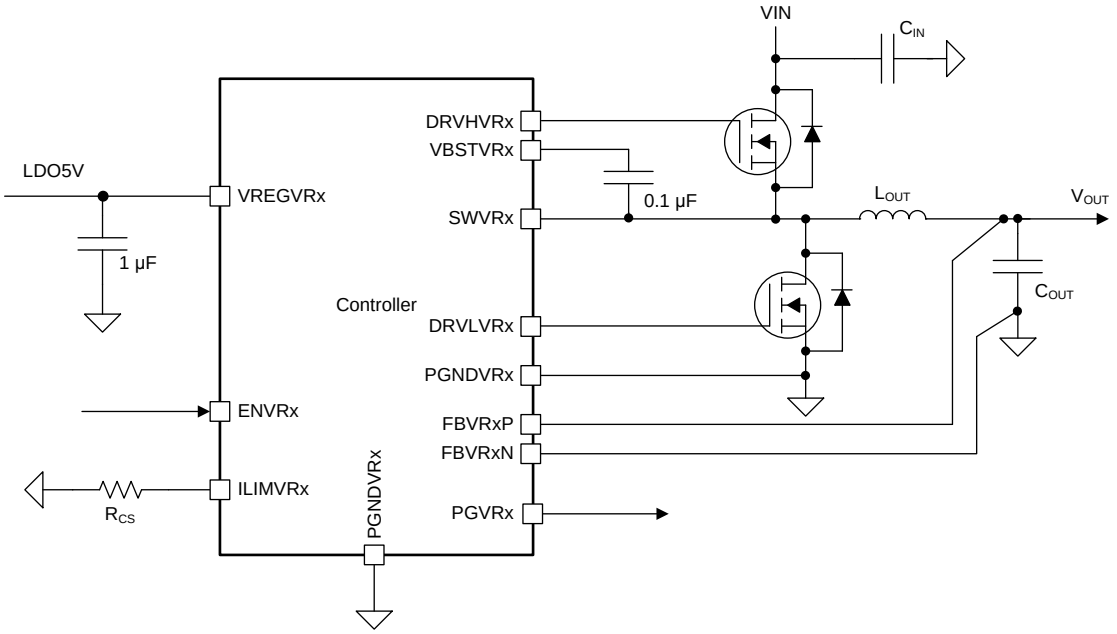





**Figure 7-2. Controller Diagram**

#### 7.2.2.1.1 Selecting the Inductor

An inductor must be placed between the external FETs and the output capacitors. The inductor and output capacitors together make the double-pole which contributes to stability. Additionally, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance increases, the ripple current decreases which, typically, increases efficiency. However, as the inductance increases, the transient performance decreases. The selected inductor must be rated for an appropriate saturation current, core losses, and DC resistance (DCR).

Use Equation 1 to calculate the recommended inductance for the controller.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{OUTmax} \times K_{IND}} \quad (1)$$

where

- $K_{IND}$ is the ratio of $I_{Lripple}$ to $I_{OUTmax}$.

TI recommends setting $K_{IND}$ from 0.2 to 0.4.

Use Equation 2 to calculate the peak current for the inductor in steady state operation, $I_{Lmax}$, with the selected inductance value. The rated saturation current of the inductor must be higher than the $I_{Lmax}$ current.

$$I_{Lmax} = I_{OUTmax} + \left( \frac{[V_{IN} - V_{OUT}] \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \right) \quad (2)$$

#### 7.2.2.1.2 Selecting the FETs

This controller is designed to drive NMOS FETs. Typically, the lowest $R_{DSon}$ value for the high-side and low-side FETs is best, however; the FETs, inductor, and output capacitors must be sized appropriately because as the $R_{DSon}$ for the low-side FET decreases, the minimum current limit increases. TI recommends using the CSD87381P or CSD87330Q3D for the controllers.

#### 7.2.2.1.3 Bootstrap Capacitor

To ensure that the internal high-side gate drivers are supplied with a stable low-noise supply voltage, a capacitor must be connected between the VBSTVRx pins and the respective SWVRx pins. TI recommends using ceramic capacitors with a value of 0.1 µF as the converters and the controllers. A 0.1-µF, size 0402, 10-V capacitor was used for the controllers for testing.

TI recommends reserving a small resistor in series with the bootstrap capacitor in case the turnon or turnoff of the FETs must be slowed to reduce voltage ringing on the switch node. This practice is common for controller design.

#### 7.2.2.1.4 Setting the Current Limits

The controller has a *valley current-limit topology*, also known as a *low-side current limit*. This type of current limit works by limiting the current only when the low-side FET is on. If the current sourced by the low-side FET is greater than the set low-side current limit, $I_{LS}$, then the controller holds the low-side FET on and the high-side FET off until the current through the low-side FET decreases below the set $I_{LS}$ value. The low-side FET ia allowed to turn off and the high-side FET to turn on only when the current through the low-side FET is less than the $I_{LS}$ values .

A fast current increase is limited by the maximum on time for the high-side FET. This limiting forces the low-side FET to turn on every period. When the low-side FET turns on, the low-side current limit can control the FETs until the current decreases below the $I_{LS}$ value. The maximum on time for the high-side FET limits the current increase to the maximum on time multiplied by the di/dt of the inductor until the low-side FET is switched on.

The $I_{OCL}$ current is the average of the peak and valley currents as shown in Figure 7-3.

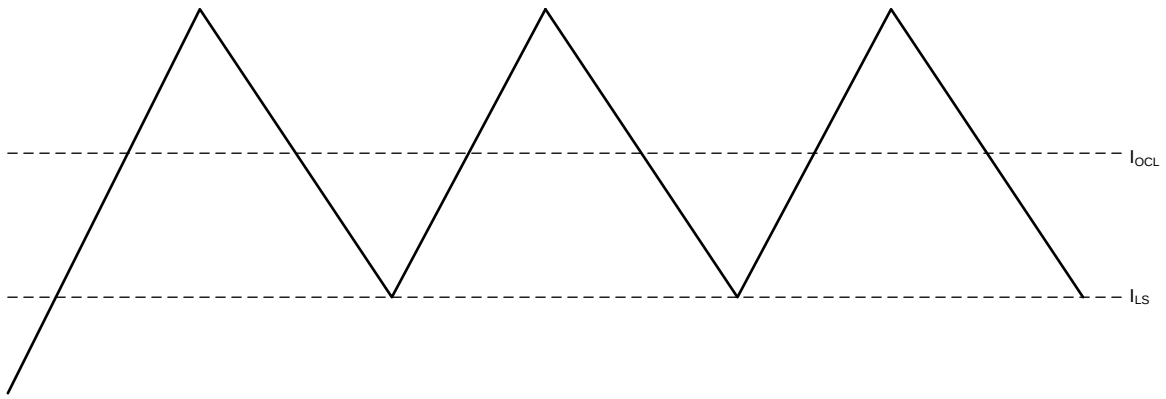



**Figure 7-3. $I_{OCL}$ Current**

The low-side current limit for the controllers is set by a resistor, $R_{CS}$, at the ILIMVRx pin. A current, $I_{TRIP}$, is sourced across the $R_{CS}$ resistor to set the voltage for the current-limit comparator. Use Equation 3 to determine the value of the $R_{CS}$ resistor.

$$R_{CS(LS)} = \frac{8 \times R_{DSon} \times 1.3 \times \left( I_{OCL} - \frac{[V_{IN} - V_{OUT}] \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \right)}{I_{TRIP}} \quad (3)$$

TI recommends setting $I_{OCL}$ to 130% of $I_{OUTmax}$ and using a resistor with ±1% or less tolerance for best results. Because the current limit occurs when the inductor current is near its maximum, TI recommends using the saturation derating of the inductor when calculating the value of $R_{CS}$.

A minimum and maximum value of $I_{OCL}$ can be achieved for the given parameters used in Equation 3. To ensure that the $R_{CS}$ resistor has been sized correctly, Equation 4 must be true across the application temperature range.

$$V_{CSmin} < I_{TRIP} \times R_{CS} < V_{CSmax} \quad (4)$$

If the controller has a high-side current limit then, use Equation 5 to calculate the high-side $R_{CS}$ resistor ($R_{CS(HS)}$). The high-side current limit must be set higher than the low-side current limit. Again, because the current limit occurs when the inductor current is near its maximum, TI recommends using the saturation derating of the inductor when calculating the value of $R_{CS}$.

$$R_{CS(HS)} = \frac{\left( R_{DSon} \times \left[ I_{OCL} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \right] \over 3200\ \Omega - 8\ \mu A \right) \times 20\ k\Omega}{I_{TRIP}} \quad (5)$$

#### 7.2.2.1.5 Selecting the Input Capacitors

Because of the nature of the switching converter and controller with a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and to minimize the interference with other circuits caused by high input-voltage spikes. For the controller, TI recommends 12 µF of input capacitance for most applications. To achieve the low-ESR requirement, use a ceramic capacitor. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. The value of the input capacitor can be increased without any limit for better input voltage filtering. Size the ceramic capacitor to achieve the recommended input capacitance. TI recommends placing a ceramic capacitor as close as possible to the respective VINx and PGNDx pins of the FETs.

The preferred capacitors for the controllers are two muRata GRM21BR61E106MA73: 10 µF, 0805, 25 V, ±20% or similar.

### 7.2.2.2 Converter Design Procedure

Designing the converter is performed in two steps: designing the output filter and selecting the input capacitors. The converter must be supplied by a 3.3-V source which can be provided by the TPS650932 controllers.

The converter requires the VREG supply and capacitors. The VREG supply should be connected to the 5-V LDO and a 1-µF, X5R, 20%, 10-V or similar capacitor should be used for decoupling.

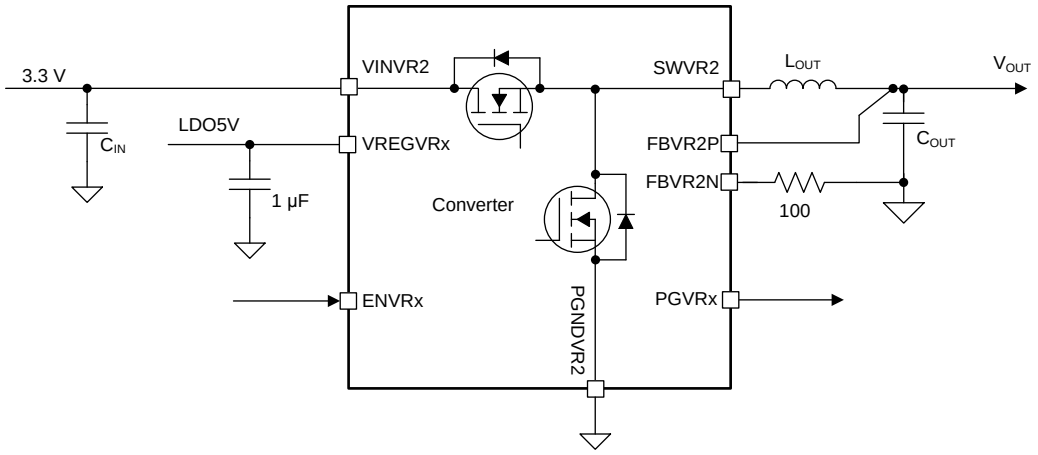





**Figure 7-4. Converter Diagram**

#### *7.2.2.2.1 Selecting the Inductor*

An inductor is required to be placed between the SWVRx and the output capacitors. The inductor and output capacitors together make the double-pole which contributes towards stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. With an increase in inductance used the ripple current decreases which, typically increases efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected has to be rated for appropriate saturation current, core losses and DC resistance (DCR).

Use Equation 6 to calculate the recommended inductance for the controller.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{OUTmax} \times K_{IND}} \quad (6)$$

where

- $K_{IND}$ is the ratio of $I_{Lripple}$ to $I_{OUTmax}$.

TI recommends setting $K_{IND}$ from 0.2 to 0.4.

Use Equation 7 to calculate the peak current for the inductor in steady state operation, $I_{Lmax}$, with the selected inductance value. The rated saturation current of the inductor must be higher than the $I_{Lmax}$ current.

$$I_{Lmax} = I_{OUTmax} + \left( \frac{[V_{IN} - V_{OUT}] \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \right) \quad (7)$$

Table 7-1 lists a selection of recommended inductors for the converter.

**Table 7-1. Recommended Inductors**

| MANUFACTURER | PART NUMBER | VALUE | SIZE | HEIGHT |
|---|---|---|---|---|
| Cyntec | PIFE32251B-R68MS | 0.68 µH | 3.2 mm × 2.5 mm | 1.2 mm |
| Cyntec | PIFE32251B-R47MS | 0.47 µH | 3.2 mm × 2.5 mm | 1.2 mm |

#### 7.2.2.2.2 Selecting the Output Capacitors

TI recommendes ceramic capacitors with low-ESR values which provide the lowest output-voltage ripple. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light-load currents, the converter operates in power-save mode and the output-voltage ripple is dependent on the output-capacitor value and the PFM peak-inductor current. Higher output-capacitor values minimize the voltage ripple in PFM Mode. To achieve the specified regulation performance and low output-voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC-bias voltage.

TI recommends using small ceramic capacitors placed as close as possible to the inductor and the respective PGND pins of the device for the output capacitors of the DC-DC converters. If, for any reason, the application requires the use of large capacitors that can not be placed close to the device, use a smaller ceramic capacitor in parallel with the large capacitor. Place the small capacitor as close as possible to the inductor and the respective PGND pins of the device.

T recommended capacitor to use with the DC-DC converters is the muRata GRM188R60J226MEAO: 22 µF, 0603, 6.3 V, ±20% or similar. This capacitor was selected to achieve the highest derated capacitance in a small 0603 package. If the selected output voltage is greater than 3.3 V then TI recommends using the muRata GRM21BR61A226ME44: 22 µF, 0805, 10 V, ± 20%, or similar. This capacitor is recommended to maintain the actual capacitance as DC bias increases.

#### 7.2.2.2.3 Selecting the Input Capacitors

Because of the nature of the switching converter and controller with a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and to minimize the interference with other circuits caused by high input-voltage spikes. For the controller, TI recommends 12 µF of input capacitance for most applications. To achieve the low-ESR requirement, use a ceramic capacitor. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. The value of the input capacitor can be increased without any limit for better input voltage filtering. Size the ceramic capacitor to achieve the recommended input capacitance. TI recommends placing a ceramic capacitor as close as possible to the respective VINx and PGNDx pins of the device.

The preferred capacitors for the controllers are two muRata GRM21BR61E106MA73: 10 µF, 0805, 25 V, ±20% or similar.

### 7.2.2.3 LDO Design Procedure

The LDO must support the fast load transients from the DDR memory for termination. Therefore, maintaining a high amount of capacitance with low ESR on the LDO outputs and inputs is important, for which ceramic capacitors are ideal.

The preferred output capacitor for the LDO is muRata GRM188R60J476M: 47 µF, 0603, 6.3 V, ±20% or similar.

The preferred input capacitor for the LDO is muRata GRM155R60J106ME44: 10 µF, 0402, 6.3 V, ±20% or similar.

#### 7.2.2.4 Board Temperature Monitoring Design Procedure

Board temperature monitoring requires only one thermistor if only one sense point is desired. The temperature monitoring can be scaled by adding as many thermistors as sense points desired. Connect a PTC thermistor that has an exponential coefficient curve from the VCOMP pin to GND and a pullup resistor to desired voltage source on the TRIPZ pin. Place the thermistor where desired. If multiple sense points are desired, string the thermistors together in a series connection while placing the thermistors where desired as shown in Figure 7-5.

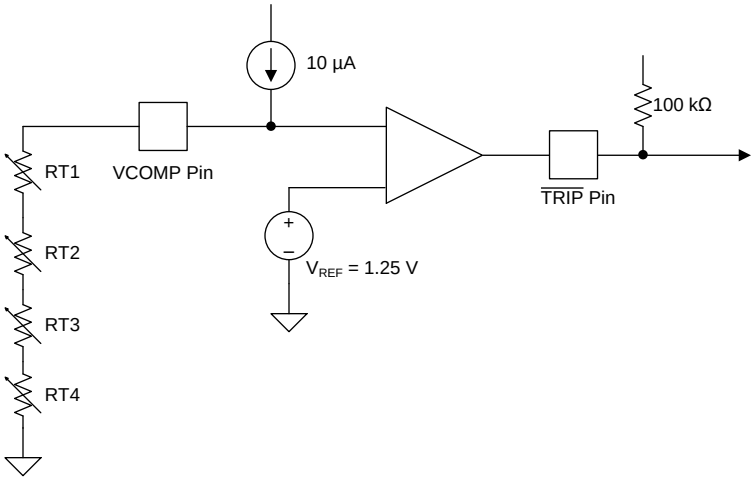



**Figure 7-5. Board Temperature Monitoring Circuit Example**

The thermistors should have low-room and mid-temperature resistance from 1 kΩ to 10 kΩ. The hot-point resistance should be approximately 10 times the mid-temperature resistance from 100 kΩ to 200 kΩ. An internal 10-µA current source provides a voltage across the thermistors. When this voltage exceeds the comparator threshold of 1.25 V, the TRIPZ pin switches to low which indicates a hot board temperature. Therefore, the resistance required for hot board temperature is 125 kΩ. Select thermistors that align this resistance with the desired setpoint of the hot temperature.

The recommended thermistors for this feature is the muRata PRF15BG102RB6RC.

### 7.2.2.5 Power-Path Design Procedure

The TPS650932 device has power-path comparators and outputs to control the power-path switches. To set the threshold to the desired value, connect a voltage divider to the adaptor and batteries. The outputs of the comparators require a pullup resistor because the comparator outputs are open-drain outputs. In order for the power-path comparators to work without supplying VIN, connect the VINPP pin to the monitored power rails by using a diode to select the highest voltage among the sources.

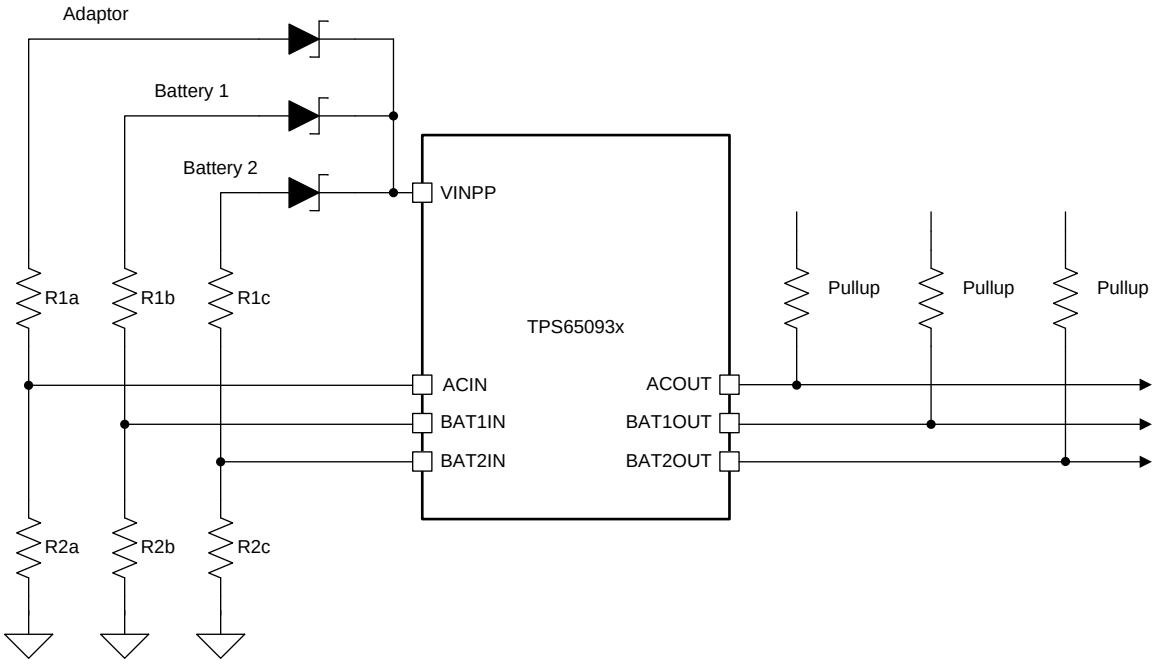





**Figure 7-6. Power-Path Comparators and VINPP Supply**

For example, measuring a battery and an adaptor is helpful to decide when to switch from the battery to the adaptor. The desired threshold voltages 9 V and 6 V respectively. Use Equation 8 to calculate the resistors required to set each threshold. The R1a and R2a resistors are required to set the 9-V. The R1b and R1a resistors are required to set the 6-V threshold.

$$R1 = R2 \times \left( \frac{V_{IN}}{V_{THRESHOLD}} - 1 \right) \tag{8}$$

### 7.2.3 Application Curves

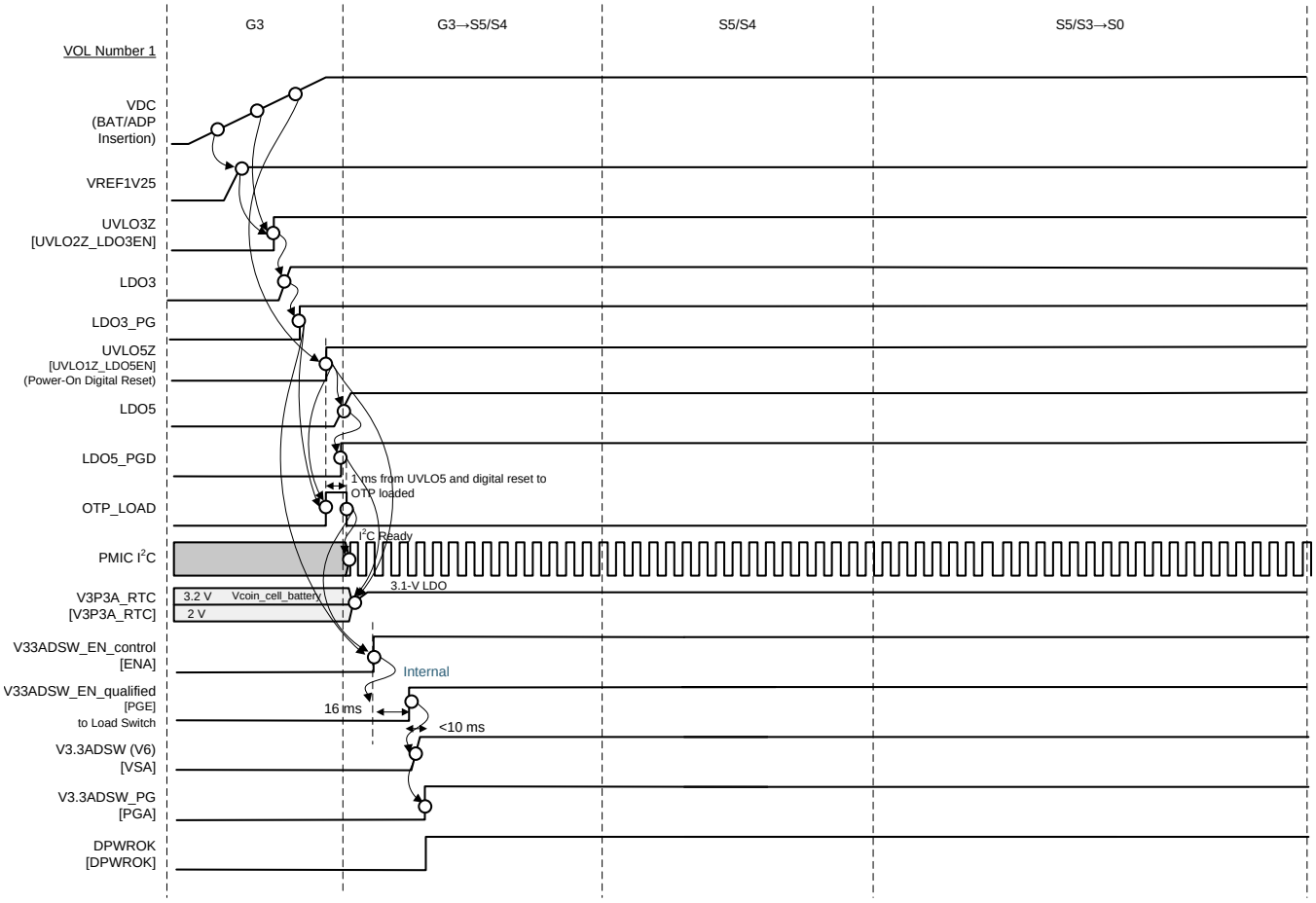



**Figure 7-7. Timing Diagram**

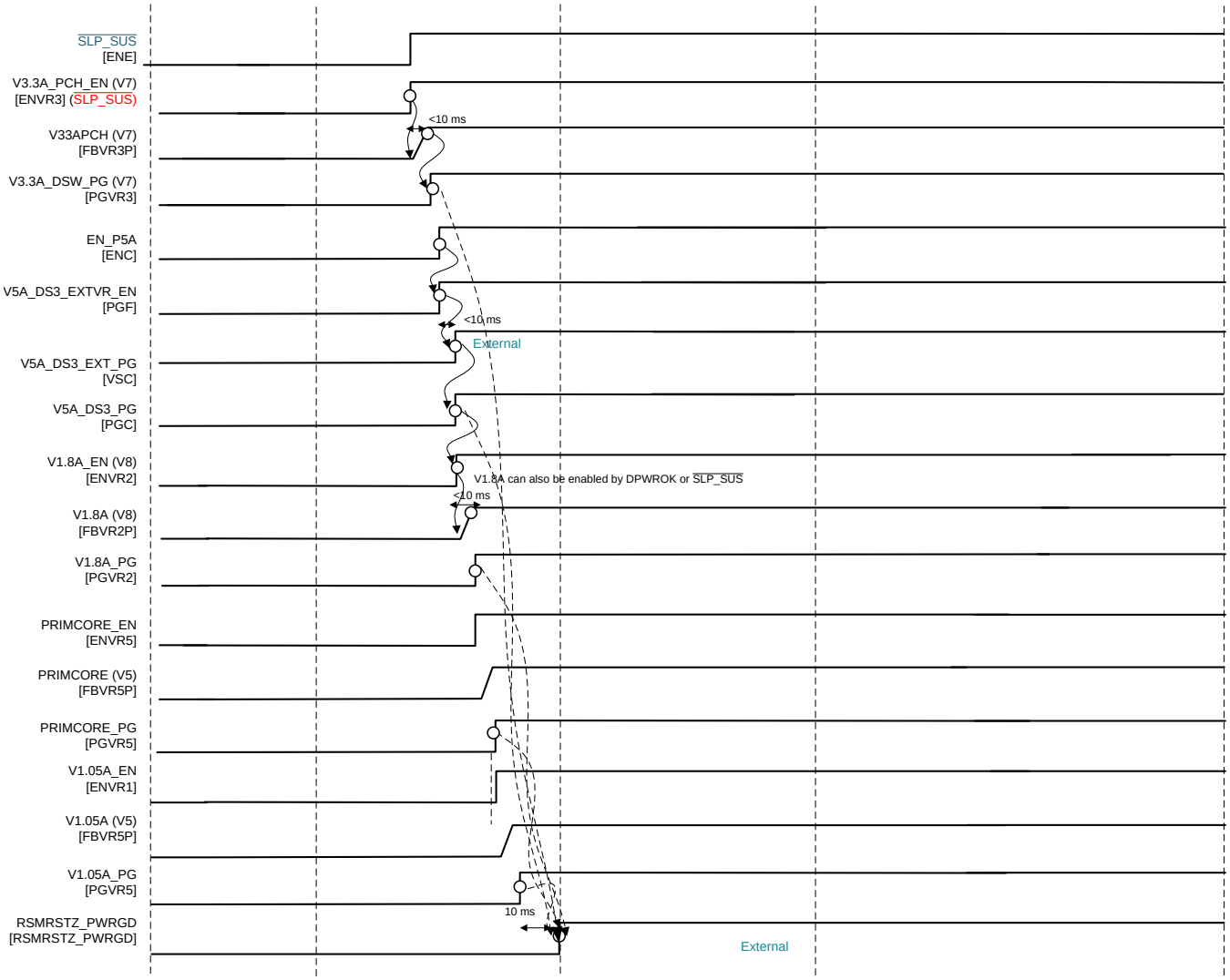



**Figure 7-8. Timing Diagram**

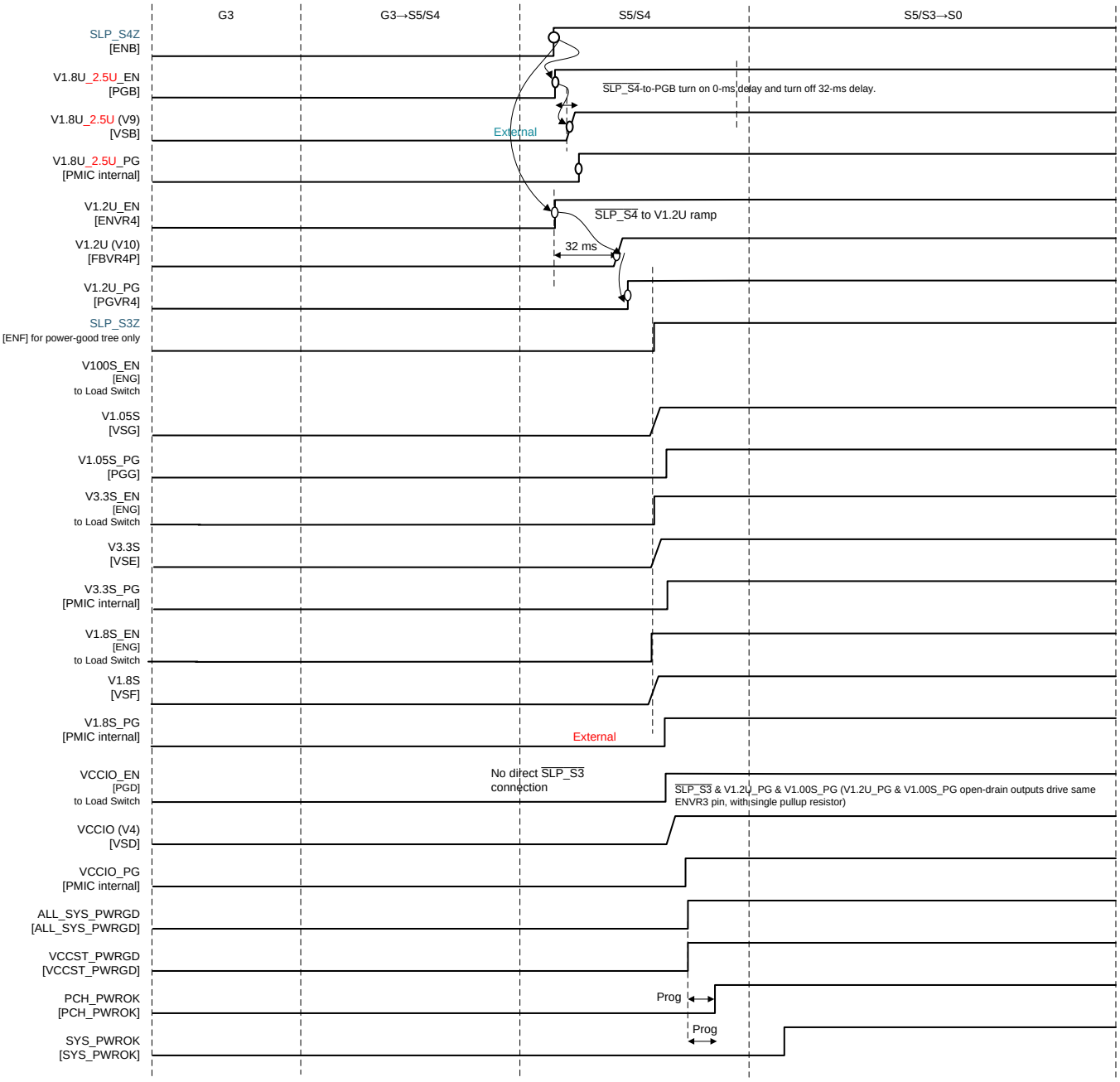
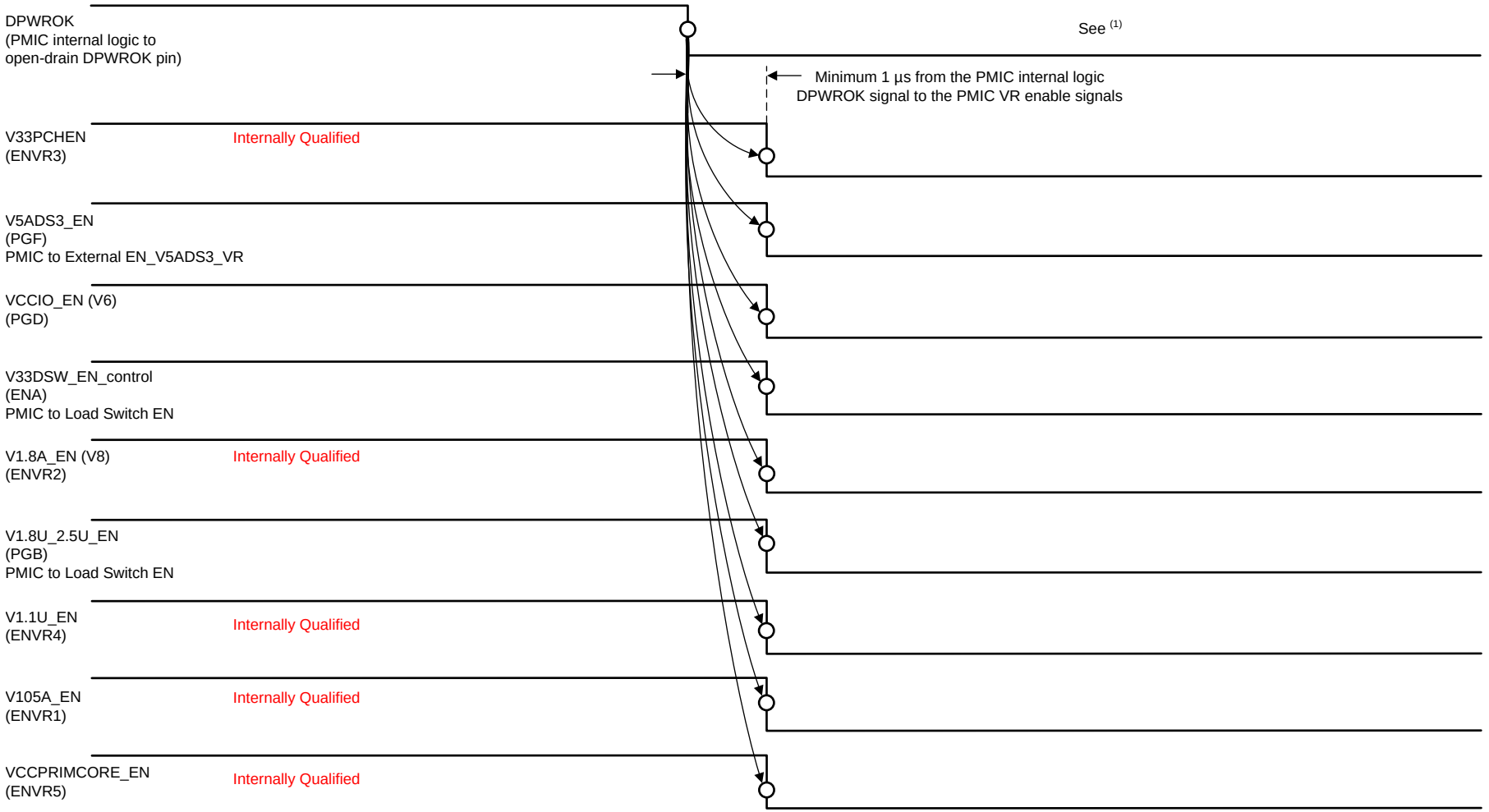



**Figure 7-9. Timing Diagram**




(1) DPWROK is the PMIC internal-logic signal controlling the PMIC open-drain DPWROK pin. If the DPWROK pin is connected to ground, then this will not be visible to the user; instead, the user would see the external net P_DPWROK from the external DPWROK pin always low.

**Figure 7-10. Emergency Reset Sequence Timing Diagram**

## 7.2.4 Layout

### 7.2.4.1 Layout Guidelines

For all switching power supplies, layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not performed carefully, the regulator could show stability problems as well as electromagnetic interference (EMI) problems. Therefore, use wide and short traces for the main current path and for the power-ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the device. Use a common ground node for the power ground and a different node for the control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the device.

The TPS650932 device is available in a 7-mm by 7-mm nFBGA package (ZAJ) with a 0.5-mm ball pitch.

#### 7.2.4.1.1 Fanout for ZAJ using Type 4 Routing

This small, 7-mm × 7-mm package uses the Type 4 routing technique to decrease system-board area as much as possible. This Type 4 routing has vias in pad, blind and buried vias, and a minimum trace width, or spacing, of 4 mm.

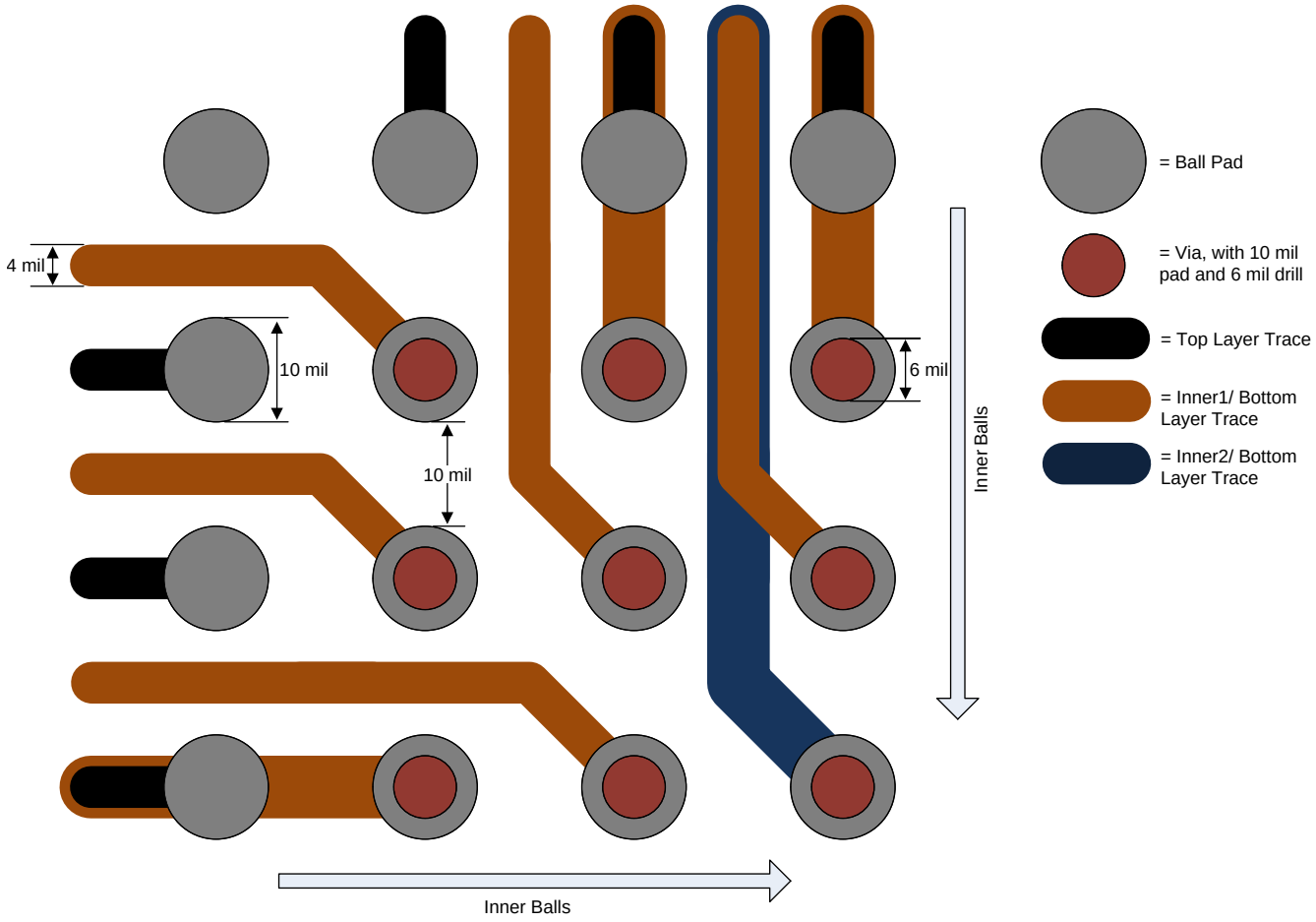



**Figure 7-11. Fanout for ZAJ Package Using Type 4 Routing**

#### 7.2.4.1.2 Layout Checklist

The general layout checklist is:

- Locate all inductors, input and output capacitors, and FETs for the converters and controller on the same board layer as the device.
- Place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible to achieve the best regulation performance.
- Place bootstrap capacitors from the SWVRx to VBSTVRx pins close to the device.
- Route the DRVLVRx signals on the same layer as the device and the FETs. Minimize the length and parasitic inductance of the trace as much as possible.
- Each converter and controller should have a separate ground, and each ground should connect separately to the common ground. The input capacitors, output capacitors, and FET grounds for each VRx converter and controller must be connected to the ground plane for the respective VRx rail. Because the PGNDs for each rail do not connect to each other or AGND, using the PGNDVRx pins for the input and output capacitors for each VRx rail is required. This ground plane should connect in one place to the common ground close to the input and output capacitor ground pads. Figure 7-12 shows a visual representation of the converter layout scheme.
- The input and output capacitors of the internal reference regulators must be close to the device pins.
- Route the FBVRxP and FBVRxN signals as a differential pair.

#### 7.2.4.1.3 Controller Layout

The routing of the controllers is critical to the performance of the power supply. To reduce the risk of the controller effecting other sensitive circuits on the board, TI recommends placing all of the controller components on the same layer as the PMIC. In addition to component placement, the DRV, SW, and PGND signals should be routed on the same layer or as few of layers possible. TI recommends placing the FETs as close as possible to the PMIC, however; placing the input capacitors within a minimal distance from the VIN and PGND pads of the FETs is imperative. The feedback signals should be routed differentially to the furthest output capacitor, which should be placed close to the load. Do not route the feedback or any sensitive analog signals under the inductor, next to the SW node, or between $C_{IN}$ and the FETs because of the high frequency switching from the edges.

If the FETs of the controller are placed far away from the PMIC, the layout of the DRV, SW, and PGND signals becomes extremely critical. The loop inductance of the traces must be minimized as much as possible. To minimize these traces, pair the DRVH and SW traces together and pair the DRVL and PGND traces together. The PGND trace is best routed as a plane. To reduce the loop inductance of the DRVL trace, the DRVL trace should be routed one layer above the PGND trace. Generally, the SW, DRVL and DRVH traces should be 20 mm or larger assuming the PGND is a plane underneath the DRVL trace.

#### 7.2.4.2 Layout Example

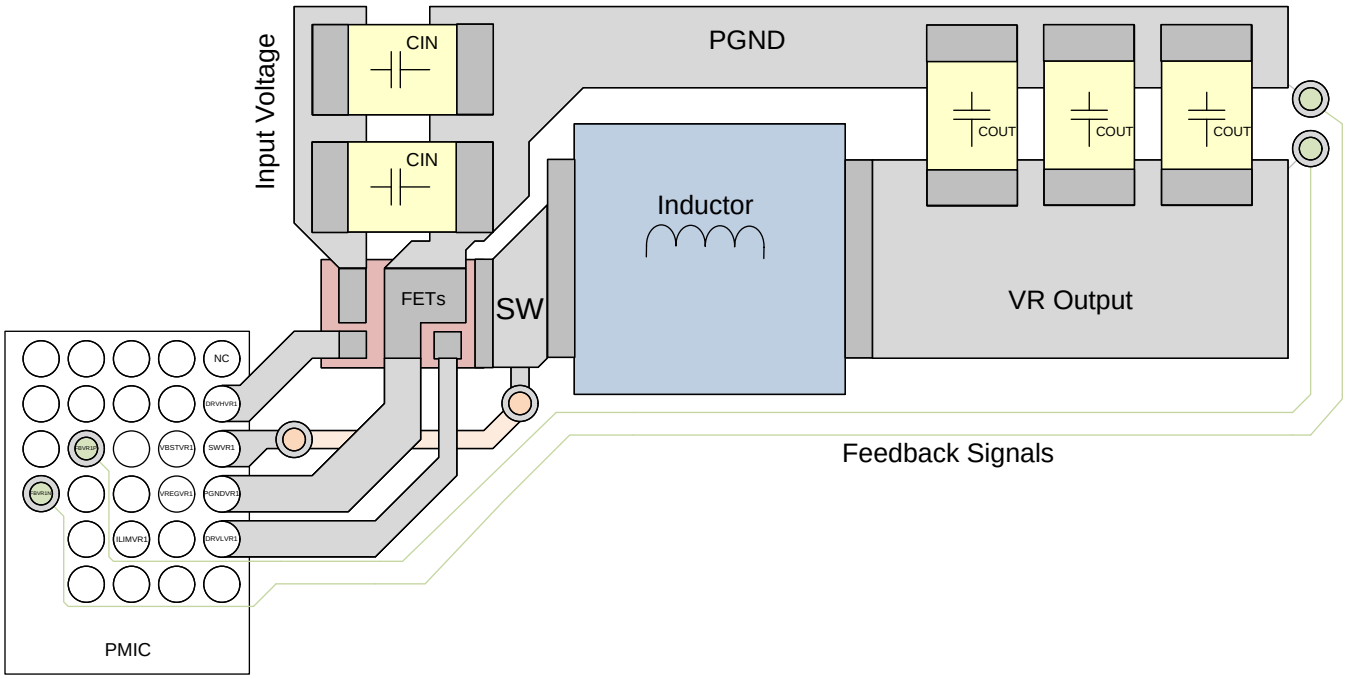



**Figure 7-12. Controller Layout Diagram**

#### 7.2.4.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Balancing thermal performance can be performed by improving the power dissipation capability of the PCB design and introducing airflow in the system.

For more information on how to use the thermal parameters in the dissipation ratings table, refer to *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and the *Semiconductor and IC Package Thermal Metrics*.

## 7.3 Power Supply Recommendations

Any power supply capable of delivering the required input power is acceptable provided that the source is within the recommended operating conditions for the VIN and VINLDO3 pins. The input voltage for the VR2 converter must always be 3.3 V. The input voltage of the controllers can vary from the VIN and VINLDO3 voltage. Ensure that the VINPP input is connected to the VIN pin or floated but is not grounded.

## 7.4 Do's and Don'ts

- Always float or connect the VINPP pin to the same voltage as the VIN pin. Never ground the VINPP pin.
- Connect the enable to ground and float the output if a voltage regulator is not used.

# 8 Device and Documentation Support

## 8.1 Device Support

### 8.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 8.1.2 Development Support

For frequently asked questions (FAQs) about the TPS650932 device, refer to the TPS65083x FAQs (http://e2e.ti.com/support/power_management/pmu/w/design_notes/2898.tps65083x-faqs)

## 8.2 Documentation Support

### 8.2.1 Related Documentation

For related documentation refer to:

- Texas Instruments, *CSD87330Q3D Synchronous Buck NexFET™ Power Block* data sheet
- Texas Instruments, *CSD87381P Synchronous Buck NexFET™ Power Block II* data sheet
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 8.5 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS650932ZAJR | PREVIEW | NFBGA | ZAJ | 168 | 2000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | TPS650932 | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

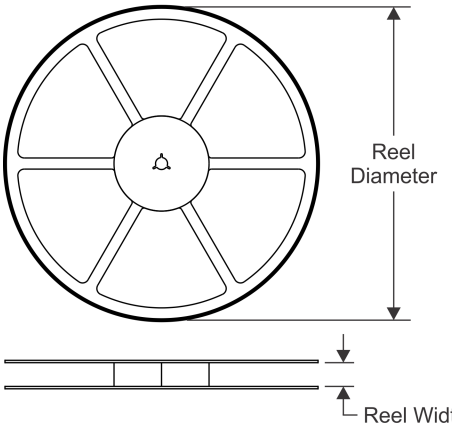
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

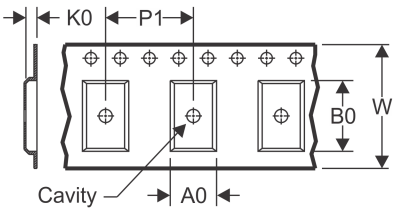
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

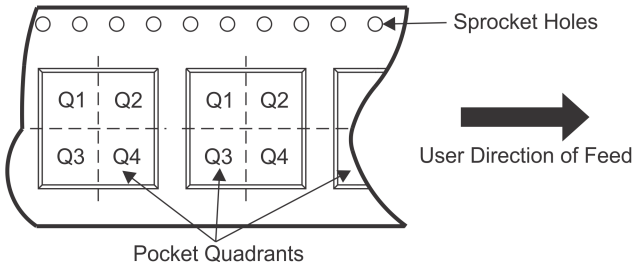



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

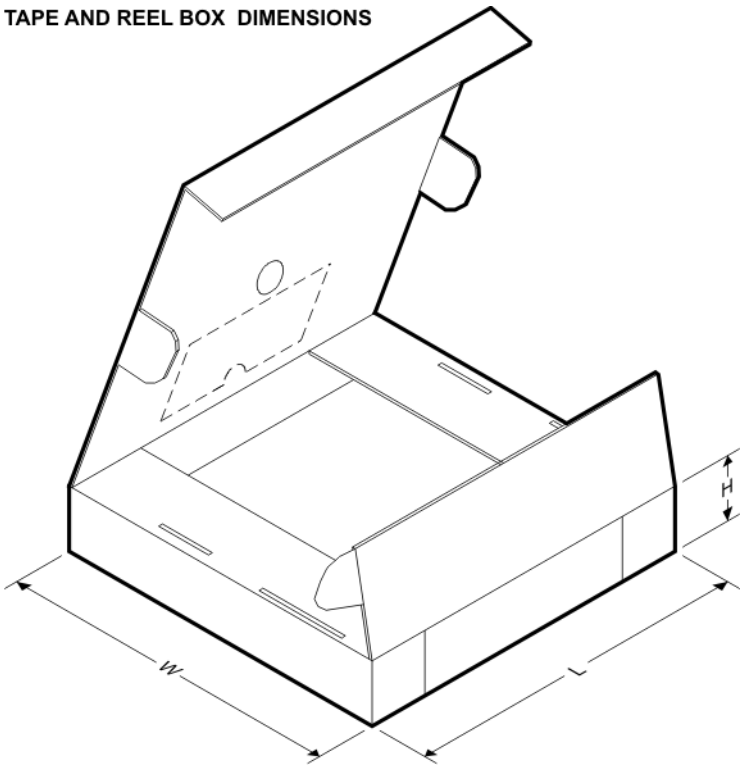
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS650932ZAJR | NFBGA | ZAJ | 168 | 2000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS650932ZAJR | NFBGA | ZAJ | 168 | 2000 | 336.6 | 336.6 | 31.8 |

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265