IXYS

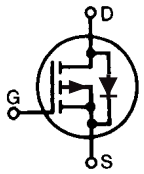
Preliminary Technical Information

TrenchP™ Power MOSFET

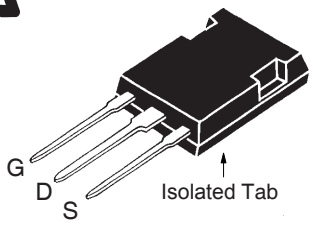
IXTR210P10T

V_{DSS} = -100V
I_{D25} = -195A
$R_{DS(on)}$ ≤ 8mΩ

P-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Rectifier



ISOPLUS247
E153432



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	-100	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	-100	V
V_{GSS}	Continuous	±15	V
V_{GSM}	Transient	±25	V
I_{D25}	T_C = 25°C (Chip Capability)	-195	A
I_{LRMS}	Lead Current Limit, RMS	-160	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	- 800	A
I_A	T_C = 25°C	-100	A
E_{AS}	T_C = 25°C	3	J
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	10	V/ns
P_D	T_C = 25°C	595	W
T_J		- 55 ... +150	°C
T_{JM}		150	°C
T_{stg}		- 55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
V_{ISOL}	50/60 Hz, 1 Minute	2500	V~
F_C	Mounting Force	20..120/4.5..27	N/lb.
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = - 250μA	-100			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 250μA	- 2.5		- 4.5	V
I_{GSS}	V_{GS} = ±15V, V_{DS} = 0V			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			- 25	μA
	T_J = 125°C			- 300	μA
$R_{DS(on)}$	V_{GS} = -10V, I_D = -105A, Note 1			8	mΩ

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- Avalanche Rated
- Extended FBSOA
- Fast Intrinsic Rectifier
- Low $R_{DS(ON)}$ and Q_G

Advantages

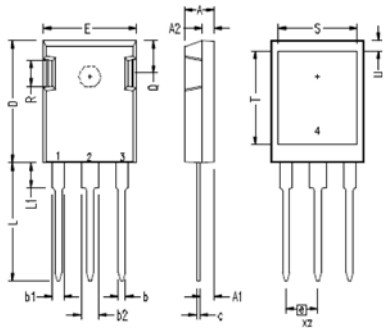
- Easy to Mount
- Space Savings
- High Power Density

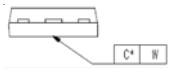
Applications

- High-Side Switching
- Push Pull Amplifiers
- DC Choppers
- Automatic Test Equipment
- Current Regulators
- Battery Charger Applications

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	V_{DS} = -10V, I_D = - 60A, Note 1	90	150	S
C_{iss}	V_{GS} = 0V, V_{DS} = - 25V, f = 1MHz		69.5	nF
C_{oss}			4070	pF
C_{rss}			1100	pF
$t_{d(on)}$	**Resistive Switching Times**		90	ns
t_r	V_{GS} = -10V, V_{DS} = 0.5 • V_{DSS}, I_D = -105A		98	ns
$t_{d(off)}$	R_G = 1Ω (External)		165	ns
t_f			55	ns
$Q_{g(on)}$	V_{GS} = -10V, V_{DS} = 0.5 • V_{DSS}, I_D = -105A		740	nC
Q_{gs}			200	nC
Q_{gd}			155	nC
R_{thJC}				0.21 °C/W
R_{thCS}			0.15	°C/W

ISOPLUS247 (IXTR) Outline





1 = Gate
2,4 = Drain
3 = Source

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.085	1.91	2.15
b2	.115	.126	2.92	3.20
C	.024	.033	0.61	0.83
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.811	19.81	20.60
L1	.150	.172	3.81	4.38
Q	.220	.244	5.59	6.20
R	.170	.191	4.32	4.85
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03
W	0	.004	0	0.10

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
I_S	V_{GS} = 0V			- 210 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			- 840 A
V_{SD}	I_F = -100A, V_{GS} = 0V, Note 1			-1.4 V
t_{rr}	I_F = -105A, -di/dt = -100A/μs			200 ns
Q_{RM}	V_R = -100V, V_{GS} = 0V		930	nC
I_{RM}			-12.4	A

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

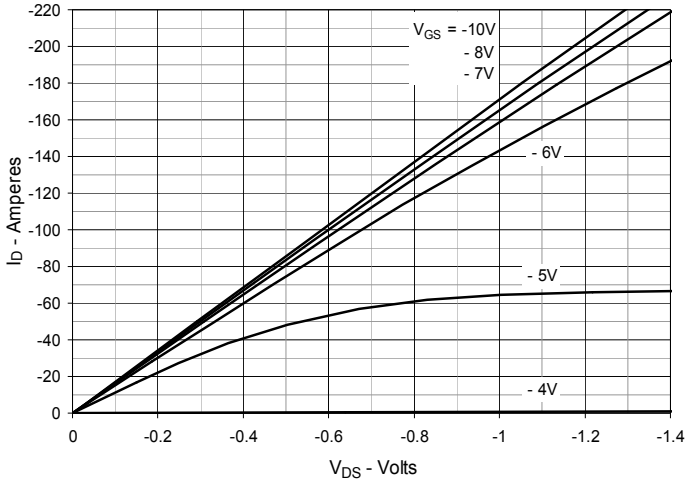


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

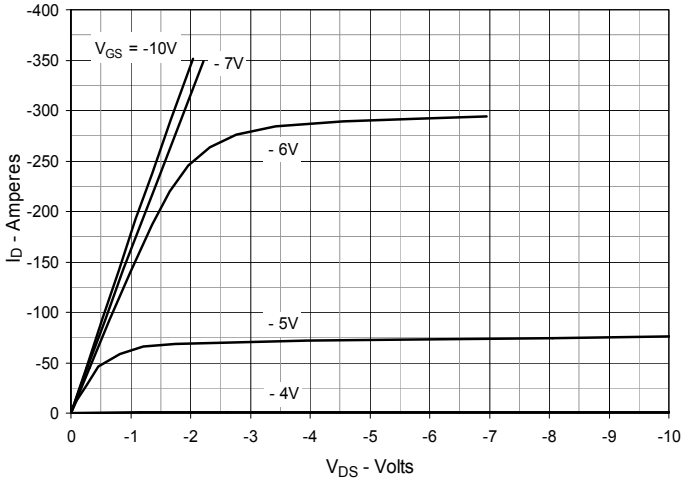


Fig. 3. Output Characteristics @ T_J = 125ºC

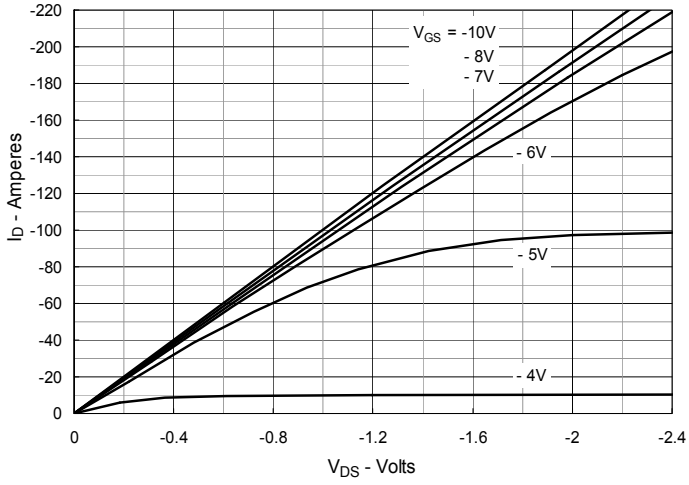


Fig. 4. $R_{DS(on)}$ Normalized to I_D = -105A Value vs. Junction Temperature

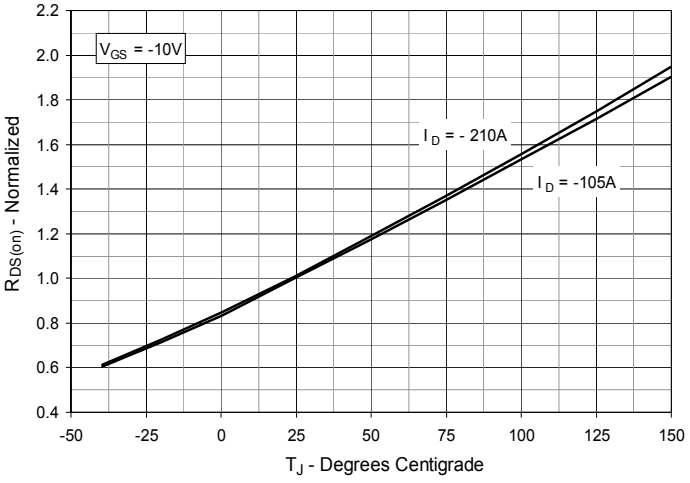


Fig. 5. $R_{DS(on)}$ Normalized to I_D = -105A Value vs. Drain Current

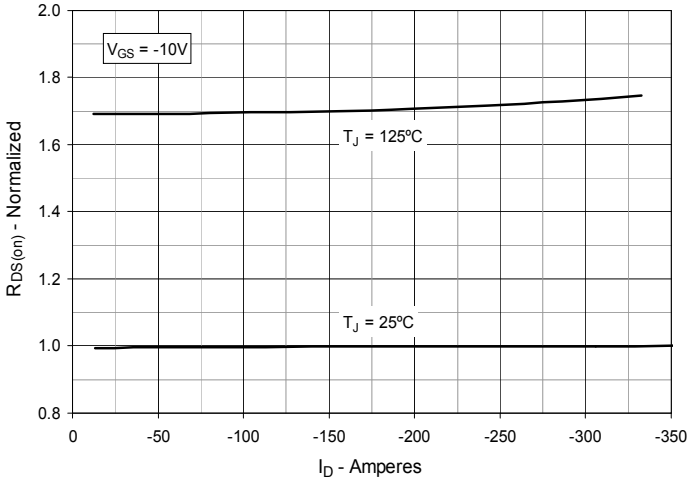


Fig. 6. Maximum Drain Current vs. Case Temperature

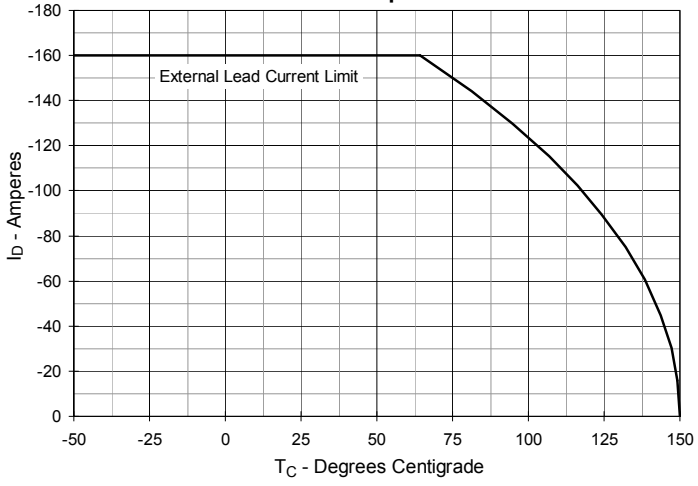


Fig. 7. Input Admittance

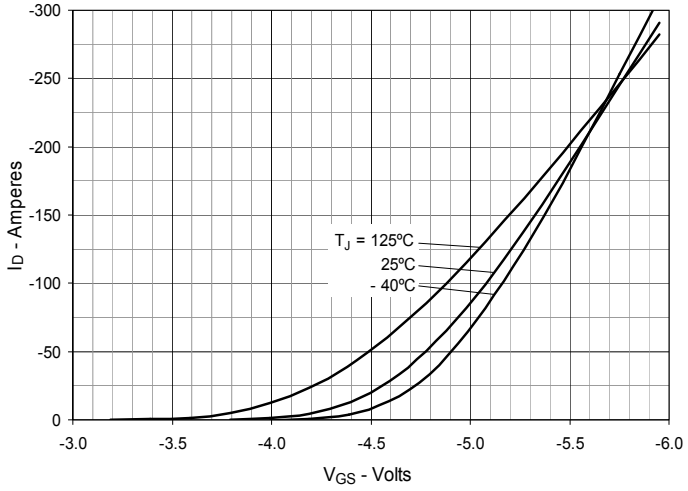


Fig. 8. Transconductance

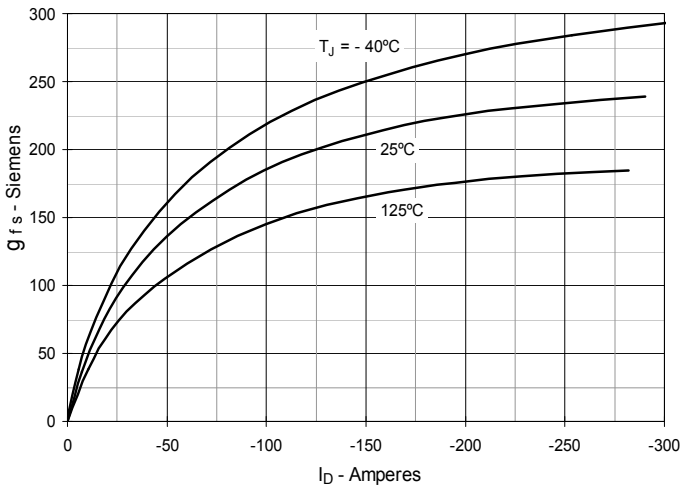


Fig. 9. Forward Voltage Drop of Intrinsic Diode

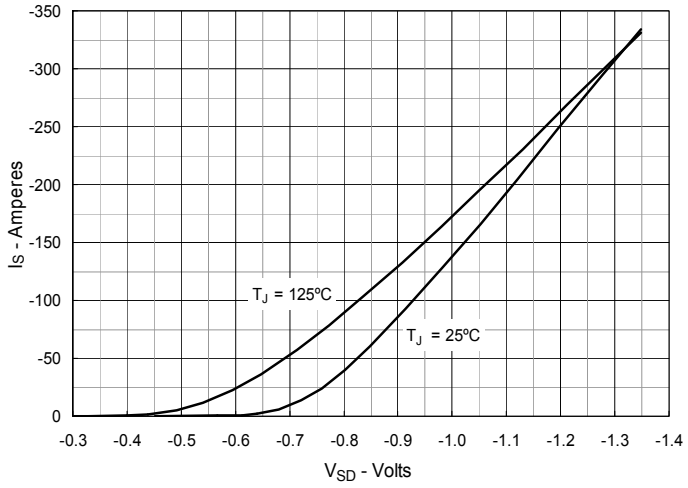


Fig. 10. Gate Charge

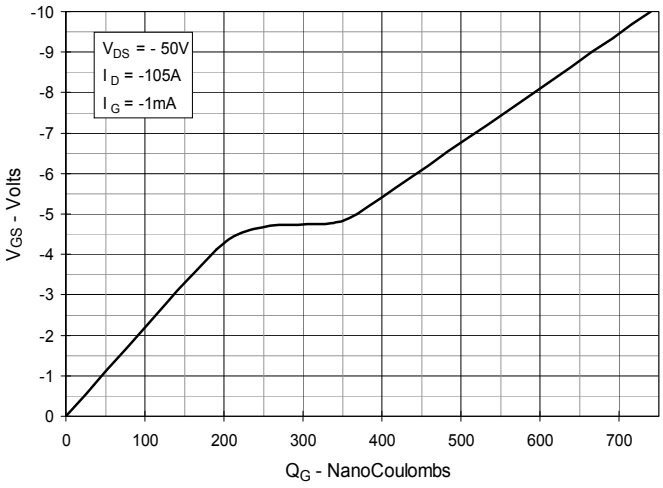


Fig. 11. Capacitance

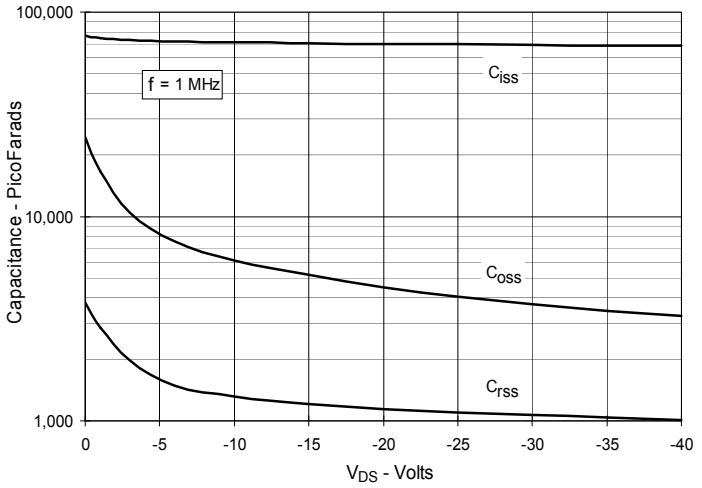


Fig. 12. Forward-Bias Safe Operating Area

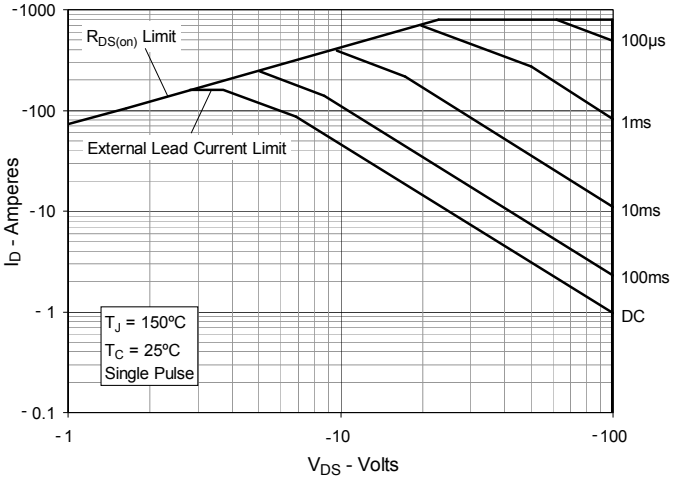


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

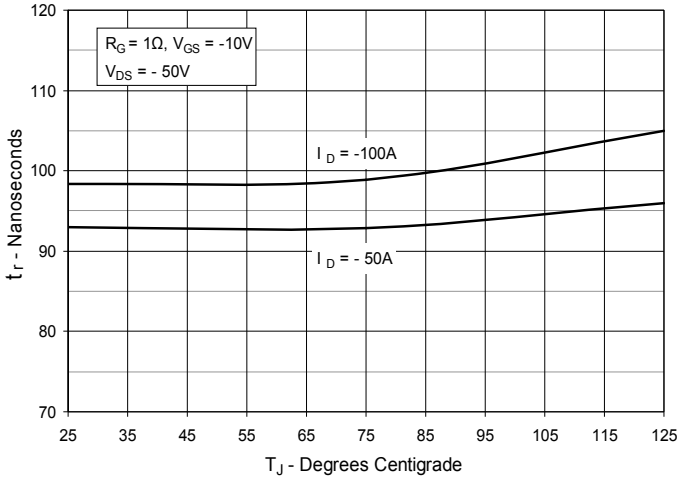


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

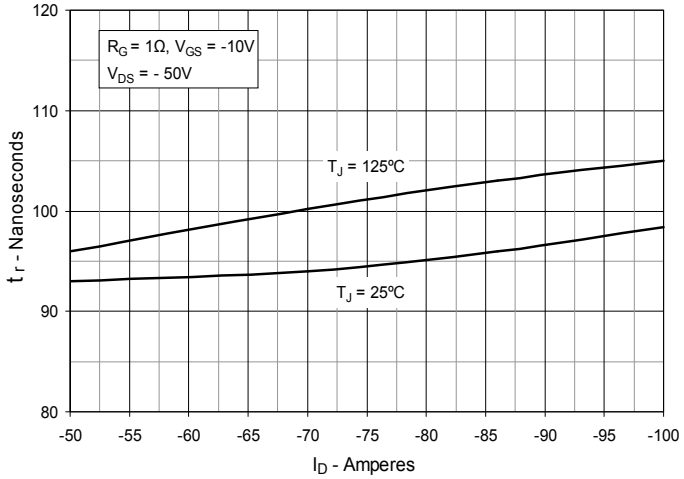


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

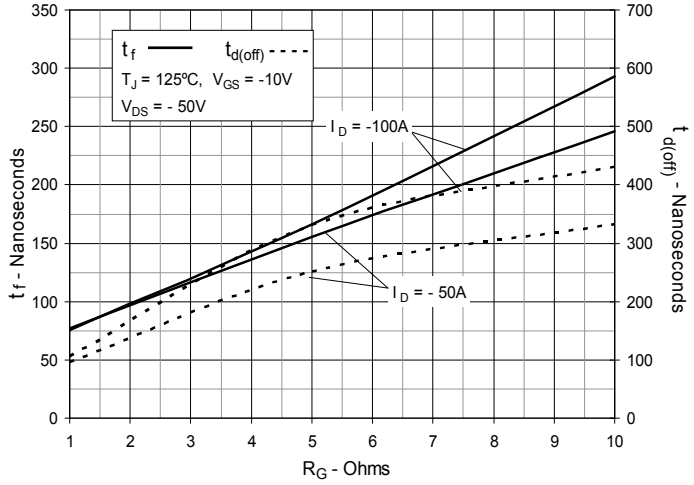


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

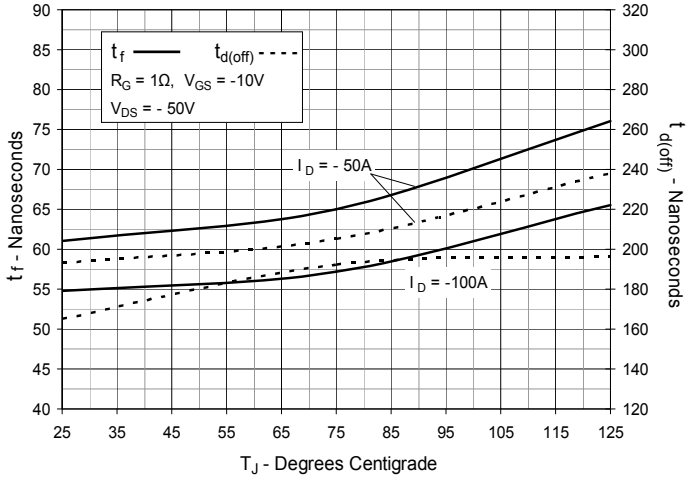


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

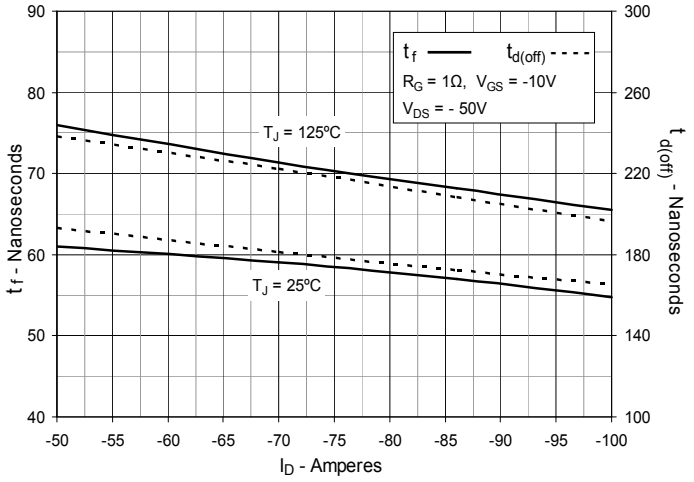


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

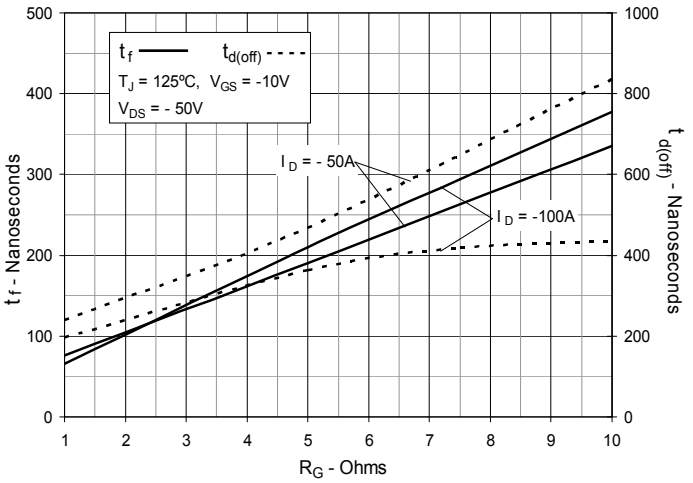


Fig. 19. Maximum Transient Thermal Impedance