NXS0102

Dual supply translating transceiver; open drain; auto direction sensing

Rev. 5 — 6 September 2021 Product data sheet

1. General description

The NXS0102 is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 2-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.65 V and 3.6 V and $V_{CC(B)}$ can be supplied at any voltage between 2.3 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.65 V to 3.6 V and $V_{CC(B)}$: 2.3 V to 5.5 V
- Maximum data rates:
  - Push-pull: 24 Mbps
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM: ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2.5 kV for A port
  - HBM: ANSI/ESDA/Jedec JS-001 Class 3B exceeds 8 kV for B port
  - CDM: ANSI/ESDA/Jedec JS-002 Class C3 exceeds 1.5 kV
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Desktop PC
- Handset
- Smartphone
- Tablet

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4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXS0102DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
NXS0102GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
NXS0102UN	-40 °C to +125 °C	WLCSP8	wafer level chip-scale package; 8 bumps; 0.75 × 1.55 × 0.60 mm	SOT8023-1

5. Marking

Table 2. Marking

Type number	Marking code
NXS0102DC	m2
NXS0102GT	m2
NXS0102UN	m2

6. Functional diagram

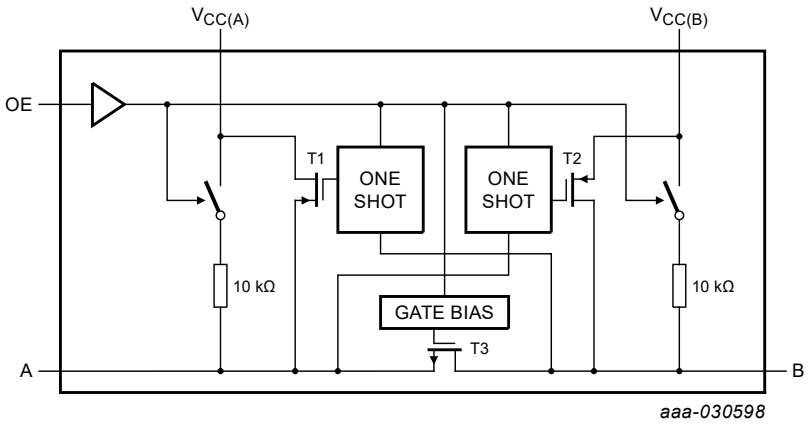


Fig. 1. Functional diagram (one channel)

7. Pinning information

7.1. Pinning

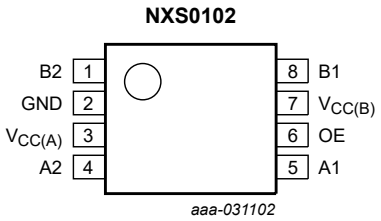


Fig. 2. Pin configuration SOT765-1 (VSSOP8)

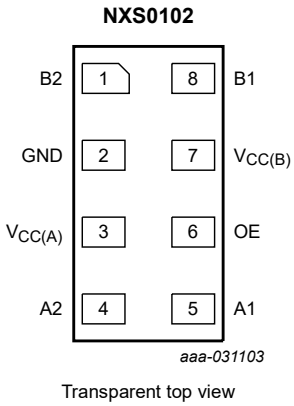


Fig. 3. Pin configuration SOT833-1 (XSON8)

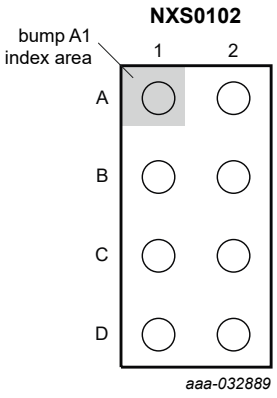


Fig. 4. Bump configuration SOT8023-1 (WLCSP8)

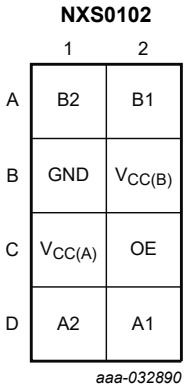


Fig. 5. Bump mapping for SOT8023-1 (WLCSP8)

7.2. Pin description

Table 3. Bump description

Symbol	Pin	Bump	Description
B2, B1	1, 8	A1, A2	data input or output (referenced to $V_{CC(B)}$)
GND	2	B1	ground (0 V)
$V_{CC(A)}$	3	C1	supply voltage A
A2, A1	4, 5	D1, D2	data input or output (referenced to $V_{CC(A)}$)
OE	6	C2	output enable input (active HIGH; referenced to $V_{CC(A)}$)
$V_{CC(B)}$	7	B2	supply voltage B

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage		Input	Input/output	
$V_{CC(A)}$ [1]	$V_{CC(B)}$	OE	An	Bn
1.65 V to 3.6 V	2.3 V to 5.5 V	L	Z	Z
1.65 V to 3.6 V	2.3 V to 5.5 V	H	input or output	output or input
GND	2.3 V to 5.5 V	X	Z	Z
1.65 V to 3.6 V	GND	X	Z	Z

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
V_I	input voltage	OE [1]	-0.5	+6.5	V
		Power-down or 3-state mode			
		A, B [1]	-0.5	+6.5	V
		Active mode			
		A, B [1] [2] [3]	-0.5	V_{CCI} + 0.5	V
V_O	output voltage	Power-down or 3-state mode			
		A, B [1]	-0.5	+6.5	V
		Active mode			
		A, B [1] [3] [4]	-0.5	V_{CCO} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
I_{OK}	output clamping current	V_O < 0 V	-50	-	mA
I_O	output current	V_O = 0 V to V_{CCO} [4]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [5]	-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCI} is the supply voltage associated with the input.
[3] V_{CCI} + 0.5 V or $V_{CCO)}$ + 0.5 V should not exceed 6.5 V.
[4] V_{CCO} is the supply voltage associated with the output.
[5] For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.
For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.
For SOT8023-1 (WLCSP8) package: P_{tot} derates linearly with 7.2 mW/K above 115 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions [1] [2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	3.6	V
$V_{CC(B)}$	supply voltage B		2.3	5.5	V
V_I	input voltage	OE	0	5.5	V
		Power-down or 3-state mode			
		A	0	3.6	V
		B	0	5.5	V
		Active mode			
		A, B [3]	0	V_{CCI}	V
V_O	output voltage	Power-down or 3-state mode			
		A	0	3.6	V
		B	0	5.5	V
		Active mode			
		A, B [4]	0	V_{CCO}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	10	ns/V
		OE input			
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
[3] V_{CCI} is the supply voltage associated with the input.
[4] V_{CCO} is the supply voltage associated with the output.

11. Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	OE input; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	-	±1	µA
I_{OZ}	OFF-state output current	A or B port; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V; OE = 0 V	-	-	±1	µA
I_{OFF}	power-off leakage current	A port; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	-	-	±1	µA
		B port; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V	-	-	±1	µA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V	-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V				
		enabled	-	10	-	pF
		disabled	-	4	-	pF
		B port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V				
		enabled	-	10	-	pF
		disabled	-	7	-	pF

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

Table 8. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$						Unit
	2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.8 V	0.1	0.5	0.1	1.5	0.1	4.6	µA
2.5 V	0.1	0.1	0.1	0.8	0.1	3.8	µA
3.3 V	-	-	0.1	0.1	0.1	2.8	µA

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port					
		$V_{CC(A)}$ = 1.65 V to 1.95 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$V_{CC(A)}$ - 0.2	$V_{CC(A)}$	$V_{CC(A)}$ - 0.2	$V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$V_{CC(A)}$ - 0.4	$V_{CC(A)}$	$V_{CC(A)}$ - 0.4	$V_{CC(A)}$	V
		B port					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$V_{CC(B)}$ - 0.4	$V_{CC(B)}$	$V_{CC(B)}$ - 0.4	$V_{CC(B)}$	V
		OE input					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$0.65V_{CC(A)}$	$V_{CC(A)}$	$0.65V_{CC(A)}$	$V_{CC(A)}$	V
V_{IL}	LOW-level input voltage	A or B port					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	0	0.15	0	0.15	V
		OE input					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	0	$0.35V_{CC(A)}$	0	$0.35V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	A port; I_O = -20 µA; $V_I \geq V_{CC(B)}$ - 0.4 V					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$0.67V_{CC(A)}$	-	$0.67V_{CC(A)}$	-	V
		B port; I_O = -20 µA; $V_I \geq V_{CC(A)}$ - 0.2 V					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$0.67V_{CC(B)}$	-	$0.67V_{CC(B)}$	-	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 1 mA; $V_I \leq 0.15$ V					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	0.4	-	0.4	V
I_I	input leakage current	OE input; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	±2	-	±12	µA
I_{OZ}	OFF-state output current	A or B port; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	±2	-	±12	µA
I_{OFF}	power-off leakage current	A port; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	-	±2	-	±12	µA
		B port; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V	-	±2	-	±12	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	OE = 0 V or $V_{CC(A)}$; An, Bn open					
		$I_{CC(A)}$					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	2.4	-	15	µA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	2.2	-	15	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-	-1	-	-8	µA
		$I_{CC(B)}$					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	12	-	30	µA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	-1	-	-5	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-	1	-	6	µA
		$I_{CC(A)} + I_{CC(B)}$					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	14.4	-	30	µA

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$ and $V_{CC(A)}$ must not exceed 3.6 V.

12. Dynamic characteristics

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9; for waveforms see Fig. 6 to Fig. 8.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	5.3	-	5.4	-	6.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	7.1	-	7.1	-	7.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	4.4	-	4.5	-	4.7	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	5.3	-	4.5	-	0.5	ns
t_{en}	enable time	OE to A, B	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A, B; no external load [1] [2]	-	35	-	35	-	35	ns
		OE to A	-	140	-	140	-	145	ns
		OE to B	-	125	-	175	-	125	ns
t_{TLH}	LOW to HIGH output transition time	A port	3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port	3.3	10.8	2.7	9.1	2.7	7.6	ns
t_{THL}	HIGH to LOW output transition time	A port	2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port	2.9	7.6	2.8	7.9	2.8	10.5	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.7	-	0.7	-	0.7	ns
t_W	pulse width	data inputs	41	-	41	-	41	-	ns
f_{data}	data rate		-	24	-	24	-	24	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 2.5 V ± 0.2 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	3.2	-	3.7	-	3.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	3.5	-	4.4	-	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	3.0	-	3.6	-	4.3	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	2.5	-	1.6	-	1.0	ns
t_{en}	enable time	OE to A, B	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A, B; no external load [1] [2]	-	35	-	35	-	35	ns
		OE to A	-	105	-	105	-	105	ns
		OE to B	-	125	-	175	-	120	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.8	7.5	2.6	6.6	1.8	6.5	ns
		B port	3.2	8.5	2.9	7.9	2.4	6.8	ns
t_{THL}	HIGH to LOW output transition time	A port	1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port	2.2	7.8	2.4	6.7	2.6	6.9	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.7	-	0.7	-	0.7	ns
t_W	pulse width	data inputs	41	-	41	-	41	-	ns
f_{data}	data rate		-	24	-	24	-	24	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	-	-	2.4	-	3.1	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	-	-	4.2	-	4.4	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	-	-	2.5	-	3.3	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	-	-	2.5	-	2.6	ns
t_{en}	enable time	OE to A, B	-	-	-	200	-	200	ns
t_{dis}	disable time	OE to A, B; no external load [1] [2]	-	-	-	35	-	35	ns
		OE to A	-	-	-	150	-	150	ns
		OE to B	-	-	-	170	-	120	ns
t_{TLH}	LOW to HIGH output transition time	A port	-	-	2.3	6.2	1.9	6.3	ns
		B port	-	-	2.5	6.9	2.1	7.4	ns
t_{THL}	HIGH to LOW output transition time	A port	-	-	2.0	5.4	1.9	5.0	ns
		B port	-	-	2.3	7.4	2.4	7.6	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	0.7	-	0.7	ns
t_W	pulse width	data inputs	-	-	41	-	41	-	ns
f_{data}	data rate		-	-	-	24	-	24	Mbps

[1] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] The disable time with no external load indicates the delay between when OE goes LOW and when outputs actually become disabled.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C

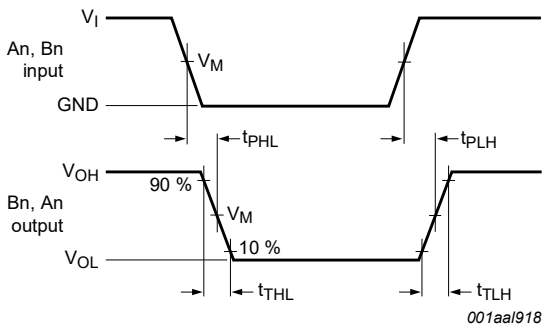
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9; for waveforms see Fig. 6 to Fig. 8.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	5.8	-	5.9	-	7.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	8.5	-	8.5	-	8.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	5.5	-	5.7	-	5.9	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	6.7	-	5.7	-	0.7	ns
t_{en}	enable time	OE to A, B	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A, B; no external load [1] [2]	-	45	-	45	-	45	ns
		OE to A	-	140	-	140	-	145	ns
		OE to B	-	125	-	175	-	125	ns
t_{TLH}	LOW to HIGH output transition time	A port	3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port	3.3	13.5	2.7	11.4	2.7	9.5	ns
t_{THL}	HIGH to LOW output transition time	A port	2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port	2.9	9.5	2.8	9.4	2.8	12.5	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.8	-	0.8	-	0.8	ns
t_W	pulse width	data inputs	50	-	41	-	41	-	ns
f_{data}	data rate		-	20	-	24	-	24	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	4.0	-	4.2	-	4.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	4.4	-	5.2	-	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	3.8	-	4.5	-	5.4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	3.2	-	2.0	-	0.9	ns
t_{en}	enable time	OE to A, B	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A, B; no external load [1] [2]	-	45	-	45	-	45	ns
		OE to A	-	105	-	105	-	105	ns
		OE to B	-	125	-	175	-	120	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port	3.2	10.4	2.9	9.7	2.4	8.3	ns
t_{THL}	HIGH to LOW output transition time	A port	1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.8	-	0.8	-	0.8	ns
t_W	pulse width	data inputs	50	-	41	-	41	-	ns
f_{data}	data rate		-	20	-	24	-	24	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	-	-	-	3.0	-	3.9	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	-	-	5.3	-	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	-	-	3.2	-	4.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	-	-	3.2	-	3.3	ns
t_{en}	enable time	OE to A, B	-	-	-	200	-	200	ns
t_{dis}	disable time	OE to A, B; no external load [1] [2]	-	-	-	45	-	45	ns
		OE to A	-	-	-	150	-	150	ns
		OE to B	-	-	-	170	-	120	ns
t_{TLH}	LOW to HIGH output transition time	A port	-	-	2.3	7.0	1.9	7.4	ns
		B port	-	-	2.5	8.0	2.1	9.3	ns
t_{THL}	HIGH to LOW output transition time	A port	-	-	2.0	6.8	1.9	6.3	ns
		B port	-	-	2.3	9.3	2.4	9.5	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	0.8	-	0.8	ns
t_W	pulse width	data inputs	-	-	41	-	41	-	ns
f_{data}	data rate		-	-	-	24	-	24	Mbps

[1] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] The disable time with no external load indicates the delay between when OE goes LOW and when outputs actually become disabled.
[3] Skew between any two outputs of the same package switching in the same direction.

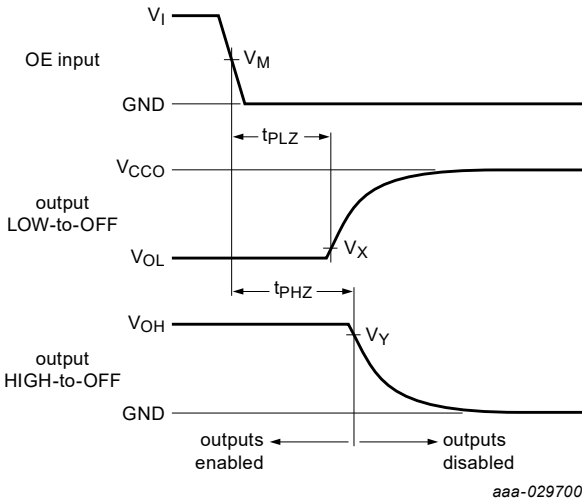
12.1. Waveforms and test circuit



Measurement points are given in Table 12.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The data input (An, Bn) to data output (Bn, An) propagation delay times

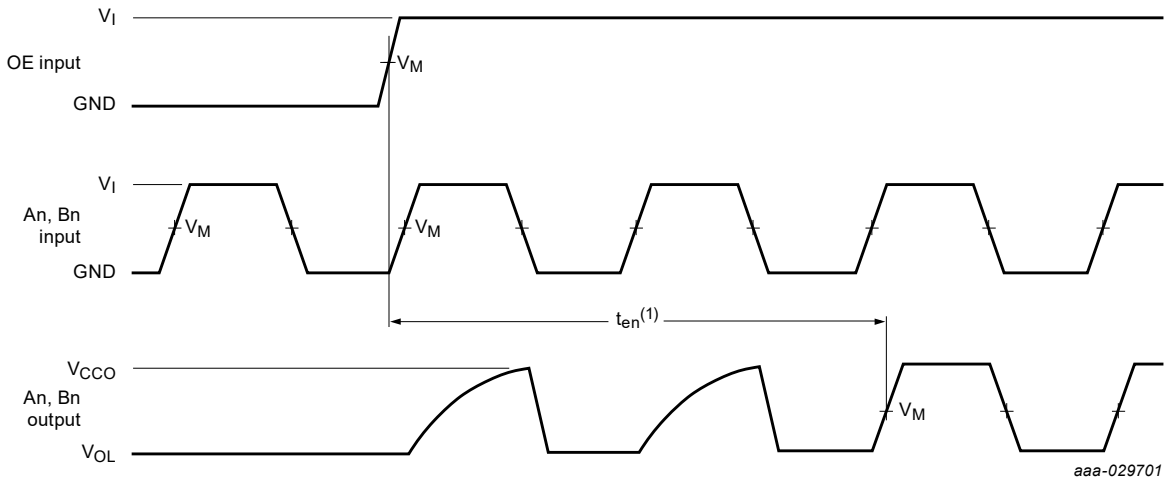


Measurement points are given in Table 12.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

V_{CCO} is the supply voltage associated with the output.

Fig. 7. Disable times



(1) The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. See also Section 13.6

Measurement points are given in Table 12.

V_{OL} is a typical output voltage level that occur with the output load.

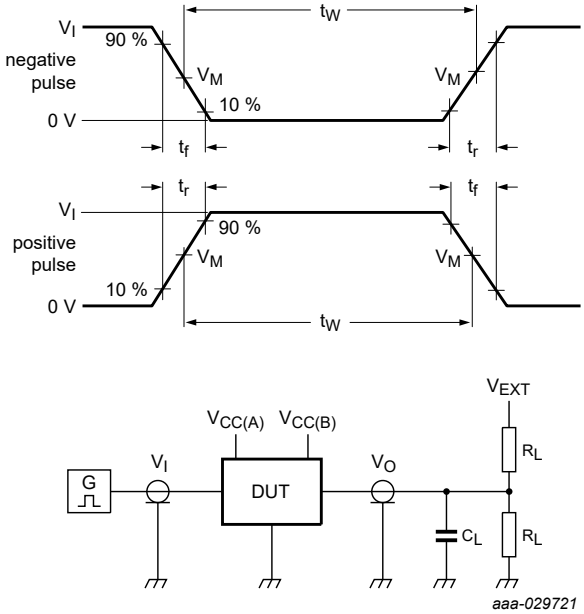
V_{CCO} is the supply voltage associated with the output.

Fig. 8. Enable times

Table 12. Measurement points

Supply voltage	Input	Output		
V_{CCO}	V_M [1]	V_M [2]	V_X	V_Y
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 13.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 13. Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	Δt/ΔV	C_L	R_L [2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.

[3] V_{CCO} is the supply voltage associated with the output.

13. Application information

13.1. Applications

Voltage level-translation applications. The NXS0102 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I^2C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports, however the NXB0102 may be more suitable.

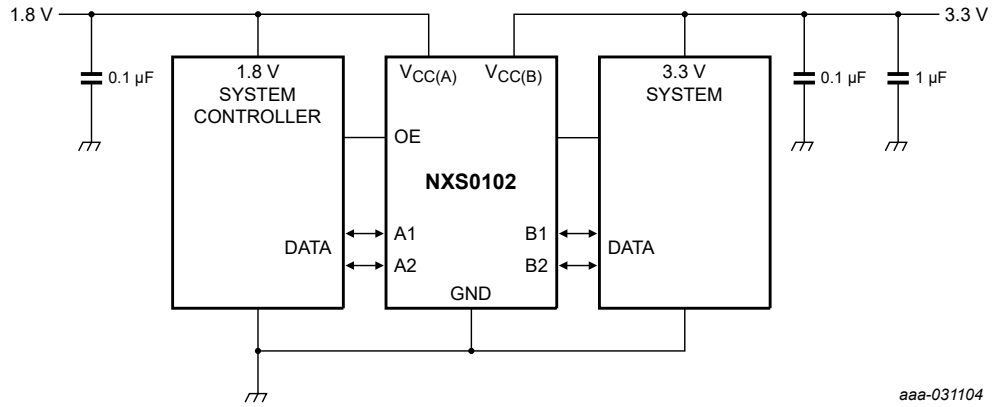


Fig. 10. Typical operating circuit

13.2. Architecture

The architecture of the NXS0102 is shown in Fig. 11. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

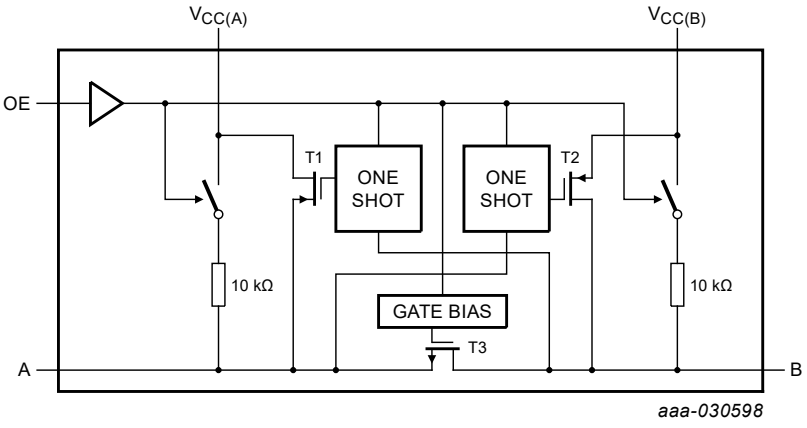


Fig. 11. Architecture of NXS0102 I/O cell (one channel)

The NXS0102 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the $V_{CC(A)}$ level of the low-voltage side. During a rising edge, the one shots turn on the PMOS transistors (T1, T2) for a short duration, accelerating the low-to-high transition. The one-shot is activated once the input transition reaches approximately $0.5V_{CCI}$. During the acceleration time the driver output resistance is between approximately 50 Ω and 70 Ω. To avoid signal contention and minimize dynamic I_{CC}, the user should wait for the one-shot circuit to turn-off before applying a

signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

13.3. Input driver requirements

As the NXS0102 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time (t_{THL}) and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50 Ω is used.

13.4. Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration.To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on NXS0102 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration.

13.5. Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so any power supply can be ramped up first. There is no special power-up sequencing required. The NXS0102 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

13.6. Enable and disable

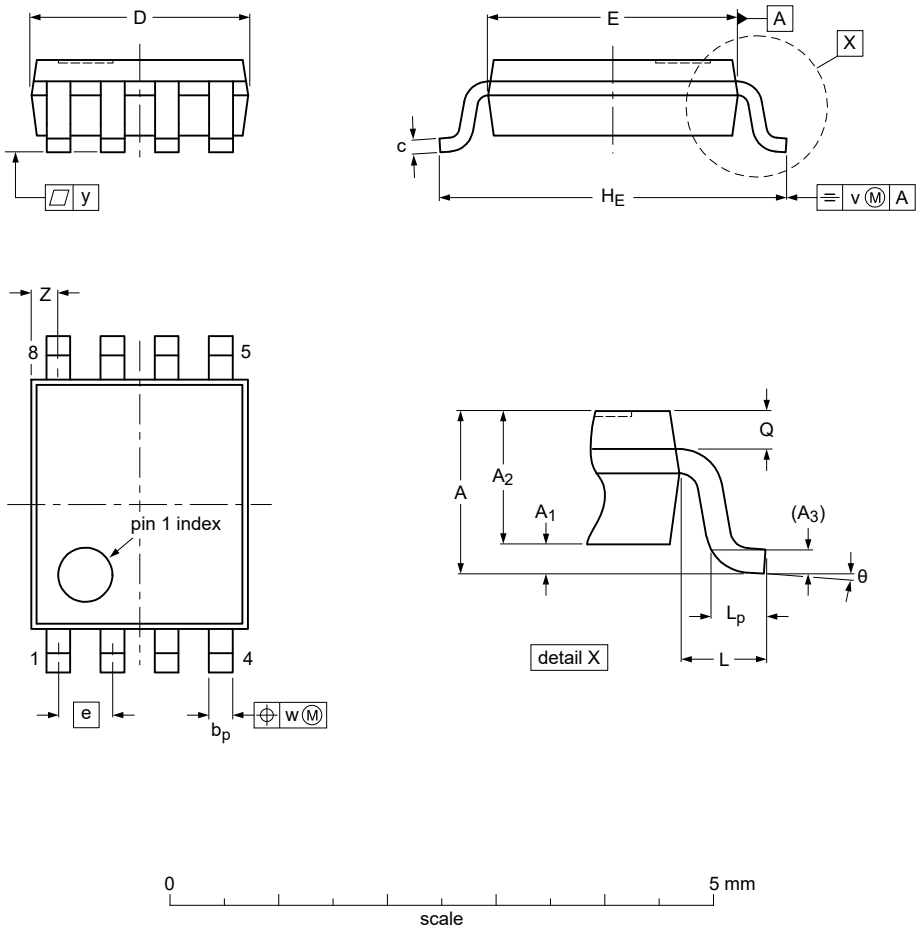
An output enable input (OE) is used to disable the device. Setting OE to LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

13.7. Pull-up or pull-down resistors on I/O lines

Each A port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(A)}$, and each B port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 kΩ, this will effect the V_{OL} level. When OE goes LOW the internal pull-ups of the NXS0102 are disabled.

14. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm max	1	0.15	0.85	0.12	0.27	0.23	2.1	2.4	0.5	3.2	0.4	0.40	0.21	0.2	0.08	0.1	0.4	8°
nom																		
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

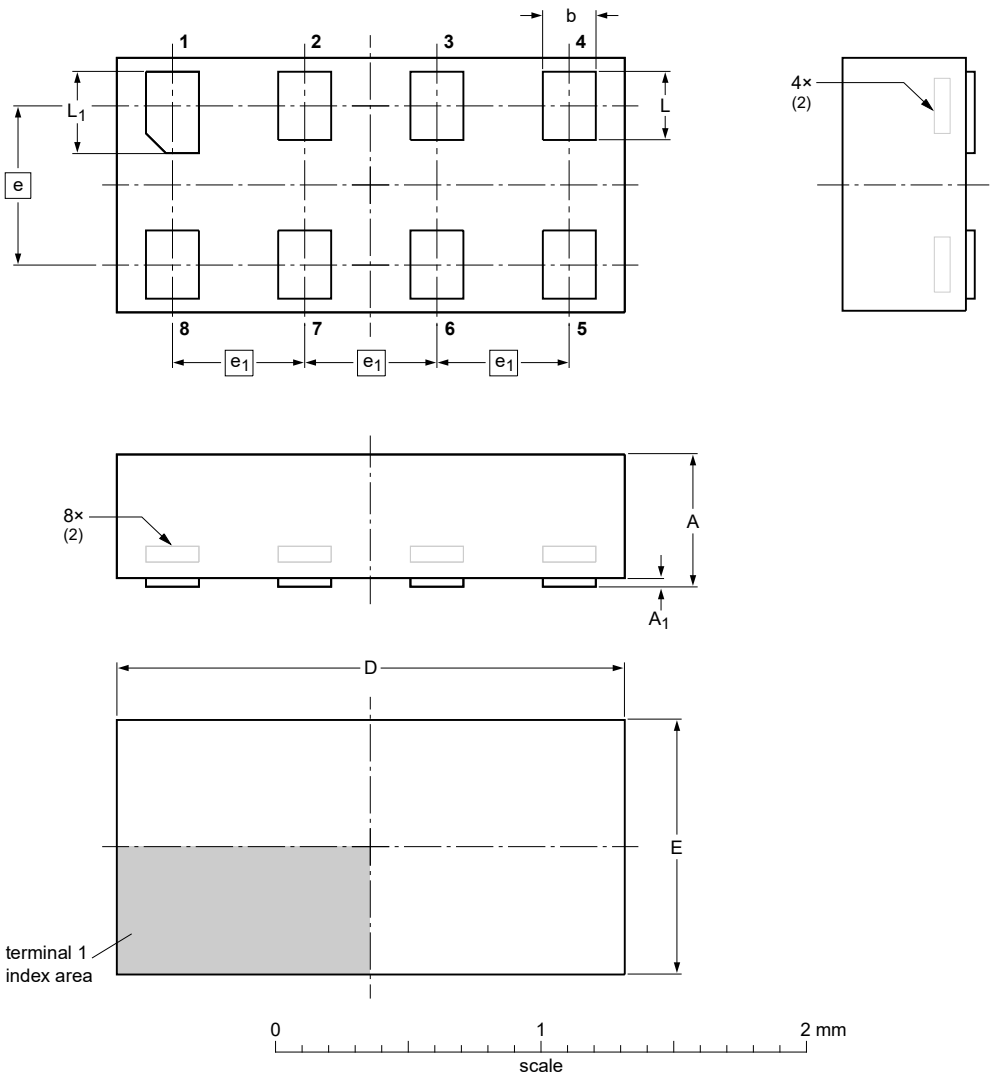
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 12. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

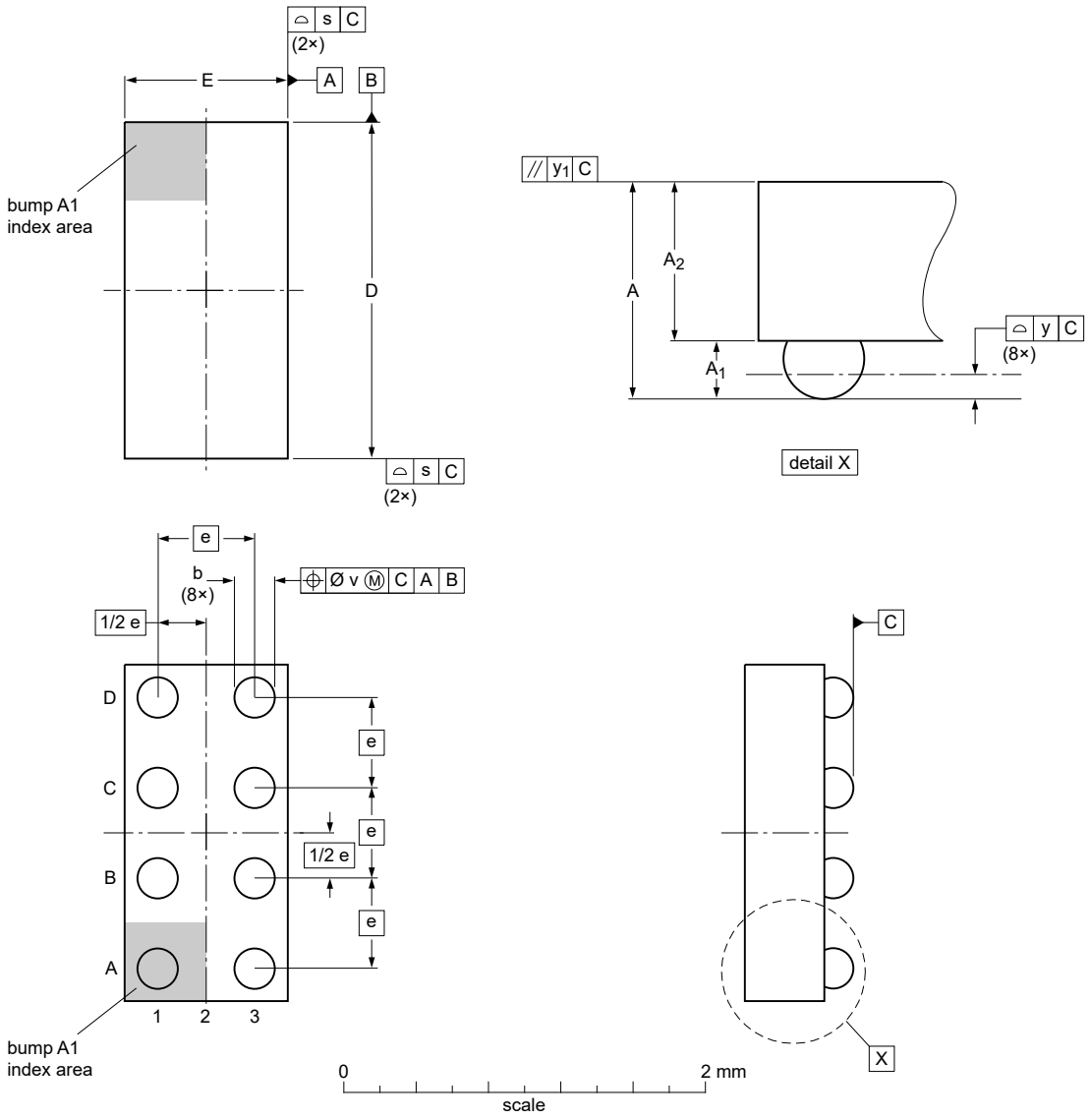
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig. 13. Package outline SOT833-1 (XSON8)

WLCSP8: wafer level chip-scale package, 8 bumps; 0.75 x 1.55 x 0.60 mm **SOT8023-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	s	v	y	y_1
mm	max	0.6325	0.183	0.4495	0.245	1.55	0.75	0.4	0.025	0.05	0.05	0.10
	nom	0.6000	0.163	0.4370	0.225							
	min	0.5675	0.143	0.4245	0.205							

sot8023-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8023-1						~~20-08-11~~ 20-08-12

Fig. 14. Package outline SOT8023-1 (WLCSP8)

15. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
PCB	Printed Circuit Board
PRR	Pulse Rate Repetition

16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXS0102 v.5	20210906	Product data sheet	-	NXS0102 v.4
Modifications:	• Product status of type number NXS0102GT (SOT833-1/XSON8) is set to released for supply.			
NXS0102 v.4	20210630	Product data sheet	-	NXS0102 v.3
Modifications:	• Type number NXS0102UN (SOT8023-1/WLCSP8) added.			
NXS0102 v.3	20201113	Product data sheet	-	NXS0102 v.2
Modifications:	• Table 10 and Table 11: Disable times updated.			
NXS0102 v.2	20200923	Product data sheet	-	NXS0102 v.1
Modifications:	• Type number NXS0102GT (SOT833-1/XSON8) added.			
NXS0102 v.1	20191217	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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