LM20143/LM20143-Q1 3-A PowerWise™ Adjustable Frequency Synchronous Buck Regulator

1 Features

- Available in AEC-Q100 Temperature Grade 1
- Input Voltage Range: 2.95 V to 5.50 V
- Accurate Current Limit Minimizes Inductor Size
- 97% Peak Efficiency
- Adjustable Output Voltage Down to 0.80 V
- Adjustable Switching Frequency (500 kHz to 1.5 MHz)
- 32-mΩ Integrated FET Switches
- Starts into Prebiased Loads
- Output Voltage Tracking
- Peak Current Mode Control
- Adjustable Soft-Start with External Capacitor
- Precision Enable Pin with Hysteresis
- Integrated OVP, UVLO, Power Good and Thermal Shutdown

2 Applications

- Simple to Design, High Efficiency Point of Load Regulation from a 5-V or 3.3-V Bus
- High Performance DSPs, FPGAs, ASICs, and Microprocessors
- Broadband, Networking, and Optical Communications Infrastructure

3 Description

The LM20143 devices are full featured PowerWise™ adjustable frequency synchronous buck regulators capable of delivering up to 3 A of continuous output current. The current mode control loop can be compensated to be stable with virtually any type of output capacitor. For most cases, compensating the device only requires two external components, providing maximum flexibility and ease of use. The device is optimized to work over the input voltage range of 2.95 V to 5.5 V, making it suited for a wide variety of low voltage systems.

The device features internal over voltage protection (OVP) and over current protection (OCP) circuits for increased system reliability. A precision enable pin and integrated UVLO allows the turn-on of the device to be tightly controlled and sequenced. Start-up inrush currents are limited by both an internally fixed and externally adjustable Soft-Start circuit. Fault detection and supply sequencing is possible with the integrated power good circuit.

The frequency of this device can be adjusted from 500 kHz to 1.5 MHz by connecting an external resistor from the RT pin to ground.

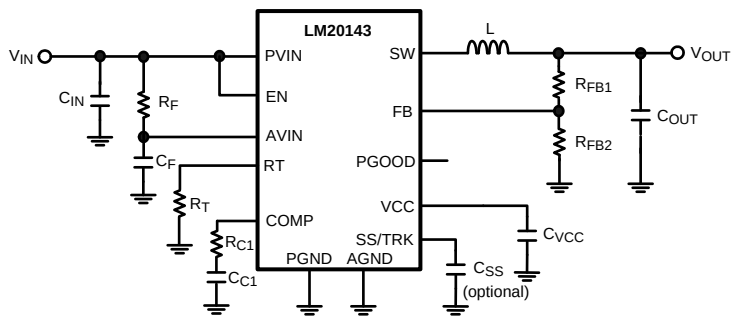
The LM20143 is designed to work well in multi-rail power supply architectures. The output voltage of the device can be configured to track a higher voltage rail using the SS/TRK pin. If the output of the LM20143 is pre-biased at startup it will not sink current to pull the output low until the internal soft-start ramp exceeds the voltage at the feedback pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM20143	HTSSOP (16)	4.40 mm × 5.00 mm
LM20143-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2013) to Revision H **Page**

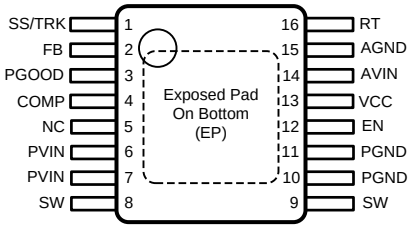
- Added *ESD Ratings* table, *Feature Description*section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision F (March 2013) to Revision G **Page**

- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	SS/TRK	I	Soft-Start or Tracking control input. An internal 5-µA current source charges an external capacitor to set the Soft-Start ramp rate. If driven by a external source less than 800 mV, this pin overrides the internal reference that sets the output voltage. If left open, an internal 1ms Soft-Start ramp is activated.
2	FB	I	Feedback input to the error amplifier from the regulated output. This pin is connected to the inverting input of the internal transconductance error amplifier. An 800-mV reference connected to the non-inverting input of the error amplifier sets the closed loop regulation voltage at the FB pin.
3	PGOOD	O	Power good output signal. Open drain output indicating the output voltage is regulating within tolerance. is recommend for most applications.
4	COMP	O	External compensation pin. Connect the compensation network to resistor and capacitor to this pin to compensate the device.
5	NC	-	This pin has no internal connection. While this pin may be left open, it is strongly recommended that this pin be connected to Ground.
6	PVIN	P	Input voltage to the power switches inside the device. These pins should be connected together at the device. A low ESR capacitor should be placed near these pins to stabilize the input voltage.
7			
8	SW	P	Switch pin. The PWM output of the internal power switches.
9			
10	PGND	G	Power ground pin for the internal power switches.
11			
12	EN	I	Precision enable input for the device. An external voltage divider can be used to set the device turn-on threshold. If not used the EN pin should be connected to PVIN.
13	VCC	P	Internal 2.7-V sub-regulator. This pin should be bypassed with a 1-µF ceramic capacitor.
14	AVIN	P	Analog input supply that generates the internal bias. Must be connected to VIN through a low pass RC filter.
15	AGND	G	Quiet analog ground for the internal bias circuitry.
16	RT	I	Frequency adjust pin. Connecting a resistor on this pin to ground will set the oscillator frequency.
EP	Exposed Pad	-	Exposed metal thermal pad on the underside of the package with a weak electrical connection to ground. It is recommended to connect this pad to the PC board ground plane copper in order to improve heat dissipation and reduce the package θ_{JA}. Do not connect to any potential other than Ground.

(1) P: Power, I: Input, O: Output, G: Ground

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
AVIN, PVIN, EN, PGOOD, SS/TRK, COMP, FB, RT	Voltages from indicated pins to GND	–0.3	6	V
Power Dissipation(2)			2.6	W
Junction Temperature			150	°C
Lead Temperature (Soldering, 10 sec)			260	°C
Storage Temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junctions-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\_MAX} = (T_{J\_MAX} – T_A) / \theta_{JA}$. The maximum power dissipations of 2.6 W is determined using T_A = 25°C, θ_{JA} = 38°C/W, and T_{J_MAX} = 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
PVIN, AVIN to GND	2.95	5.5	V
Junction Temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM20143 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (3)	20.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) On JEDEC 4-Layer test board (JESD 51-7) with eight (8) thermal vias.
(3) θ_{JC} refers to center of the Exposed Pad on the bottom of the package as the case.

6.5 Electrical Characteristics

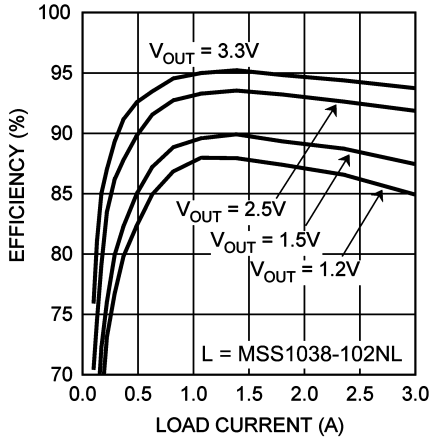
Unless otherwise stated, the following conditions apply: AVIN = PVIN = VIN = 5 V. All Typical limits are for T_J = 25°C only, all Minimum and Maximum limits apply over the junction temperature (T_J) range of –40°C to 125°C(1). Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback pin voltage	V_{IN} = 2.95 V to 5.5 V	0.788	0.8	0.812	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 100 mA to 3 A		0.08		%/A
I_{CL}	Switch Current Limit Threshold	V_{IN} = 3.3 V	4.3	4.8	5.3	A
R_{DS_ON}	High-Side Switch On Resistance	I_{SW} = 3.5 A		36	55	mΩ
R_{DS_ON}	Low-Side Switch On Resistance	I_{SW} = 3.5 A		32	52	mΩ
I_Q	Operating Quiescent Current	Non-switching, V_{FB} = V_{COMP}		3.5	6	mA
I_{SD}	Shutdown Quiescent current	V_{EN} = 0 V		90	180	µA
V_{UVLO}	VIN Under Voltage Lockout	Rising V_{IN}	2.45	2.7	2.95	V
V_{UVLO_HYS}	VIN Under Voltage Lockout Hysteresis	Falling V_{IN}		45	100	mV
V_{VCC}	VCC Voltage	I_{VCC} = 0 µA	2.45	2.7	2.95	V
I_{SS}	Soft-Start Pin Source Current	$V_{SS/TRK}$ = 0 V	2	4.5	7	µA
V_{TRACK}	SS/TRK Accuracy, V_{SS} - V_{FB}	$V_{SS/TRK}$ = 0.4 V	–10	3	15	mV
OSCILLATOR						
F_{OSCH}	Oscillator Frequency	R_T = 49.9 kΩ	1350	1500	1650	kHz
F_{OSCL}	Oscillator Frequency	R_T = 249 kΩ	450	510	570	kHz
DC_{MAX}	Maximum Duty Cycle	I_{LOAD} = 0 A		85%		
T_{ON_TIME}	Minimum On Time			100		ns
T_{CL_BLANK}	Current Sense Blanking Time	After Rising V_{SW}		80		ns
ERROR AMPLIFIER AND MODULATOR						
I_{FB}	Feedback pin bias current	V_{FB} = 0.8 V		1	100	nA
I_{COMP_SRC}	COMP Output Source Current	V_{FB} = V_{COMP} = 0.6 V	80	100		µA
I_{COMP_SNK}	COMP Output Sink Current	V_{FB} = 1.0 V, V_{COMP} = 0.6 V	80	100		µA
Gm	Error Amplifier Transconductance	I_{COMP} = ± 50 µA	450	510	600	µmho
A_{VOL}	Error Amplifier Voltage Gain			2000		V/V
POWER GOOD						
V_{OVP}	Over Voltage Protection Rising Threshold	With respect to V_{FB}	105%	108%	111%	
V_{OVP_HYS}	Over Voltage Protection Hysteresis	With respect to V_{FB}		2%	3%	
V_{PGTH}	PGOOD Rising Threshold	With respect to V_{FB}	92%	94%	96%	
V_{PGHYS}	PGOOD Falling Hysteresis	With respect to V_{FB}		2%	3%	
T_{PGOOD}	PGOOD deglitch time			16		µs
I_{OL}	PGOOD Low Sink Current	V_{PGOOD} = 0.4 V	0.6	1		mA
I_{OH}	PGOOD High Leakage Current	V_{PGOOD} = 5 V		5	100	nA
ENABLE						
V_{IH_EN}	EN Pin turn-on Threshold	V_{EN} Rising	1.08	1.18	1.28	V
V_{EN_HYS}	EN Pin Hysteresis			66		mV
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown			160		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			10		°C

(1) Minimum and Maximum limits are specified by test, design, or statistical correlation.

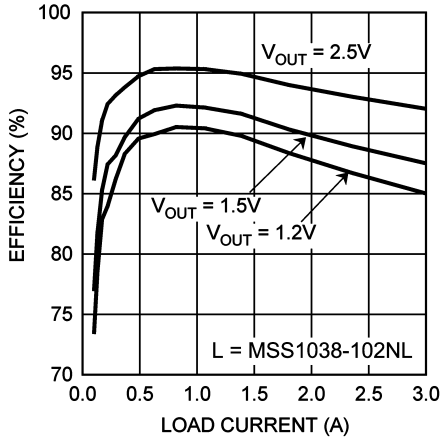
6.6 Typical Characteristics

Unless otherwise specified: $C_{IN} = C_{OUT} = 100$ µF, L = 1.0 µH, $V_{IN} = 5$ V, $V_{OUT} = 1.2$ V, $R_{LOAD} = 1.2$ Ω, $f_{SW} = 1$ MHz, $T_A = 25°C$ for efficiency curves, loop gain plots and waveforms, and $T_J = 25°C$ for all others.



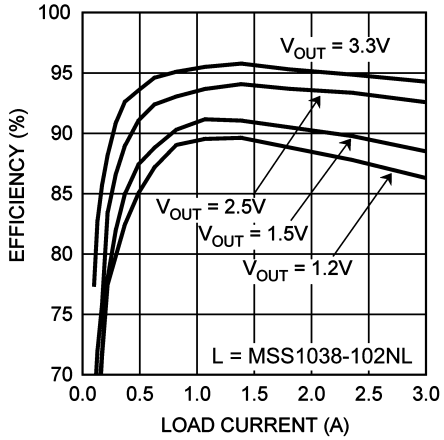
V_{IN} = 5 V f_{SW} = 1.5 MHz

Figure 1. Efficiency vs Load Current



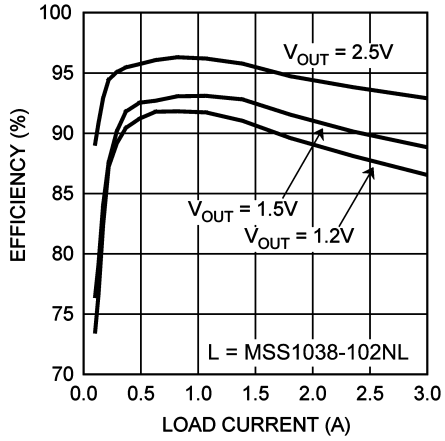
V_{IN} = 3.3 V f_{SW} = 1.5 MHz

Figure 2. Efficiency vs Load Current



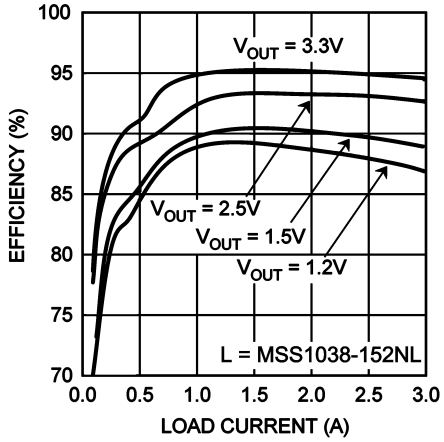
V_{IN} = 5 V f_{SW} = 1.0 MHz

Figure 3. Efficiency vs Load Current



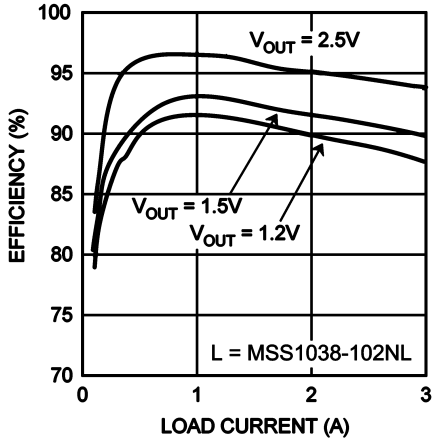
V_{IN} = 3.3 V f_{SW} = 1.0 MHz

Figure 4. Efficiency vs Load Current



V_{IN} = 5.0 V f_{SW} 500 kHz

Figure 5. Efficiency vs Load Current



V_{IN} = 3.3 V f_{SW} = 500 kHz

Figure 6. Efficiency vs Load Current

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = C_{OUT} = 100 µF, L = 1.0 µH, V_{IN} = 5 V, V_{OUT} = 1.2 V, R_{LOAD} = 1.2 Ω, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

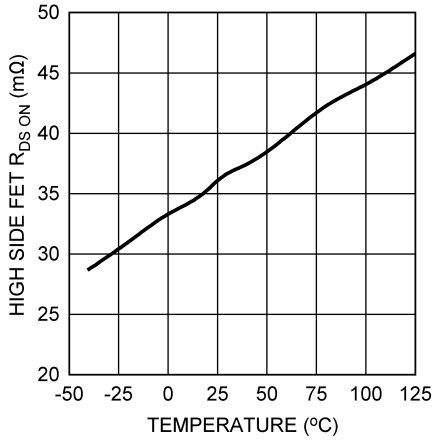


Figure 7. High-Side FET Resistance vs Temperature

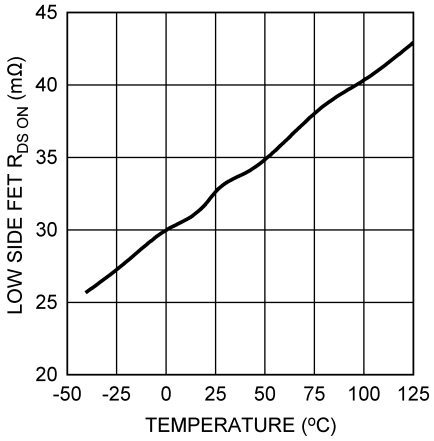


Figure 8. Low-Side FET Resistance vs Temperature

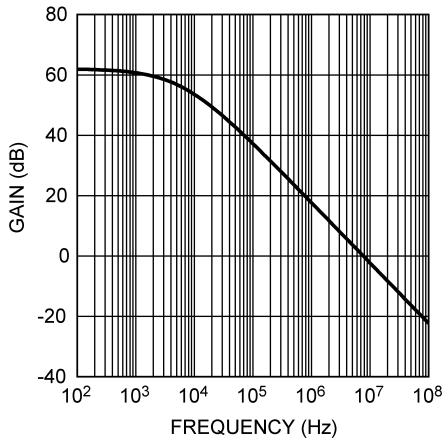


Figure 9. Error Amplifier Gain vs Frequency

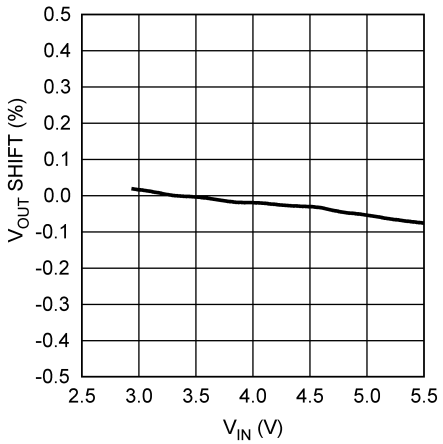


Figure 10. Line Regulation

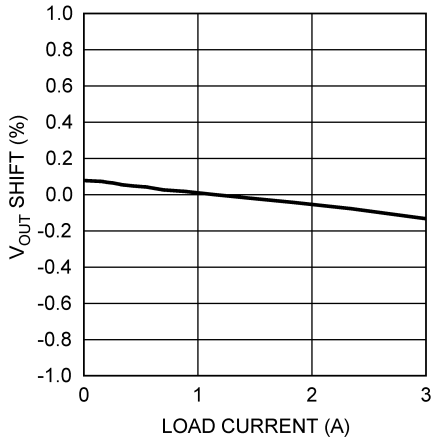


Figure 11. Load Regulation

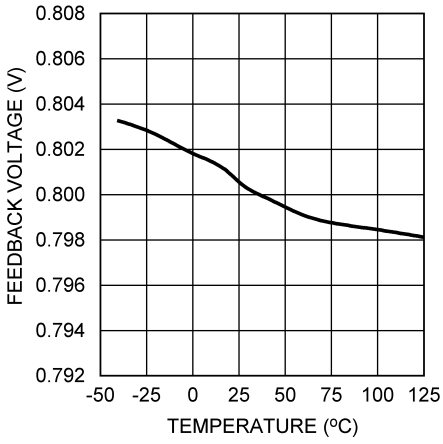


Figure 12. Feedback Pin Voltage vs Temperature

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = C_{OUT} = 100 µF, L = 1.0 µH, V_{IN} = 5 V, V_{OUT} = 1.2 V, R_{LOAD} = 1.2 Ω, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

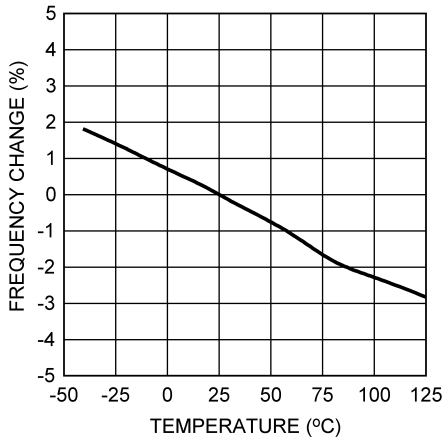


Figure 13. Switching Frequency vs Temperature

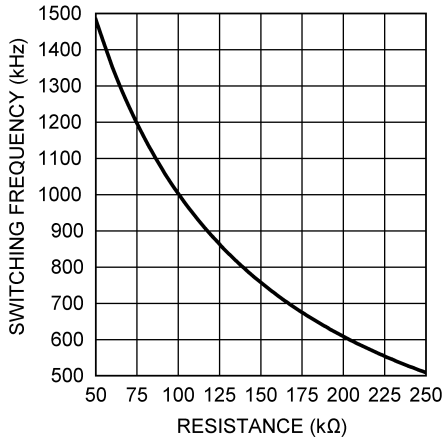


Figure 14. Switching Frequency vs R_T

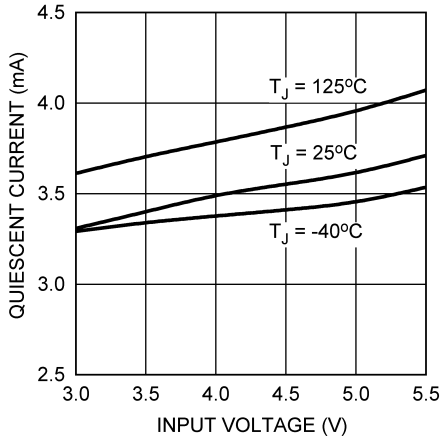


Figure 15. Quiescent Current vs V_{IN} (Not Switching)

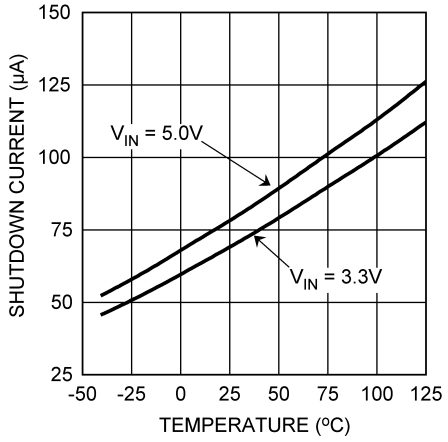


Figure 16. Shutdown Current vs Temperature

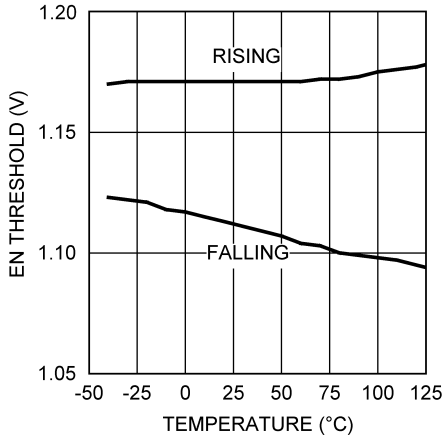


Figure 17. Enable Threshold vs Temperature

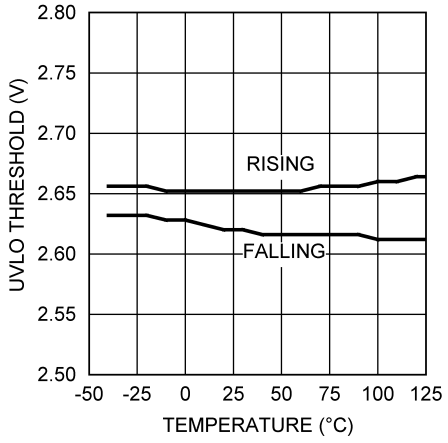


Figure 18. UVLO Threshold vs Temperature

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = C_{OUT} = 100 µF, L = 1.0 µH, V_{IN} = 5 V, V_{OUT} = 1.2 V, R_{LOAD} = 1.2 Ω, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

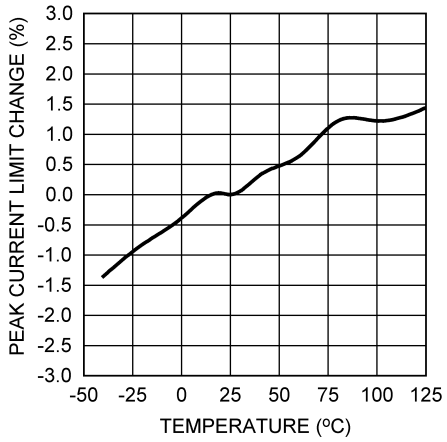


Figure 19. Peak Current Limit vs Temperature

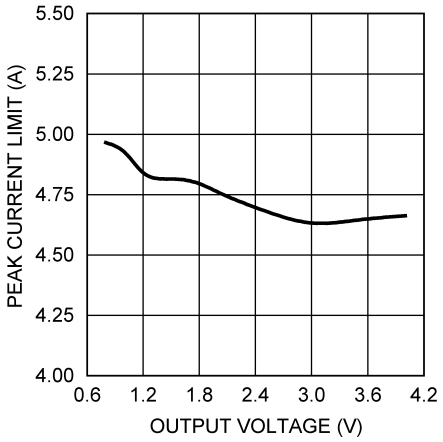


Figure 20. Peak Current Limit vs V_{OUT}

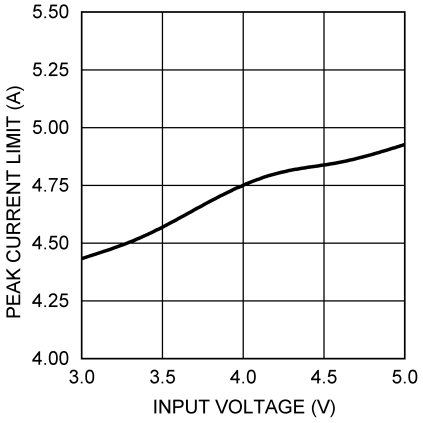


Figure 21. Peak Current Limit vs V_{IN}

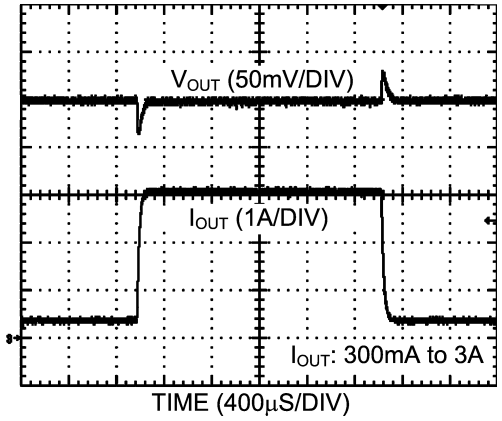


Figure 22. Load Transient Response

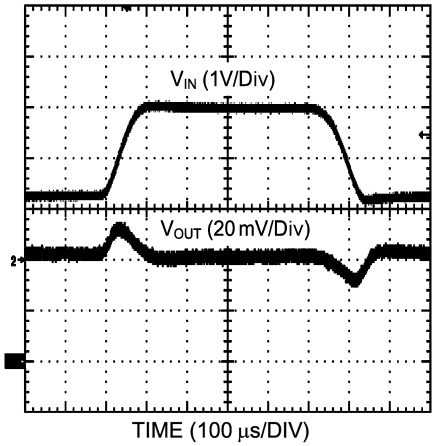


Figure 23. Line Transient Response

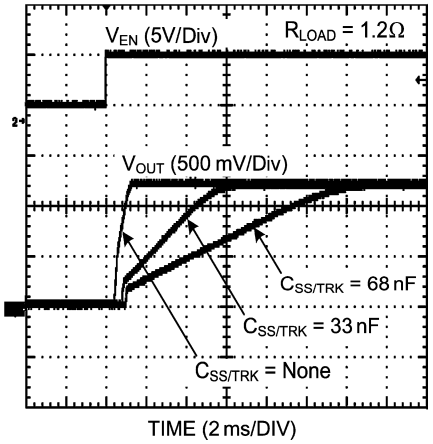


Figure 24. Start Up (Soft-Start)

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = C_{OUT} = 100 µF, L = 1.0 µH, V_{IN} = 5 V, V_{OUT} = 1.2 V, R_{LOAD} = 1.2 Ω, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

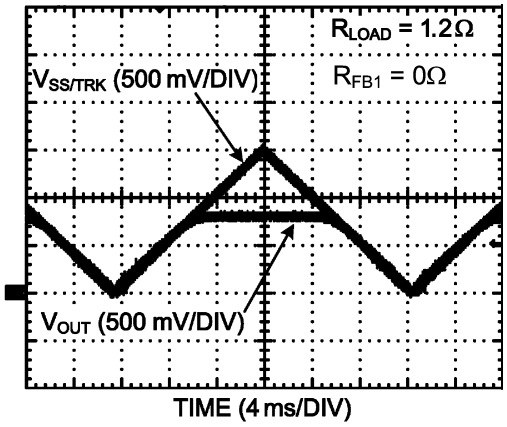


Figure 25. Start Up (Tracking)

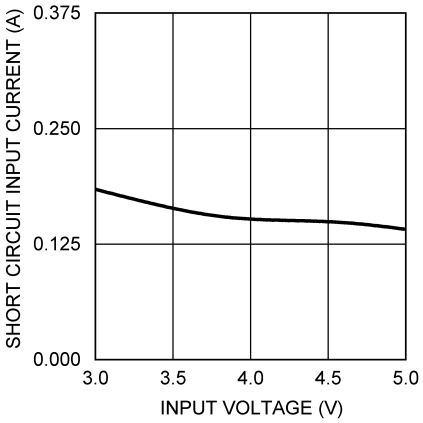


Figure 26. Short Circuit Input Current vs V_{IN}

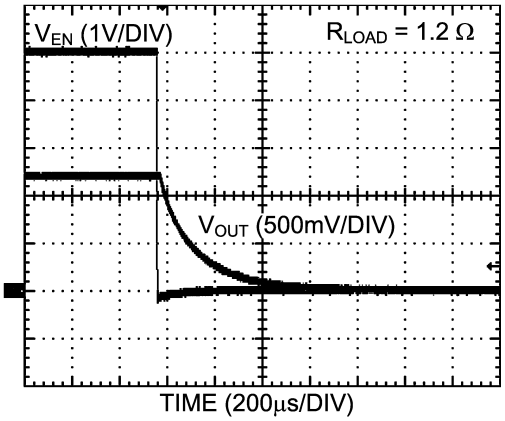


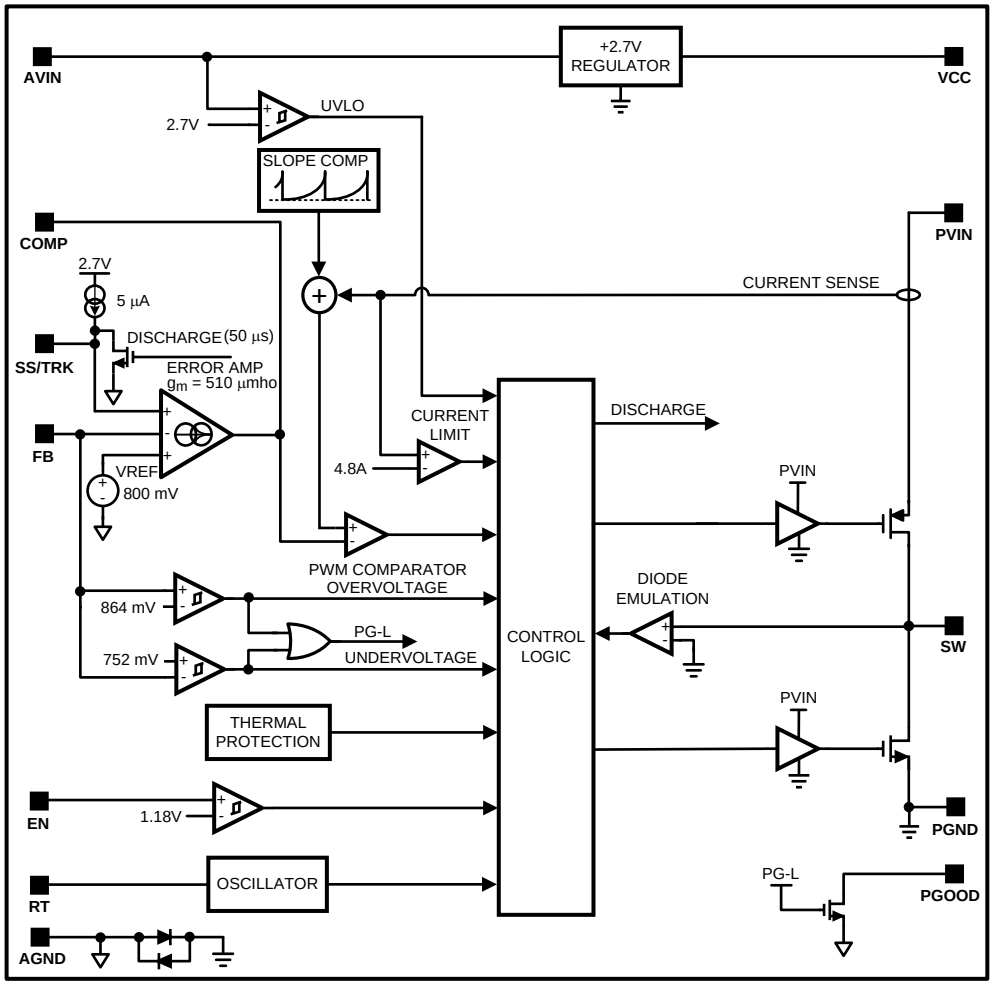
Figure 27. Power Down

7 Detailed Description

7.1 Overview

The LM20143 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy to use regulator features two integrated switches and is capable of supplying up to 3 A of continuous output current. The regulator utilizes peak current mode control with nonlinear slope compensation to optimize stability and transient response over the entire output voltage range. Peak current mode control also provides inherent line feed-forward, cycle-by-cycle current limiting and easy loop compensation. The switching frequency can be varied from 500 kHz to 1.5 MHz with an external resistor to ground. The device can operate at high switching frequency allowing use of a small inductor while still achieving efficiencies as high as 96%. The precision internal voltage reference allows the output to be set as low as 0.8 V. Fault protection features include: current limiting, thermal shutdown, over voltage protection, and shutdown capability. The device is available in the HTSSOP 16-pin package featuring an exposed pad to aid thermal dissipation. The LM20143 can be used in numerous applications to efficiently step-down from a 5 V or 3.3 V bus. The typical application circuit for the LM20143 is shown in Figure 32 in the design guide.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Peak Current Mode Control

In most cases, the peak current mode control architecture used in the LM20143 only requires two external components to achieve a stable design. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device.

For duty cycles above 50% all current mode control buck converters require the addition of an artificial ramp to avoid sub-harmonic oscillation. This artificial linear ramp is commonly referred to as slope compensation. What makes the LM20143 unique is the amount of slope compensation will change depending on the output voltage. When operating at high output voltages the device will have more slope compensation than when operating at lower output voltages. This is accomplished in the LM20143 by using a non-linear parabolic ramp for the slope compensation. The parabolic slope compensation of the LM20143 is much better than the traditional linear slope compensation because it optimizes the stability of the device over the entire output voltage range.

7.3.2 Precision Enable

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.2 V (typical). The EN pin has 100 mV of hysteresis and will disable the output when the enable voltage falls below 1.1 V (typical). If the EN pin is not used, it should be connected to VIN. Since the enable pin has a precise turn-on threshold it can be used along with an external resistor divider network from V_{IN} to configure the device to turn-on at a precise input voltage. The precision enable circuitry will remain active even when the device is disabled.

7.3.3 Current Limit

The precise current limit of the LM20143 is set at the factory to be within 10% over the entire operating temperature range. This enables the device to operate with smaller inductors that have lower saturation currents. When the peak inductor current reaches the current limit threshold, an over current event is triggered and the internal high-side FET turns off and the low-side FET turns on allowing the inductor current to ramp down until the next switching cycle. For each sequential over-current event, the reference voltage is decremented and PWM pulses are skipped resulting in a current limit that does not aggressively fold back for brief over-current events, while at the same time providing frequency and voltage foldback protection during hard short circuit conditions.

7.3.4 Pre-Bias Start Up Capability

The LM20143 is in a pre-biased state when the device starts up with an output voltage greater than zero. This often occurs in many multi-rail applications such as when powering an FPGA, ASIC, or DSP. In these applications the output can be pre-biased through parasitic conduction paths from one supply rail to another. Even though the LM20143 is a synchronous converter it will not pull the output low when a pre-bias condition exists. During start up the LM20143 will not sink current until the Soft-Start voltage exceeds the voltage on the FB pin. Since the device can not sink current it protects the load from damage that might otherwise occur if current is conducted through the parasitic paths of the load.

7.3.5 Soft-Start and Voltage Tracking

The SS/TRK pin is a dual function pin that can be used to set the start up time or track an external voltage source. The start up or Soft-Start time can be adjusted by connecting a capacitor from the SS/TRK pin to ground. The Soft-Start feature allows the regulator output to gradually reach the steady state operating point, thus reducing stresses on the input supply and controlling start up current. If no Soft-Start capacitor is used the device defaults to the internal Soft-Start circuitry resulting in a start up time of approximately 1 ms. For applications that require a monotonic start up or utilize the PGOOD pin, an external Soft-Start capacitor is recommended. The SS/TRK pin can also be set to track an external voltage source. The tracking behavior can be adjusted by two external resistors connected to the SS/TRK pin as shown in Figure 29.

Feature Description (continued)

7.3.6 Power Good and Overvoltage Fault Handling

The LM20143 has built in under and over voltage comparators that control the power switches. Whenever there is an excursion in output voltage above the set OVP threshold, the part will terminate the present on-pulse, turn-on the low-side FET, and pull the PGOOD pin low. The low-side FET will remain on until either the FB voltage falls back into regulation or the zero cross detection is triggered which in turn tri-states the FETs. If the output reaches the UVP threshold the part will continue switching and the PGOOD pin will be asserted and go low. Typical values for the PGOOD resistor are on the order of 100 kΩ or less. To avoid false tripping during transient glitches the PGOOD pin has 16 µs of built in deglitch time to both rising and falling edges.

7.3.7 UVLO

The LM20143 has a built-in under-voltage lockout protection circuit that keeps the device from switching until the input voltage reaches 2.7 V (typical). The UVLO threshold has 45 mV of hysteresis that keeps the device from responding to power-on glitches during start up. If desired the turn-on point of the supply can be changed by using the precision enable pin and a resistor divider network connected to V_{IN} as shown in Figure 31. in the design guide.

7.3.8 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the LM20143 tri-states the power FETs and resets soft start. After the junction cools to approximately 150°C, the part starts up using the normal start up routine. This feature is provided to prevent catastrophic failures from accidental device overheating.

7.4 Device Functional Modes

7.4.1 Light Load Operation

The LM20143 offers increased efficiency when operating at light loads. Whenever the load current is reduced to a point where the peak to peak inductor ripple current is greater than two times the load current, the part will enter the diode emulation mode preventing significant negative inductor current. The point at which this occurs is the critical conduction boundary and can be calculated by Equation 1

$$I_{BOUNDARY} = \frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f_{SW}} \quad (1)$$

Several diagrams are shown in Figure 28 illustrating continuous conduction mode (CCM), discontinuous conduction mode, and the boundary condition.

It can be seen that in diode emulation mode, whenever the inductor current reaches zero the SW node will become high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the parasitic capacitance at the node. If this ringing is of concern an additional RC snubber circuit can be added from the switch node to ground.

At very light loads, usually below 100 mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

Device Functional Modes (continued)

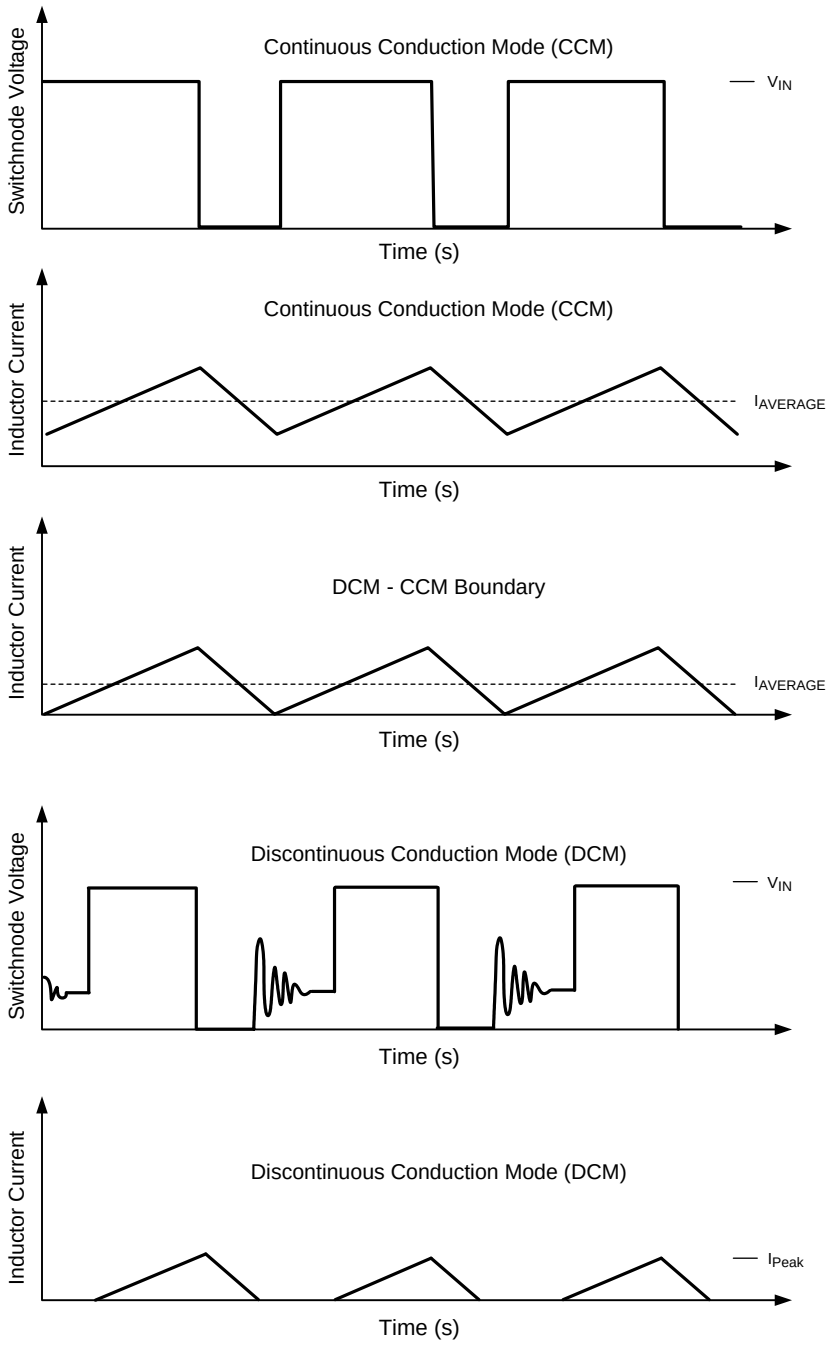


Figure 28. Modes of Operation for LM20143

Device Functional Modes (continued)

7.4.2 Tracking an External Supply

By using a properly chosen resistor divider network connected to the SS/TRK pin, as shown in Figure 29, the output of the LM20143 can be configured to track an external voltage source to obtain a simultaneous or ratiometric start up.

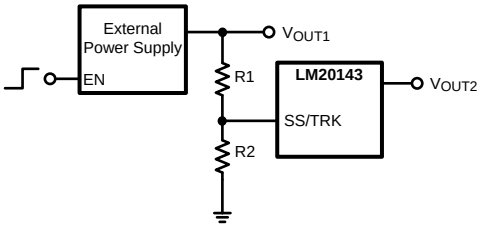


Figure 29. Tracking an External Supply

Since the Soft-Start charging current I_{SS} is always present on the SS/TRK pin, the size of R2 should be less than 10 kΩ to minimize the errors in the tracking output. Once a value for R2 is selected the value for R1 can be calculated using appropriate equation in Figure 30, to give the desired start up. Figure 30 shows two common start up sequences; the top waveform shows a simultaneous start up while the waveform at the bottom illustrates a ratiometric start up.

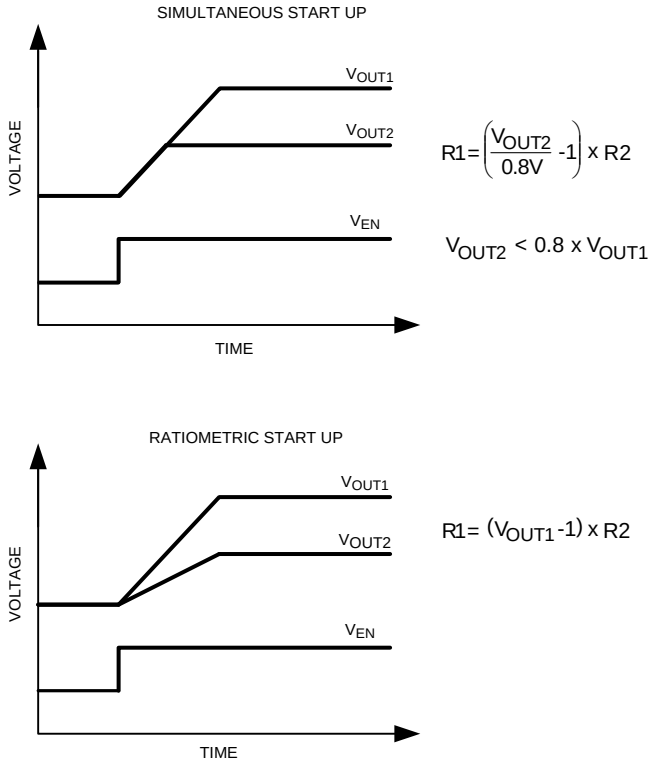


Figure 30. Common Start Up Sequences

A simultaneous start up is preferred when powering most FPGAs, DSPs, or other microprocessors. In these systems the higher voltage, V_{OUT1}, usually powers the I/O, and the lower voltage, V_{OUT2}, powers the core. A simultaneous start up provides a more robust power up for these applications since it avoids turning on any parasitic conduction paths that may exist between the core and the I/O pins of the processor.

Device Functional Modes (continued)

The second most common power on behavior is known as a ratiometric start up. This start up is preferred in applications where both supplies need to be at the final value at the same time.

Similar to the Soft-Start function, the fastest start up possible is 1ms regardless of the rise time of the tracking voltage. When using the track feature the final voltage seen by the SS/TRACK pin should exceed 1V to provide sufficient overdrive and transient immunity.

7.4.3 Using Precision Enable and Power Good

The precision enable (EN) and power good (PGOOD) pins of the LM20143 can be used to address many sequencing requirements. The turn-on of the LM20143 can be controlled with the precision enable pin by using two external resistors as shown in Figure 31.

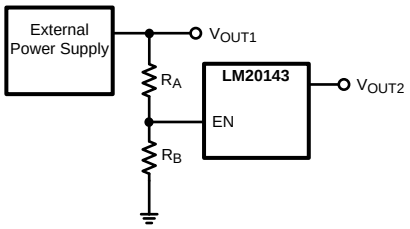


Figure 31. Sequencing LM20143 with Precision Enable

The value for resistor R_B can be selected by the user to control the current through the divider. Typically this resistor will be selected to be between 10 kΩ and 1 MΩ. Once the value for R_B is chosen the resistor R_A can be solved using Equation 2 to set the desired turn-on voltage.

$$R_A = \left(\frac{V_{TO}}{V_{IH\_EN}} - 1 \right) \times R_B \tag{2}$$

When designing for a specific turn-on threshold (V_{TO}) the tolerance on the input supply, enable threshold (V_{IH_EN}), and external resistors needs to be considered to insure proper turn-on of the device.

The LM20143 features an open drain power good (PGOOD) pin to sequence external supplies or loads and to provide fault detection. This pin requires an external resistor (R_{PG}) to pull PGOOD high while when the output is within the PGOOD tolerance window. Typical values for this resistor range from 10 kΩ to 100 kΩ.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM20143 is a step down DC/DC converter, typically used for to convert 3.3 V or 5 V rail to lower DC voltages with a maximum output current of 3 A. The following design procedure can be used to select all the external components for the LM20143. Alternately, the WEBENCH® Design Tool may be used to complete the design. By using this tool the user can optimize the design by using an iterative design procedure and selecting different components from the extensive component database. Along with this datasheet and WEBENCH, the user can reference the LM20143 Quickstart Calculator tool as a free download. The Quickstart tool is an excel sheet summary of the *Typical Applications* section.

8.2 Typical Applications

Several circuit designs can be created for applications with differing requirements. Three examples demonstrating this are detailed in this section.

8.2.1 3.3-V or 5-V Supply Rail Design

This section walks the designer through the steps necessary to select the external components to build a fully functional power supply. As with any DC-DC converter numerous trade-offs are possible to optimize the design for efficiency, size, or performance. These will be taken into account and highlighted throughout this section. The circuit shown in Figure 32 may be used as a reference to facilitate component selection. Unless otherwise indicated all formulas assume units of amps (A) for current, farads (F) for capacitance, henries (H) for inductance and volts (V) for voltages.

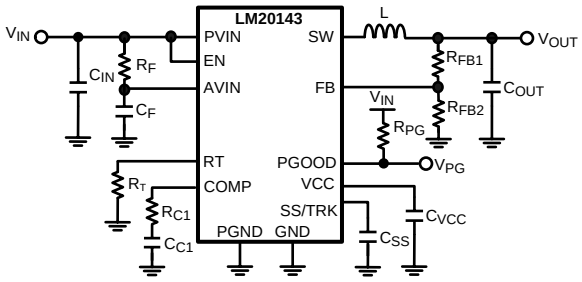


Figure 32. Typical Application Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.3 V to 5 V
Output voltage	1.2 V
Operating frequency	1.5 MHz
Output current rating	3 A

8.2.1.2 Detailed Design Procedure

Table 2 lists components chosen for a circuit design with the listed specifications. The example calculations in this section will use values representative of this circuit design.

Table 2. Bill of Materials

Designator	Description	Part Number	Manufacturer	Qty
U1	Synchronous Buck Regulator	LM20143	Texas Instruments	1
C_{IN}	47 µF, 1210, X5R, 6.3 V	GRM32ER60J476ME20	Murata	1
C_{OUT}	47 µF, 1210, X5R, 6.3 V	GRM32ER60J476ME20	Murata	1
L	1.2 µH, 17 mΩ	DO1813H-122ML	Coilcraft	1
R_{PG}	10 kΩ, 0603	CRCW06031002F-e3	Vishay-Dale	1
R_F	1 Ω, 0603	CRCW06031R0J-e3	Vishay-Dale	1
C_F	100 nF, 0603, X7R, 16 V	GRM188R71C104KA01	Murata	1
C_{VCC}	1 µF, 0603, X5R, 6.3 V	GRM188R60J105KA01	Murata	1
R_{C1}	1 kΩ, 0603	CRCW06031001F-e3	Vishay-Dale	1
C_{C1}	4.7 nF, 0603, X7R, 25 V	VJ0603Y472KXXA	Vishay-Vitramon	1
C_{SS}	33 nF, 0603, X7R, 25 V	VJ0603Y333KXXA	Vishay-Vitramon	1
R_T	49.9 kΩ, 0603	CRCW06034992F-e3	Vishay-Dale	1
R_{FB1}	4.99 kΩ, 0603	CRCW06034991F-e3	Vishay-Dale	1
R_{FB2}	10 kΩ, 0603	CRCW06031002F-e3	Vishay-Dale	1

8.2.1.2.1 Duty Cycle Calculation

The first equation to calculate for any buck converter is duty-cycle. Ignoring conduction losses associated with the FETs and parasitic resistances it can be approximated with Equation 3.

$$D = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

The example design the typical duty cycle is calculated to be 66%.

8.2.1.2.2 Inductor Selection (L)

The inductor value is determined based on the operating frequency, load current, ripple current, and duty cycle. To optimize the performance and prevent the device from entering current limit at maximum load, the inductance is typically selected such that the ripple current, ΔiL, is between 25% and 50% of the rated output current. In general, the inductor ripple current, Δi_L, should be greater than 10% of the rated output current to provide adequate current sense information for the current mode control loop. Figure 33 illustrates the switch and inductor ripple current waveforms. Once the input voltage, output voltage, operating frequency, and desired ripple current are known, the minimum value for the inductor can be calculated with Equation 4.

$$\frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot 0.5 \cdot I_{OUT(max)}} \leq L \leq \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot 0.25 \cdot I_{OUT(max)}} \tag{4}$$

For the example design the calculated inductance is between .405 µH and 0.810 µH.

The inductor selected should have a saturation current rating greater than the peak current limit of the device listed in the *Electrical Characteristics* table. Keep in mind the specified current limit does not account for delay of the current limit comparator, therefore the current limit in the application may be higher than the specified value. Peak current can be calculated using Equation 5. This value needs to be less than the part current limit threshold. If needed, slightly smaller value inductors can be used, however, the peak inductor current should be kept below the peak current limit of the device.

$$I_{L(max)} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \cdot D}{L \cdot f_{SW}} \tag{5}$$

For the example design the peak inductor current is between 4.563 A and 6.125 A for the selected inductor ripple current range.

Due to exceeding current limit and adding flexibility to accommodate the entire output voltage range a inductance of 1.2 µH was selected, resulting in a peak inductor current of 4.056 A.

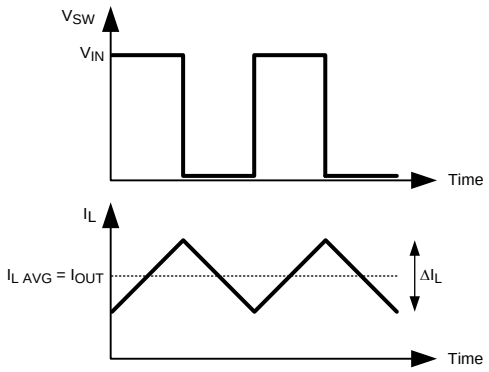


Figure 33. Switch and Inductor Current Waveforms

8.2.1.2.3 Output Capacitor Selection (C_{OUT})

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM20143 that provide excellent performance. The best performance is typically obtained using ceramic, SP, or OSCON type chemistries. Typical trade-offs are that the ceramic capacitor provides extremely low ESR to reduce the output ripple voltage and noise spikes, while the SP and OSCON capacitors provide a large bulk capacitance in a small volume for transient loading conditions.

When selecting the value for the output capacitor the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated by using Equation 6.

$$\Delta V_{OUT} = \Delta i_L \times \left[R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

where

- ΔV_{OUT} (V) is the amount of peak to peak voltage ripple at the power supply output
- R_{ESR} (Ω) is the series resistance of the output capacitor
- f_{SW}(Hz) is the switching frequency
- C_{OUT} (F) is the output capacitance used in the design (6)

The amount of output ripple that can be tolerated is application specific; however a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Keep in mind ceramic capacitors are sometimes preferred because they have very low ESR; however, depending on package and voltage rating of the capacitor the value of the capacitance can drop significantly with applied voltage. The output capacitor selection will also affect the output voltage droop during a load transient. The peak droop on the output voltage during a load transient is dependent on many factors; however, an approximation of the transient droop ignoring loop bandwidth can be obtained using Equation 7. Both the tolerance and voltage coefficient of the capacitor needs to be examined when designing for a specific output ripple or transient drop target.

$$V_{DROOP} = \Delta I_{OUTSTEP} \times R_{ESR} + \frac{L \times \Delta I_{OUTSTEP}^2}{C_{OUT} \times (V_{IN} - V_{OUT})}$$

where

- C_{OUT} (F) is the minimum required output capacitance
- L (H) is the value of the inductor
- V_{DROOP} (V) is the output voltage drop ignoring loop bandwidth considerations
- $\Delta I_{OUTSTEP}$ (A) is the load step change
- R_{ESR} (Ω) is the output capacitor ESR
- V_{IN} (V) is the input voltage
- V_{OUT} (V) is the set regulator output voltage (7)

For the example design, a 47-µF ceramic capacitor is selected for the output capacitor to provide good transient and DC performance in a relatively small package. From the technical specifications of this capacitor, the ESR is roughly 3 mΩ, and the effective in-circuit capacitance is approximately 32 µF (reduced from 47 µF due to the 1.2 V DC bias). With these values, the peak-to-peak voltage ripple on the output when operating from a 5-V input can be calculated to be 3 mV. A load transient from 1.5 A to 3 A is calculated to create a 27-mV droop.

8.2.1.2.4 Input Capacitor Selection (C_{IN})

Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. In general it is recommended to use a ceramic capacitor for the input as they provide both a low impedance and small footprint. One important note is to use a good dielectric for the ceramic capacitor such as X5R or X7R. These provide better over temperature performance and also minimize the DC voltage derating that occurs on Y5V capacitors. For most applications, a 22-µF, X5R, 6.3-V input capacitor is sufficient; however, additional capacitance may be required if the connection to the input supply is far from the PVIN pins. The input capacitor should be placed as close as possible PVIN and PGND pins of the device.

Non-ceramic input capacitors should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating is given by Equation 8.

$$I_{IN\text{-}RMS} = I_{OUT} \sqrt{D(1 - D)} \tag{8}$$

As indicated by the RMS ripple current equation, highest requirement for RMS current rating occurs at 50% duty cycle. For this case, the RMS ripple current rating of the input capacitor should be greater than half the output current. For best performance, low ESR ceramic capacitors should be placed in parallel with higher capacitance capacitors to provide the best input filtering for the device.

For the example design the rated RMS current must be at least 1.5 A. A 47-µF ceramic capacitor provides the necessary input capacitance for the evaluation board. For improved bypassing, a small 1-µF high frequency capacitor is placed in parallel with the 47-µF bulk capacitor to filter high frequency noise pulses on the supply.

8.2.1.2.5 Setting the Output Voltage (R_{FB1}, R_{FB2})

The resistors R_{FB1} and R_{FB2} are selected to set the output voltage for the device. For most applications, R_{FB1} should be between 4.99 kΩ to 49.9 kΩ.

$$R_{FB1} = \left(\frac{V_{OUT}}{0.8} - 1 \right) \times R_{FB2} \tag{9}$$

For the example design R_{FB1} = 4 kΩ and R_{FB2} = 10 kΩ to set the output voltage at 1.2 V.

Table 3 contains common output voltage values for R_{FB1} and R_{FB2}.

Table 3. Suggested Values for R_{FB1} and R_{FB2}

R_{FB1}(kΩ)	R_{FB2}(kΩ)	V_{OUT}
short	open	0.8
4.99	10	1.2
8.87	10.2	1.5
12.7	10.2	1.8
21.5	10.2	2.5
31.6	10.2	3.3

8.2.1.2.6 Adjusting the Operating Frequency (R_T)

The LM20143 supports a wide range of switching frequencies from 500 kHz to 1.5 MHz. The operating frequency of the LM20143 can be adjusted by connecting a resistor from the RT pin to ground. The choice of switching frequency is usually a compromise between efficiency and the size of the circuit. Lower switching frequency implies reduced switching losses, usually resulting in higher overall efficiency. However, higher switching frequency allows use of smaller inductor and output capacitor components, resulting in a smaller design. The optimal switching frequency is usually a tradeoff in a given application and thus should be determined on a case-by-case basis. For the design example a relatively high switching frequency was selected to minimize circuit size. Equation 10 can be used to calculate the value of R_T for a given operating frequency.

$$R_T = \left(\frac{154750}{f_{SW}}\right) - 55 \quad (10)$$

where

- f_{SW} is the switching frequency in kHz
- R_T is the frequency adjust resistor in kΩ

Please refer to the curve Oscillator Frequency verses R_T in the typical performance characteristics section. If the R_T resistor is omitted the device will not operate.

For the example design RT was calculated to be 49.9 kΩ to give a switching frequency of 1.5 MHz.

8.2.1.2.7 AVIN Filtering Components (C_F and R_F)

To prevent high frequency noise spikes from disturbing the sensitive analog circuitry connected to the AVIN and AGND pins, a high frequency RC filter is required between PVIN and AVIN. These components are shown in Figure 32 as C_F and R_F. The required value for R_F is 1 Ω. C_F must be used. Recommended value of C_F is 1.0 µF. The filter capacitor, C_F should be placed as close to the IC as possible with a direct connection from AVIN to AGND. A good quality X5R or X7R ceramic capacitor should be used for C_F.

For the example design, R_F 1 Ω and C_F is 1.0 µF, providing greater than 16 dB of attenuation at the set 1.5-MHz switching frequency.

8.2.1.2.8 Sub-Regulator Bypass Capacitor (C_{VCC})

The capacitor at the VCC pin provides noise filtering and stability for the internal sub-regulator. The recommended value of C_{VCC} should be no smaller than 1 µF and no greater than 10 µF. The capacitor should be a good quality ceramic X5R or X7R capacitor. In general, a 1-µF ceramic capacitor is recommended for most applications. In the example design, C_{VCC} is 1 µF.

8.2.1.2.9 Setting the Start Up Time (C_{SS})

The addition of a capacitor connected from the SS pin to ground sets the time at which the output voltage will reach the final regulated value. Larger values for CSS will result in longer start up times. While the Soft-Start capacitor can be sized to meet many start up requirements, there are limitations to its size. The Soft-Start time can never be faster than 1 ms due to the internal default 1-ms start up time. When the device is enabled there is an approximate time interval of 50 µs when the Soft-Start capacitor will be discharged just prior to the Soft-Start ramp. If the enable pin is rapidly pulsed or the Soft-Start capacitor is large there may not be enough time for CSS to completely discharge resulting in start up times less than predicted. To aid in discharging of Soft-Start capacitor during long disable periods an external 1-MΩ resistor from SS/TRK to ground can be used without greatly affecting the start up time. Equation 11 can be used to calculate the desired soft start time. For the LM20143, I_{SS} is nominally 5 µA, that may be found in the electrical characteristics table.

$$t_{SS} = \frac{0.8V \cdot C_{SS}}{I_{SS}} \quad (11)$$

For the example design the start-up time was set to be around 5ms resulting in a 33 nF capacitor.

Table 4 shows values of C_{SS} for some common start up times.

Table 4. Start Up Times for Different Soft-Start Capacitors

Start Up Time (ms)	C_{SS} (nF)
1	none
5	33
10	68
15	100
20	120

8.2.1.2.10 Loop Compensation (R_{C1}, C_{C1})

The purpose of loop compensation is to meet static and dynamic performance requirements while maintaining adequate stability. Optimal loop compensation depends on the output capacitor, inductor, load, and the device itself. Table 5 gives values for the compensation network that will result in a stable system when using a 100-µF, 6.3-V ceramic X5R output capacitor and 1-µH inductor.

Table 5. Recommended Compensation for C_{OUT} = 100 µF, L = 1 µH & f_{SW} = 1 MHz

V_{IN}	V_{OUT}	C_{C1} (nF)	R_{C1} (kΩ)
5.00	3.30	4.7	17.8
5.00	2.50	4.7	12.1
5.00	1.80	4.7	7.68
5.00	1.50	4.7	5.9
5.00	1.20	4.7	3.57
5.00	0.80	4.7	1.58
3.30	2.50	4.7	13
3.30	1.80	4.7	9.76
3.30	1.50	4.7	6.49
3.30	1.20	4.7	4.64
3.30	0.80	4.7	1.58

If the desired solution differs from those provided, the loop transfer function should be analyzed to optimize the loop compensation. The overall loop transfer function is the product of the power stage and the feedback network transfer functions. For stability purposes, the objective is to have a loop gain slope that is –20 db/decade from a very low frequency to beyond the crossover frequency. Figure 34 shows the transfer functions for power stage, feedback/compensation network, and the resulting closed loop system for the LM20143.

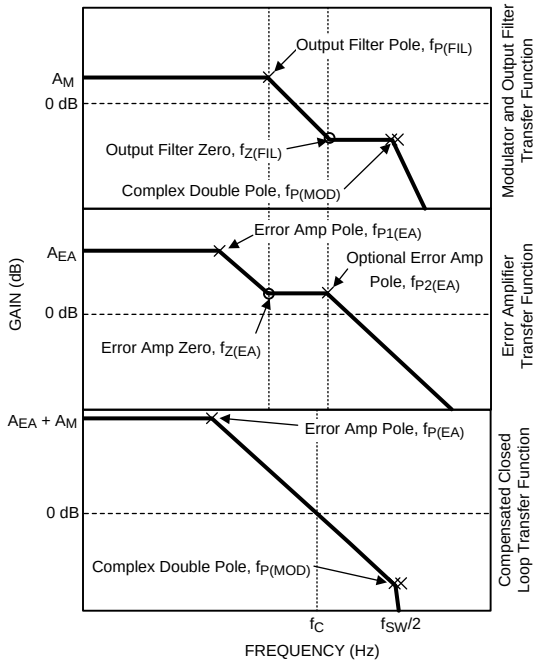


Figure 34. LM20143 Loop Compensation

The power stage transfer function is dictated by the modulator, output LC filter, and load; while the feedback transfer function is set by the feedback resistor ratio, error amp gain, and external compensation network.

To achieve a –20 dB/decade slope, the error amplifier zero, located at $f_{Z(EA)}$, should positioned to cancel the output filter pole ($f_{P(FIL)}$). An additional error amp pole, located at $f_{P2(EA)}$, can be added to cancel the output filter zero at $f_{Z(FIL)}$. Cancellation of the output filter zero is recommended if larger value, non-ceramic output capacitors are used.

Compensation of the LM20143 is achieved by adding an RC network as shown in Figure 35.

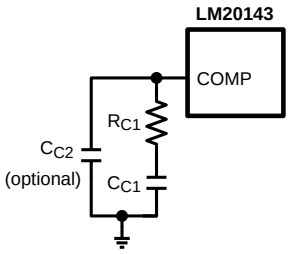


Figure 35. Compensation Network for LM20143

A good starting value for C_{C1} for most applications is 4.7 nF. Once the value of C_{C1} is chosen the value of RC should be calculated using Equation 12 to cancel the output filter pole ($f_{P(FIL)}$) as shown in Figure 34.

$$R_{C1} = \left[\frac{C_{C1}}{C_{OUT}} \times \left[\frac{I_{OUT}}{V_{OUT}} + \frac{1\text{-}D}{f_{SW} \times L} + \frac{15 \times D}{V_{IN}} \right] \right]^{-1} \quad (12)$$

A higher crossover frequency can be obtained, usually at the expense of phase margin, by lowering the value of C_{C1} and recalculating the value of R_{C1}. Likewise, increasing C_{C1} and recalculating R_{C1} will provide additional phase margin at a lower crossover frequency. As with any attempt to compensate the LM20143 the stability of the system should be verified for desired transient droop and settling time.

If the output filter zero, $f_{Z(FIL)}$ approaches the crossover frequency (F_C), an additional capacitor (C_{C2}) should be placed at the COMP pin to ground. This capacitor adds a pole to cancel the output filter zero assuring the crossover frequency will occur before the double pole at f_{SW} / 2 degrades the phase margin. The output filter zero is set by the output capacitor value and ESR as shown in Equation 13.

$$f_{Z(FIL)} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{ESR}} \tag{13}$$

If needed, the value for C_{C2} should be calculated using Equation 14.

$$C_{C2} = \frac{C_{OUT} \times R_{ESR}}{R_{C1}} \tag{14}$$

where

- R_{ESR} is the output capacitor series resistance
- R_{C1} is the calculated compensation resistance

For the example design R_{C1} is 1 kΩ, C_{C1} is 4.7 nF and $C_{C2}$is left open.

8.2.1.3 Application Curves

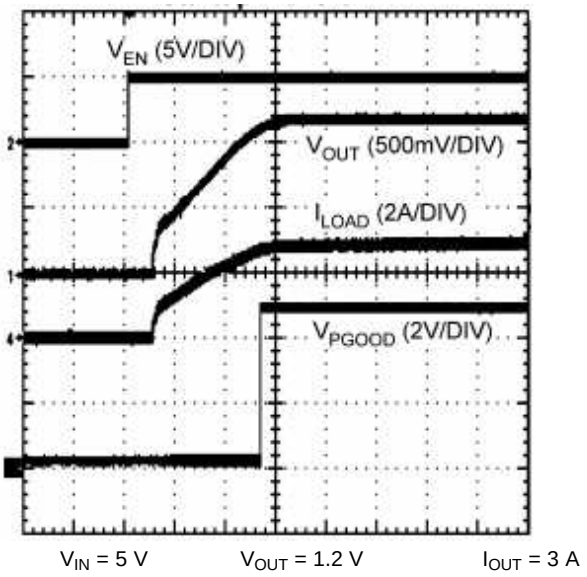


Figure 36. Startup

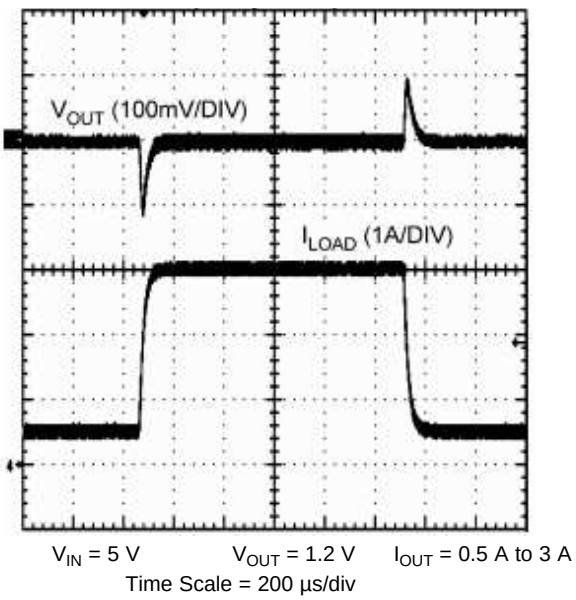


Figure 37. Load Transient

8.2.2 5-V Supply Rail Design

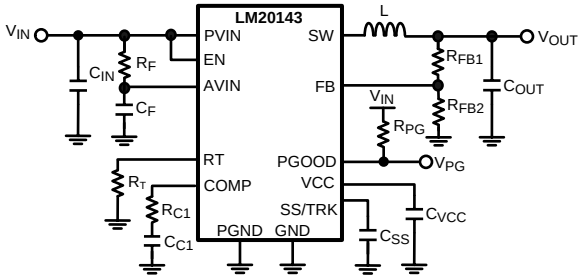


Figure 38. Typical Application Circuit

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 6 as the input parameters.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5 V
Output voltage	3.3 V
Operating frequency	750 kHz
Output current rating	3 A

8.2.2.2 Detailed Design Procedure

Table 7 lists a selection of components using the design procedure explained in *3.3-V or 5-V Supply Rail Design* for a circuit design with the listed specifications.

Table 7. Bill of Materials

Designator	Description	Part Number	Manufacturer	Qty
U1	Synchronous Buck Regulator	LM20143	Texas Instruments	1
C_{IN}	47 µF, 1210, X5R, 6.3 V	GRM32ER60J476ME20	Murata	1
C_{OUT}	100 µF, 1210, X5R, 6.3 V	GRM32ER60J107ME20	Murata	1
L	1.5 µH, 8.1 mΩ	MSS1038-152NL	Coilcraft	1
R_F	1 Ω, 0603	CRCW06031R0J-e3	Vishay-Dale	1
C_F	100 nF, 0603, X7R, 16 V	GRM188R71C104KA01	Murata	1
C_{VCC}	1 µF, 0603, X5R, 6.3 V	GRM188R60J105KA01	Murata	1
R_{C1}	10 kΩ, 0603	CRCW06031002F-e3	Vishay-Dale	1
C_{C1}	3.3 nF, 0603, X7R, 25 V	VJ0603Y332KXXA	Vishay-Vitramon	1
C_{SS}	33 nF, 0603, X7R, 25 V	VJ0603Y333KXXA	Vishay-Vitramon	1
R_T	150 kΩ, 0603	CRCW06031503F-e3	Vishay-Dale	1
R_{FB1}	31.6 kΩ, 0603	CRCW06033162F-e3	Vishay-Dale	1
R_{FB2}	10.2 kΩ, 0603	CRCW06031022F-e3	Vishay-Dale	1

8.2.3 3-V Supply Rail Design

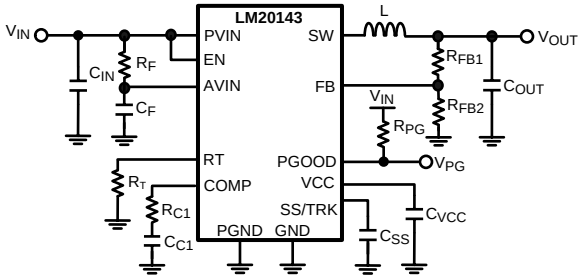


Figure 39. Typical Application Circuit

8.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 8 as the input parameters.

Table 8. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.3 V
Output voltage	1.2 V
Operating frequency	750 kHz
Output current rating	3 A

8.2.3.2 Detailed Design Procedure

Table 9 lists a selection of components using the design procedure explained in *3.3-V or 5-V Supply Rail Design* for a circuit design with the listed specifications.

Table 9. Bill of Materials

Designator	Description	Part Number	Manufacturer	Qty
U1	Synchronous Buck Regulator	LM20143	Texas Instruments	1
C_{IN}	47 µF, 1210, X5R, 6.3 V	GRM32ER60J476ME20	Murata	1
C_{OUT}	100 µF, 1210, X5R, 6.3 V	GRM32ER60J107ME20	Murata	1
L	1.2 µH, 17 mΩ	DO1813H-122ML	Coilcraft	1
R_F	1 Ω, 0603	CRCW06031R0J-e3	Vishay-Dale	1
C_F	100 nF, 0603, X7R, 16 V	GRM188R71C104KA01	Murata	1
C_{VCC}	1 µF, 0603, X5R, 6.3 V	GRM188R60J105KA01	Murata	1
R_{C1}	2 kΩ, 0603	CRCW06032001F-e3	Vishay-Dale	1
C_{C1}	4.7 nF, 0603, X7R, 25 V	VJ0603Y472KXXA	Vishay-Vitramon	1
C_{SS}	33 nF, 0603, X7R, 25 V	VJ0603Y333KXXA	Vishay-Vitramon	1
R_T	150 kΩ, 0603	CRCW06031503F-e3	Vishay-Dale	1
R_{FB1}	4.99 kΩ, 0603	CRCW06034991F-e3	Vishay-Dale	1
R_{FB2}	10 kΩ, 0603	CRCW06031002F-e3	Vishay-Dale	1

9 Power Supply Recommendations

The LM20143 converter is designed to operate from either a 3.3-V or 5-V rail. The input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. Further more the input supply must be able to supply the required average input current to the regulated load. The average input current can be estimated with Equation 15.

$$C_{C2} = \frac{C_{OUT} \times R_{ESR}}{R_{C1}}$$

where

- η is efficiency

(15)

If the regulator is connected to the input supply through long wires or PCB traces with large impedance, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables may have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit may cause overvoltage transients at the PVIN pin each time the input supply is cycled on and off. The parasitic resistance causes the PVIN voltage to dip when the load on the regulator is switched on or exhibits a transient. If the regulator is operating close to the minimum input voltage, this dip may cause false UVLO fault triggering and system reset. The best way to solve these types of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, an EMI input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is carefully designed. The user guide Simple Success with Conducted EMI for DC-DC Converters, SNVA489, provides helpful suggestions when designing an input filter for any switching regulator.

10 Layout

10.1 Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability.

Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched very fast. The first loop starts from the input capacitor, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the output capacitor and load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the inductor and then out to the load (see Figure 40). To minimize both loop areas the input capacitor should be placed as close as possible to the PVIN pin. Grounding for both the input and output capacitor should consist of a small localized top side plane that connects to PGND and the die attach pad (DAP). The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. Since the LM20143 has the SW pins on opposite sides of the package it is recommended to via these pins down to the bottom or internal layer with 2 to 4 vias on each SW pin. The SW pins should be directly connected with a trace that runs across the bottom of the package. To minimize IR losses this trace should be no smaller that 50 mils wide, but no larger than 100 mils wide to keep the copper area to a minimum. In general the SW pins should not be connected on the top layer since it could block the ground return path for the power ground. The inductor should be placed as close as possible to one of the SW pins to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds located under the DAP. The ground connections for the compensation, feedback, and Soft-Start components should be connected together then routed to the AGND pin of the device. The AGND pin should connect to PGND under the DAP. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled poor grounding can result in degraded load regulation or erratic switching behavior.

Layout Guidelines (continued)

4. Minimize trace length to the FB pin. Since the feedback node can be high impedance the trace from the output resistor divider to FB pin should be as short as possible. This is most important when high value resistors are used to set the output voltage. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.
6. Provide adequate device heatsinking. Use as many vias as is possible to connect the DAP to the power plane heatsink. For best results use a 4x4 via array with a minimum via diameter of 12 mils. See *Thermal Considerations* section to insure enough copper heatsinking area is used to keep the junction temperature below 125°C.

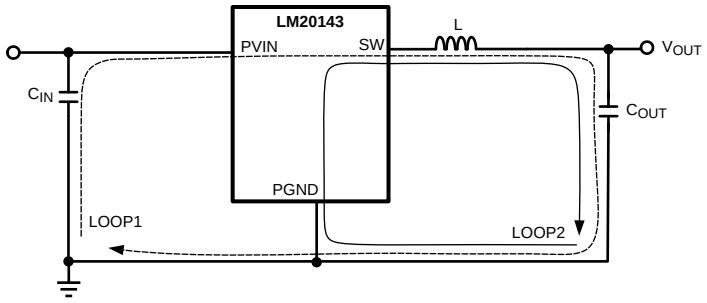


Figure 40. Schematic of LM20143 Highlighting Layout Sensitive Nodes

10.2 Layout Example

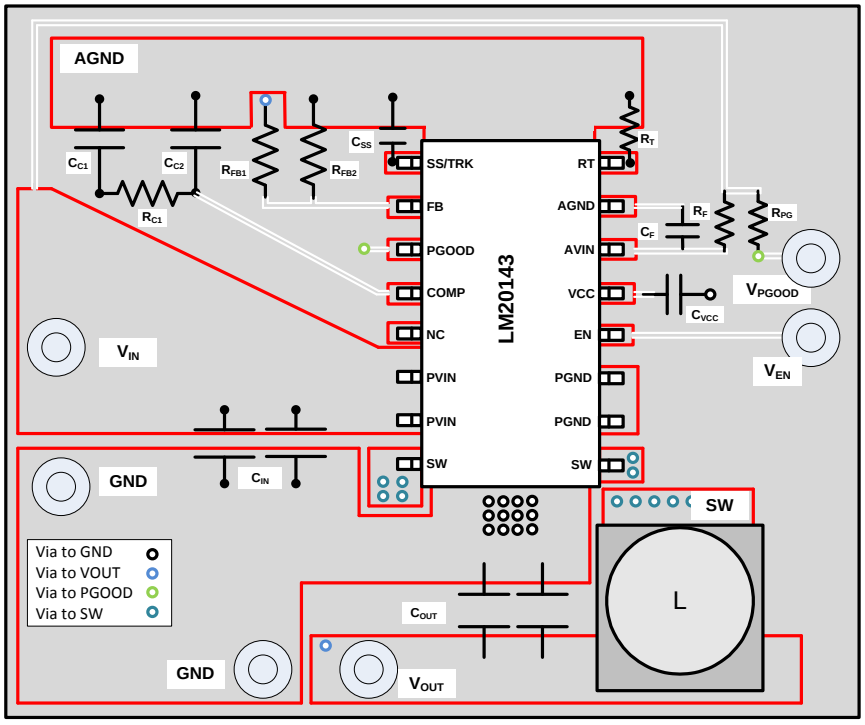


Figure 41. Example Layout

10.3 Thermal Considerations

The thermal characteristics of the LM20143 are specified using the parameter θ_{JA}, which relates the junction temperature to the ambient temperature. Although the value of θ_{JA} is dependant on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one may use Equation 16 and Equation 17.

$$T_J = P_D \theta_{JA} + T_A \quad (16)$$

$$P_D = P_{IN} \times (1 - \text{Efficiency}) - 1.1 \times I_{OUT}2 \times \text{DCR}$$

where

- T_J is the junction temperature in °C
- P_{IN} is the input power in Watts ($P_{IN} = V_{IN} \times I_{IN}$)
- θ_{JA} is the junction to ambient thermal resistance for the LM20143
- T_A is the ambient temperature in °C
- I_{OUT} is the output load current
- DCR is the inductor series resistance (17)

It is important to always keep the operating junction temperature (T_J) below 125°C for reliable operation. If the junction temperature exceeds 160°C the device will cycle in and out of thermal shutdown. If thermal shutdown occurs it is a sign of inadequate heatsinking or excessive power dissipation in the device.

Figure 42 provides a better approximation of the θ_{JA} for a given PCB copper area. The PCB heatsink area consists of 2 oz. copper located on the bottom layer of the PCB directly under the HTSSOP exposed pad. The bottom copper area is connected to the HTSSOP exposed pad by means of a 4 x 4 array of 12 mil thermal vias.

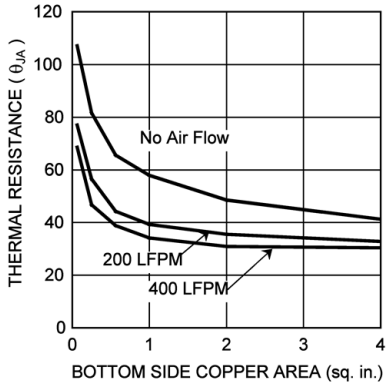


Figure 42. Thermal Resistance vs PCB Area

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

LM20143 Quickstart Design Tool, http://www.ti.com/tool/lm20143design-calc

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- AN-1691 LM20143 Evaluation Board, SNVA277
- AN-2162: Simple Success with Conducted EMI from DC-DC Converters, SNVA489

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM20143	Click here	Click here	Click here	Click here	Click here
LM20143-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

PowerWise is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM20143MH/NOPB	ACTIVE	HTSSOP	PWP	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	20143 MH	Samples
LM20143MHE/NOPB	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	20143 MH	Samples
LM20143MHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	20143 MH	Samples
LM20143QMH/NOPB	ACTIVE	HTSSOP	PWP	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	20143 QMH	Samples
LM20143QMHE/NOPB	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	20143 QMH	Samples
LM20143QMHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	20143 QMH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM20143, LM20143-Q1 :

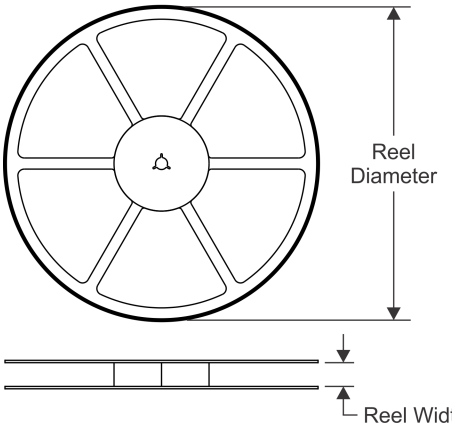
- Catalog: LM20143
- Automotive: LM20143-Q1

NOTE: Qualified Version Definitions:

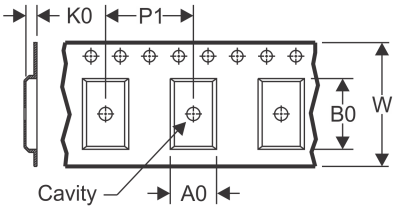
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

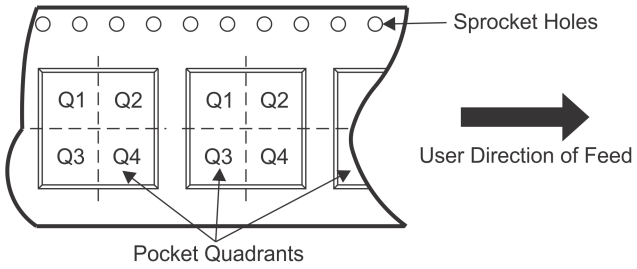


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

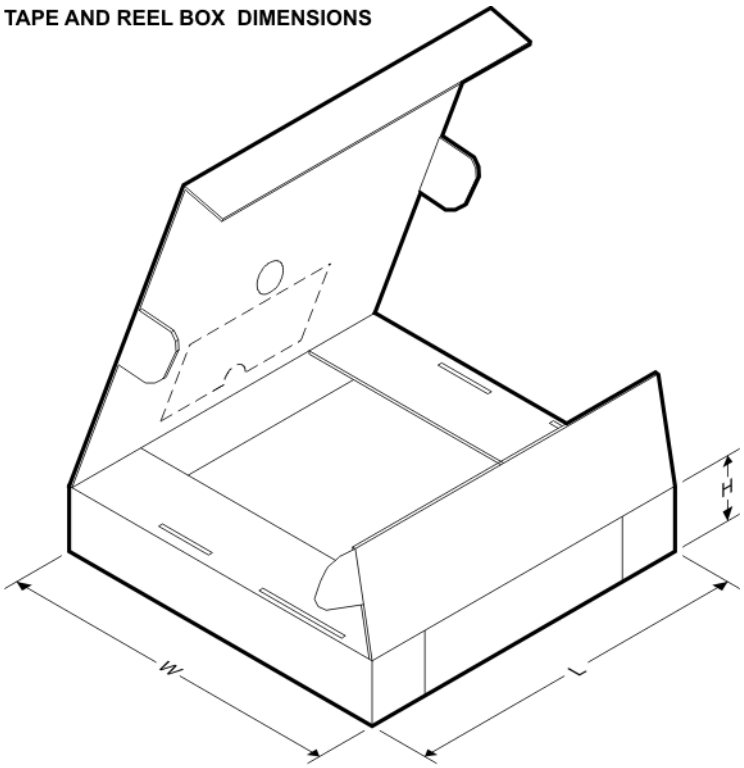
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM20143MHE/NOPB	HTSSOP	PWP	16	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM20143MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM20143QMHE/NOPB	HTSSOP	PWP	16	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM20143QMHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

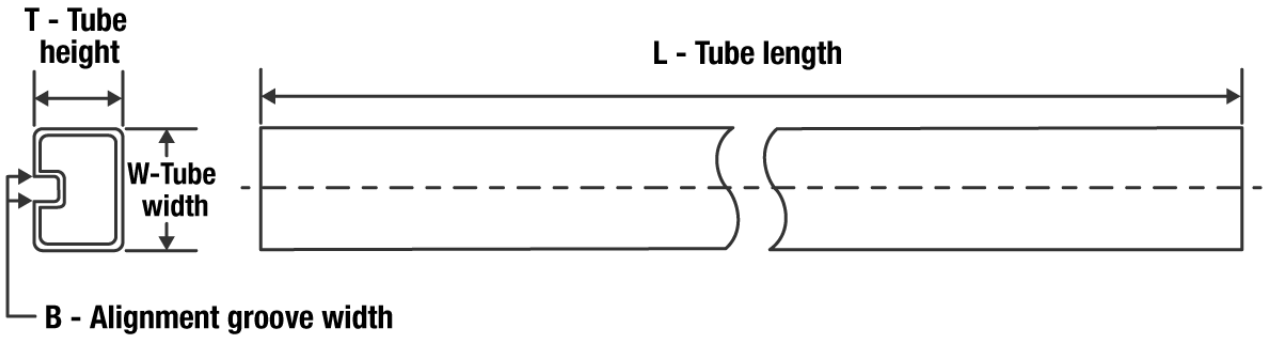
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

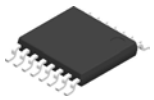
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM20143MHE/NOPB	HTSSOP	PWP	16	250	210.0	185.0	35.0
LM20143MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM20143QMHE/NOPB	HTSSOP	PWP	16	250	210.0	185.0	35.0
LM20143QMHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM20143MH/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM20143QMH/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06

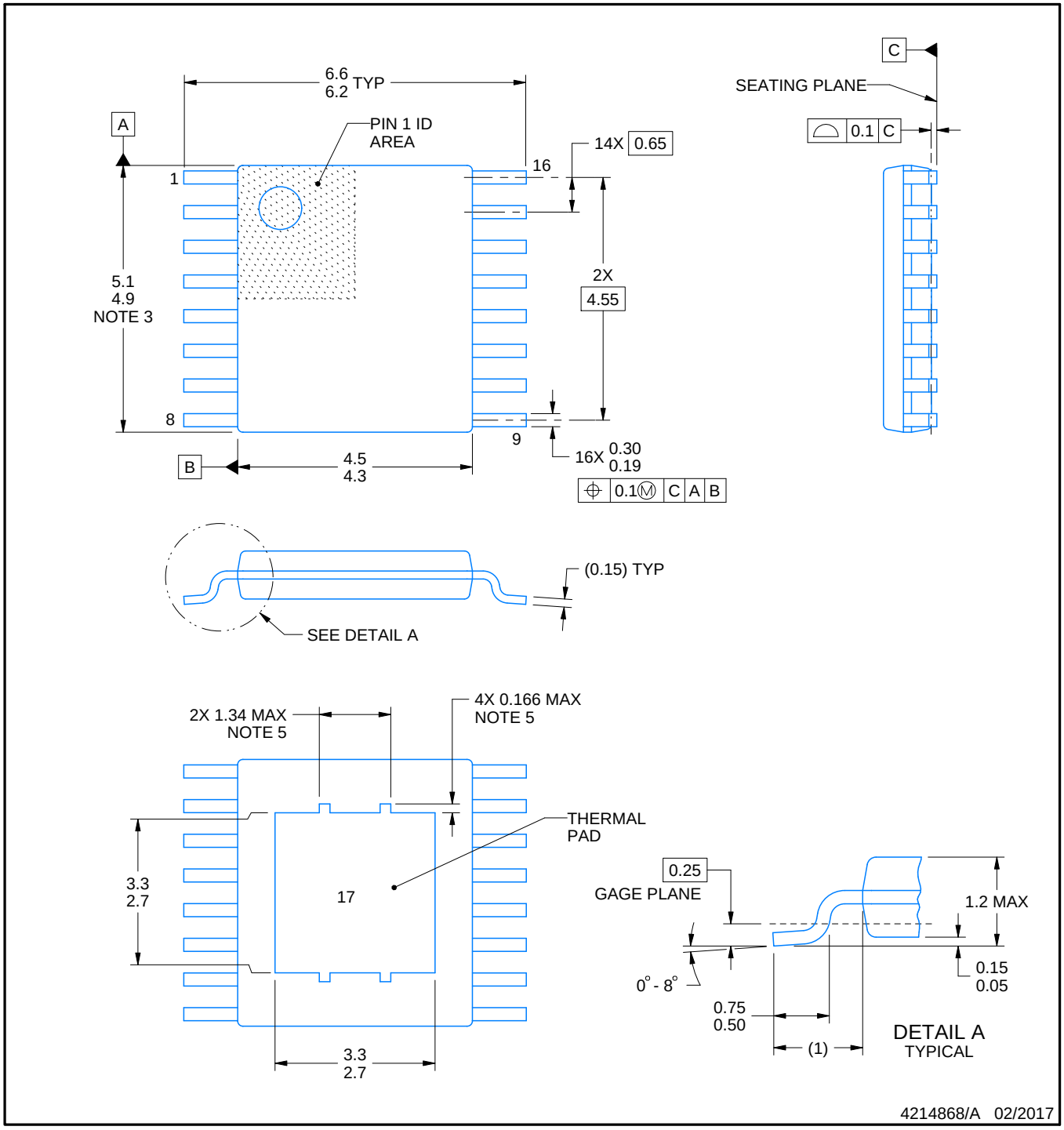


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

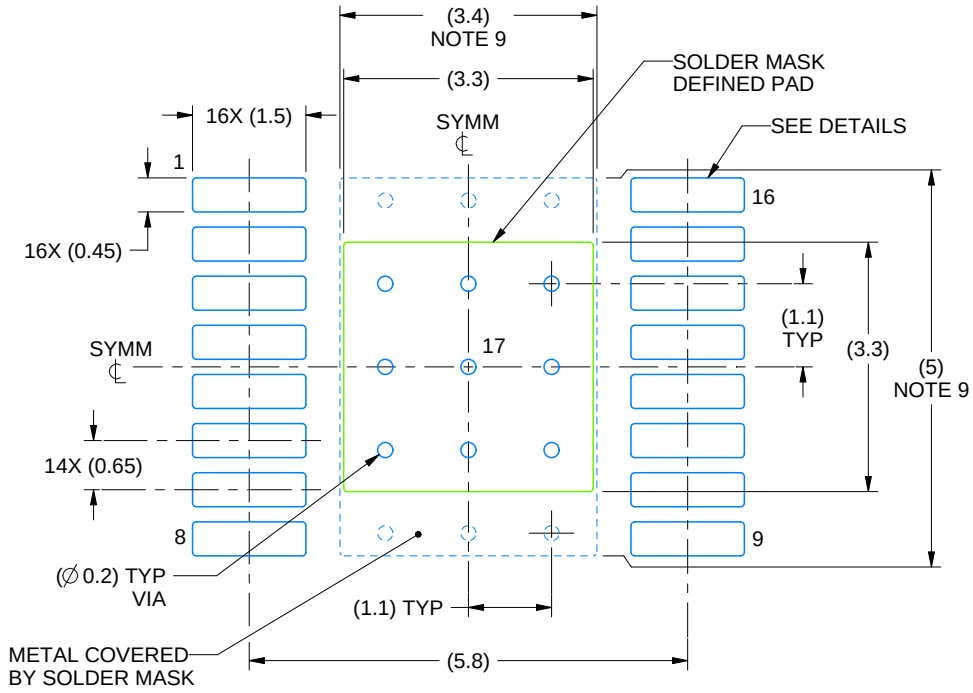
PLASTIC SMALL OUTLINE



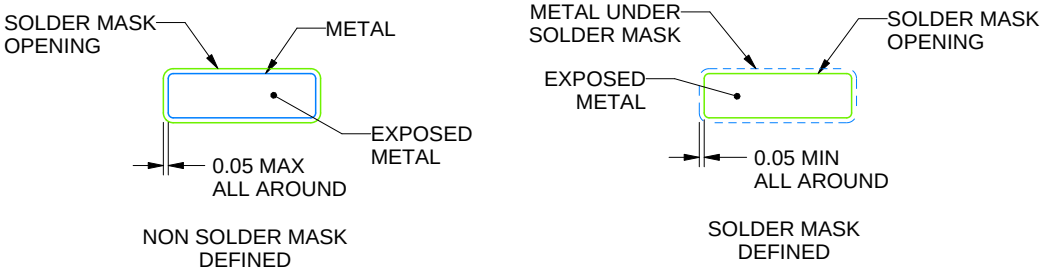
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS
PADS 1-16

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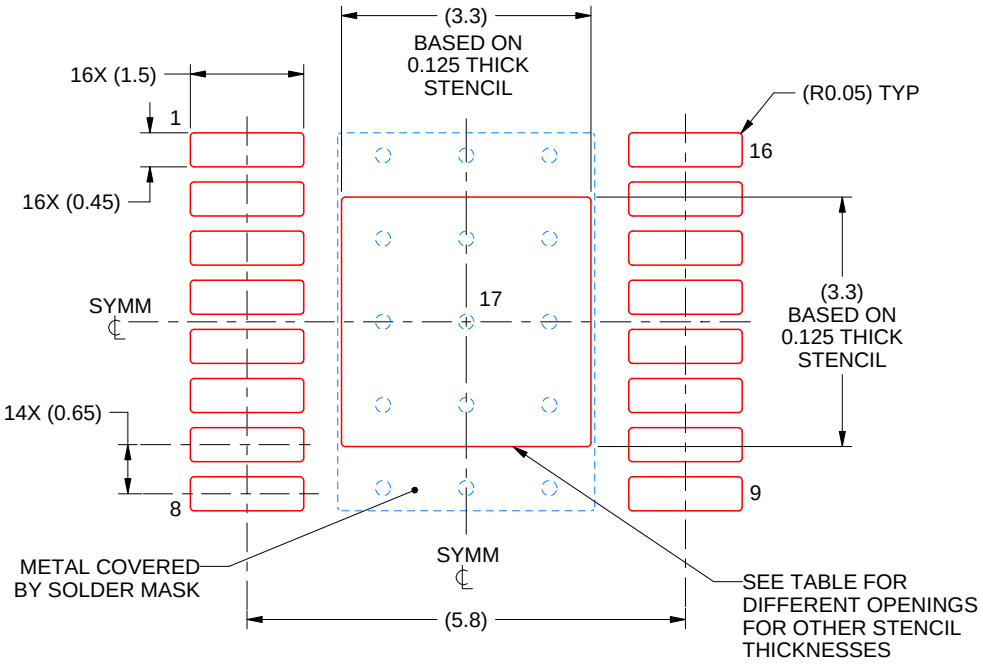
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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