LM158QML Low Power Dual Operational Amplifiers

Check for Samples: LM158QML

FEATURES

- **Available with Radiation Specification**
  - **High Dose Rate 100 krad(Si)**
  - **ELDRS Free 100 krad(Si)**
- **Internally Frequency Compensated for Unity Gain**
- **Large DC Voltage Gain: 100 dB**
- **Wide Bandwidth (Unity Gain): 1 MH z(Temperature Compensated)**
- **Wide Power Supply Range:**
  - **Single Supply: 3V to 32V**
  - **Or Dual Supplies: ±1.5V to ±16V**
- **Very Low Supply Current Drain (500 µA) − Essentially Independent of Supply Voltage**
- **Low Input Offset Voltage: 2 mV**
- **Input Common-mode Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to the Power Supply Voltage**
- **Large Output Voltage Swing: 0V to V^+ − 1.5V**

UNIQUE CHARACTERISTICS

- In the Linear Mode the Input Common-Mode Voltage Range Includes Ground and the Output Voltage can also Swing to Ground, even though Operated from only a Single Power Supply Voltage.
- The Unity Gain Cross Frequency is Temperature Compensated.
- The Input Bias Current is also Temperature Compensated.

ADVANTAGES

- Two Internally Compensated Op Amps
- Eliminates Need for Dual Supplies
- Allows Direct Sensing Near Gnd and V_O also Goes to Gnd
- Compatible with all Forms of Logic
- Power Drain Suitable for Battery Operation

DESCRIPTION

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Connection Diagrams

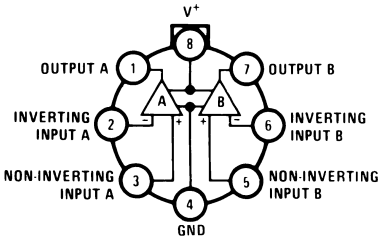


Figure 1. TO-99 Package
See Package Number LMC0008C

Top View

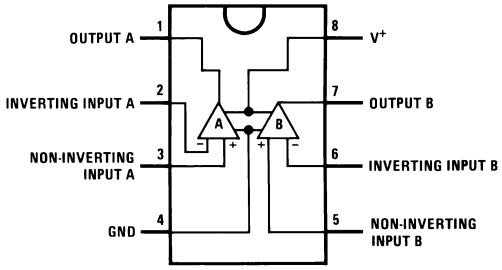


Figure 2. CDIP Package
See Package Number NAB0008A

Top View

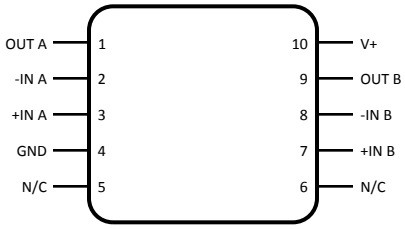
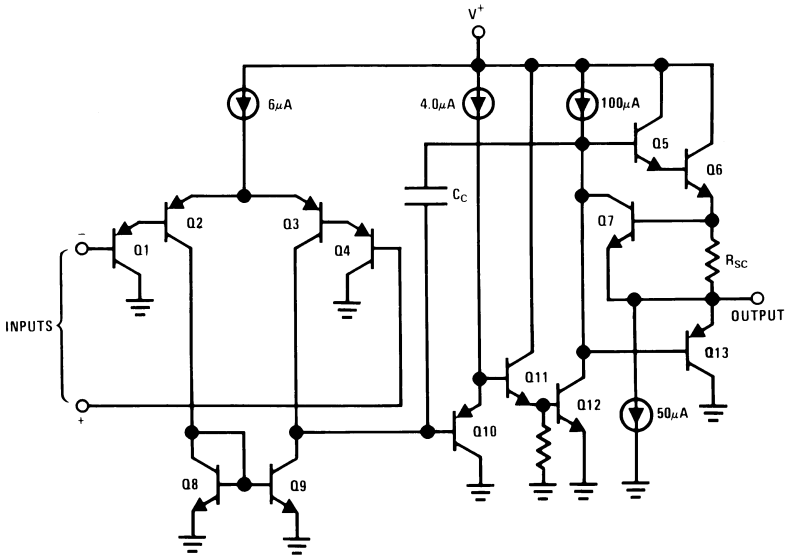


Figure 3. 10 Lead CLGA Package
See Package Number NAC0010A

Schematic Diagram

(Each Amplifier)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage, V^+			$32V_{DC}$
Differential Input Voltage			$32V_{DC}$
Input Voltage			$-0.3V_{DC}$ to $+32V_{DC}$
Power Dissipation(2)			830 mW
Output Short-Circuit to GND(3) (One Amplifier) $V^+ \le 15V_{DC}$ and $T_A = 25°C$			Continuous
Maximum Junction Temperature (T_{Jmax})			150°C
Input Current ($V_I < -0.3V$)(4)			50 mA
Operating Temperature Range			$-55°C \le T_A \le +125°C$
Storage Temperature Range			$-65°C \le T_A \le +150°C$
Lead Temperature (Soldering, 10 seconds)		TO-99	300°C
		CDIP	260°C
		CLGA	260°C
Thermal Resistance	θ_{JA}	TO-99 (Still Air)	155°C/W
		TO-99 (500LF/Min Air Flow)	80°C/W
		CDIP (Still Air)	132°C/W
		CDIP (500LF/Min Air Flow)	81°C/W
		CLGA (Still Air)	195°C/W
		CLGA (500LF/Min Air Flow)	131°C/W
	θ_{JC}	TO-99	42°C/W
		CDIP	23°C/W
		CLGA	33°C/W
Package Weight	TO-99		1,000mg
	CDIP		1,100mg
	CLGA		220mg
ESD Tolerance(5)			250V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

(4) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

(5) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LM158 Electrical Characteristics SMD 5962–8771001 DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Power Supply Current	$+V_{CC}$ = 5V, R_L = 100K, V_O = 1.4V			1.2	mA	1, 2, 3
		$+V_{CC}$ = 30V, R_L = 100K, V_O = 1.4V			3.0	mA	1
					4.0	mA	2, 3
V_{OH}	Output Voltage High	$+V_{CC}$ = 30V, R_L = 2KΩ		26		V	1, 2, 3
		$+V_{CC}$ = 30V, R_L = 10KΩ		27		V	1, 2, 3
V_{OL}	Output Voltage Low	$+V_{CC}$ = 30V, R_L = 10KΩ			20	mV	1, 2, 3
		$+V_{CC}$ = 30V, I_{Sink} = 1µA			20	mV	1, 2, 3
		$+V_{CC}$ = 5V, R_L = 10KΩ			20	mV	1, 2, 3
I_{Sink}	Output Sink Current	$+V_{CC}$ = 15V, V_O = 200mV, $+V_I$ = 0V, $-V_I$ = +65mV		12		µA	1
		$+V_{CC}$ = 15V, V_O = 2V, $+V_I$ = 0V, $-V_I$ = +65mV		10		mA	1
				5.0		mA	2, 3
I_{Source}	Output Source Current	$+V_{CC}$ = 15V, V_O = 2V, $+V_I$ = 0V, $-V_I$ = -65mV			-20	mA	1
					-10	mA	2, 3
I_{OS}	Short Circuit Current	$+V_{CC}$ = 5V, V_O = 0V		-60		mA	1
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 30V, V_{CM} = 28.5V, R_S = 50Ω, V_O = 1.4V		-5.0	5.0	mV	1
		$+V_{CC}$ = 30V, V_{CM} = 28V, R_S = 50Ω, V_O = 1.4V		-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 5V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
CMRR	Common Mode Rejection Ratio	$+V_{CC}$ = 30V, R_S = 50Ω V_I = 0V to 28.5V,		70		dB	1
$\pm I_{IB}$	Input BIas Current	$+V_{CC}$ = 5V, V_{CM} = 0V	See (1)	-150	-1.0	nA	1
			See (1)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	$+V_{CC}$ = 5V, V_{CM} = 0V		-30	30	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 5V to 30V, V_{CM} = 0V		65		dB	1
V_{CM}	Common Mode Voltage Range	$+V_{CC}$ = 30V	See (2), (3)		28.5	V	1
			See (2), (3)		28.0	V	2, 3
V_{Diff}	Differential Input Voltage		See (4)		32	V	1, 2, 3
A_{VS}	Large Signal Gain	$+V_{CC}$ = 15V, R_L = 2KΩ, V_O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(2) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage, independent of the magnitude of V^+.
(3) Specified by input offset voltage.
(4) Specified parameter not tested.

LM158A Electrical Characteristics SMD 5962–8771002, High Dose Rate DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Power Supply Current	$+V_{CC}$ = 5V, R_L = 100K, V_O = 1.4V			1.2	mA	1, 2, 3
		$+V_{CC}$ = 30V, R_L = 100K, V_O = 1.4V			3.0	mA	1
					4.0	mA	2, 3
V_{OH}	Output Voltage High	$+V_{CC}$ = 30V, R_L = 2KΩ		26		V	1, 2, 3
		$+V_{CC}$ = 30V, R_L = 10KΩ		27		V	1, 2, 3
V_{OL}	Output Voltage Low	$+V_{CC}$ = 30V, R_L = 10KΩ			40	mV	1
					100	mV	2, 3
		$+V_{CC}$ = 30V, I_{Sink} = 1µA			40	mV	1
					100	mV	2, 3
		$+V_{CC}$ = 5V, R_L = 10KΩ			40	mV	1
					100	mV	2, 3
I_{Sink}	Output Sink Current	$+V_{CC}$ = 15V, V_O = 200mV, $+V_I$ = 0V, $-V_I$ = +65mV		12		µA	1
		$+V_{CC}$ = 15V, V_O = 2V, $+V_I$ = 0V, $-V_I$ = +65mV		10		mA	1
				5.0		mA	2, 3
I_{Source}	Output Source Current	$+V_{CC}$ = 15V, V_O = 2V, $+V_I$ = 0V, $-V_I$ = -65mV			-20	mA	1
					-10	mA	2, 3
I_{OS}	Short Circuit Current	$+V_{CC}$ = 5V, V_O = 0V		-60		mA	1
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		$+V_{CC}$ = 30V, V_{CM} = 28.5V, R_S = 50Ω, V_O = 1.4V		-2.0	2.0	mV	1
		$+V_{CC}$ = 30V, V_{CM} = 28V, R_S = 50Ω, V_O = 1.4V		-4.0	4.0	mV	2, 3
		$+V_{CC}$ = 5V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
CMRR	Common Mode Rejection Ratio	$+V_{CC}$ = 30V, R_S = 50Ω V_I = 0V to 28.5V,		70		dB	1
$\pm I_{IB}$	Input BIas Current	$+V_{CC}$ = 5V, V_{CM} = 0V	See (1)	-50	-1.0	nA	1
			See (1)	-100	-1.0	nA	2, 3
I_{IO}	Input Offset Current	$+V_{CC}$ = 5V, V_{CM} = 0V		-10	10	nA	1
				-30	30	nA	2, 3
PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 5V to 30V, V_{CM} = 0V		65		dB	1
V_{CM}	Common Mode Voltage Range	$+V_{CC}$ = 30V	See (2) (3)		28.5	V	1
			See (2) (3)		28.0	V	2, 3
V_{Diff}	Differential Input Voltage		See (4)		32	V	1, 2, 3
A_{VS}	Large Signal Gain	$+V_{CC}$ = 15V, R_L = 2KΩ, V_O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(2) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage, independent of the magnitude of V^+.
(3) Specified by input offset voltage.
(4) Specified parameter not tested.

SMD 5962–8771002, High Dose Rate DC Drift Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground. Delta calculations are performed on QMLV devices at Group B, Subgroup 5 only.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-0.5	0.5	mV	1
		$+V_{CC}$ = 30V, V_{CM} = 28.5V, R_S = 50Ω, V_O = 1.4V		-0.5	0.5	mV	1
		$+V_{CC}$ = 5V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 5V, V_{CM} = 0V	See (1)	-10	10	nA	1

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

SMD 5962–8771002, High Dose Rate SMD 5962–8771002, High Dose Rate 100K Post Radiation Limits @ +25°C (1) DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub - groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V	See (1)	-4.0	4.0	mV	1
		$+V_{CC}$ = 30V, V_{CM} = 28.5V, R_S = 50Ω, V_O = 1.4V	See (1)	-4.0	4.0	mV	1
		$+V_{CC}$ = 5V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V	See (1)	-4.0	4.0	mV	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 5V, V_{CM} = 0V	See (1)(2)	-60	-1.0	nA	1
I_{CC}	Power Supply Current	$+V_{CC}$ = 5V, R_L = 100K, V_O = 1.4V	See (1)		1.5	mA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate sensitivity. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

LM158A Electrical Characteristics SMD 5962–8771003 ELDRS Free Only DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Power Supply Current	$+V_{CC}$ = 5V, R_L = 100K, V_O = 1.4V			1.2	mA	1, 2, 3
		$+V_{CC}$ = 30V, R_L = 100K, V_O = 1.4V			3.0	mA	1,
					4.0		2, 3
V_{OH}	Output Voltage High	$+V_{CC}$ = 30V, R_L = 2KΩ		26		V	1, 2, 3
		$+V_{CC}$ = 30V, R_L = 10KΩ		27		V	1, 2, 3
V_{OL}	Output Voltage Low	$+V_{CC}$ = 30V, R_L = 10KΩ			40	mV	1
					100	mV	2, 3
		$+V_{CC}$ = 30V, I_{Sink} = 1µA			40	mV	1
					100	mV	2, 3
		$+V_{CC}$ = 5V, R_L = 10KΩ			40	mV	1
					100	mV	2, 3

LM158A Electrical Characteristics SMD 5962–8771003 ELDRS Free Only DC Parameters (continued)

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
I_{Sink}	Output Sink Current	$+V_{CC}$ = 15V, V_O = 200mV, $+V_I$ = 0V, $-V_I$ = +65mV		12		µA	1
		$+V_{CC}$ = 15V, V_O = 2V, $+V_I$ = 0V, $-V_I$ = +65mV		10		mA	1
				5.0		mA	2, 3
I_{Source}	Output Source Current	$+V_{CC}$ = 15V, V_O = 2V, $+V_I$ = 0V, $-V_I$ = -65mV			-20	mA	1
					-10	mA	2, 3
I_{OS}	Short Circuit Current	$+V_{CC}$ = 5V, V_O = 0V		-60		mA	1
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		$+V_{CC}$ = 30V, V_{CM} = 28.5V, R_S = 50Ω, V_O = 1.4V		-2.0	2.0	mV	1
		$+V_{CC}$ = 30V, V_{CM} = 28V, R_S = 50Ω, V_O = 1.4V		-4.0	4.0	mV	2, 3
		$+V_{CC}$ = 5V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
CMRR	Common Mode Rejection Ratio	$+V_{CC}$ = 30V, R_S = 50Ω V_I = 0V to 28.5V,		70		dB	1
$\pm I_{IB}$	Input BIas Current	$+V_{CC}$ = 5V, V_{CM} = 0V	See (1)	-50	-1.0	nA	1
			See (1)	-100	-1.0	nA	2, 3
I_{IO}	Input Offset Current	$+V_{CC}$ = 5V, V_{CM} = 0V		-10	10	nA	1
				-30	30	nA	2, 3
PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 5V to 30V, V_{CM} = 0V		65		dB	1
V_{CM}	Common Mode Voltage Range	$+V_{CC}$ = 30V	See (2), (3)		28.5	V	1
			See (2), (3)		28.0	V	2, 3
V_{Diff}	Differential Input Voltage		See (4)		32	V	1, 2, 3
A_{VS}	Large Signal Gain	$+V_{CC}$ = 15V, R_L = 2KΩ, V_O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(2) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage, independent of the magnitude of V^+.
(3) Specified by input offset voltage.
(4) Specified parameter not tested.

SMD 5962–8771003 ELDRS Free Only DC Drift Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.
Delta calculations are performed on QMLV devices at Group B, Subgroup 5 only.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-0.5	0.5	mV	1
		$+V_{CC}$ = 30V, V_{CM} = 28.5V, R_S = 50Ω, V_O = 1.4V		-0.5	0.5	mV	1
		$+V_{CC}$ = 5V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V		-0.5	0.5	mV	1

SMD 5962–8771003 ELDRS Free Only DC Drift Parameters (continued)

The following conditions apply, unless otherwise specified. All voltages referenced to device ground. Delta calculations are performed on QMLV devices at Group B, Subgroup 5 only.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 5V, V_{CM} = 0V	See (1)	-10	10	nA	1

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

SMD 5962–8771003 ELDRS Free Only 100K Post Radiation Limits @ +25°C (1) DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub - groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V	See (1)	-4.0	4.0	mV	1
		$+V_{CC}$ = 30V, V_{CM} = 28.5V, R_S = 50Ω, V_O = 1.4V	See (1)	-4.0	4.0	mV	1
		$+V_{CC}$ = 5V, V_{CM} = 0V, R_S = 50Ω, V_O = 1.4V	See (1)	-4.0	4.0	mV	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 5V, V_{CM} = 0V	See (1) (2)	-60	-1.0	nA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Typical Performance Characteristics

Input Voltage Range

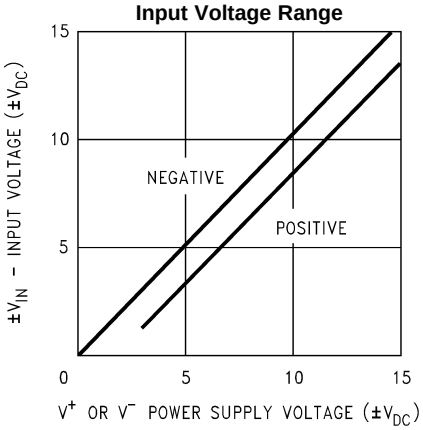


Figure 4.

Input Current

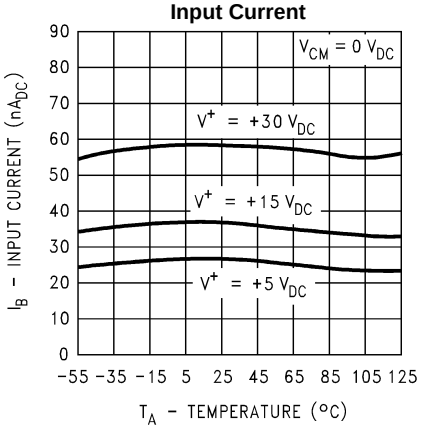


Figure 5.

Supply Current

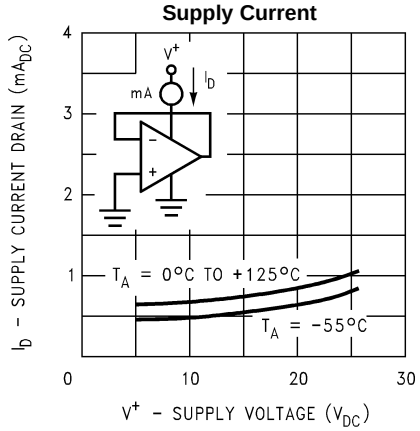


Figure 6.

Voltage Gain

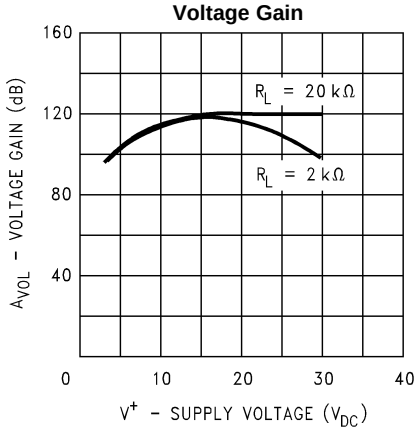


Figure 7.

Open Loop Frequency Response

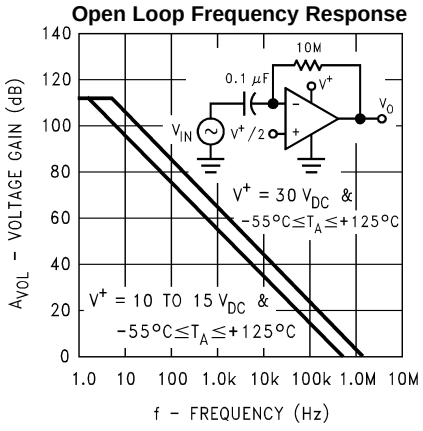


Figure 8.

Common-Mode Rejection Ratio

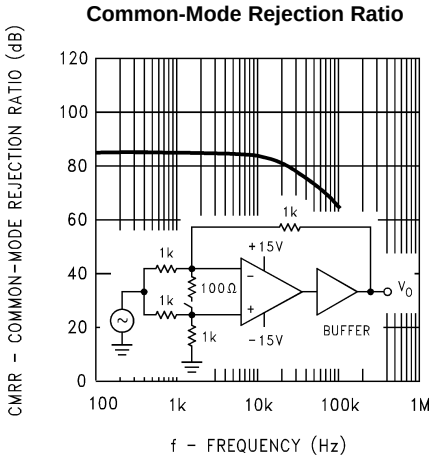


Figure 9.

Typical Performance Characteristics (continued)

Voltage Follower Pulse Response

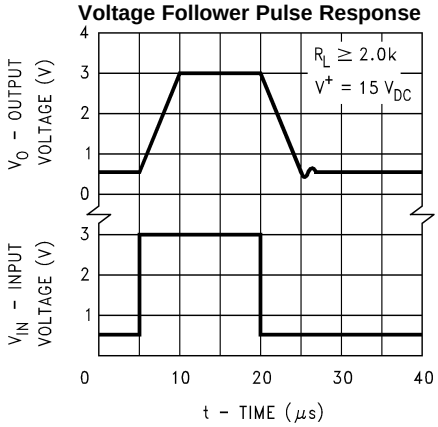


Figure 10.

Voltage Follower Pulse Response (Small Signal)

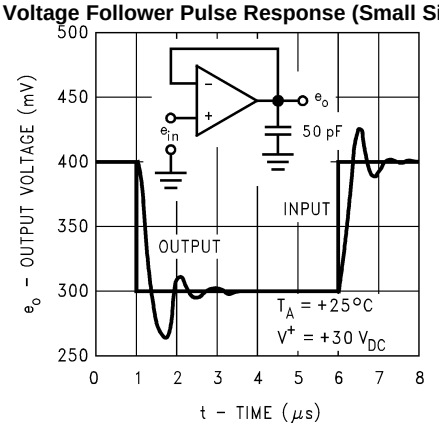


Figure 11.

Large Signal Frequency Response

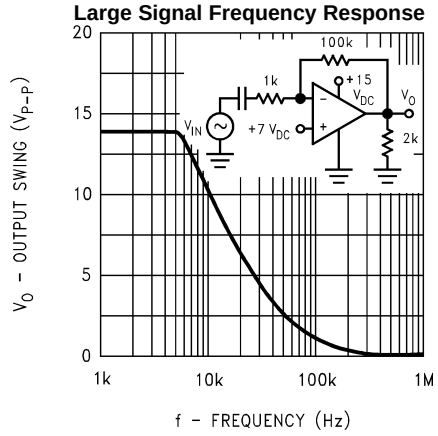


Figure 12.

Output Characteristics Current Sourcing

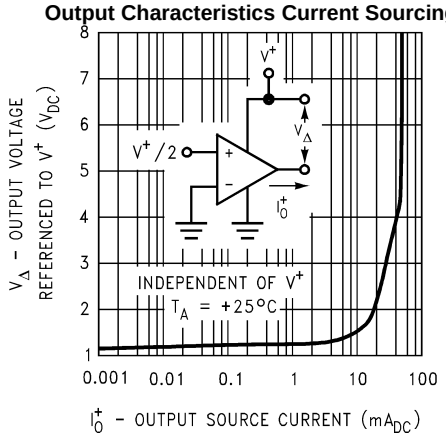


Figure 13.

Output Characteristics Current Sinking

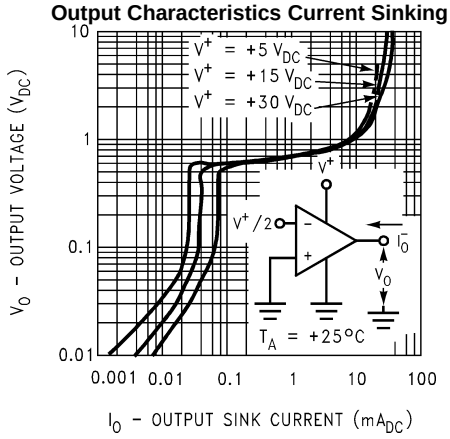


Figure 14.

Current Limiting

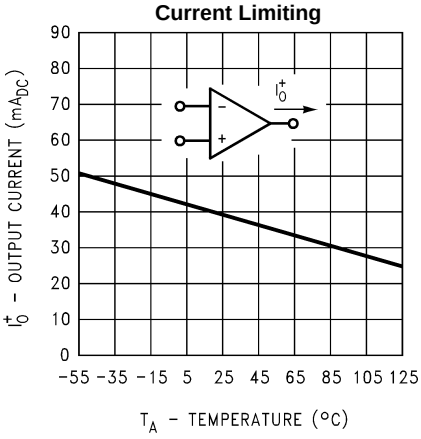


Figure 15.

APPLICATION HINTS

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

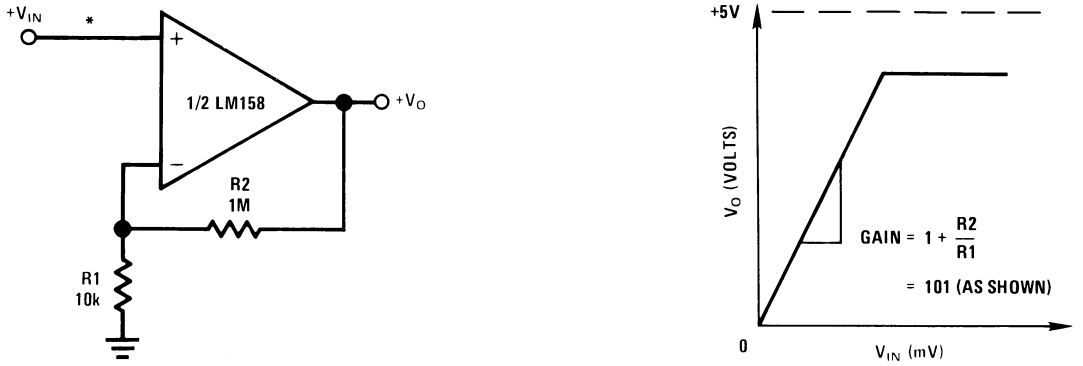
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see Typical Performance Characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

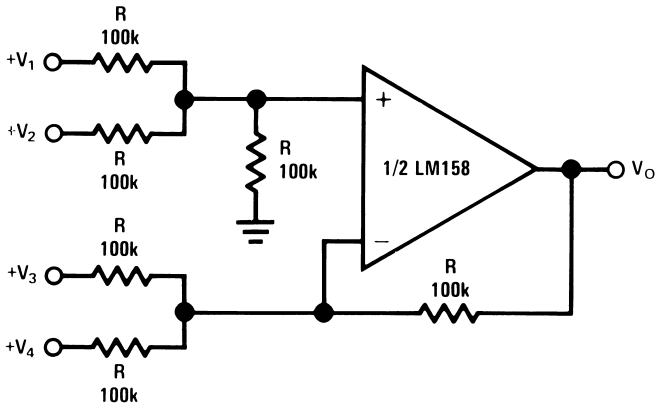
Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})



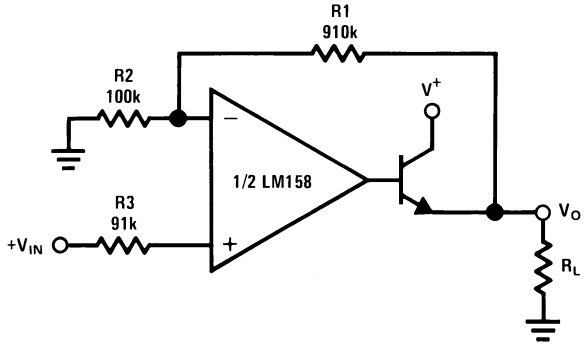
*R not needed due to temperature independent I_{IN}

Figure 16. Non-Inverting DC Gain (0V Output)



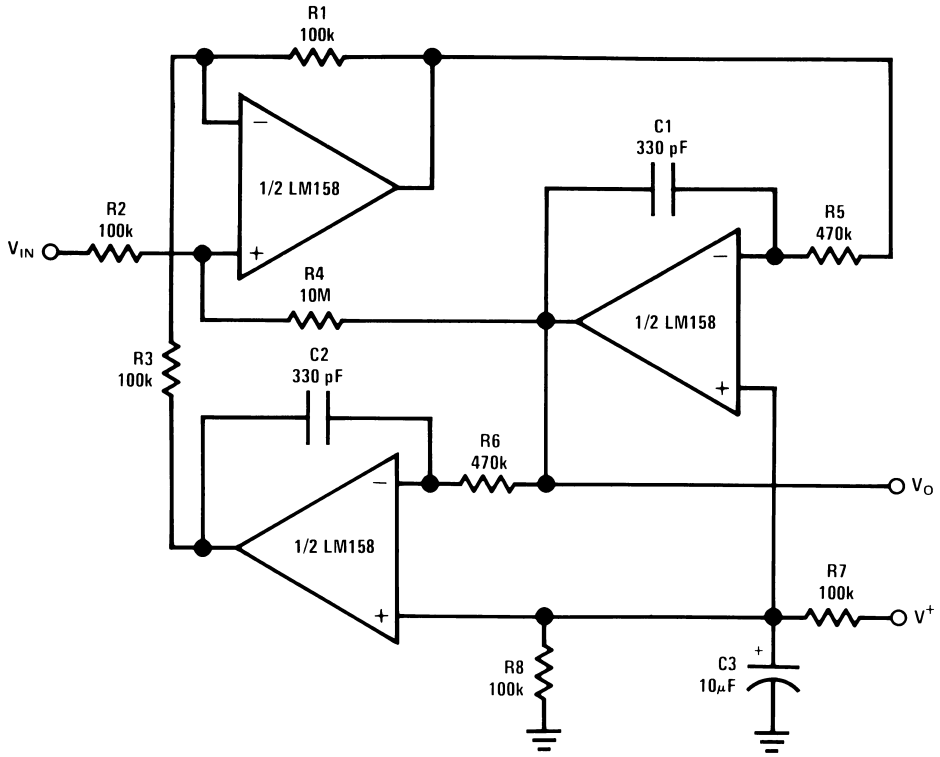
Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0$ V_{DC}

Figure 17. DC Summing Amplifier ($V_{IN'S} \geq 0$ V_{DC} and $V_O \geq 0$ V_{DC})



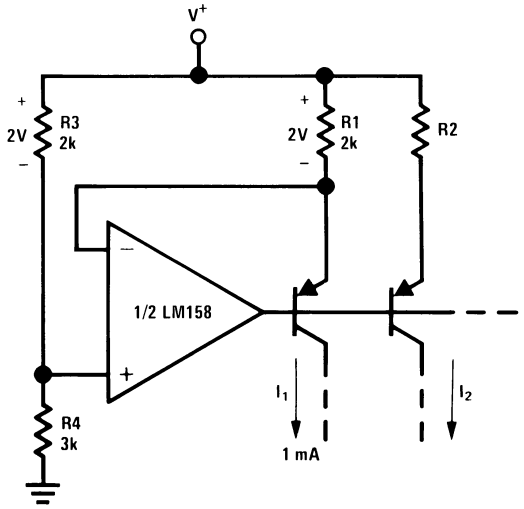
V_O = 0 V_{DC} for V_{IN} = 0 V_{DC}
A_V = 10

Figure 18. Power Amplifier



f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

Figure 19. "BI-QUAD" RC Active Bandpass Filter



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Figure 20. Fixed Current Sources

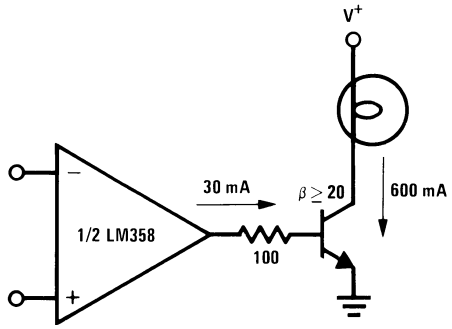


Figure 21. Lamp Driver

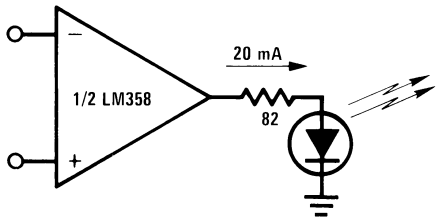
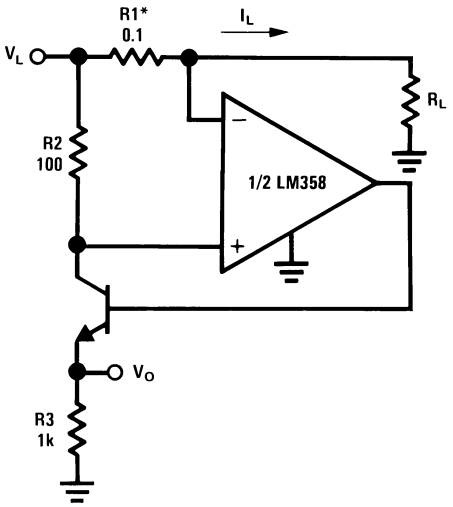


Figure 22. LED Driver



$$V_O = \frac{1V\ (I_L)}{1A}$$

*(Increase R1 for I_L small)

$V_L \leq V^+ - 2V$

Figure 23. Current Monitor

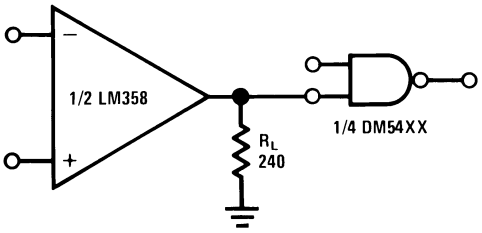
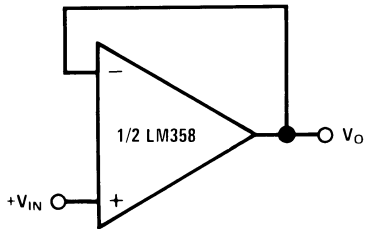


Figure 24. Driving TTL



$V_O = V_{IN}$

Figure 25. Voltage Follower

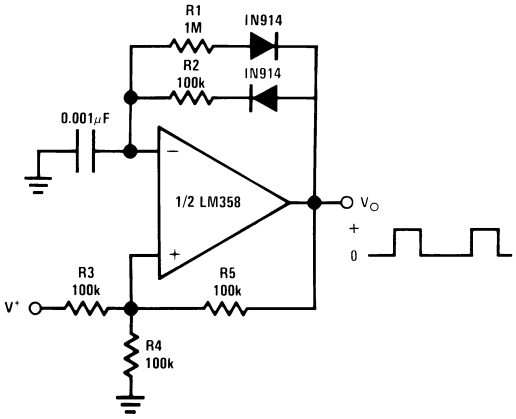


Figure 26. Pulse Generator

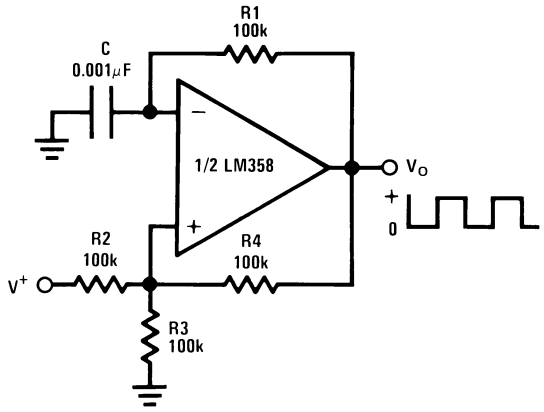


Figure 27. Squarewave Oscillator

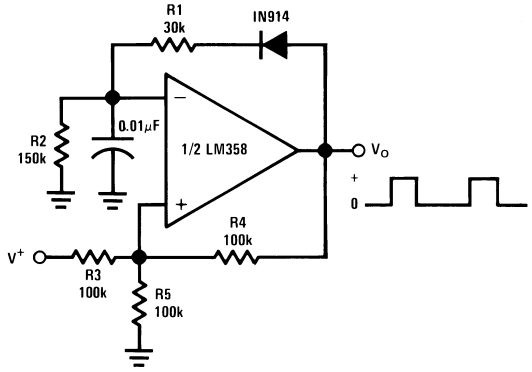
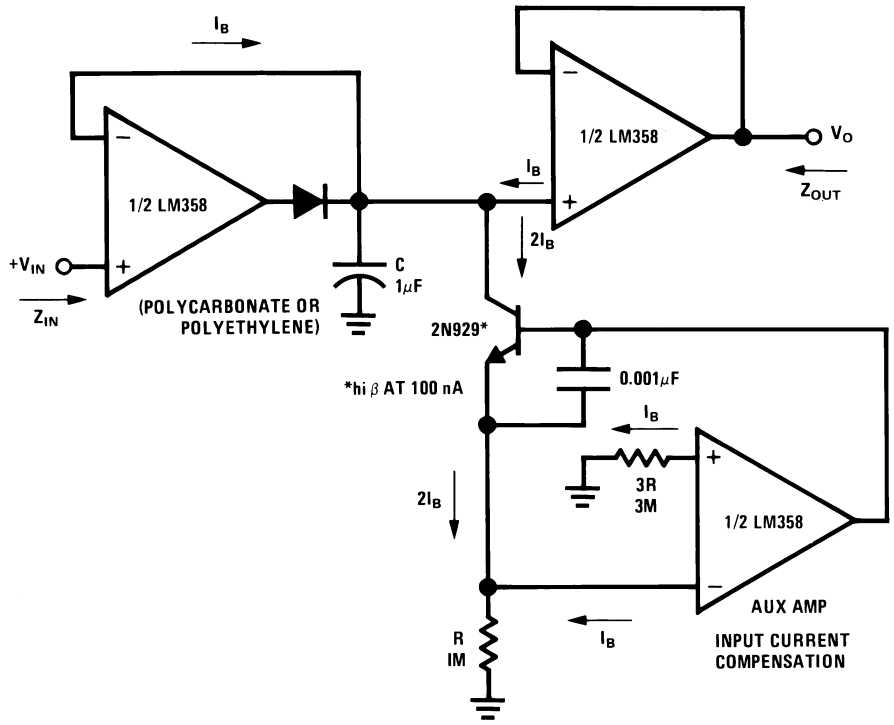
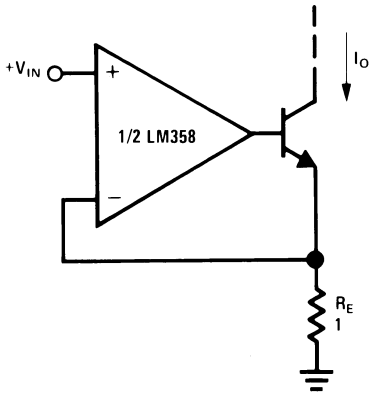


Figure 28. Pulse Generator



HIGH Z_{IN}
LOW Z_{OUT}

Figure 29. Low Drift Peak Detector



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

Figure 30. High Compliance Current Sink

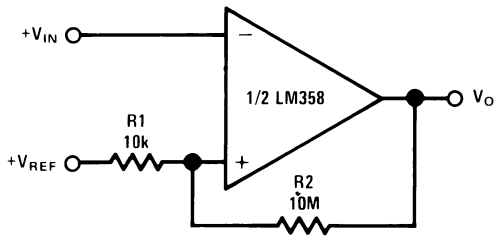
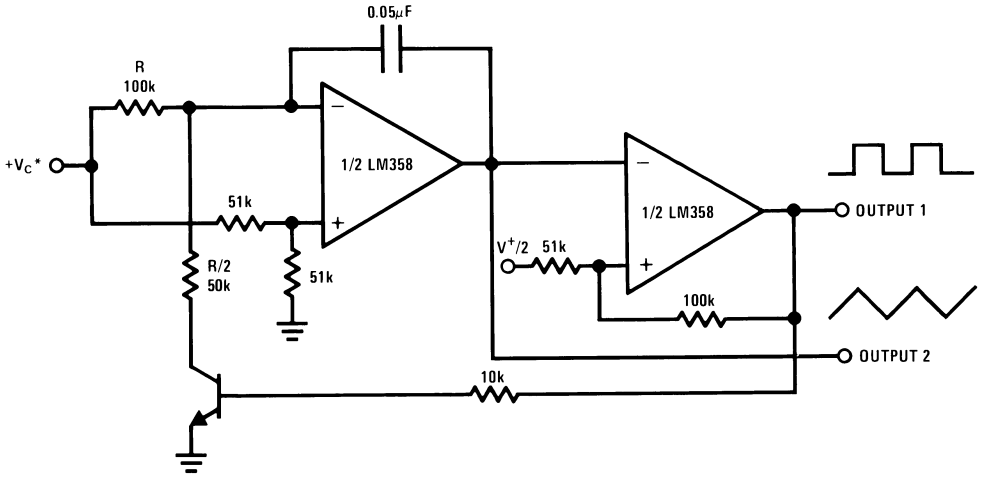
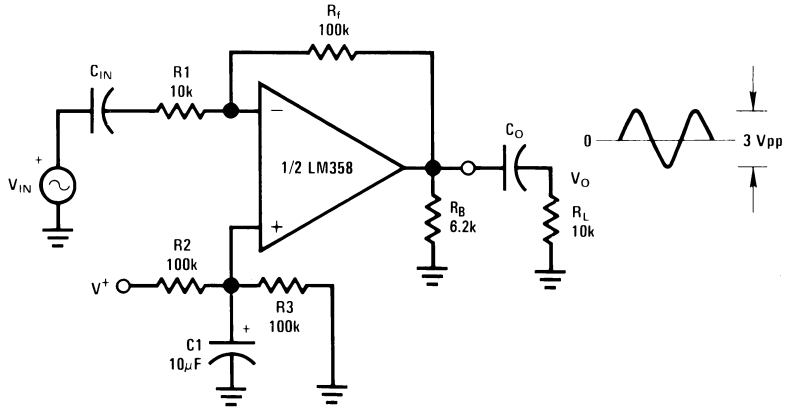


Figure 31. Comparator with Hysteresis



*WIDE CONTROL VOLTAGE RANGE: 0 $V_{DC} \leq V_C \leq 2$ ($V^+ - 1.5V_{DC}$)

Figure 32. Voltage Controlled Oscillator (VCO)



$$A_V = \frac{R_f}{R1} \text{ (As shown, } A_V = 10)$$

Figure 33. AC Coupled Inverting Amplifier

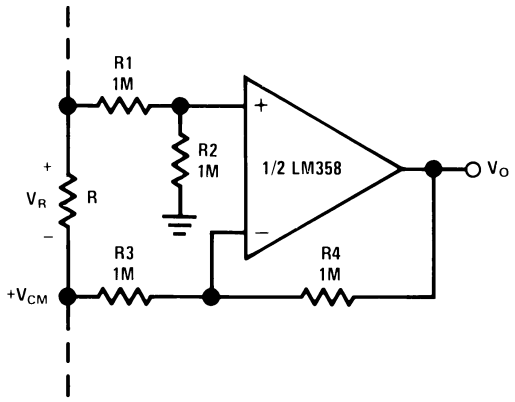
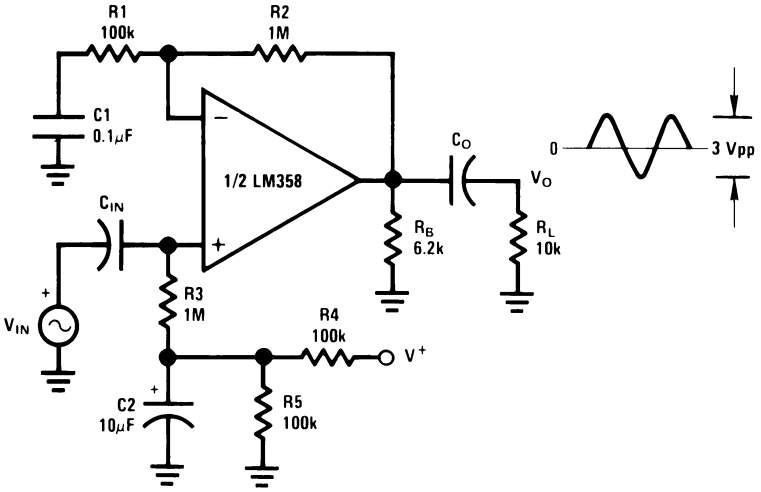


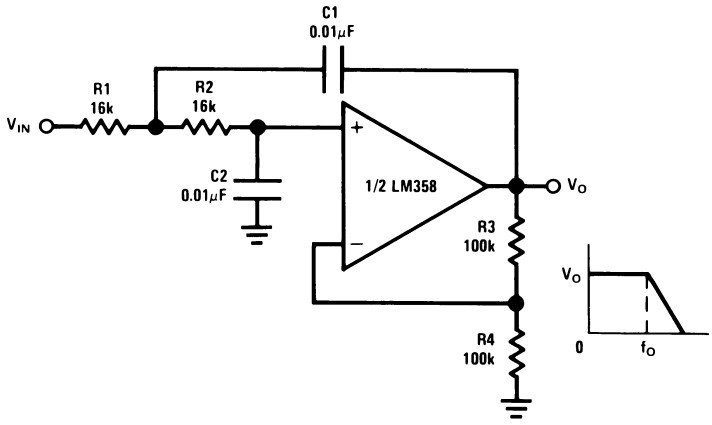
Figure 34. Ground Referencing a Differential Input Signal



$$A_V = 1 + \frac{R2}{R1}$$

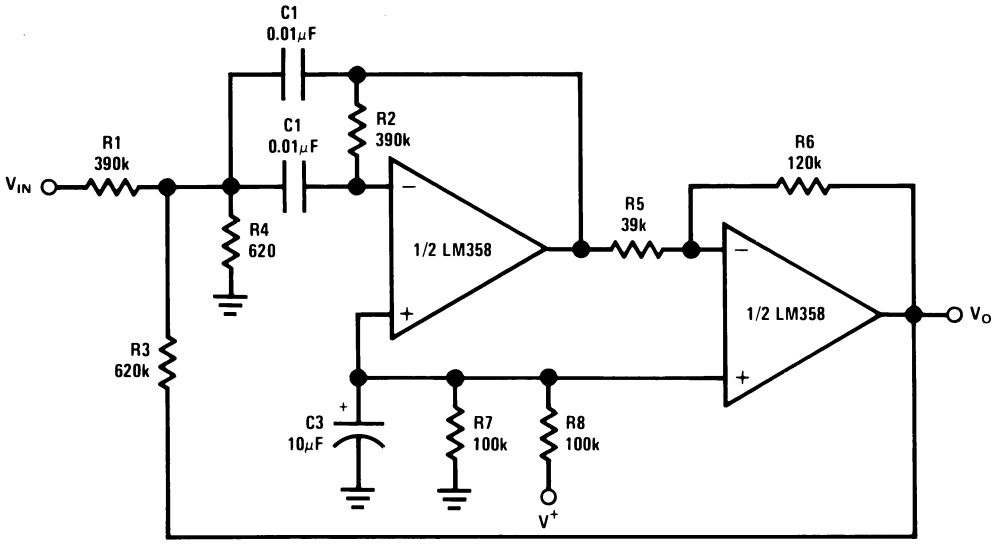
A_V = 11 (As Shown)

Figure 35. AC Coupled Non-Inverting Amplifier



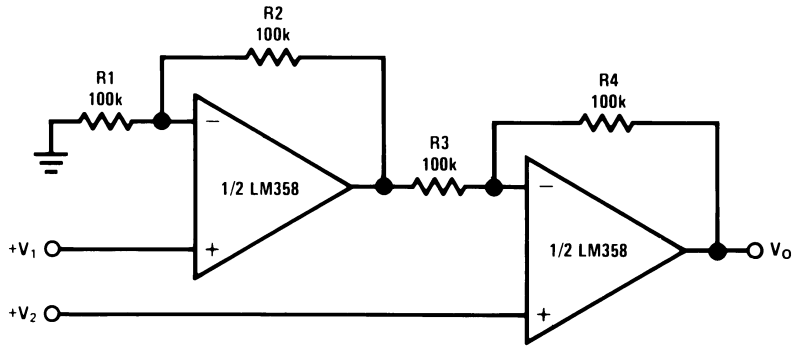
f_o = 1 kHz
Q = 1
A_V = 2

Figure 36. DC Coupled Low-Pass RC Active Filter



f_o = 1 kHz
Q = 25

Figure 37. Bandpass Active Filter



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As Shown: $V_O = 2(V_2 - V_1)$

Figure 38. High Input Z, DC Differential Amplifier

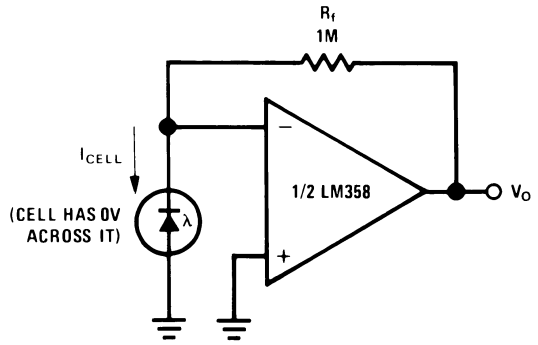
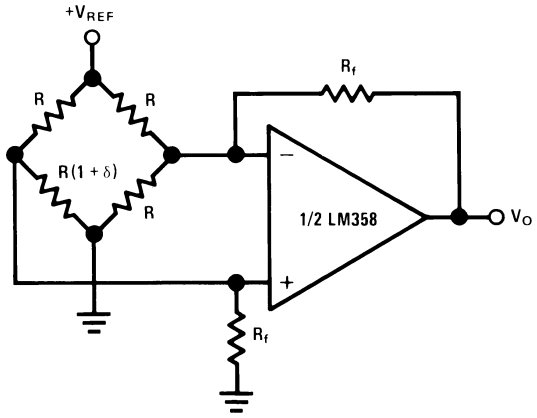


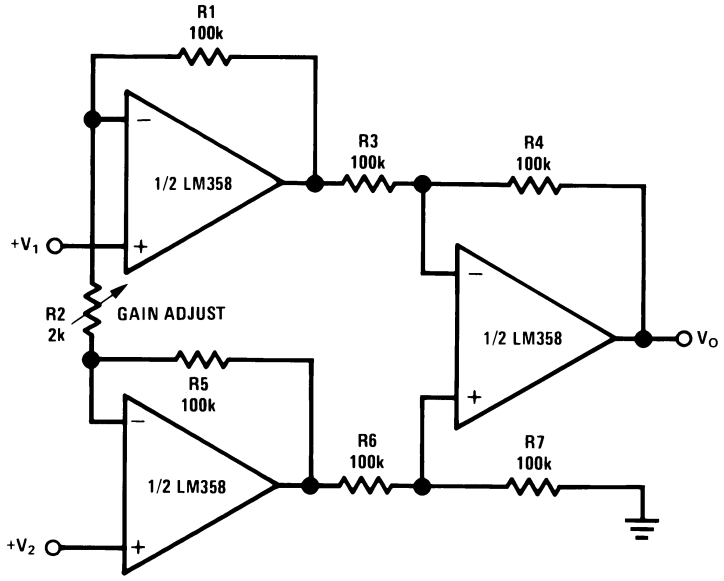
Figure 39. Photo Voltaic-Cell Amplifier



For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

Figure 40. Bridge Current Amplifier



If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101\,(V_2 - V_1)$

Figure 41. High Input Z Adjustable-Gain DC Instrumentation Amplifier

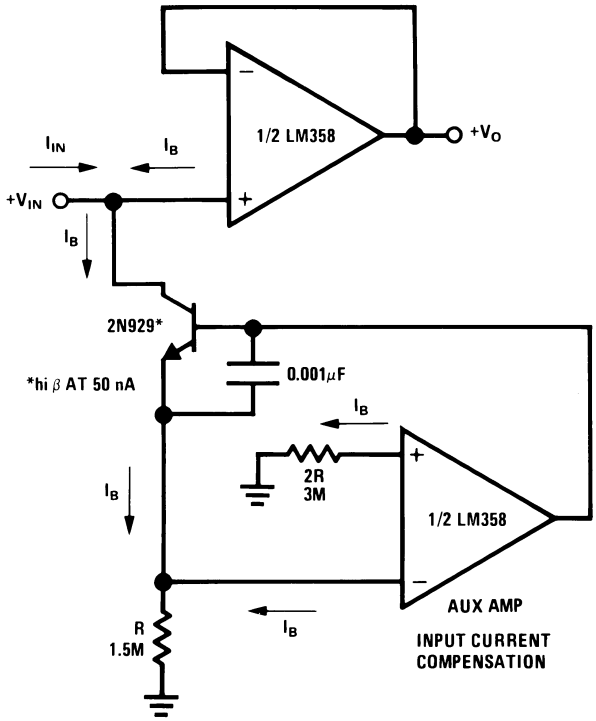


Figure 42. Using Symmetrical Amplifiers to Reduce Input Current (General Concept)

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8771002GA	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AH-SMD 5962-8771002GA Q A CO 5962-8771002GA Q > T	Samples
5962-8771002QXA	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AWG /883 Q 5962-87710 (02QXA ACO, 02QYA ACO) (02QXA >T, 02QYA > T)	Samples
5962R8771002V9A	ACTIVE	DIESALE	Y	0	38	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
5962R8771002VGA	ACTIVE	TO-99	LMC	8	20	Non-RoHS & Non-Green	Call TI	Call TI	-55 to 125	LM158AHRQMLV 5962R8771002VGA Q ACO 5962R8771002VGA Q >T	Samples
5962R8771002VPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AJRQMLV 5962R87710 02VPA Q ACO 02VPA Q >T	Samples
5962R8771002VXA	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AWG (RLQMLV Q, RQMLV Q) 5962R87710 02VXA ACO 02VXA >T	Samples
5962R8771003V9A	ACTIVE	DIESALE	Y	0	38	RoHS & Green	Call TI	Level-1-NA-UNLIM	25 to 25		Samples
5962R8771003VGA	ACTIVE	TO-99	LMC	8	20	Non-RoHS & Non-Green	Call TI	Call TI	-55 to 125	LM158AHRLQMLV 5962R8771003VGA Q ACO 5962R8771003VGA Q >T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R8771003VPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AJRLQV 5962R87710 03VPA Q ACO 03VPA Q >T	Samples
5962R8771003VXA	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AWG RLQMLV Q 5962R87710 03VXA ACO 03VXA >T	Samples
LM158 MD8	ACTIVE	DIESALE	Y	0	400	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM158A MDE	ACTIVE	DIESALE	Y	0	38	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM158A MDR	ACTIVE	DIESALE	Y	0	38	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM158AH-SMD	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AH-SMD 5962-8771002GA Q A CO 5962-8771002GA Q > T	Samples
LM158AH/883	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AH/883 Q ACO LM158AH/883 Q >T	Samples
LM158AHRLQMLV	ACTIVE	TO-99	LMC	8	20	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AHRLQMLV 5962R8771003VGA Q ACO 5962R8771003VGA Q >T	Samples
LM158AHRQMLV	ACTIVE	TO-99	LMC	8	20	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AHRQMLV 5962R8771002VGA Q ACO 5962R8771002VGA Q >T	Samples
LM158AJ/883	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AJ/883 5962-87710 02PA Q ACO 02PA Q >T	Samples
LM158AJRLQMLV	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AJRLQV 5962R87710 03VPA Q ACO	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										03VPA Q >T	
LM158AJRQMLV	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AJRQMLV 5962R87710 02VPA Q ACO 02VPA Q >T	Samples
LM158AWG/883	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AWG /883 Q 5962-87710 (02QXA ACO, 02QYA ACO) (02QXA >T, 02QYA >T)	Samples
LM158AWGRLQMLV	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AWG RLQMLV Q 5962R87710 03VXA ACO 03VXA >T	Samples
LM158AWGRQMLV	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158AWG (RLQMLV Q, RQMLV Q) 5962R87710 02VXA ACO 02VXA >T	Samples
LM158H/883	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM158H/883 Q ACO LM158H/883 Q >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

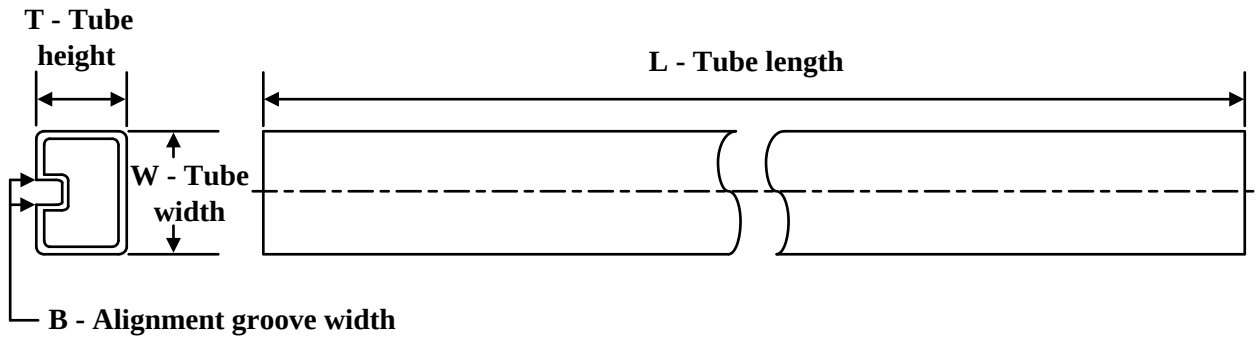
OTHER QUALIFIED VERSIONS OF LM158QML, LM158QML-SP :

- Military : LM158QML
- Space : LM158QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

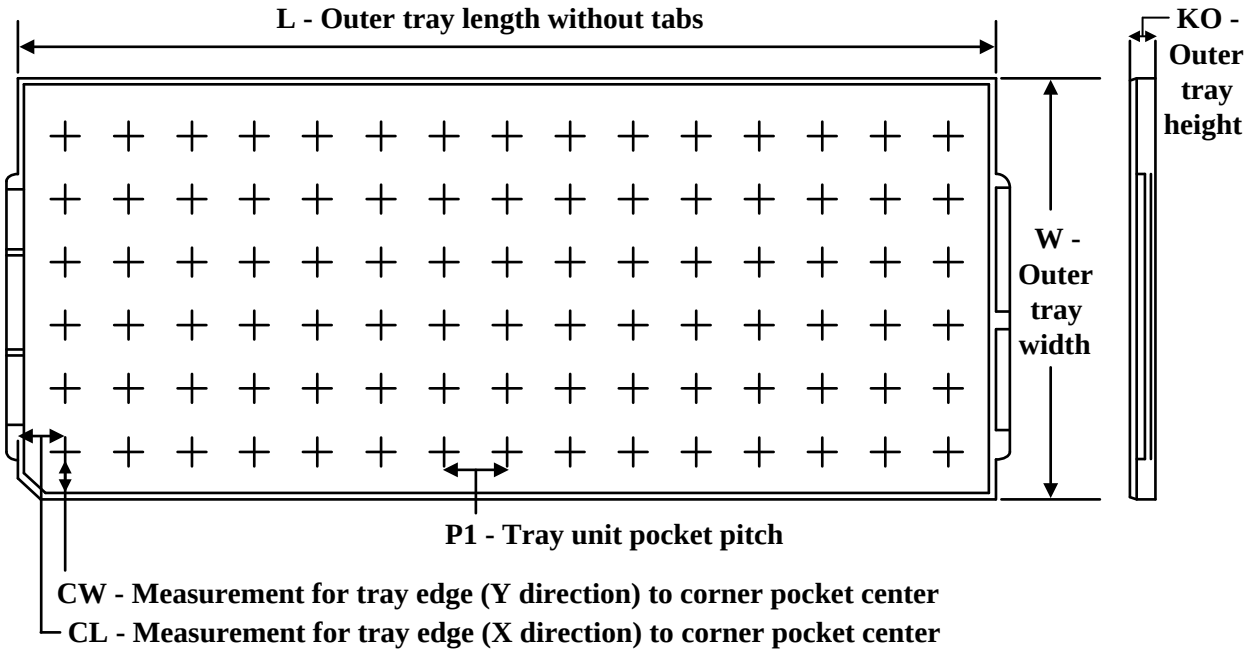
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R8771002VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
5962R8771003VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM158AJ/883	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM158AJRLQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM158AJRQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA

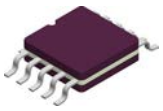
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-8771002GA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
5962-8771002QXA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
5962R8771002VGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
5962R8771002VXA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
5962R8771003VGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
5962R8771003VXA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LM158AH-SMD	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM158AH/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM158AHRLQMLV	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM158AHRQMLV	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM158AWG/883	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LM158AWGRLQMLV	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LM158AWGRQMLV	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LM158H/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

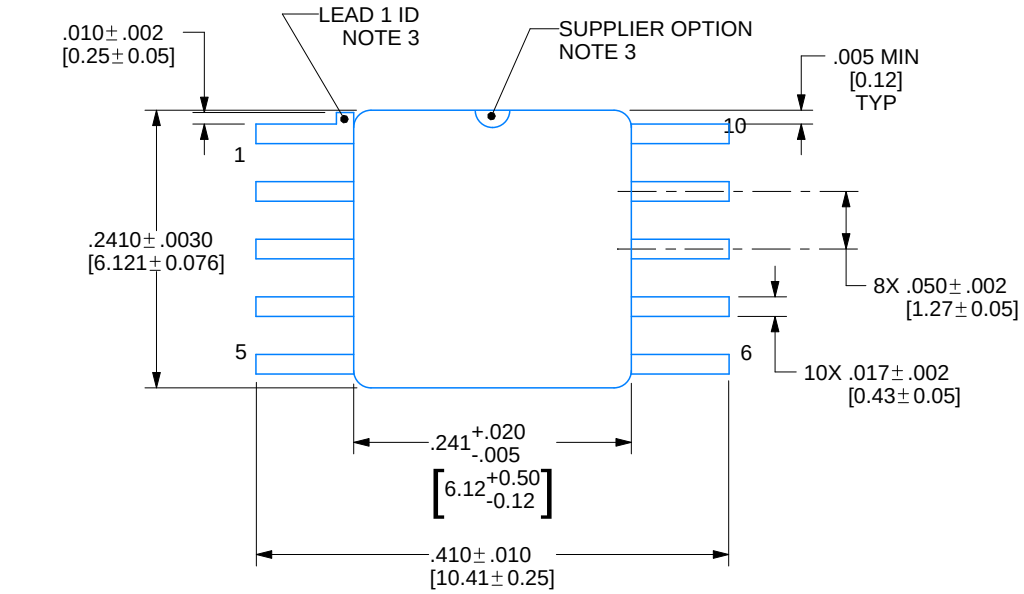


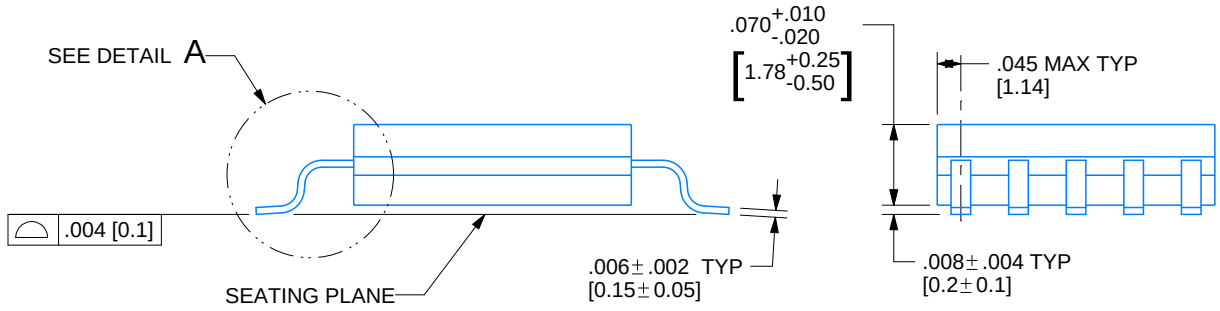
PACKAGE OUTLINE

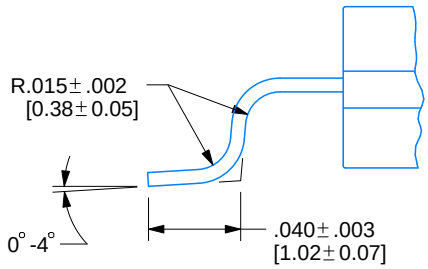
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK







DETAIL A
TYPICAL

4215196/D 08/2022

NOTES:

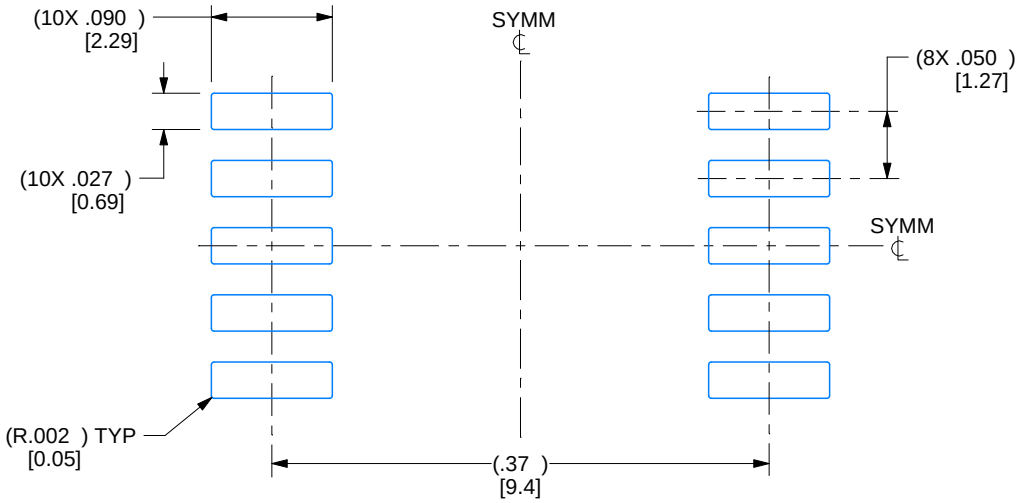
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

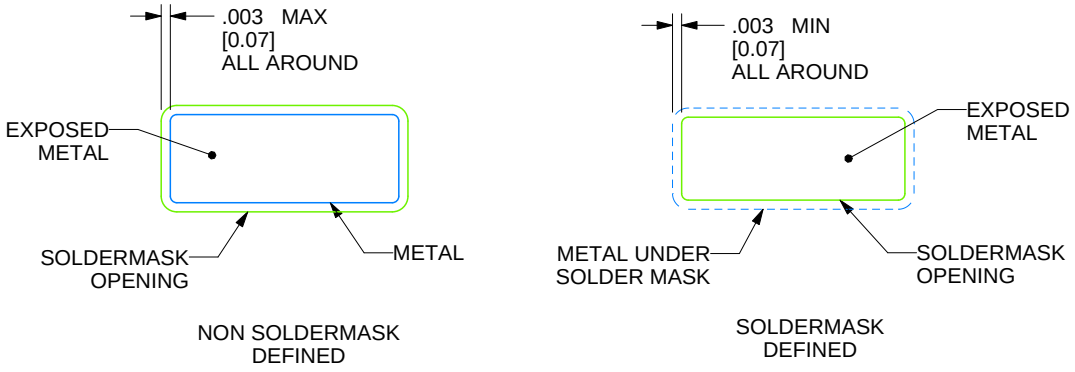
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X

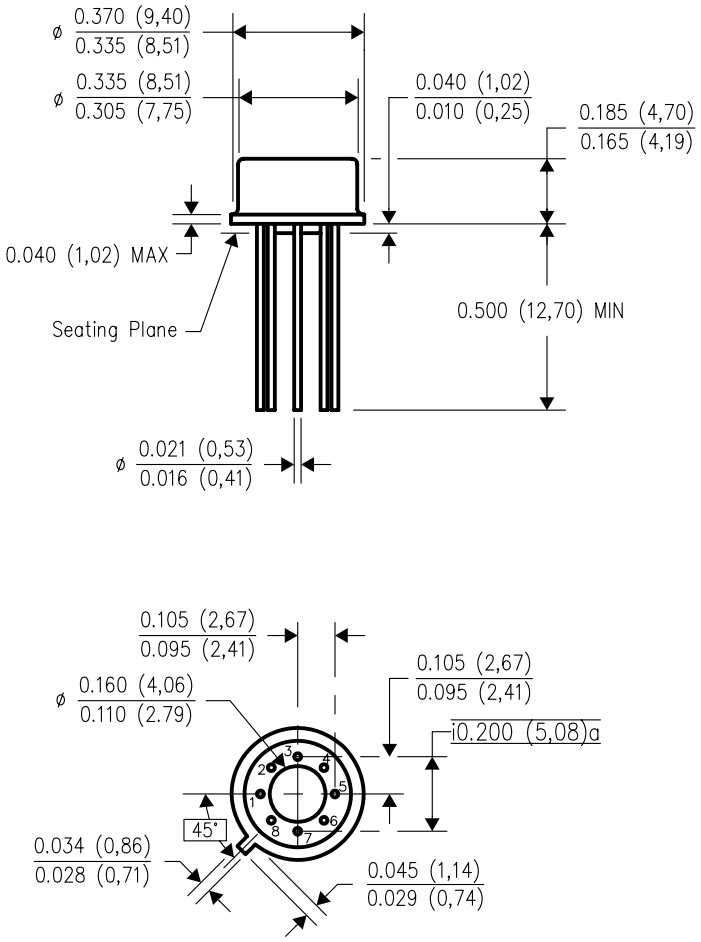


4215196/D 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197877	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198820	02/14/2022	K. SINCERBOX
C	CHANGE PIN 1 ID LOCATION ON PIN	2198845	02/18/2022	D. CHIN / K. SINCERBOX
D	.2410± .0030 WAS .2700 +.0012/-.0002;	2200915	08/08/2022	D. CHIN / K. SINCERBOX

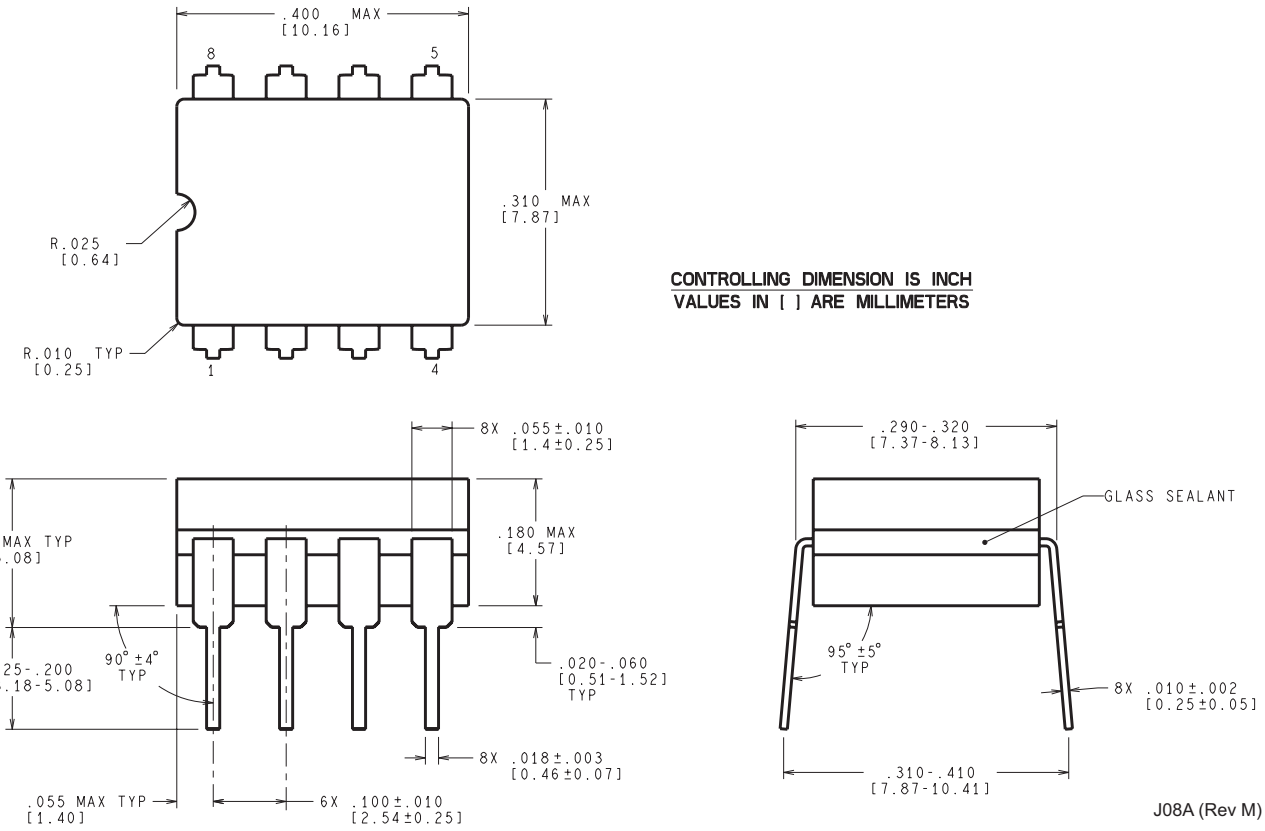
LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265